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Hitachi 8/16-Bit

Microcomputer Peripheral LSI

DATA BOOK

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HITACHI

Hitachi 8/16-Bit Microcomputer

Peripheral LSI
Data Book

HITACHI

ADE-402-003A

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Quick Reference Guide

Display Control LSI

	CRTC-II		CRTC+	GDP	ACRTC	GMIC
Type	**HD6345**	**HD6445**	**HD64460*2**	**HD64400**	**HD63484**	**HD63485**
Process	CMOS	CMOS	CMOS	CMOS	CMOS	Hi-BiCMOS
Supply voltage (V)	5	5	5	5	5	5
Operating temperature (°C)	−20 to +75*1	−20 to +75*1	0 to +70	0 to +70	0 to +70*1	0 to +70
Operating frequency (MHz)	1, 1.5, 2	4	32, 37	16, 20	4, 6, 8, 9.8	32, 48, 64
Features	●CRT display timing: 4.5 MHz ●MPRAM control ●Upward pin/ software compatibility with HD6845S ●Horizontal screen 4-split function ●68 system interface	●CRT display timing: 4.5 MHz ●MPRAM control ●Upward software compatibility with HD6845S ●Horizontal screen 4-split function ●80 system interface	●Color logic operation ●On-chip color palette ●Bit mask/ memory plane mask function ●Possible direct interface with 256k-byte memory	●Overlapping of up to 4 windows ●High-speed drawing: character drawing corresponding to bit map, high-speed raster operation ●Flexible graphic processing commands ●VDI-based command system	●Elliptic commands: Circle, ellipse, rectangle, straight line, line dot, paint ●Frame buffer: 2 Mbytes (max. 4,096 × 4,096 dots) independent of main memory ●Horizontal screens 3-split window ●Smooth scrolling in any direction	●Frame buffer direct drive enabled ●DRAM control signal generation (row/column address) ●Direct interface with ACRTC
Function	CRT controller		High integration CRT controller	Graphic data processor	Advanced CRT controller	Graphic memory interface controller
Package	DP-40 CP-44	DP-40 CP-44	FP-136	PC-135	DC-64, DP-64 DP-64S, CP-68 PC-68	DP-64S CP-68

Note *1: For wide temperature range version (−40°C to +85°C), ask our service station.
*2: Preliminary

	GVAC	MIVAC	LCTC			LVIC	
Type	**HD63486**	**HD63487**	**HD63645**	**HD64645**	**HD64646**	**HD66840**	**HD66841*1**
Process	Hi-BiCMOS	Hi-BiCMOS	CMOS	CMOS	CMOS	CMOS	CMOS
Supply voltage (V)	5	5	5	5	5	5	5
Operating temperature (°C)	0 to +70	0 to +70	−20 to +75	−20 to +75	−20 to +75	−20 to +75	−20 to +75
Operating frequency (MHz)	32, 48, 64	33	2	4	4	25, 30	30
Features	●On-chip shift register for video signals ●Quick video signal generation (64 MHz max) ●Direct interface with ACRTC	●Direct interface with ACRTC and from buffer ●Video signal generation ●GMIC and GVAC in one chip	●Display capacity of 1,024 × 4,096 dots ●Software-compatible with HD6845 ●Smooth scrolling ●68 system interface	●Display capacity of 1,024 × 4,096 dots ●Software-compatible with HD6845 ●Smooth scrolling ●80 system interface	●Changed phase of CL1/CL2 signal of HD64645	●Direct conversion of video signals into LCD signals ●Possible interface with monochrome/color LCD driver ●LCD driver interface: 4, 8, 12-bit parallel	●Direct conversion of video signals into LCD signals ●Possible interface with monochrome/color LCD driver ●LCD driver interface: 4, 8, 12-bit parallel ●On-chip gray scale palette
Function	Graphic video attribute controller	Memory interface video attribute controller	LCD timing controller	LCD timing controller	LCD timing controller	LCD video interface controller	LCD video interface controller
Package	DP-64S CP-68	CP-68	FP-80	FP-80	FP-80B	FP-100A	FP-100A

*1 Preliminary

Document Image Processor

	DIPP	DICEP	DICEP-A	DICEP-E
Type	**HD63084**	**HD63085**	**HD63183**	**HD63185*1**
Process	CMOS	CMOS	CMOS	CMOS
Supply voltage (V)	5	5	5	5
Operating temperature (°C)	0 to +70	0 to +70	0 to +70	0 to +70
Operating frequency (MHz)	10	8	8	16
Features	●Quick image signal reading: 5M pixels/sec. ●Automatic line density checker ●Bus interface with 68/80 system	●Various coding systems ●Image data DMA transfer: Up to 4 Mbytes/sec. ●Perfect compatibility with GIII/GIV FAX of international standards	●Address space of 4 Mbytes ●Throughput improved by processing on a line/page basis ●FIFO of 2 channels	●On-chip line memory for high-speed encode/decode processing ●16 Mbytes of address space ●Line-by-line alternate encode/decode processing
Function	Document image preprocessor	Document image compression/expansion processor		
Package	DP-64S, FP-64A	PC-72, DP-64S	DP-64S, FP-80A	FP-100A

*1: Under Development

	CPLT				
Type	**HD153108**	**HD153109**	**HD153119**	**HD153110*1**	**HD153129*1**
Process	Hi-BiCMOS	Hi-BiCMOS	Hi-BiCMOS	Hi-BiCMOS	Hi-BiCMOS
Supply voltage (V)	5	5	5	5	5
Operating temperature (°C)	0 to +70	0 to +70	0 to +70	0 to +70	0 to +70
Operating frequency (MHz)	50	65	65	65	65
Features	●Simultaneous display of 256 colors selected from 4,096 ●4-bit D/A conversion on R.G.B. channels ●Overlay display ●On-chip 12-bit × 256-word color palette	●Simultaneous display of 256 colors selected from 260,000 ●6-bit D/A conversion on R.G.B. channels ●Overlay display ●On-chip 18-bit × 256-word color palette	●On-chip 3-channel, 6-bit DAC ●Simultaneous display of 256 colors out of 260,000-color palette ●260,000-color simultaneous display function ●Digital output for color panel control ●On-chip 18-bit × 256-word color palette	●On-chip 3-channel, 8-bit DAC ●Simultaneous display of 256 colors out of 16,700,000-color palette ●16,700,000-color simultaneous display function ●Digital output for color panel control ●On-chip 24-bit × 256-word color palette	●On-chip 3-channel, 6-bit DAC ●Simultaneous display of 256 colors out of 260,000-color palette ●On-chip 18-bit × 256-word color palette ●Digital output for color panel control
Function	Color palette	Color palette	Color palette	Color palette	Color palette
Package	DP-42S, CP-44	CP-44, FP-64B MP-44S	CP-68, FP-80A	FP-80B	DP-28S

*1: Preliminary

Quick Reference Guide

File LSI

	FDC	HDC	FDP	SCSI controller
Type	HD63265	HD63463	HD64950S*1	HD64951
Process	CMOS	CMOS	CMOS	Bi-CMOS
Supply voltage (V)	5	5	5	5
Operating temperature (°C)	0 to +70	0 to +70	0 to +70	0 to +70
Operating frequency (MHz)	16	8		1.5
Feature	●20 types of powerful commands ●On-chip IBM/ECMA-formatted data ●On-chip high-accuracy VFO	●On-chip large data buffer ●ST505/SMD interface support ●Automatic error correction	●Conforms with various drive interfaces ●User-programmable data processing	●High-speed asynchronous transfer of 1.5 Mbytes/sec. (max.) ●Operable as initiator/target ●On-chip driver (48 mA sink)/receiver
Function	Floppy disk controller	Hard disk controller	File data processor	SCSI controller
Package	DP-48, FP-64	DP-48, CP-52	CP-68, FP-80A	MP-68

*1: Preliminary

General I/O LSI

	UPP	UPP-III
Type	HD63140	HD63143
Process	CMOS	CMOS
Supply voltage (V)	5	5
Operating temperature (°C)	−20 to +75*1	−20 to +75*1
Operating frequency (MHz)	4	4
Features	●On-chip 10-bit 10-channel A/D converter ●On-chip 1,024-byte SRAM ●On-chip watch-dog timer ●Pulse input and operation processing by 15 types of commands	●On-chip 1,024-byte SRAM ●Pulse input and operation processing by 15 types of commands ●On-chip two SCIs —Asynchronous —Synchronous
Function	Universal pulse processor	
Package	DP-64S, CP-68	DP-64S, CP-68

Note *1: For wide temperature range version (−40°C to +85°C), ask our service station.

System Control LSI

	S-DPRAM
Type	HD63310R
Process	CMOS
Supply voltage (V)	5
Operating temperature (°C)	0 to +70
Operating frequency (MHz)	—
Features	●Dual port large-capacity buffer space of 1 kbytes ●Access time of 220ns
Function	Smart dual port RAM
Package	DP-48

Digital Signal Processors (DSP)

	DSP	DSP-RAM	DSP-W	DSP-E
Type	**HD61810**	**HD61811**	**HD81810**	**HD81820*1**
Process	CMOS	CMOS	CMOS	CMOS
Supply voltage (V)	5	5	5	5
Operating temperature (°C)	0 to +70	0 to +70	−40 to +85	−20 to +75
Operational system	Floating/fixed point	Floating/fixed point	Floating/fixed point	Floating/fixed point
Instruction set	77	77	77	90
Features	●68 system interface ●Data RAM: 200W×16 bits ●Data ROM: 128W×16 bits ●Instruction ROM: 512W×22 bits	●68 system interface ●Data RAM(1): 200W×16 bits ●Data RAM(2): 128W×16 bits ●Instruction RAM: 512W×22 bits	●68 system interface ●Data RAM: 200W×16 bits ●Data ROM: 128W×16 bits ●Instruction ROM: 512W×22 bits	●Max. 16 bit serial I/O ●68 system interface ●Data RAM: 512W×20 bits ●Data ROM: 512W×20 bits ●Instruction ROM: 2,048W×22 bits
Operation cycle (ns)	250	250	250	100
Product sum operation (ns)	250	250	250	100
Package	DP-40, DC-40, CP-52	PC-68	DP-40	DP-40

	DSP-E	DSP-I
Type	**HD817820*1**	**HD81831Y10*1**
Process	CMOS	CMOS
Supply voltage (V)	5	5
Operating temperature (°C)	0 to +70	0 to +70
Operational system	Floating/fixed point	Floating/fixed point
Instruction set	90	132
Features	●ZTAT version on HD81820 ●Instruction PROM: 2,048W×22 bits ●Data RAM: 512W×20 bits ●Data PROM: 512W×20 bits	●16 bit parallel I/O ●Signal transmission in multiple use ●External extended memory (instruction 15KW data 16MW) direct I/O ●Data RAM internal: 512W×4 pages×16 bits external: 16MW×16 bits ●On-chip instruction RAM: 1,024W×48 bits (external 15KW×48 bits)
Operation cycle (ns)	100	100
Product sum operation (ns)	100	100
Package	DP-40, CP-44	PC-135

*1: Preliminary

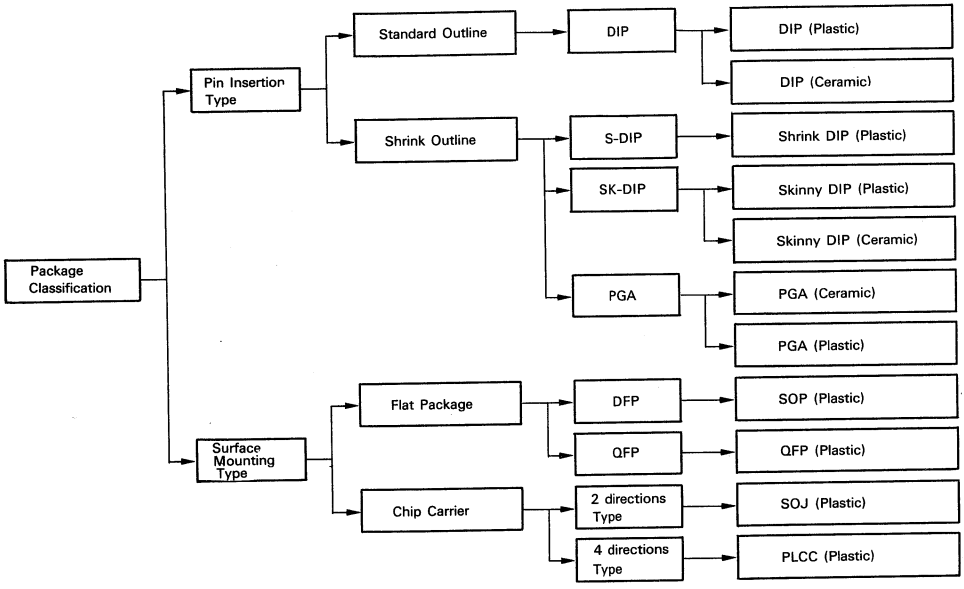
Introduction of Packages

Hitachi microcomputer devices include various types of package which meet a lot of requirements such as ever smaller, thinner and more versatile electric appliances. When selecting a package suitable for the customers' use, please refer to the following for Hitachi microcomputer packages.

1. Package Classification

There are pin insertion types, surface mounting types and multi-function types, applicable to each kind of mounting method. Also, plastic and ceramic materials are offered according to use.

Figure 1 shows the package classification according to the mounting types on the Printed Circuit Board (PCB) and the materials.



DIP; DUAL IN LINE PACKAGE
S-DIP; SHRINK DUAL IN LINE PACKAGE
PGA; PIN GRID ARRAY
DFP; DUAL IN LINE FLAT PACKAGE
QFP; QUAD FLAT PACKAGE
SOP; SMALL OUTLINE PACKAGE
SOJ; SMALL OUTLINE J-LEAD PACKAGE
PLCC; PLASTIC LEADED CHIP CARRIER

Figure 1 Package Classification according to the Mounting Type on the Printed Circuit Board and the Materials.

2. Type No. and Package Code Indication

Type No. of Hitachi 8/16 bit microcomputer peripheral device is followed by package material and outline specifications, as shown below. The package type used for each device is identified by code as follows, illustrated in the data sheet of each device.

When ordering, please write the package code beside the type number.

Type No. Indication



Package Classification

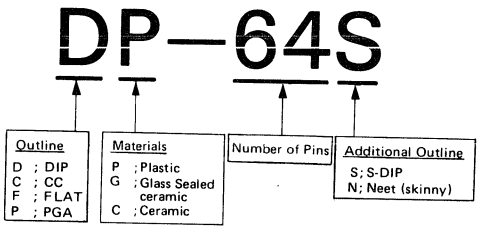
No Indication	; Ceramic DIP
P	; Plastic DIP
F (FP)	; SOP, QFP
CP	; PLCC
Y	; PGA (16-bit microcomputer device)

(Note) The HD63450 with shrink type plastic DIP (DP-64S) has a different type No. from other devices.

Type No.; HD63450PS8

Package designation

Package Code Indication



(Note) PGA packages of 16-bit microcomputer devices have a different indication.

Package Code Indication; PGA-68

Package Classification

Number of Pins

3. Package Dimensional Outline

Hitachi multi-chip microcomputer device employs the packages shown in Table 1 according to the mounting method on the PCB.

Table 1 Package List

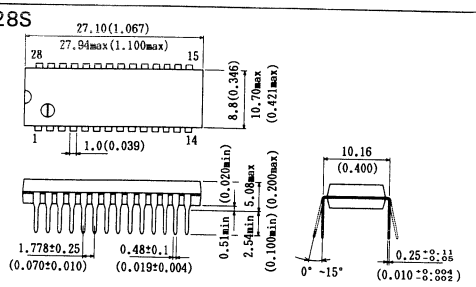
Method of Mounting	Package Classification		Package Material	Package Code
Pin Insertion Type	Standard Outline (DIP)		Plastic	DP-40, DP-48, DP-64
			Ceramic	DC-40, DC-64
	Shrink Outline	S-DIP	Plastic	DP-28S, DP-42S, DP-64S
	Standard Outline	PGA	Glass Sealed Ceramic	PC-68, PC-72, PC-135
Surface Mounting Type	Flat Package	QFP	Plastic	FP-64, FP-64A, FP-64B, FP-80, FP-80A, FP-80B, FP-100A, FP-136, MP-44S, MP-68
	Chip Carrier	PLCC		CP-44, CP-52, CP-68

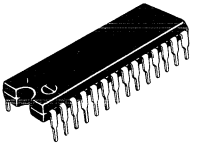
Introduction of packages

Plastic DIP

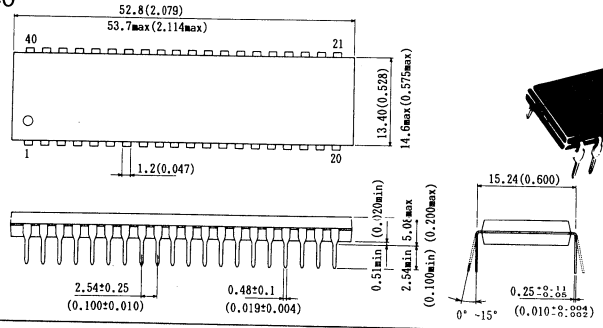
Unit: mm (inch)

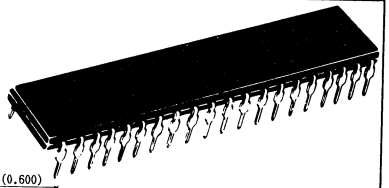
● DP-28S



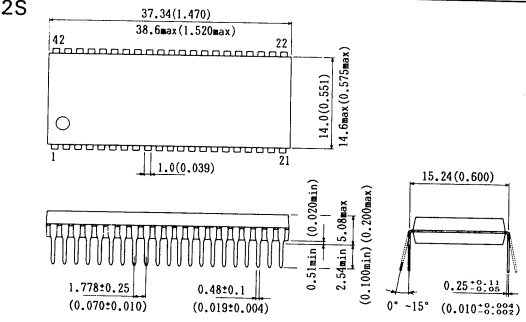


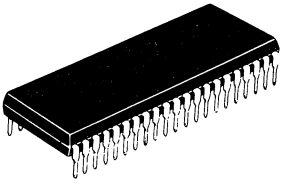
● DP-40



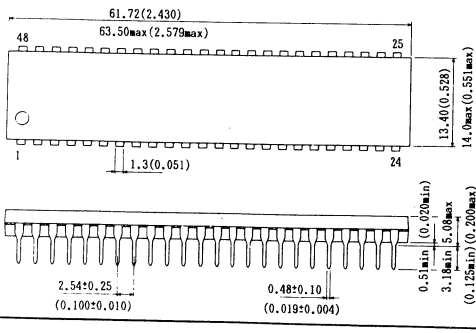


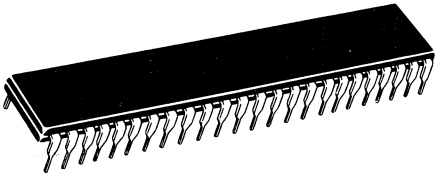
● DP-42S





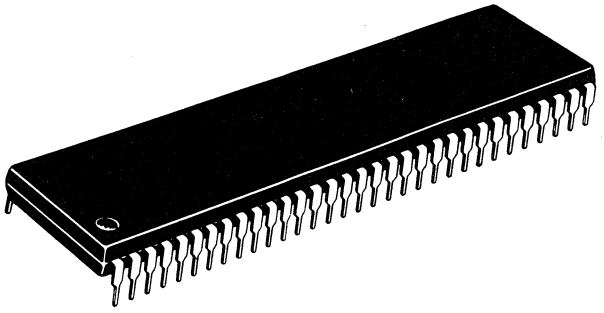
● DP-48

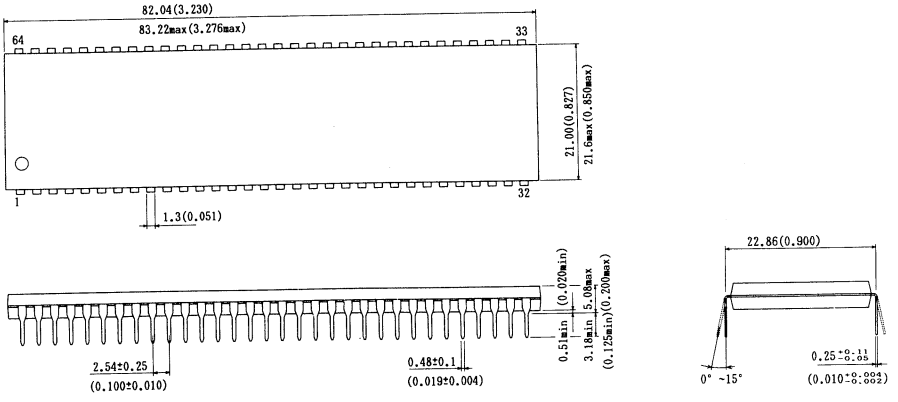




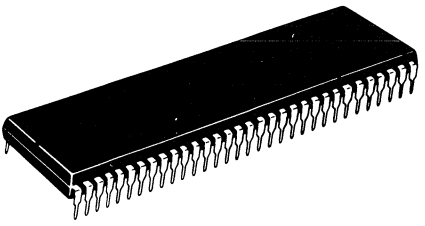
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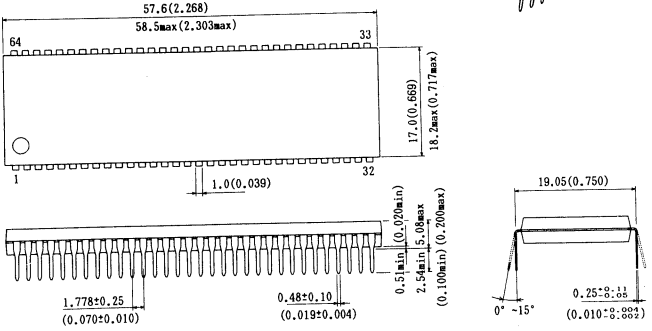
● DP-64





● DP-64S



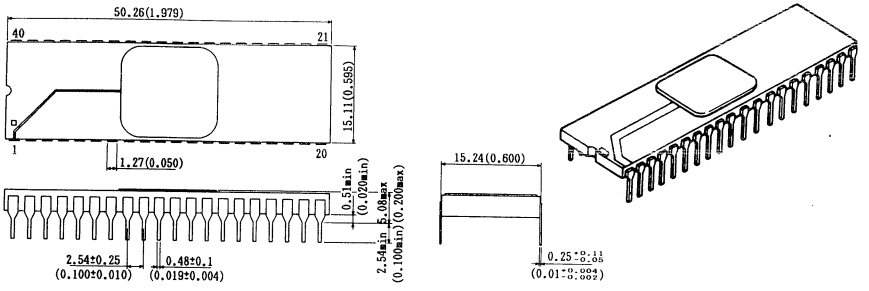


Introduction of packages

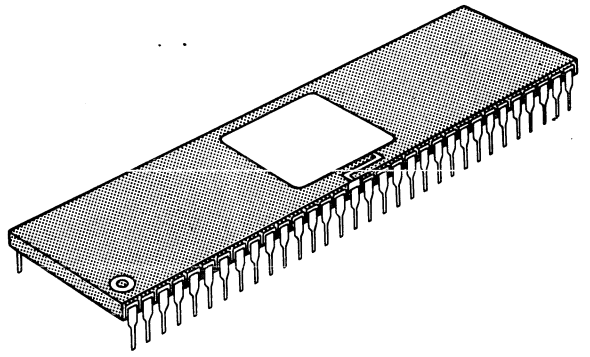
Ceramic DIP

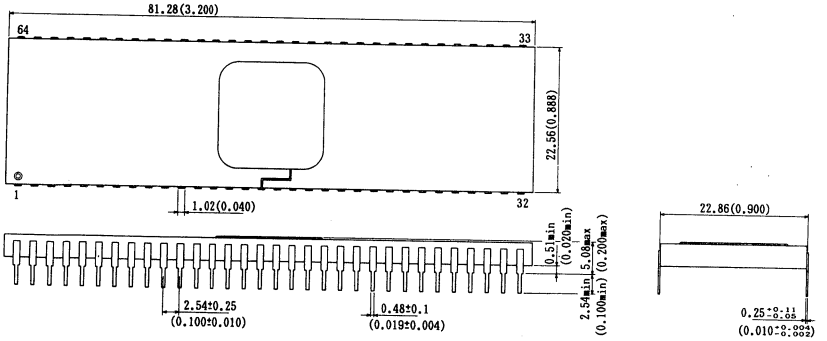
Unit: mm (inch)

● DC-40



● DC-64

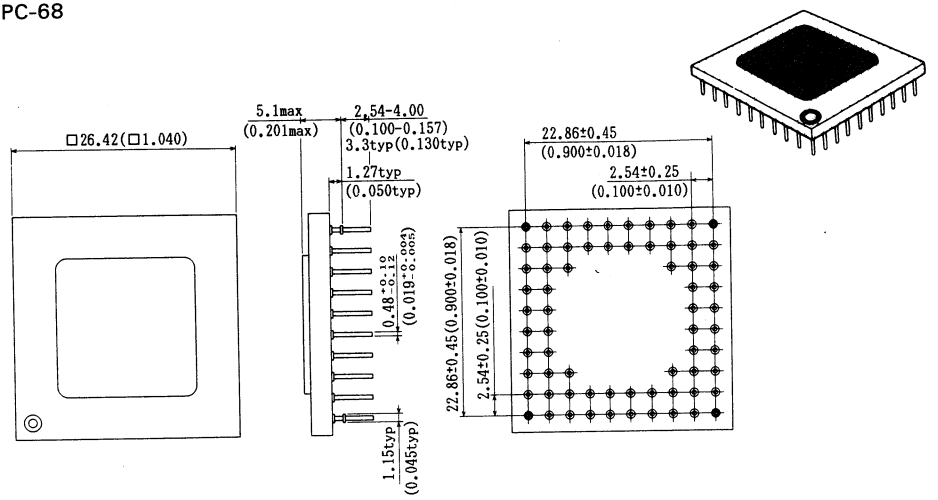




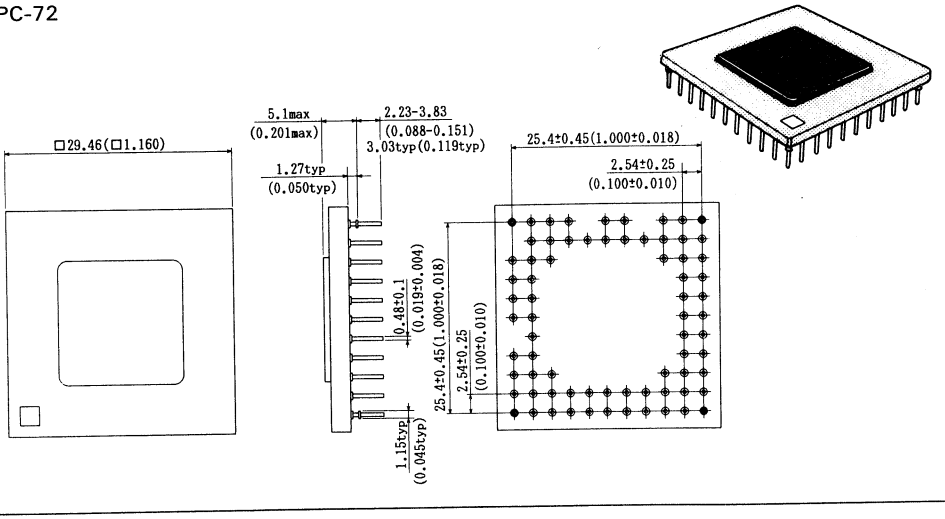
Pin grid array

Unit: mm (inch)

● PC-68



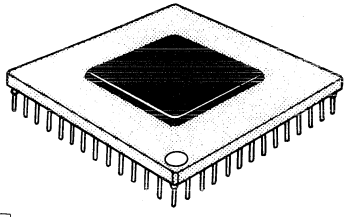
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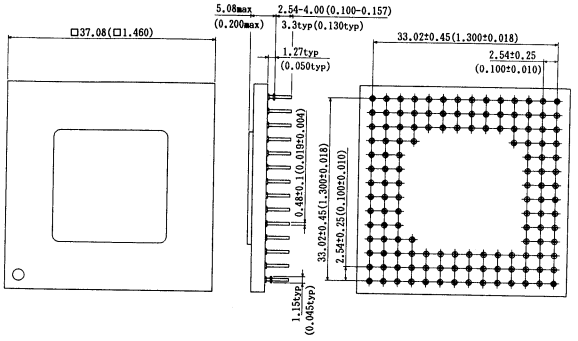


Introduction of packages

Unit: mm (inch)

● PC-135

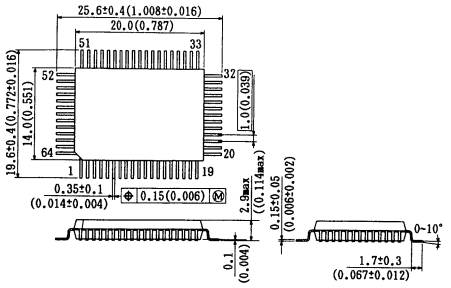




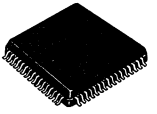
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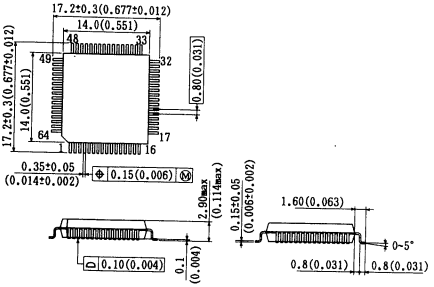
● FP-64





● FP-64A

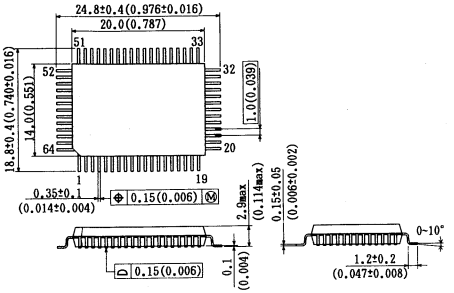




HITACHI

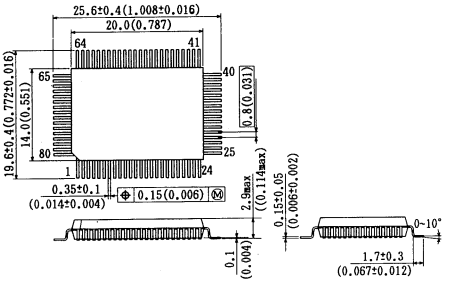
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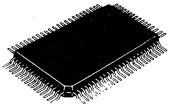
● FP-64B



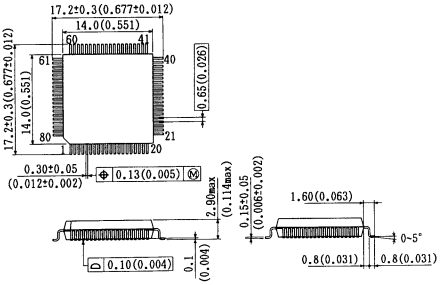


● FP-80



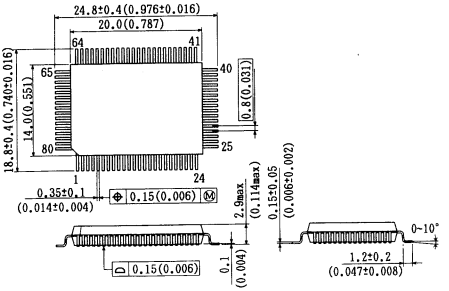


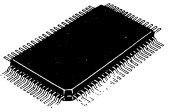
● FP-80A





● FP-80B

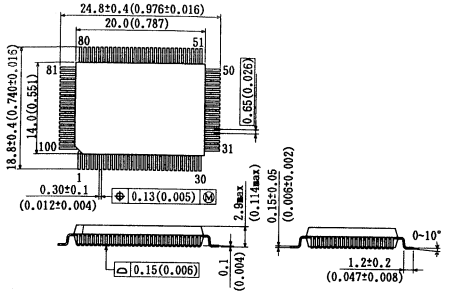


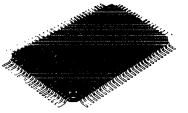


Introduction of packages

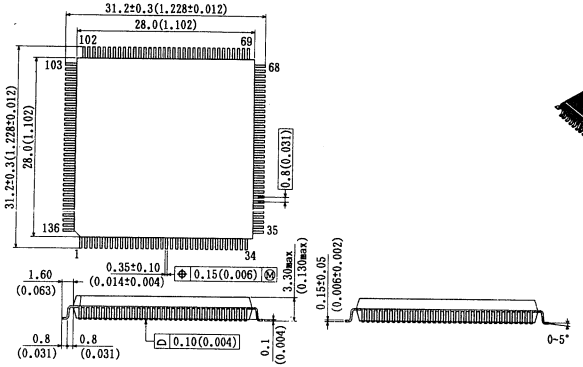
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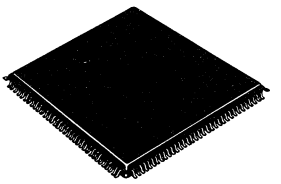
● FP-100A



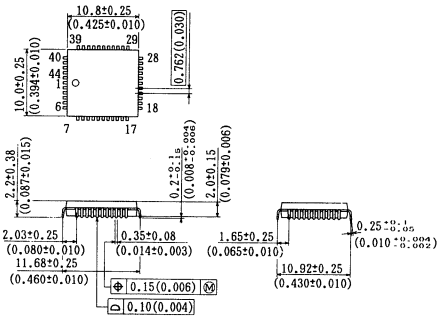


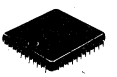
● FP-136





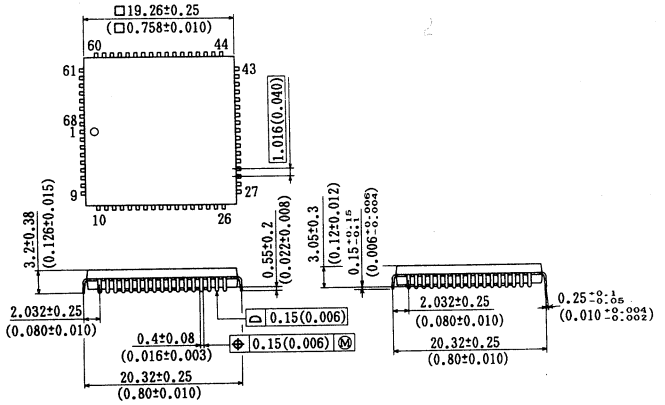
● MP-44S





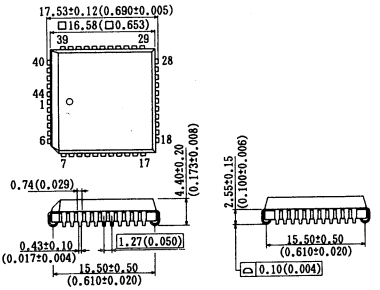
Unit: mm (inch)

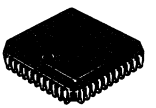
● MP-68



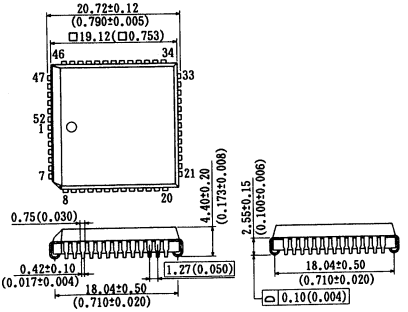
Chip carrier

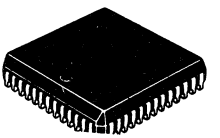
● CP-44





● CP-52

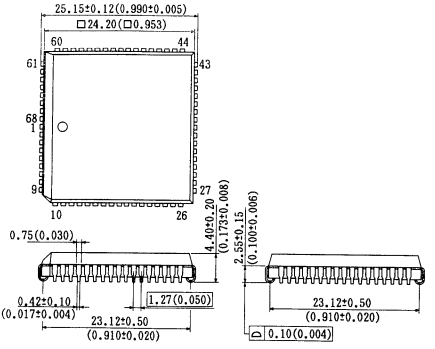


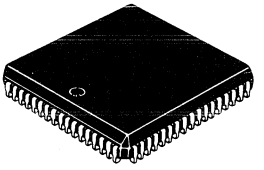


Introduction of packages

Unit: mm (inch)

● CP-68





4. Mounting Method on Board

Lead pins of the package have surface treatment, such as solder coating or solder plating, to make them easy to mount on the PCB. The lead pins are connected to the package by eutectic solder. The following explains the common connecting method of leads and precautions.

4.1 Mounting Method of Pin Insertion Type Package

Insert lead pins of the package into through-holes (usually about ϕ0.8mm) on the PCB. Soak the lead part of the package in a wave solder tub.

Lead pins of the package are held by the through-holes. Therefore, it is easy to handle the package through the process up to soldering, and easy to automate the soldering process. When soldering the lead part of the package in the wave solder tub , be careful not to get the solder on the package, because the wave solder will damage it.

4.2 Mounting Method of Surface Mounting Type Package

Apply the specified quantity of solder paste to the pattern on any printed board by the screen printing method, and put a package on it. The package is now temporarily fixed to the printed board by the surface tension of the paste. The solder paste melts when heated in a reflowing furnace, and the leads of the package and the pattern of the printed board are fixed together by the surface tension of the melted solder and the self alignment.

The size of the pattern where the leads are attached, partly depending on paste material or furnace adjustment, should be 1.1 to 1.3 times the leads' width.

The temperature of the reflowing furnace depends on package material and also package types. Fig. 2 lists the adjustment of the reflowing furnace for QFP. Pre-heat the furnace to 150°C The surface temperature of the resin should be kept at 235°C max. for 10 minutes or less.

(1) The temperature of the leads should be kept at 260°C for 10 minutes or less.
(2) The temperature of the resin should be kept at 235°C for 10 minutes or less.
(3) Below is shown the temperature profile when soldering a package by the reflowing method.

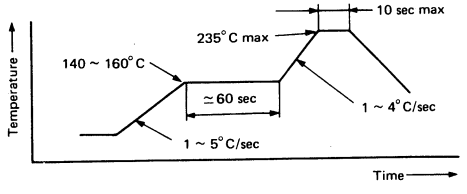


Figure 2 Reflowing Furnace Adjustment for QFP

Ensure good heater or temperature controls because the material of a plastic package is black epoxy-resin which damages easily. When an infrared heater is used, if the temperature is higher than the glass transition point of epoxy-resin (about 150°C), for a long time, the package may be damaged and the reliability lowered. Equalize the temperature inside and outside the packages by lessening the heat of the upper surface of the packages.

Leads of QFP may be easily bent under shipment or during handling and cannot be soldered onto the printed board. If they are, heat the bent leads again with a soldering iron to reshape them.

Use a rosin flux when soldering. Don't use a chloric flux because the chlorine in the flux tends to remain on the leads and lower the reliability of the product.

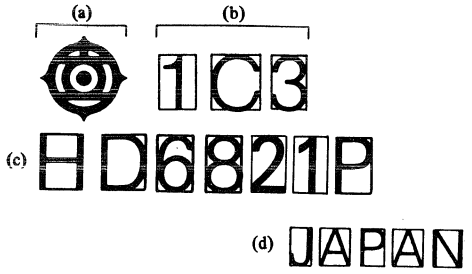
Even if you use a rosin flux, remaining flux can cause the leads to deteriorate. Some cleaning liquids may make the mark on the devices illegible if the devices remain too long in contact with those liquids.

5. Marking

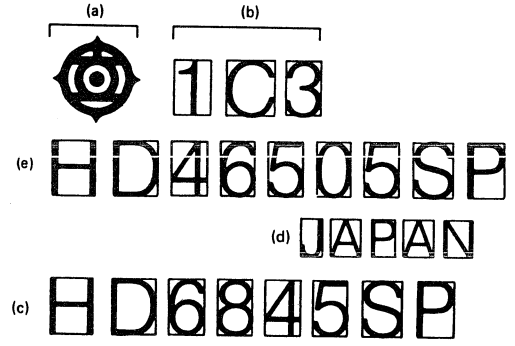
Hitachi trademark, product type No., etc. are printed on packages. Case I and Case II give examples of marks and Nos. Case I applies to products which have only a standard type No. Case II applies to products which have an old type No. and a standard type No.

Introduction of packages

Case I; Includes a standard type No.



Case II; Includes an old type No. and a standard type No.



Meaning of Each Mark

(a)	Hitachi Trademark
(b)	Lot Code
(c)	Standard Type No.
(d)	Japan Mark
(e)	Old Type No.

Reliability and Quality Assurance

1. VIEWS ON QUALITY AND RELIABILITY

Hitachi basic views on quality are based on the principle that manufacturers should make products from the standpoint of customers with their need and expectations. It is ideal to make such product as will meet the customers requirement 100%. To fill this gap Hitachi has made best effort below.

(1) Build the reliability in design at the stage of new product development.
(2) Build the quality at the sources of manufacturing process.
(3) Execute the harder inspection and reliability confirmation of final products.
(4) Make quality level higher with field data feed back.
(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely sude and execution of design standardization, device design (including process design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishment of design rule, and standardization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices, only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by TEG (Test element group)

TEG is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of TEG are as follows;
   - Making clear about fundamental failure mode
   - Analysis of relation between failure mode and manufacturing process condition
   - Search for failure mechanism analysis
   - Establishment of QC point in manufacturing
2. Effectiveness of evaluation by TEG are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

   etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competitive power of products, the major purpose of design review is to ensure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows;

(1) Description of the products based on specified design documents.
(2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub-program of calculation, experiments, investigation, etc. will be carried out.
(3) Determine contents of reliability and methods, etc. based on design document and drawing.
(4) Check process ability of manufacturing line to achieve design goal.
(5) Discussion about preparation for production.
(6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.
(7) Reference of past failure experiences with similar devices, confirmation of method to prevent them, and planning and execution of test program for confirmation of them. These studies and decisions are made using check lists made individually depending on the objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows;

(1) Problems in individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.
(2) Feedback of information should be made to ensure satisfied level of process ability.
(3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To ensure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2.

The views on quality approval are as follows;

(1) The inspection section performs approval objectively from the standpoint of customers.
(2) Fully consider past failure experiences and information from field.
(3) Approval is needed for design change and work change.
(4) Intensive approval is executed on parts material and process.
(5) Study process ability and fluctuation factor, and set up control points at mass production stage.

Considering the views mentioned above, quality approval shown in Figure 1 is performed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total

function flow is shown in Figure 2. The main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices are getting higher, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

The other activities of quality assurance are as follows:

(1) Outside Vendor Technical Information Meeting
(2) Approval on outside vendors, and guidance of outside vendors
(3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments,

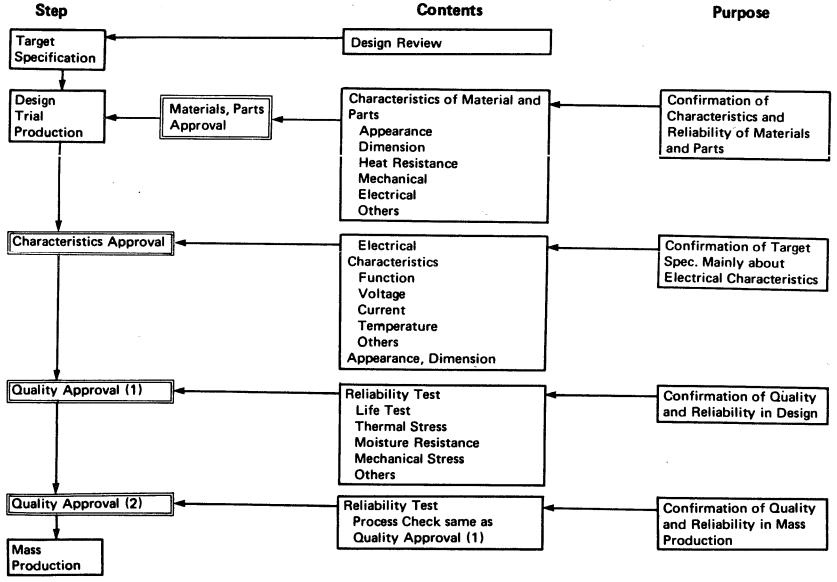


Figure 1 Flow Chart of Quality Approval

circumstances and sub-materials. The quality control in the manufacturing process is shown in Figure 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and the quality control in the manufacturing process is tightly executed – rigid check in each process and each lot, 100% inspection in appropriate ways to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semifinal products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of countermeasures
- Transmission of information about quality

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Equipments for manufacturing semiconductor devices have been developing extraordinarily with necessary high performance devices and improvement of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain proper operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are checked one by one not to make any omission. As for adjustment and maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-materials

Quality and reliability of semiconductor device is highly

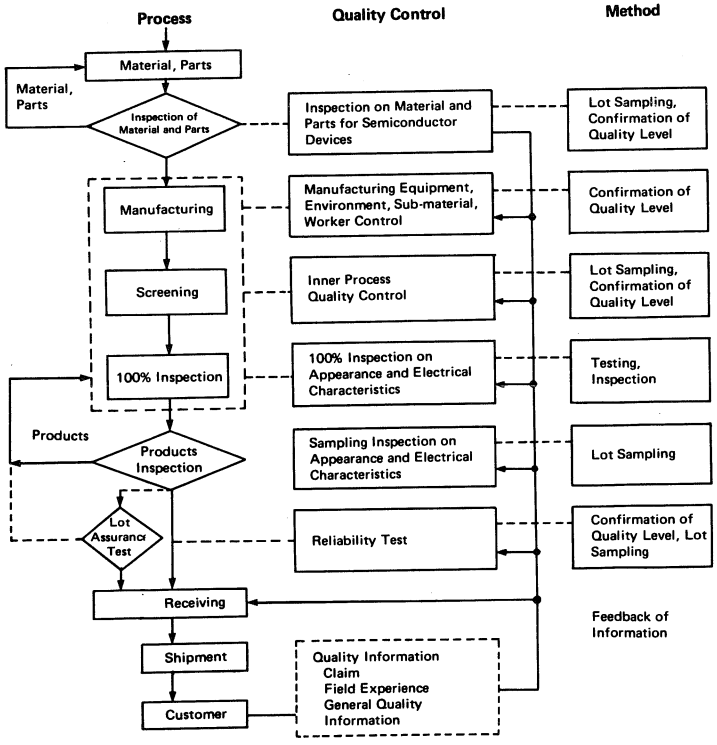


Figure 2 Flow Chart of Quality Control in Manufacturing Process

affected by manufacturing process. Therefore, the controls of manufacturing circumstances – temperature, humidity, particle – and the control of submaterials – gas, pure water – used in manufacturing process are intensively executed. Particle control is described in more detail below.

Particle control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, air-conditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating particle in room, falling particle and dirtiness of floor.

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Periodical Reliability Test

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

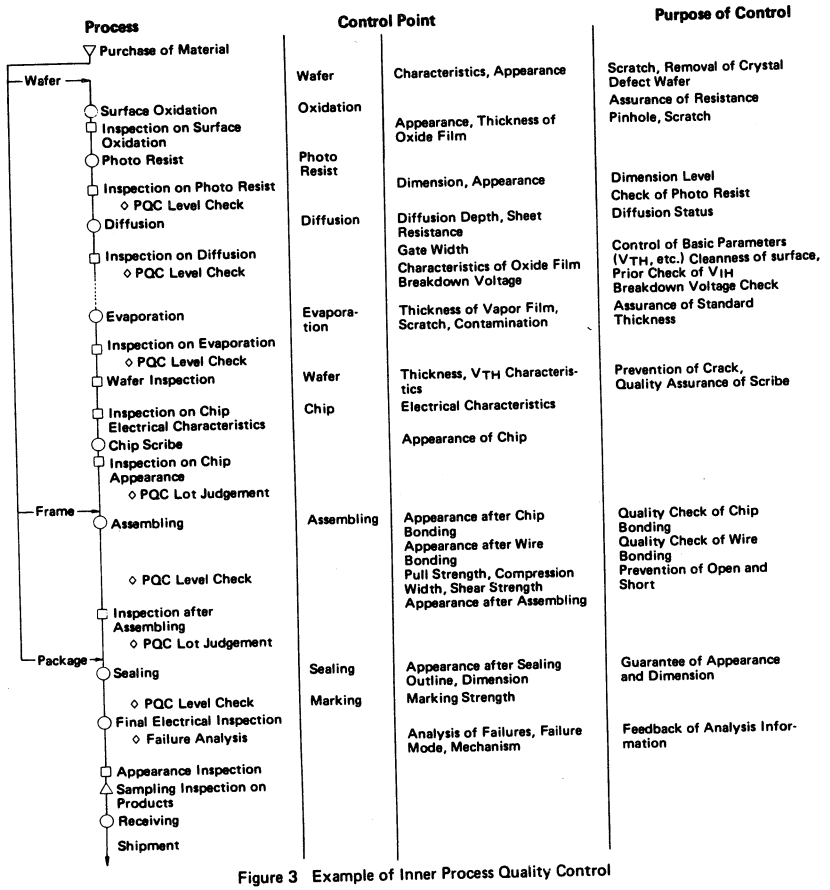


Figure 3 Example of Inner Process Quality Control

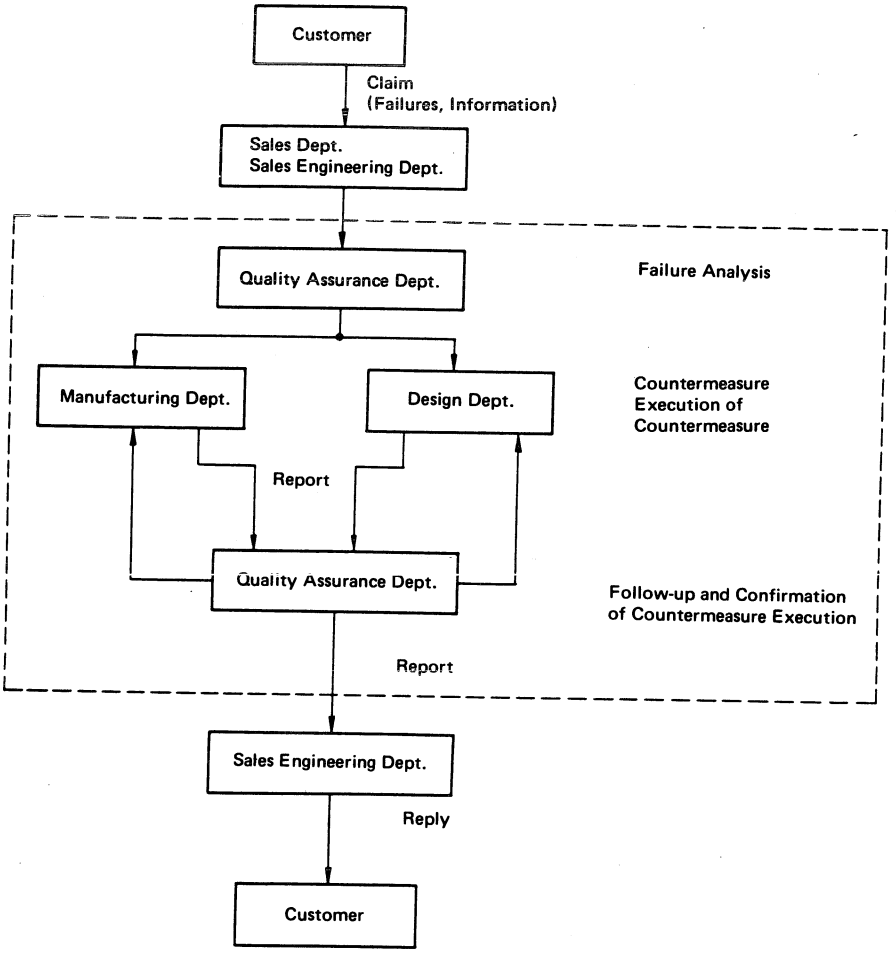


Figure 4 Process Flow Chart of Field Failure

Reliability Test Data of Microcomputer

1. INTRODUCTION

Microcomputer is required to provide higher reliability and quality with increasing function, enlarging scale and widening application. To meet this demand, Hitachi is improving the quality by evaluating reliability, building up quality in process, strengthening inspection and analyzing field data etc..

This chapter describes reliability and quality assurance data for Hitachi 8-bit and 16-bit microcomputer Peripheral based on test and failure analysis results. More detail data and new information will be reported in another reliability data sheet.

2. PACKAGE AND CHIP STRUCTURE

2.1 Package

The reliability of plastic molded types has been greatly improved, recently their applications have been expanded to automobiles measuring and control systems, and computer terminal equipment operated under relatively severe conditions and production output and application of plastic molded types will continue to increase.

To meet such requirements, Hitachi has considerably improved moisture resistance, operation stability, and chip and plastic manufacturing process.

Plastic and ceramic package type structure are shown in Figure 1 and Table 1.

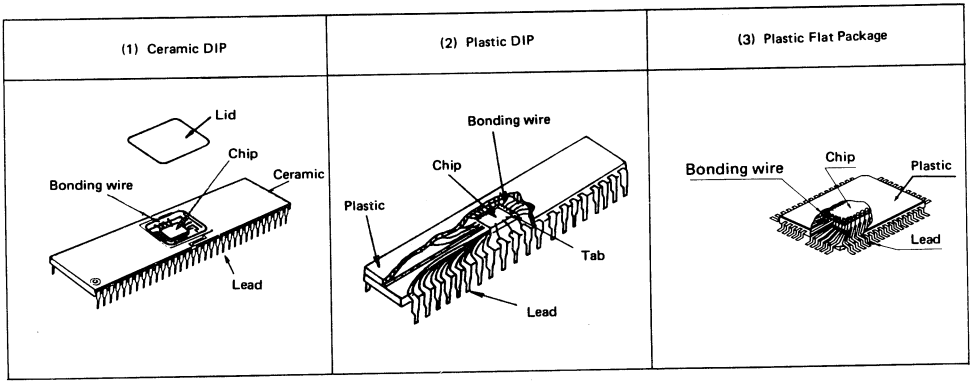


Figure 1 Package Structure

Table 1 Package Material and Properties

Item	Ceramic DIP	Plastic DIP	Plastic Flat Package
Package	Alumina	Epoxy	Epoxy
Lead	Tin plating Brazed Alloy 42	Solder dipping Alloy 42 or Cu	Solder plating Alloy 42 or Cu
Seal	Au-Sn Alloy	N.A	N.A
Die bond	Au-Si	Au-Si or Ag paste	Au-Si or Ag paste
Wire bond	Ultrasonic	Thermo compression	Thermo compression
Wire	Al	Au	Au

2.2 Chip Structure

Hitachi microcomputers are produced in NMOS E/D technology or low power CMOS technology. Si-gate process is used in both types because of high reliability and high density. Chip structure and basic circuit are shown in Figure 2.

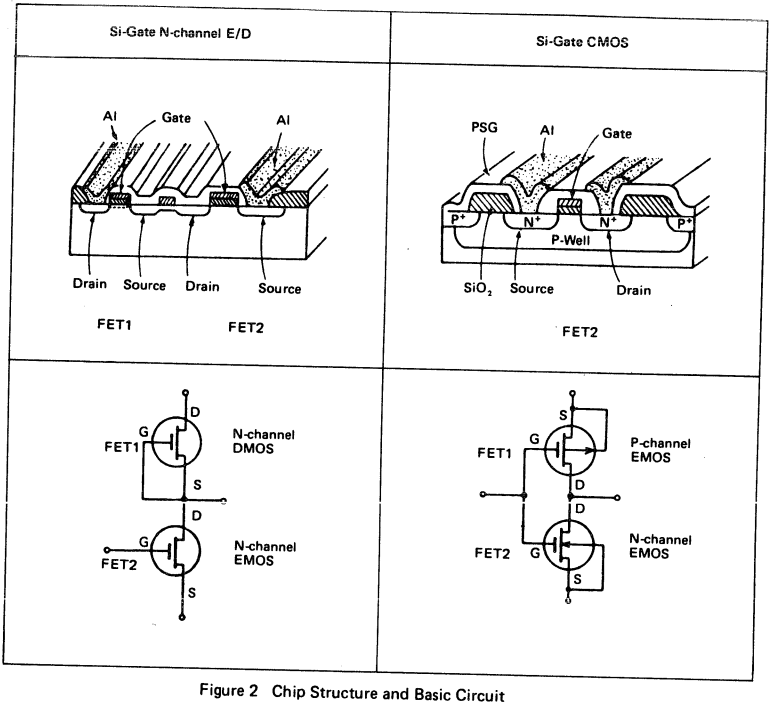


Figure 2 Chip Structure and Basic Circuit

3. QUALITY QUALIFICATION AND EVALUATION

3.1 Reliability Test Methods

Reliability test methods shown in Table 2 are used to qualify and evaluate the new products and new process.

Table 2 Reliability Test Methods

Test Items	Test Condition	MIL-STD-883B Method No.
Operating Life Test	125°C, 1000hr	1005,2
High Temp, Storage	Tstg max, 1000hr	1008,1
Low Temp, Storage	Tstg min, 1000hr	
Steady State Humidity	65°C 95%RH, 1000hr	
Steady State Humidity Biased	85°C 85%RH, 1000hr	
Temperature Cycling	-55°C ~ 150°C, 10 cycles	1010,4
Temperature Cycling	-20°C ~ 125°C, 200 cycles	
Thermal Shock	0°C ~ 100°C, 100 cycles	
Soldering Heat	260°C, 10 sec	1011,3
Mechanical Shock	1500G 0.5 msec, 3 times/X, Y, Z	
Vibration Fatigue	60Hz 20G, 32hrs/X, Y, Z	2002,2
Variable Frequency	20~2000Hz 20G, 4 min/X, Y, Z	2005,1
Constant Acceleration	20000G, 1 min/X, Y, Z	2007,1
Lead Integrity	225gr, 90° 3 times	2001,2
		2004,3

3.2 Reliability Test Result

Reliability Test Result of microcomputer Peripheral devices is shown in Table 3 to Table 8. There is little difference according to device series, as the design and production process, etc. are standardized.

Table 3. Dynamic Life Test

(Ta = 125°C)

Type No.	Sample Size	Component Hours	Failures
HD6345P	45	45000	0
HD6445P	45	45000	0
HD63265P	80	80000	0
HD63310P	70	70000	0
HD63645F	50	50000	0
HD64645F	50	50000	0
HD63140P	90	90000	0
HD63143P	90	90000	0
HD66840F	45	45000	0
HD63463P	45	45000	0
HD63484P	80	80000	0
HD63485P	45	45000	0
HD63486P	45	45000	0
HD63487CP	45	45000	0
HD63084P	45	45000	0
HD63085P	45	45000	0
HD81810P	45	45000	0
HD153108P	70	70000	0
HD153109F	50	50000	0
HD153119F	22	22000	0
Total	1102	1102000	0

Estimated Field Failure Rate = 0.084% / 1000 Hours at Ta = 125°C
(Confidence Level 60%)

Table 4. High Temperature, High Humidity Test

(1) 85°C, 85% RH Bias Test

Type No.	V_{cc} Bias	168 Hours	500 Hours	1000 Hours
HD6345P	5.5V	0/22	0/22	0/22
HD6445P	5.5V	0/22	0/22	0/22
HD63265P	5.5V	0/22	0/22	0/22
HD63310P	5.5V	0/22	0/22	0/22
HD63645F	5.5V	0/22	0/22	0/22
HD64645F	5.5V	0/22	0/22	0/22
HD63463P	5.5V	0/22	0/22	0/22
HD63484P	5.5V	0/22	0/22	0/22
HD63085P	5.5V	0/45	0/45	0/45
HD81810P	5.5V	0/45	0/45	0/45
Total		0/266	0/266	0/266

Reliability Test Data of Microcomputer

(2) High Temperature – High Humidity Storage Life Test

Type No.	Condition	168 Hours	500 Hours	1000 Hours
HD6345P	65°C 95%RH	0/110	0/110	0/110
HD6445P	65°C 95%RH	0/100	0/100	0/100
HD63265P	65°C 95%RH	0/110	0/110	0/110
HD63310P	65°C 95%RH	0/100	0/100	0/100
HD63645F	65°C 95%RH	0/95	0/95	0/95
HD64645F	65°C 95%RH	0/100	0/100	0/100
HD63140P	65°C 95%RH	0/77	0/77	0/77
HD66840F	65°C 95%RH	0/45	0/45	0/45
HD63463P	65°C 95%RH	0/100	0/100	0/100
HD63484P	65°C 95%RH	0/100	0/100	0/100
HD63486P	65°C 95%RH	0/45	0/45	0/45
HD63487CP	65°C 95%RH	0/45	0/45	0/45
HD63084P	65°C 95%RH	0/60	0/60	0/60
HD63085P	65°C 95%RH	0/70	0/70	0/70
HD81810P	65°C 95%RH	0/60	0/60	0/60
HD153109F	65°C 95%RH	0/45	0/45	0/45

(3) Pressure Cooker Test
(Condition; 2atm 121°C)

Type No.	40 Hours	60 Hours	100 Hours	200 Hours
HD6345P	0/22	0/22	0/22	–
HD6445P	0/22	0/22	0/22	–
HD63265P	0/22	0/22	0/22	–
HD63310P	0/22	0/22	0/22	–
HD63645F	0/22	0/22	0/22	–
HD64645F	0/22	0/22	0/22	–
HD63140P	0/22	0/22	0/22	–
HD66840F	0/22	0/22	0/22	–
HD63463P	0/22	0/22	0/22	–
HD63484P	0/22	0/22	0/22	–
HD63485P	0/22	0/22	0/22	–
HD63486P	0/22	0/22	0/22	–
HD63487CP	0/22	0/22	0/22	–
HD63084P	0/22	0/22	0/22	–
HD81810P	0/22	0/22	0/22	0/22
HD153108P	0/22	0/22	0/22	–
HD153109F	0/22	0/22	0/22	–
HD153119F	0/22	0/22	0/22	–

Table 5. Temperature Cycling Test

(-55°C to 25°C to 150°C)

Type No.	10 Cycles	100 Cycles	200 Cycles
HD6345P	0/45	0/45	0/45
HD6445P	0/45	0/45	0/45
HD63265P	0/45	0/45	0/45
HD63310P	0/45	0/45	0/45
HD63645F	0/45	0/45	0/45
HD64645F	0/45	0/45	0/45
HD63140P	0/45	0/45	0/45
HD66840F	0/45	0/45	0/45
HD63463P	0/45	0/45	0/45
HD63484P	0/45	0/45	0/45
HD63485P	0/45	0/45	0/45
HD63486P	0/45	0/45	0/45
HD63487CP	0/45	0/45	0/45
HD63084P	0/100	—	—
HD63085P	0/45	0/45	—
HD81810P	0/45	0/45	0/45
HD153108P	0/45	0/45	0/45
HD153109F	0/45	0/45	0/45
HD153119F	0/45	0/45	0/45

Table 6. High Temperature, Low Temperature Storage Life Test

Temperature	168 Hours	500 Hours	1000 Hours
150°C	0/237	0/237	0/237
-55°C	0/237	0/237	0/237

Table 7. Mechanical and Environmental Test (8-bit microcomputer peripheral)

Test Item	Condition	Plastic DIP		Ceramic Package	
		Sample Size	Failure	Sample Size	Failure
Thermal Shock	0°C ~ 100°C 10 cycles	110	0	22	0
Soldering Heat	260°C, 10 sec.	180	0	44	0
Solderability	230°C, 5 sec. Rosin flux	159	0	22	0
Mechanical Shock	1500G, 0.5 ms 3 times/X, Y, Z	110	0	22	0
Vibration Fatigue	60 Hz, 20G 32 hrs/X, Y, Z	110	0	22	0
Vibration Variable Freq.	100 ~ 2000 Hz 20G, 4 times/X, Y, Z	110	0	22	0
Lead Integrity	250 g, 90° Bonding 3 times	65	0	22	0
He leak	1×10^{-8} cc/sec.	—	—	44	0
Bubble leak		—	—	44	0

Table 8. Mechanical and Environmental Test (16-bit microcomputer peripheral)

Test Item	Condition	Result
High Temperature Storage	Ta = 150°C, 1000 hrs	0/22
Low Temperature Storage	Ta = −55°C, 1000 hrs	0/42
Temperature Cycling (1)	−55°C ~ 25°C ~ 150°C 10 cycles	0/45
Temperature Cycling (2)	−20°C ~ 25°C ~ 125°C 500 cycles	0/22
Thermal Shock	−55°C ~ 125°C 15 cycles	0/22
Soldering heat	260°C, 10 sec	0/22
Solderability	230°C, 5 sec	0/22
Mechanical Shock	1500G, 0.5 msec 3 times/X, Y, Z	0/22
Vibration Variable Freq.	100 ~ 2000 Hz, 20G 4 times/X, Y, Z	0/22
Constant Acceleration	20000G 1 min/X, Y, Z	0/22

4. PRECAUTION

4.1 Storage

It is preferable to store semiconductor devices in the following ways to prevent detrioration in their electrical characteristics, solderability, and appearance, or breakage.

(1) Store in an ambient temperature of 5 to 30°C, and in a relative humidity of 40 to 60%.
(2) Store in a clean air environment, free from dust and active gas.
(3) Store in a container which does not induce static electricity.
(4) Store without any physical load.
(5) If semiconductor devices are stored for a long time, store them in the unfabricated form. If their lead wires are formed beforehand, bent parts may corrode during storage.
(6) If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at -30°C or lower. Unpacked devices must not be stored for over 3 months.
(7) Take care not to allow condensation during storage due to rapid temperature changes.

4.2 Transportation

As with storage methods, general precautions for other electronic component parts are applicable to the transportation of semiconductors, semiconductor-incorporating units and other similar systems. In addition, the following considerations must be given, too:

(1) Use containers or jigs which will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive container or aluminium foil.
(2) In order to prevent device breakage from clothes-induced static electricity, workers should be properly grounded with a resistor while handling devices. The resistor of about 1 M ohm must be provided near the worker to protect from electric shock.
(3) When transporting the printed circuit boards on which semiconductor devices are mounted, suitable preventive measures against static electricity induction must be taken; for example, voltage built-up is prevented by shorting terminal circuit. When a belt conveyor is used, prevent the conveyor belt from being electrically charged by applying some surface treatment.
(4) When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock.

4.3 Handling for Measurement

Avoid static electricity, noise and surge-voltage when semiconductor devices are measured. It is possible to prevent breakage by shorting their terminal circuits to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, their terminals are left open to provide the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, belt conveyor, etc. The device will fail if it touches something which leaks current or has a static charge. Take care not to allow curve tracers, synchroscopes, pulse generators, D.C. stabilizing power supply units etc. to leak current through their terminals or housings.

Especially, while the devices are being tested, take care not to apply surge voltage from the tester, to attach a clamping circuit to the tester, or not to apply any abnormal voltage through a bad contact from a current source.

During measurement, avoid miswiring and short-circuiting. When inspecting a printed circuit board, make sure that no soldering bridge or foreign matter exists before turning on the power switch.

Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further details.

4.4 Soldering

Semiconductor devices should not be left at high temperatures for a long time. Regardless of the soldering method, soldering must be done in a short time and at the lowest possible temperature. Soldering work must meet soldering heat test conditions, namely, 260°C for 10 seconds and 350°C for 3 seconds at a point 1 to 1.5 mm away from the end of the device package.

Use of a strong alkali or acid flux may corrode the leads, deteriorating device characteristics. The recommended soldering iron is the type that is operated with a secondary voltage supplied by a transformer and grounded to protect from lead current. Solder the leads at the farthest point from the device package.

4.5 Removing Residual Flux

To ensure the reliability of electronic systems, residual flux must be removed from circuit boards. Detergent or ultrasonic cleaning is usually applied. If chloric detergent is used for the plastic molded devices, package corrosion may occur. Since cleaning over extended periods or at high temperatures will cause swollen chip coating due to solvent permeation, select the type of detergent and cleaning condition carefully. Lotus Solvent and Dyfron Solvent are recommended as a detergent. Do not use any trichloroethylene solvent. For ultrasonic cleaning, the following conditions are advisable:

- Frequency: 28 to 29 kHz (to avoid device resonation)
- Ultrasonic output: 15W/ℓ
- Keep the devices out of direct contact with the power generator.
- Cleaning time: Less than 30 seconds

4.6 Precautions when using surface mount packages

(1) Internal temperature distribution

The most common method used for mounting surface mount packages is the infrared reflow method. Since packages are made of black epoxy resin, they are prone to heat absorption and high temperatures when exposed directly to infrared rays. In figure 3, the temperature of the surface directly exposed to the infrared rays is 20–30°C higher than the soldered leads and 40–50°C higher than the bottom surface of the package. Under these conditions it is possible that reflow operation results in cracks of the packages.

To overcome this problem, Hitachi recommends using white metal covers over the resin surfaces of packages to reflect the infrared rays during the infrared reflow procedure. When a 2 mm thick aluminum reflective plate is used as a cover, resin surfaces and the bottom of the packages are kept at 175°C for a peak lead temperature of 240°C.

(2) Moisture absorption

The epoxy resin used for plastic packages is prone to absorb moisture when stored in areas of high humidity. During soldering a high amount of moisture absorption results in sudden vaporization, peeling of the resin/lead frame surfaces, and in the worst case, cracking of the package. Therefore it is very important to store packages, especially thin packages, within a moisture proof environment.

To avoid the effects of moisture absorption during shipment, storage or handling, it is recommended to bake the packages for 16 to 24 hours at 125°C before the soldering process.

(3) Sudden temperature changes

Another method used for the soldering of components is the flow solder dipping method. When compared with the reflow method, however, the heat transfer coefficient for this method is much higher. As a result, thermal shock to the plastic components will increase, the formation of cracks in the package will develop, and moisture resistance will be reduced. Therefore, we recommend flow solder dipping method to not be used.

Even with the reflow method, sudeen temperature rises of falls should be avoided. Temperature changes should be kept below a rate of 4°C/second.

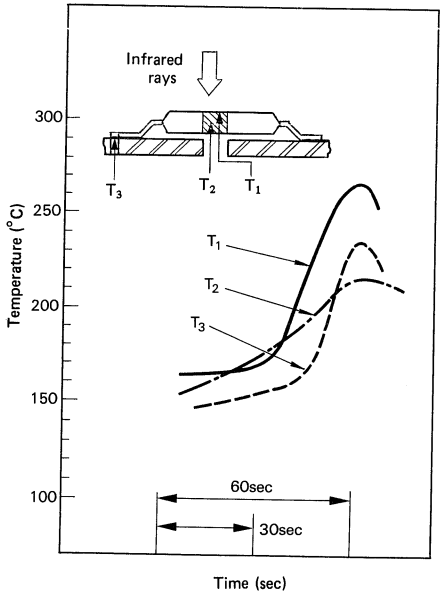


Figure 3 Temperature Profile During Infrared Head Soldering (Example)

(4) Ambient pollutants

It is recommended that rosin flux be used during the soldering process. Chlorine-contained flux should not be used because it tends to leave chlorine deposits around the package, contributing to a loss of product reliability.

Even in the case of rosin flux, care must be taken to sufficiently clean and remove any flux residue. Rosin flux residue can cause corrosion of the package leads. Some cleaning liquids may make the mark on the devices illegible if the devices remain too long in contact with those liquids.

The above are all general precautions, but the actual individual reflow conditions will vary in accordance with package configuration, board size the reflow method being employed and the equipment being used. As a point of reference, figure 4 shows a reflow condition example in which a QFP infrared reflow oven is used. The values inside of the figure are package resin temperatures, but the leads must be raised to a maximum temperature of 260°C for less than ten seconds.

Although the infrared reflow method is the most common, other methods such as the vapor-phase reflow method, can also be used. Figure 5 shows the reflow conditions for the vapor-phase reflow method.

Finally, you should consult with the mounting manual of the particular surface mounting package being used for further details. Should you have any questions or points which demand more clarification, consult with your local Hitachi representative.

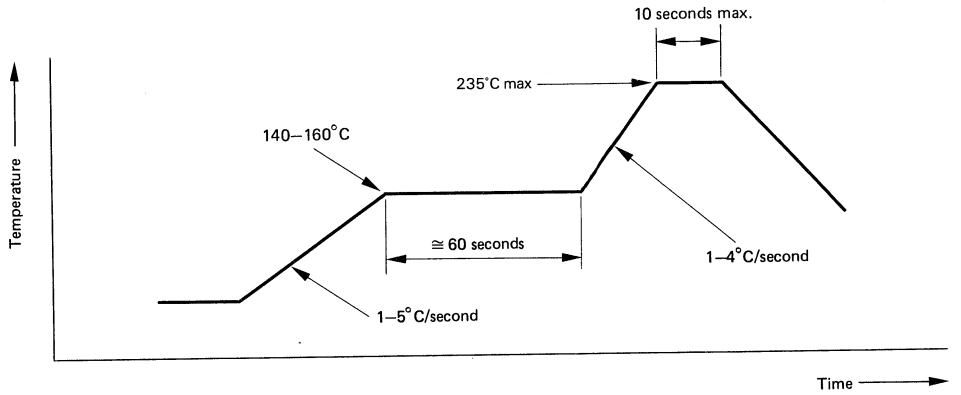


Figure 4 Recommended Reflow Conditions for QFP

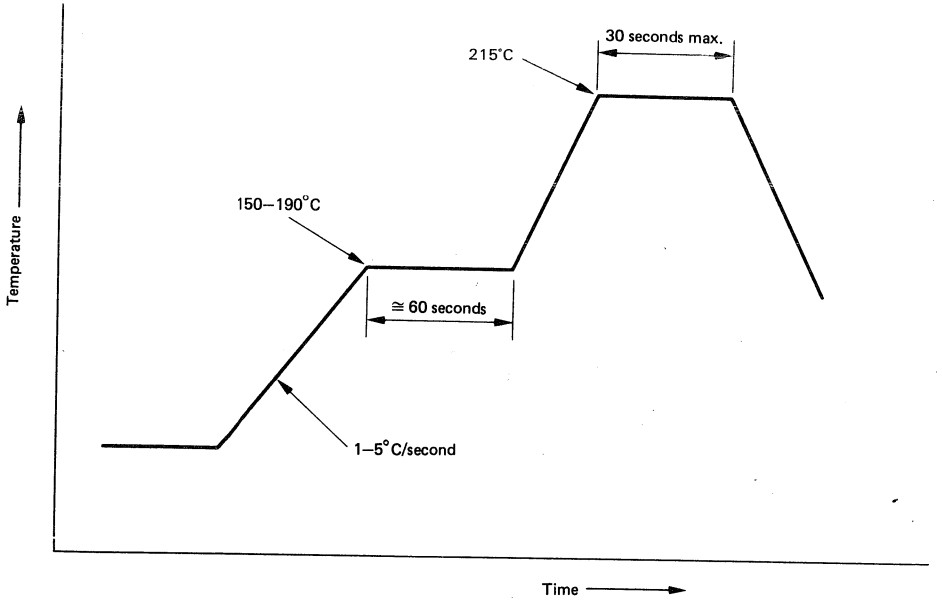


Figure 5 Example Vapor-phase Reflow Conditions

Display
Control LSI

Data Sheets

HD6345/HD6445

CRTC-II(CRT Controller)

The HD6345/HD6445 CRTC-II provides an interface between MPU and a raster scan CRT display. The HD6345 is upward-compatible with the NMOS CRTC HD6845S in pin and software, and has a 68 system bus interface. The HD6445 has a 80 system bus interface. A power dissipation is lowered by adopting the CMOS process.
The CRTC-II offers a variety of functions under MPU control, such as programmable timing signal outputs for CRT monitor and display screen control operation. It can be widely applied to the various types of CRT display systems.

FEATURES

FLEXIBLE SCREEN FORMAT

- Programmable numbers of characters per screen and rasters per character row
- Programmable horizontal/vertical sync signals and display timing signals
- Up to 16k words refresh memory (14-bit) addressable
- Programmable raster scanning modes: Non-Interlace, Interlace sync, or Interlace sync and video modes
- Up to 256 character rows per field
- High-speed display operation at 4.5 MHz character clock
- Double-size vertical display by raster interpolation

VERSATILE DISPLAY FUNCTIONS

- Screen split (max. 4 screens configurable, horizontally)
- Paging and scrolling for each screen
- Smooth scrolling
- Two cursors with programmable width
- Programmable refresh memoly width

FACILITATED SYSTEM CONFIGURATION

- 68 system bus interface (HD6345)
- 80 system bus interface (HD6445)
- Three-state control of memory address and raster address
- External synchronization in Master-slave or TV syne modes
- Interrupt request by vertical blanking or light pen strobe detection
- Programmable timing signal for dual-port RAM in MPRAM mode

PIN AND SOFTWARE UPWARD-COMPATIBLE WITH HD6845S

SINGLE+5V POWER SUPPLY

CMOS PROCESS

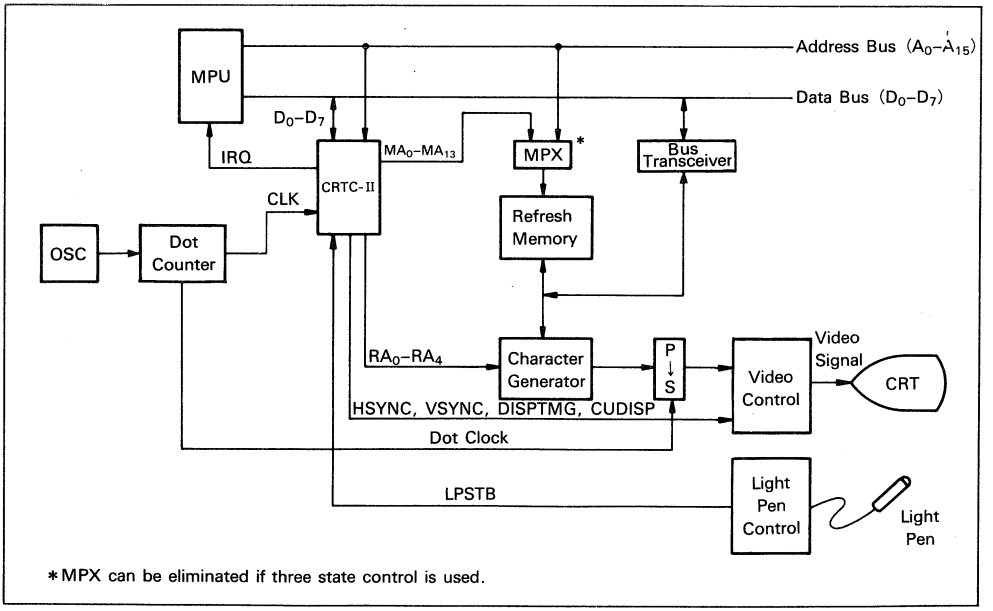
OPERATING TEMPERATURE SPECIFICATIONS

- Normal -20°C~+75°C
- J Version -40°C~+85°C

TYPE OF PRODUCTS

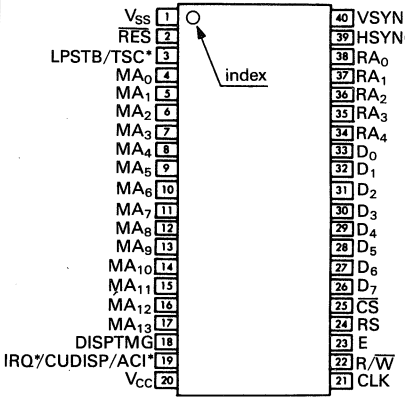
Specification	Bus Interface	Type No.	Bus Timing	Package	CRT Display Timing
Normal	6800 system Bus interface	HD6345P	1.0 MHz	DP-40 (40 pin plastic Dip)	4.5 MHz (max)
		HD63A45P	1.5 MHz		
		HD63B45P	2.0 MHz		
		HD6345CP	1.0 MHz	CP-44 (44 pin PLCC)	
		HD63A45CP	1.5 MHz		
		HD63B45CP	2.0 MHz		
	80 system Bus interface	HD6445P4	4.0 MHz	DP-40	
		HD6445CP4		CP-44	
J version (wide temperature range)	6800 system Bus interface	HD6345CPJ	1.0 MHz	CP-44	4.5 MHz (max)
		HD63A45CPJ	1.5 MHz		
		HD63B45CPJ	2.0 MHz		
	80 system Bus interface	HD6445CP4J	4.0 MHz		

SYSTEM BLOCK DIAGRAM



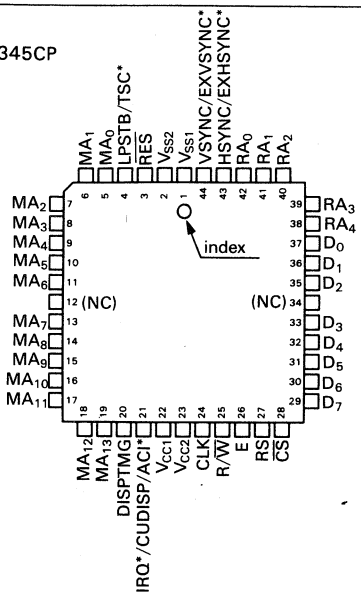
PIN ARRANGEMENT

HD6345P



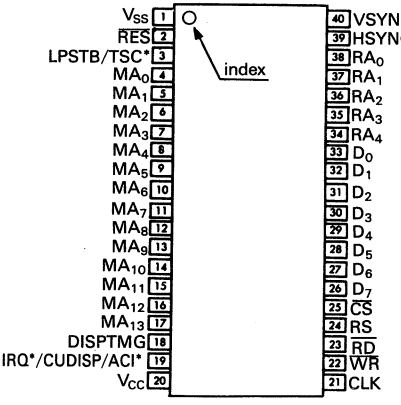
(Top View)
DP-40

HD6345CP



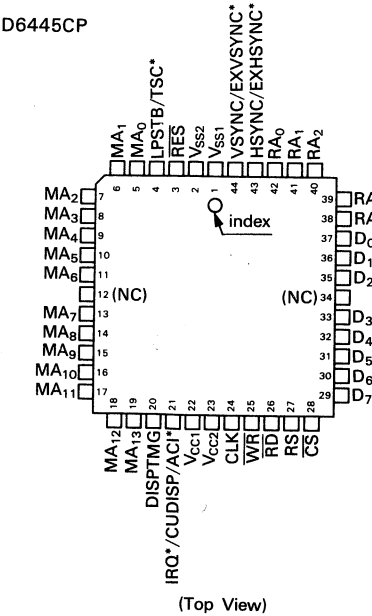
(Top View)
CP-44

HD6445P



(Top View)
DP-40

HD6445CP



(Top View)
CP-44

* Providing additional functions to the HD6845S.

PIN FUNCION

Pin No.					
DP-40	**CP-44**	**Symbol**	**Pin Name**	**Input/ Output**	**functions**
1	1,2	Vss(V_{SS1}, V_{SS2})**	V_{SS}	–	Ground (GND) pin
2	3	$\overline{RES}$	RESET	Input	Performs external reset on CRTC-II $\overline{RES}$ assertion causes CRTC-II: (1) Clear all the internal counters (2) Set all the output signals at "L" (D_0-D_7 are excluded.) (3) Clear registers R30 (Control 1), R31 (Control 2/Status), and R32 (Control 3) (Other registers are not affected at all) $\overline{RES}$ is valid only while LPSTB is "L"
3	4	LPSTB	LIGHT PEN STROBE	Input	Informs ligt pen strobe pulse detection
		TSC	THREE STATE CONTROL	Input	Performs three-state control on memory and raster addresses
4-17	5-11, 13-19	MA_0-MA_{13}	MEMORY ADDRESS 0-13	Output	Suppiles memory address for periodical memory refresh
18	20	DISPTMG	DISPLAY TIMING	Output	Indicates a screen display period
19	21	CUDISP	CURSOR DISPLAY	Output	Display cursor on a screen Enabled during DISPTMG is "H"
		ACI	ACCESS INHIBIT	Output	Supplies MPRAM access inhibit timing (programmable)
		IRQ	INTERRUPT REQUEST	Output	Indicates interrupt request to MPU Enabled during DISPTMG is "L"
20	22, 23	V_{CC}(V_{CC1}, V_{CC2})**	V_{CC}	–	Power supply (+5V) pin
21	24	CLK	Vcc CHARACTER CLOCK	Input	Receives character clock timing
22	25	R/$\overline{W}$	READ/WRITE	Input	Controls data transfer direction between MPU and CRTC-II
		$\overline{WR}$*	WRITE	Input	Inputs write signal from MPU
23	26	E	ENABLE	Input	Enables register read/write strobe signals from MPU
		$\overline{RD}$*	READ	Input	Inputs read signal from MPU
24	27	RS	REGISTER SELECT	Input	Selects either of address register or other registers Address reg. selected when at "L", and others at "H" Normaliy, requested to connect to "A_0" of MPU address bus
25	28	$\overline{CS}$	CHIP SELECT	Input	Performs addressing on CRTC-II MPU Read/write upon CRTC-II registers enabled when $\overline{CS}$ is "L"

Notes: *Marked pins are of the HD6445.
**Marked pins are of the CP-44.

Pin No.					
DP-40	**CP-44**	**Symbol**	**Pin Name**	**Input/ Output**	**functions**
33-26	37-35, 33-29	D_0-D_7	DATA BUS 0-7	Input/ Output	Bidirectional bus for data transfer between MPU and CRTC-II
38-34	42-38	RA_0-RA_4	RASTER ADDRESS 0-4	Output	Supplies raster address for selecting raster on character generator
39	43	HSYNC	HORIZONTAL SYNC	Output	Supplies horizontal sync signal
		EXHSYNC	EXTERNAL HORIZONTAL SYNC	Input	Receives external horizontal sync signal
40	44	VSYNC	VERTICAL SYNC	Output	Supplies vertical sync signal
		EXVSYNC	EXTERNAL VERTICAL SYNC	Input	Receives external vertical sync signal

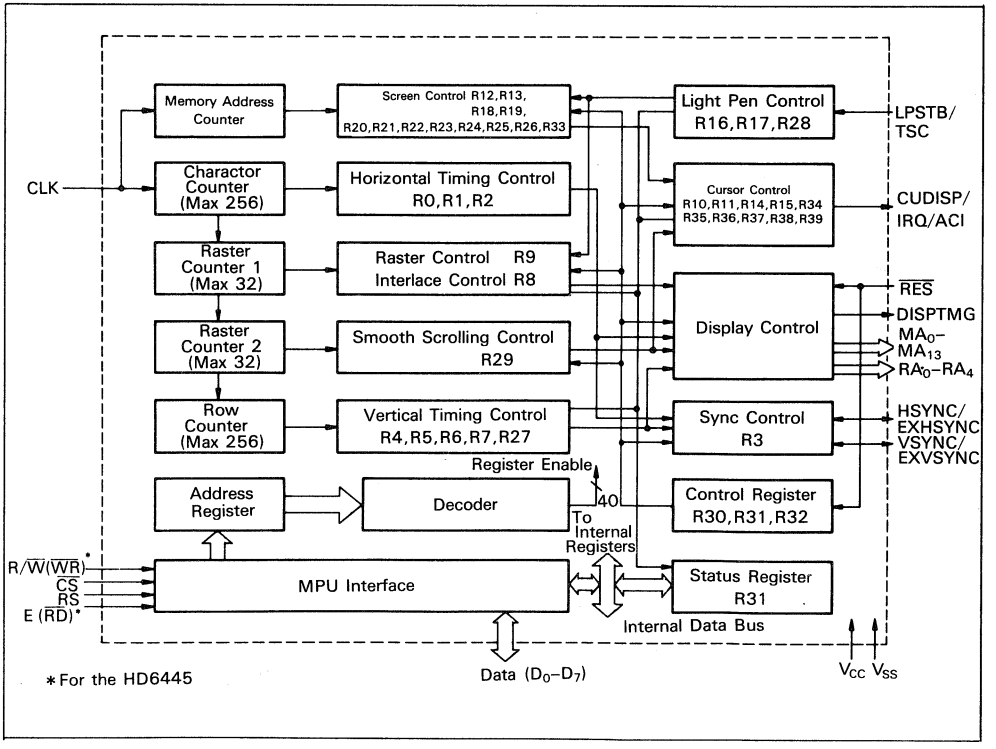
FUNCTON TABLE

Item	Descriptions	Remarks
Programmable Screen Format	Horizontal scan cycle	Programmable by char. clock time
	Vertical scan cycle (by row)	Programmable by char. row time
	Vertical scan cycle (Adjust)	Programmable by raster time
	Number of displayed chars./row	
	Number of char. rows/screen	
	Number of rasters/char. row	
	Horizontal display position	Enabled by programming sync signal output timings
	Vertical display position	
	Vertical sync position (Adjust)	Programmable by raster time
	HSYNC pulse width	
	VSYNC pulse width	
	DISPTMG skew	1 or 2 character skew
Screen Split	4 split-screens start positions programmable	Discretely programmable (Unit: row) 2/3/4 screens format selectable
Cursor Control	Cursor display position	Two 14-bit cursor registers 1 or 2 cursors displayed
	Cursor height	Display start/end rasters programmable within a row
	Cursor width	Programmable by char. clock time
	Cursor blink	1/16 or 1/32 field rate selectable
	Simultaneous output of 2 cursors (Only 1 availble in MPRAM mode)	Discretely programmable
	Cursor display mode	OR/EOR mode selectable
	CUDISP skew	1 or 2 character skew
Raster Scan Mode	Non-Interlace mode	Either one of three modes selectable
	Interlace sync mode	
	Interlace sync and video mode	
Memory Format	Memory width set	Memory width programmable wider than display width (Unit: char.)
Smooth Scrolling	Display start raster address set	Programmable by char. clock time
	Target screen set	Any screen selectable
Raster Interpolation	Double-size vertical display	Same raster address supplied twice
	Vertical scan cycle doubled	
External Synchronization	Synchronization with external sync signals	Superimposed display enhabled on other CRT or TV screens
Interrput Request	Interrupt request signal caused by vertical ratrace period or light pen detection (Disabled in MPRAM mode)	Interrupt reqest mode programmable
Light Pen	14-bit Light pen register	Light pen raster address detected
	Light pen raster register	
Refresh Memory Addressing	14-bit refresh memory address output	Up to 16k words refresh memory accessible
	Four 14-bit screen start address regs. (Display start address programmable for each screen)	Paging and scrolling enabled each screen
Three-State Control	Three-state control on MA and RA	Controlled by TSC pin input
Programmable Timing Output	Programmable timing signal supplied from access inhibit pin	In MPRAM mode

CRTC-II NEWLY ADOPTED FEATURES

1. Screen Partition (horizontally split into 4 screens)
2. Smooth Scrolling
3. External Synchronization
4. Interrupt request
5. Raster Interpolation
6. Sync Position Adjustment
7. Light Pen Raster Address
8. Second Cursor
9. Display Memory Width Setting
10. 256 Rows Max
11. Timing Signal for MPRAM
12. Three-state Control of MA/RA Output

INTERNAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PROGRAMMABLE SCREEN FORMAT

Figure 1 illustrates the screen format example, in Non-Interlace mode, when programming CRTC-II registers as listed in Tabel 1. Figure 2 shows the relation between memory address (MA_0-MA_{13}), raster address (RA_0-RA_4) and the location on the CRT screen.

The timing charts of CRT interface signals are shown in Figure 3, and those details are partially shown in Figure 4 and 5.

Tabel 1 Programmed Values in Each Register

Register No.	Register Name	Programmed Values
R0	HORIZONTAL TOTAL CHARACTERS	Nht
R1	HORIZONTAL DISPLAYED CHARACTERS	Nhd
R2	HORIZONTAL SYNC POSITION	Nhsp
R3	SYNC WIDTH	Nvsw, Nhsw
R4	VERTICAL TOTAL ROWS	Nvt
R5	VERTICAL TOTAL ADJUST	Nadj
R6	VERTICAL DISPLAYED ROWS	Nvd
R7	VERTICAL SYNC POSITION	Nvsp
R9	MAX. RASTER ADDRESS	Nr
R12	SCREEN 1 START ADDRESS (H)	0
R13	SCREEN 1 START ADDRESS (L)	0
R30	CONTROL 1	0
R31	CONTROL 2/STATUS	0
R32	CONTROL 3	0

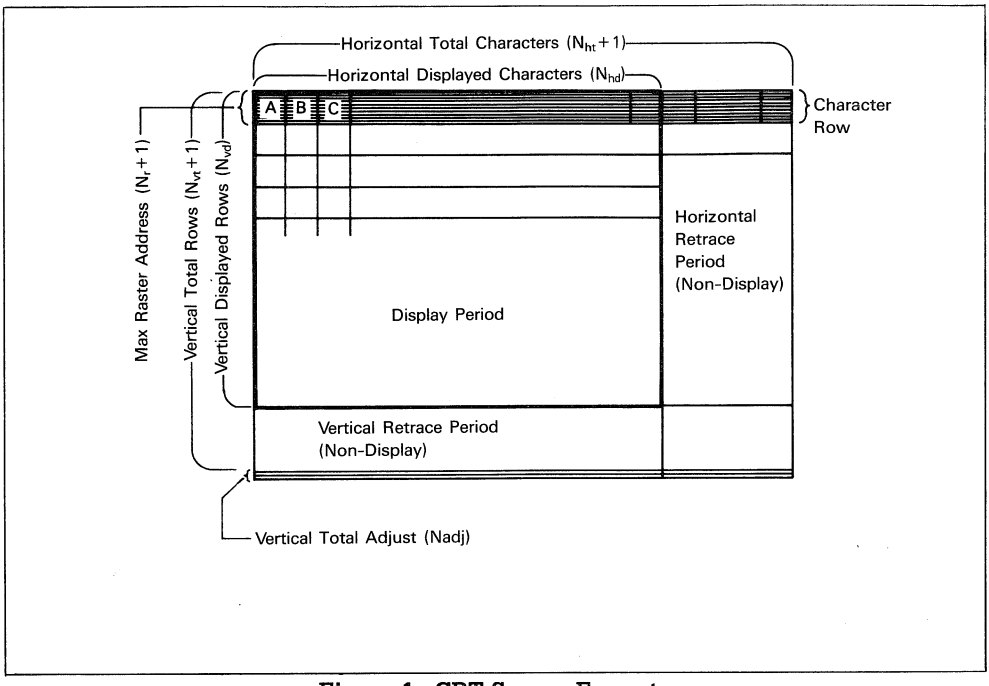
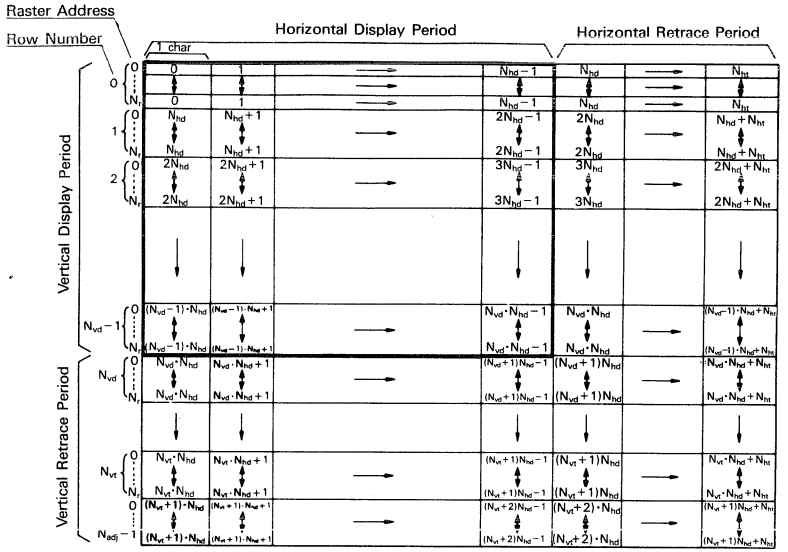


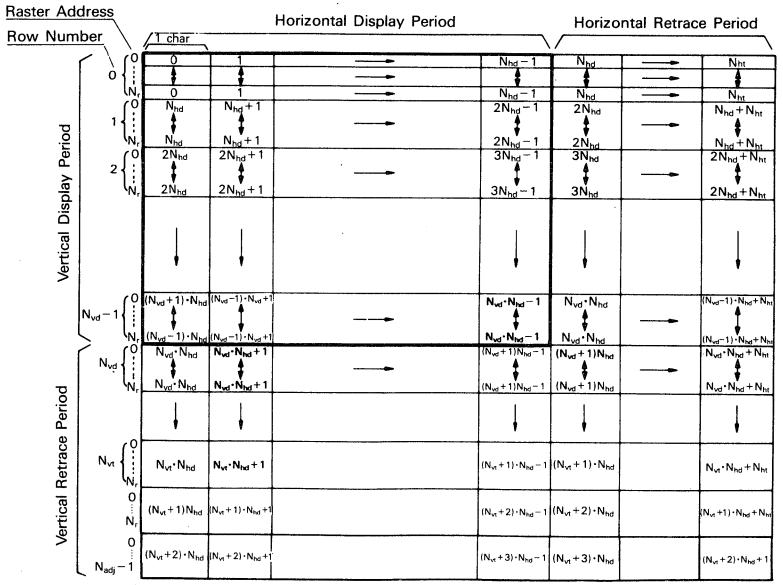
Figure 1 CRT Screen Format

① $N_{adj} - 1 \leqq N_r$



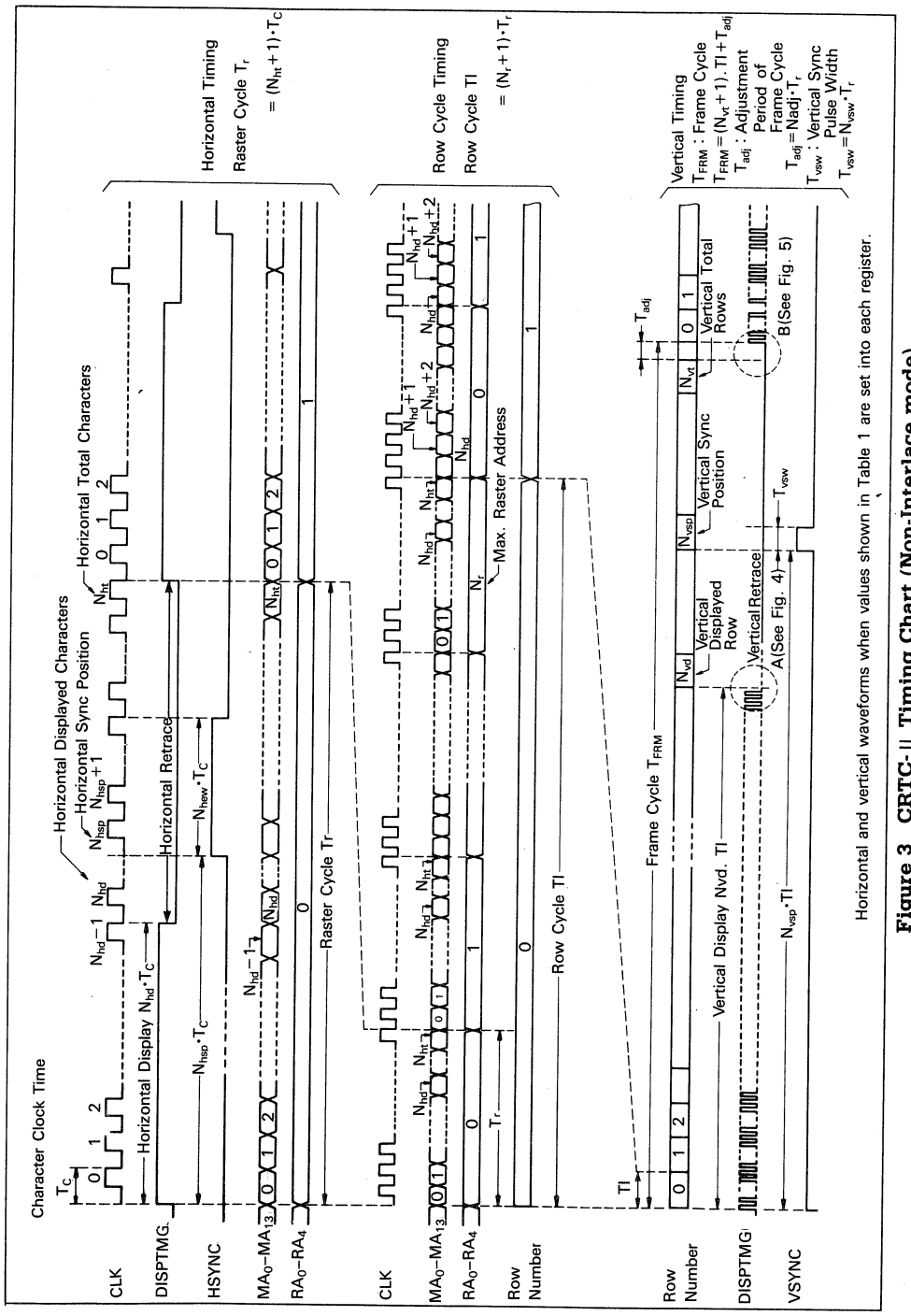
Valid memory addresses [0 thru (N_{vd} -1) or 0 (N_{hd} -1)] are shown within the thick-line square. Memory addresses are provided even during horizontal and vertical retrace period. This is an example in the case where the programmed value of start address register is 0.

② $N_{adj} - 1 > N_r$



Valid memory addresses [0 thru (N_{vd} -1) or 0 (N_{hd} -1)] are shown within the thick-line square. Memory addresses are provided even during horizontal and vertical retrace period. This is an example in the case where the programmed value of start address register is 0.

Figure 2 Memory Address and Raster Address



Horizontal and vertical waveforms when values shown in Table 1 are set into each register.

Figure 3 CRTC-II Timing Chart (Non-Interlace mode)

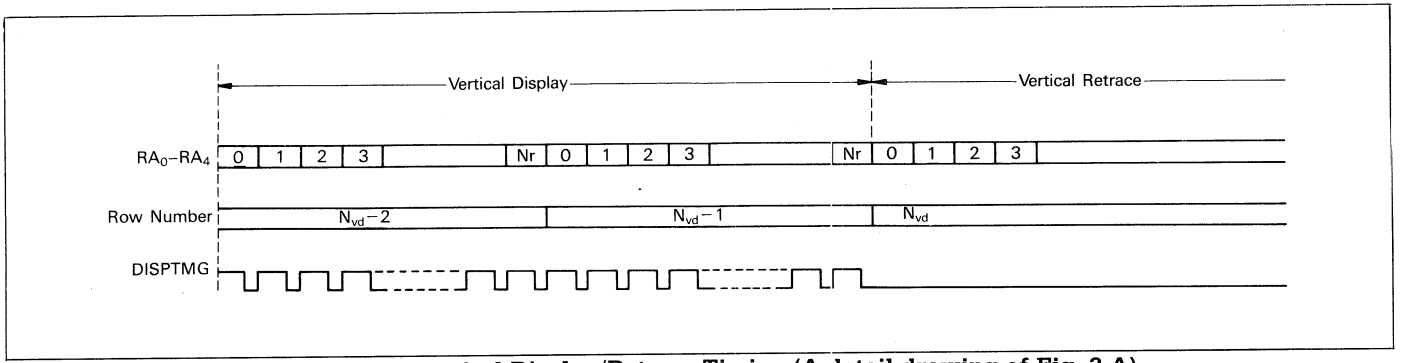


Figure 4 Vertical Display/Retrace Timing (A detail drawing of Fig. 3 A)

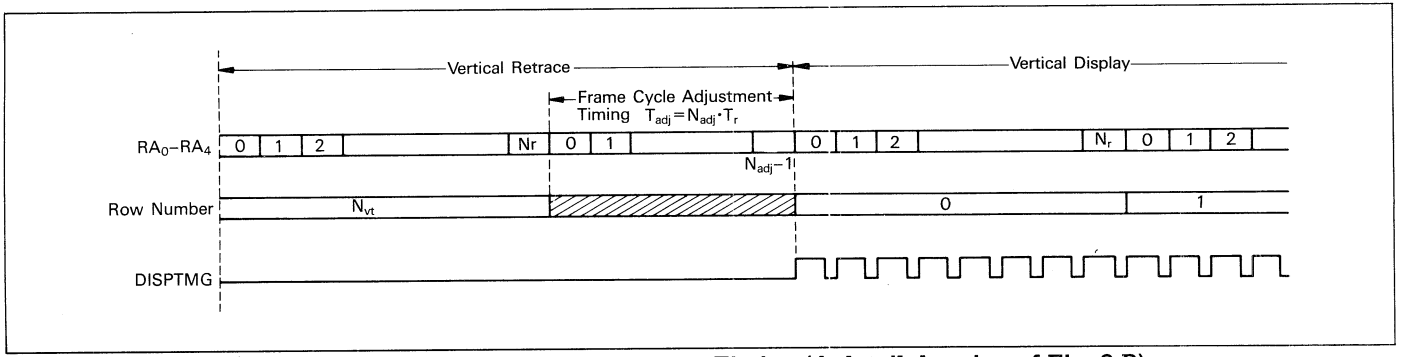


Figure 5 Frame Cycle Adjustment Timing (A detail drawing of Fig. 3 B)

SCREEN SPLIT

A display screen can be divided into up to four parts in the horizontal direction. Divided four parts are defined as split-screen 1, split-screen 2, split-screen 3, and split-screen 4.

The starting positions of each split-screen are determined in the number of character row. Split-screen 1 is the base screen, and always starts at row 0, while the other three split-screens start at any row except row 0. Paging or scrolling (by character) is performed in each split-screen independently.

Screen split is controlled by the SP0 and the Sp1 bits of the control 1 register (R30) and the screen start position registers (R18, R21, R24). If the same value is programmed in more than one screen start position register or a start position which is out of display row is programmed in those registers, the corresponding split-screens will not be displayed.

The following is examples of screen split:

When the same value are programmed into more than one screen start position registers, split-screens corresponding to these registers are not displayed.

Table 2 Screen Split

Control 1 Register		Number of effective screen			
SP1	SP0	1	2	3	4
0	0	○	–	–	–
0	1	○	○	–	–
1	0	○	○	○	–
1	1	○	○	○	○

○ : effective screen
– : invalid screen

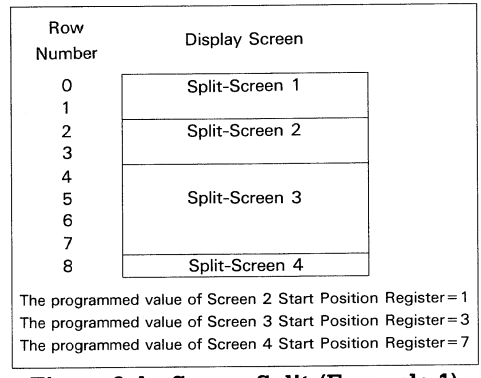


Figure 6-A Screen Split (Example 1)

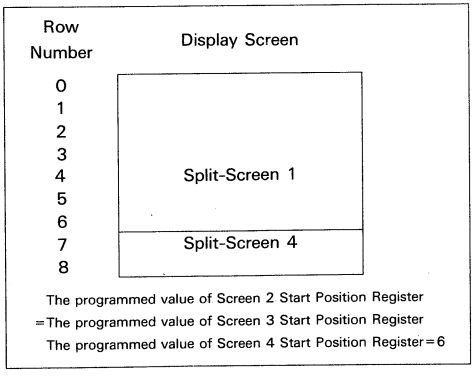


Figure 6-B Screen Split (Example 2)

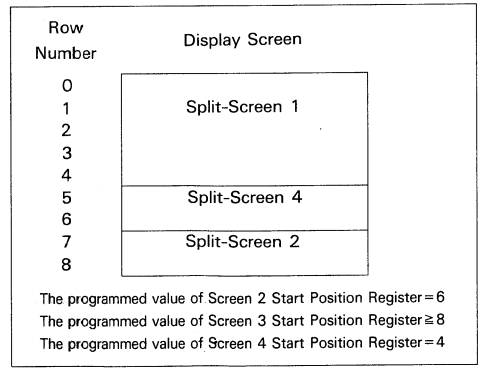


Figure 6-C Screen Split (Example 3)

CURSOR CONTROL

The CRTC-II can display two separate cursors (cursor 1, cursor 2) simultaneously on the screen. These two cursors are controlled independently. The cursor 1 is always valid, while the cursor 2 becomes valid by setting the C_2 bit of the control 3 register (R32).
In the MPRAM mode, the cursor 2 cannot be displayed. The CRTC-II controls cursors as follows:

1) Starting Position
   Starting position is controlled by the cursor 1 address registers (R14, R15), and the cursor 2 address registers (R36, R37).
2) Cursor Heights
   The heights of the cursor 1 and the cursor 2 can be specified independently in units of rasters by the cursor start registers (R10, R34), and the cursor end registers (R11, R35).
3) Cursor Widths
   The widths of the cursor 1 and the cursor 2 can be specified independently in units of characters by the cursor width registers (R38, R39). The R38 register is enabled when 1 is set into the CW1 bit of the control 3 register (R32). The R39 register's enable bit is the CW2.
   If the cursor width extends over the following row, the cursor in the following row will not be displayed.
4) Cursor Blink
   Cursor display, non-display, and blink rate can be controlled by the bits B_1 and P_1 of the cursor 1 start register (R10), and bits the B_2 and P_2 of the cursor 2 start register (R34).
5) Cursor Display Mode
   When the cursor 1 and the cursor 2 are overlapped on the screen, cursor display mode in the overlapped area can be selected by the CM bit of the control 3 register (R32), as shown in Figure 8.

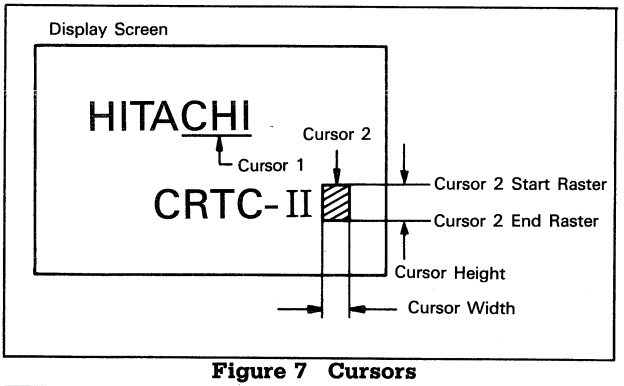


Figure 7 Cursors

Table 3 Cursor Blink Mode

B_1	P_1	Cursor Blink Mode
0	0	No blink
0	1	No cursor
1	0	Blink, 1/16 field rate
1	1	Blink, 1/32 field rate

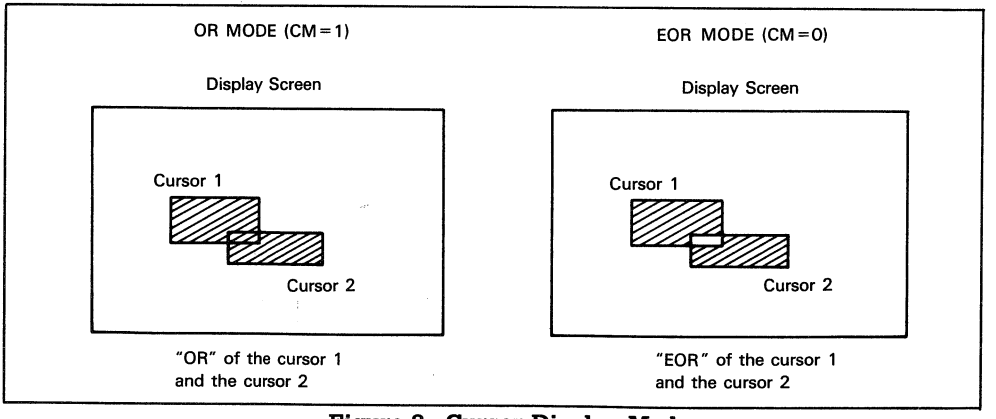


Figure 8 Cursor Display Mode

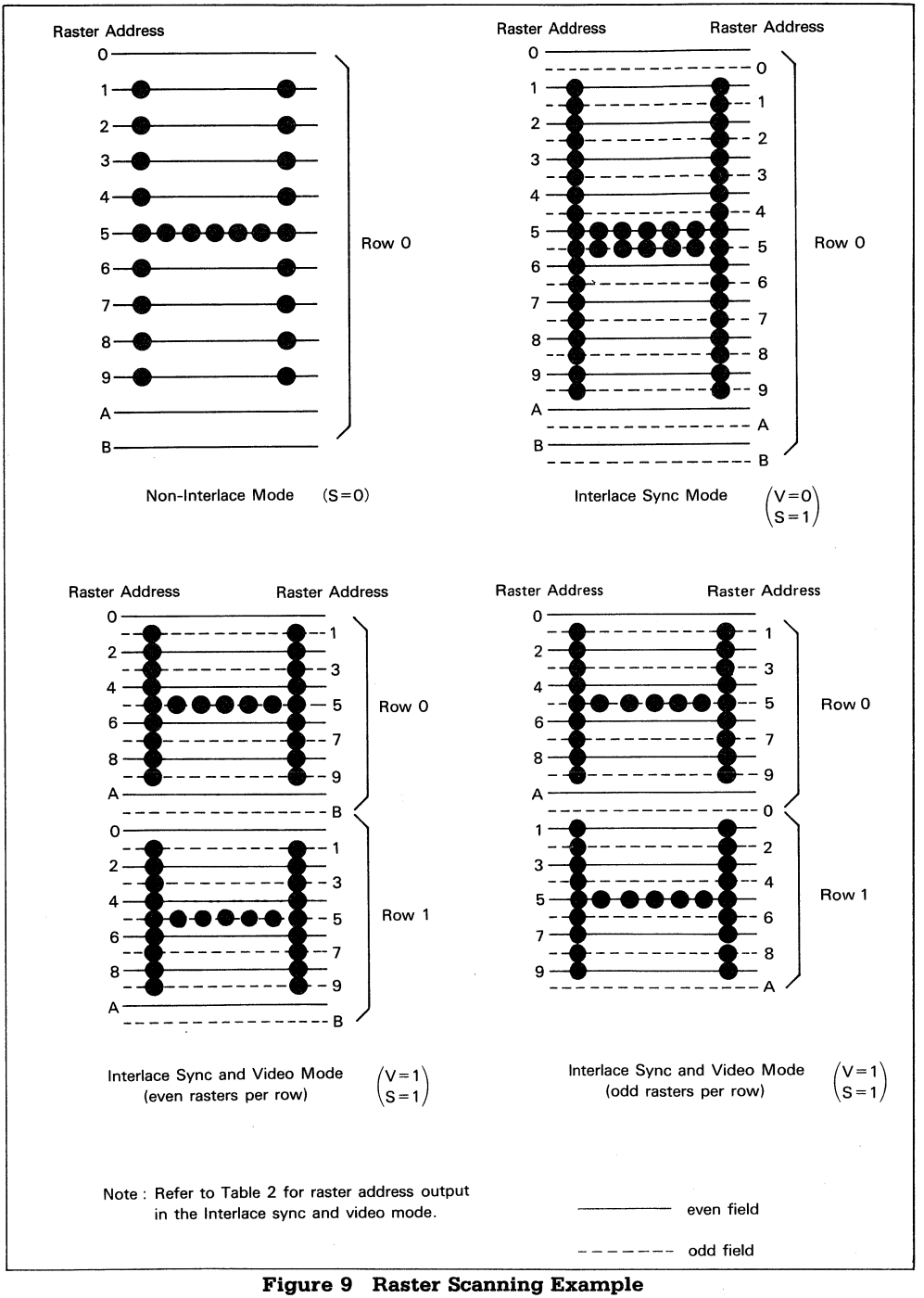


Figure 9 Raster Scanning Example

In the Interlace sync mode, the rasters in the odd field are placed downward by 1/2 raster line space from those in the even field because of the difference in HSYNC/VSYNC phases between two alternating fields.

In the Interlace sync and video mode, the placement of the rasters is the same as in the Interlace sync mode. However, the alternating even and odd resters are displayed in the alternating even and odd fields. Note that the raster address is supplied in the different way according to the total number of rasters in a row, even or odd, as shown in Table 4. Figure 9 illustrates the raster scanning example in each mode.

SMOOTH SCROLLING

Smooth scrolling in the vertical direction can be accomplished by changing the start raster address in a character row. Whether scrolling in each split-screen is available or not can be selected. Selected split-screens scroll in the same way up to four split-screens simultaneously.

Smooth scrolling is performed by the bits SS_1-SS_4 of the control 2 register (R31), and the smooth scrolling register (R29). It can be used in the Non-Interlace mode and the Interlace sync mode, but not in the Interlace sync and video mode.

Tabel 4 Start Raster Address for Each Row (In Interlace sync and video mode)

No. of Rasters per Row		Field	
		Even Field	Odd Field
Even		Even address	Odd address
Odd	Even Char. Row*	Even address	Odd address
	Odd Char. Row*	Odd address	Even address

* The start row address is assumed to be 0 (even).

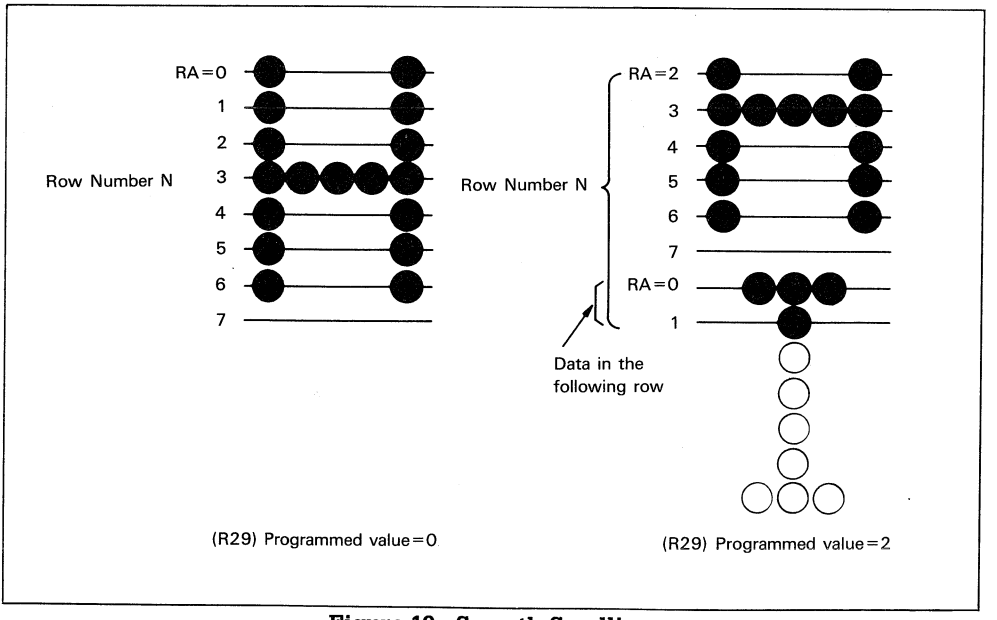


Figure 10 Smooth Scrolling

MEMORY WIDTH SETTING

The offset value is the difference between the display screen width and the display memory width in the horizontal direction. It can be specified in units of characters. (See Figure. 11)

Scrolling in any direction can be accomplished in units of characters, by setting the display memory width (horizontal direction) and the offset value, and by changing the start memory addresses. This is performed by the memory width offset register (R33) and the MW bit of the control 3 register (R32).

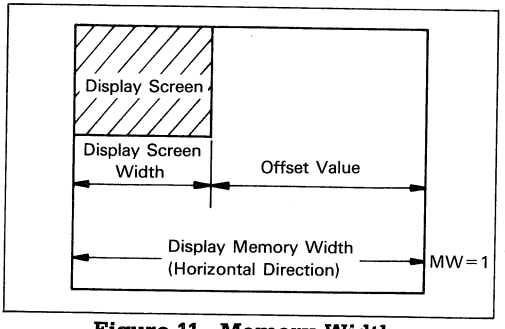


Figure 11 Memory Width

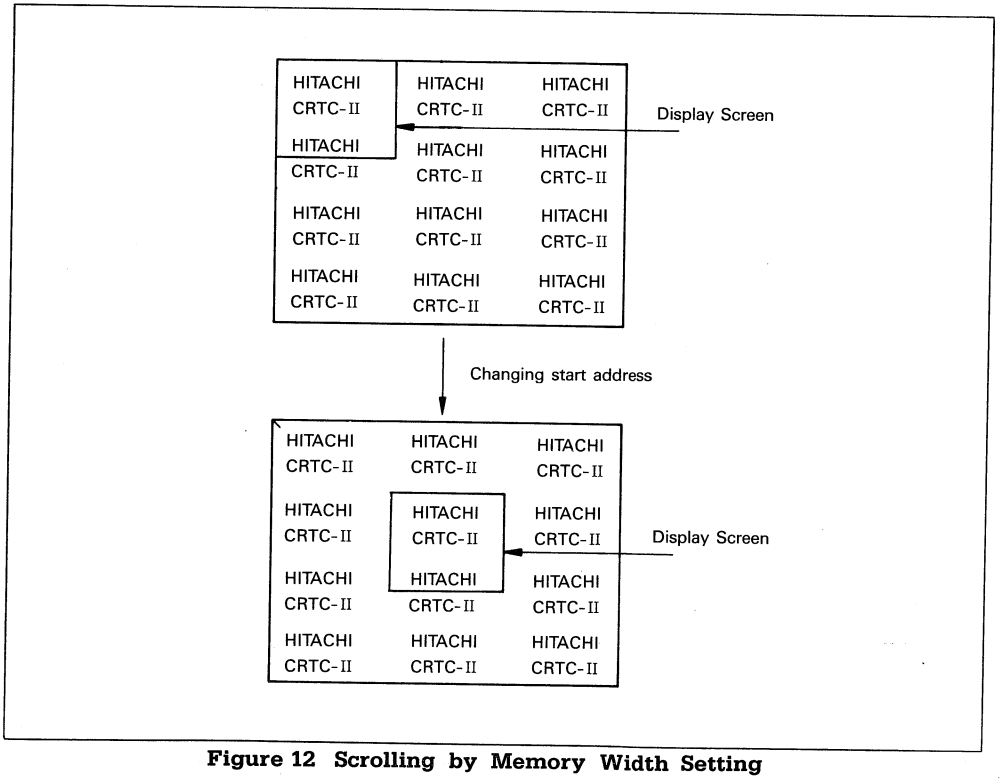
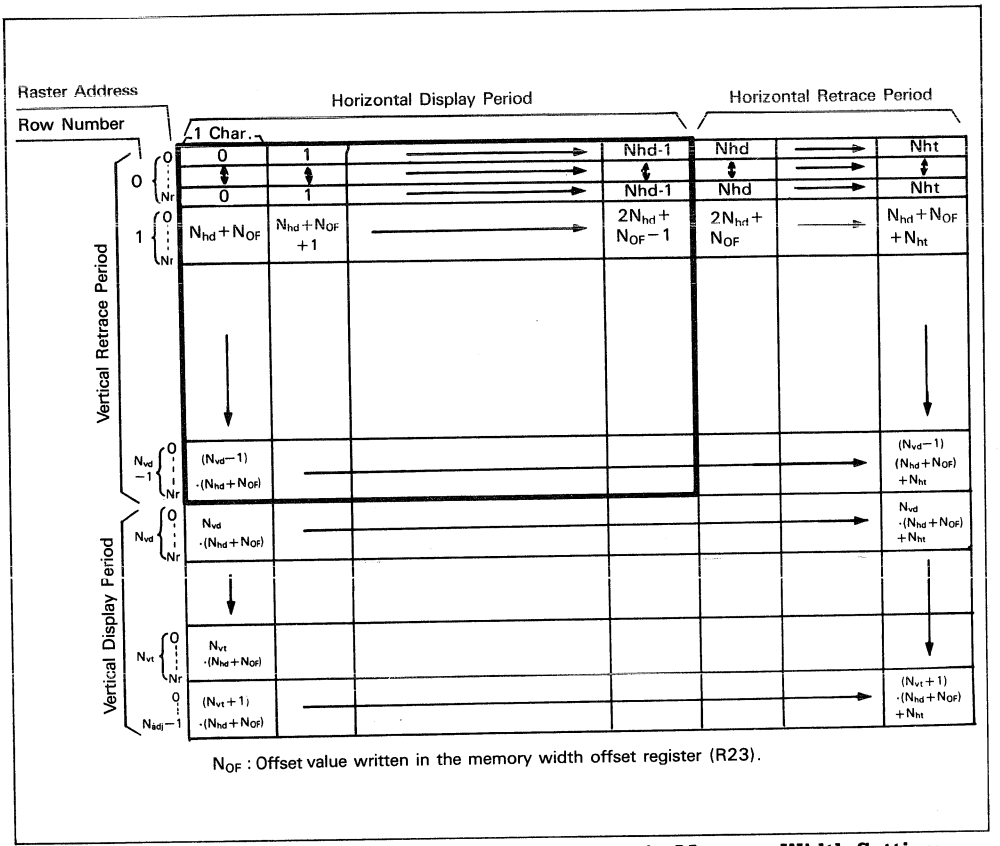


Figure 12 Scrolling by Memory Width Setting



N_{OF} : Offset value written in the memory width offset register (R23).

Figure 13 Memory Address and Raster Address in Memory Width Setting

RASTER INTERPOLATION

Raster interpolation function increments the raster address every two rasters, doubling the vertical scan cycle; thus the display image is doubled in the vertical direction.

Raster interpolation function is controlled by the RI bit of the control 2 register (R31). This function can be used in the non-interlace mode and the interlace sync mode, but not in the interlace sync and video mode. Figure 14 is a display example using raster interpolation function.

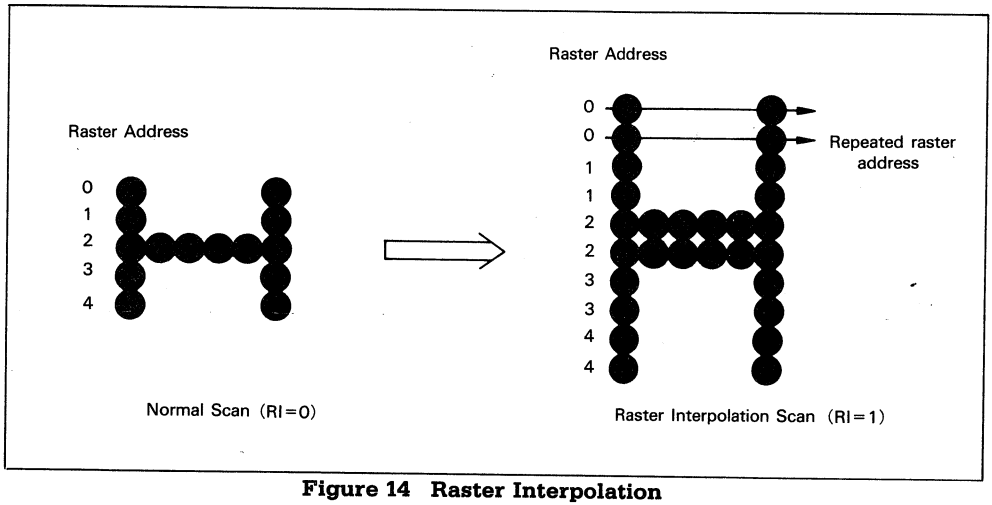


Figure 14 Raster Interpolation

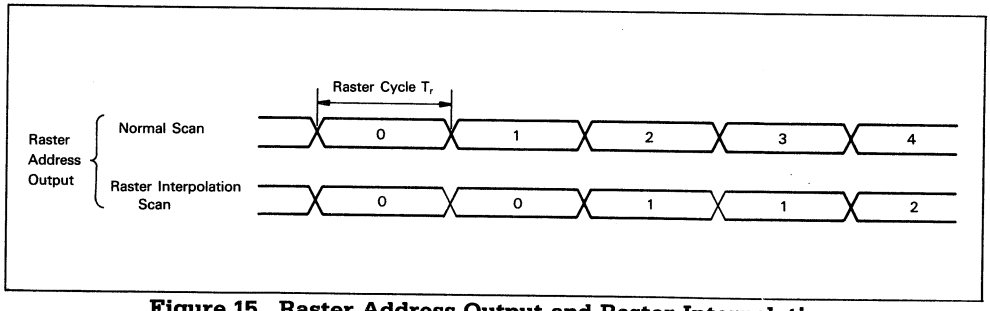


Figure 15 Raster Address Output and Raster Interpolation

EXTERNAL SYNCHRONIZATION

There are master/slave mode and TV sync mode in external synchronization.

The external synchronization is controlled by the bits VE, VS, and TV of the control 1 register (R30).

Master/slave mode is used to synchronize slave CRTC-IIs with a master CRTC-II by the VSYNC of a master CRTC-II. When superimposing a master screen with slave screen on the same CRT, clocks of a master and slave CRTC-IIs can operate in different frequency under conditions as follows.

(1) Phase of a master CRTC-II clock matches with a slave CRTC-II clock at rising edge of VSYNC.
(2) Both master and slave CRTC-IIs have the same horizontal/vertical scan cycle.

Figure 16 illustrates the system configuration. In the Interlace sync mode and the Interlace sync and video mode, the control 1 register must be set as to provide a VSYNC output in odd fields of a master CRTC-II.

TV sync mode is used to synchronize the CRTC-II with the HSYNC and VSYNC signals of a TV's video signal.

In the TV sync mode, the HSYNC/EXHSYNC pin inputs the EXHSYNC signal and the VSYNC/EXVSYNC pin inputs the EXVSYNC signal. The length of horizontal back porch is specified by the bits 0-3 of the sync width register (R3).

Figure 17 illustrates the system configuration.

In TV sync mode, when performing raster interpolation of slave CRTC-IIs, Interlace sync mode or Interlace sync and video mode must not be set in a master CRTC-II; this causes the screen moves up and down by one raster.
In the Interlace sync and video mode, the TV sync mode cannot be used.

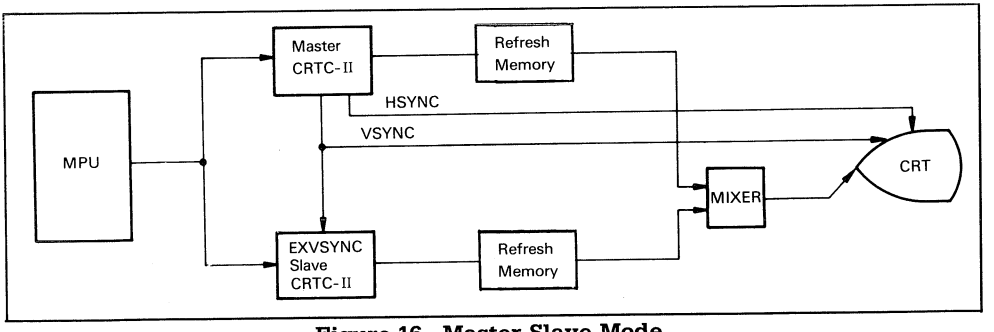


Figure 16 Master-Slave Mode

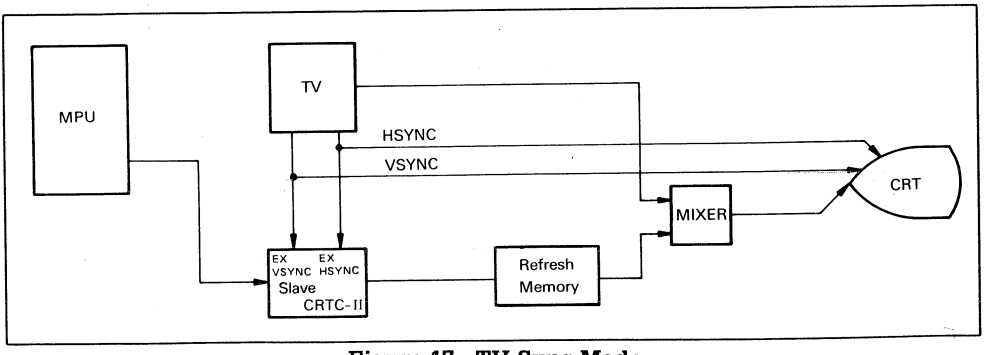


Figure 17 TV Sync Mode

Table 5 External Synchronization

				Function			
VE	**VS**	**TV**	**Mode**	**EXHSYNC /HSYNC**	**EXVSYNC /VSYNC**	**DISPTMG**	**States**
0	0	0	Master /slave mode	OUTPUT	OUTPUT	Active	Set as master CRTC-II in master-slave mode. "000" is to be set when CRTC-II is in nomal states (HD6845 compatible mode) or master mode.
0	1	0				"Low"	Set as master CRTC-II in master slave mode. Display is inhibited by setting DISPTMG "0". VSYNC signal is supplied only in odd field scan except the non-interlace mode.
1	0	0		OUTPUT	INPUT	Active	Set as slave CRTC-II in master slave mode. EXHSYNC is not used for the synchronization.
1	1	0				"Low"	Set as slave CRTC-II in master slave mode. EXVSYNC is used for the synchronization.
0	0	1	TV sync mode	INPUT	OUTPUT	Active	Program inhibited
0	1	1				"Low"	Program inhibited
1	0	1		INPUT	INPUT	Active	Set as slave CRTC-II in TV sync mode. EXHSYNC, EXVSYNC inputs are used as sync signal.
1	1	1				"Low"	Set as slave CRTC-II in TV sync mode. Display is inhibited by setting DISPTMG "0". EXHSYNC, EXVSYNC inputs are used as sync signal.

Note : Slave CRTC-IIs are always Non-Interlace mode in TV sync mode.

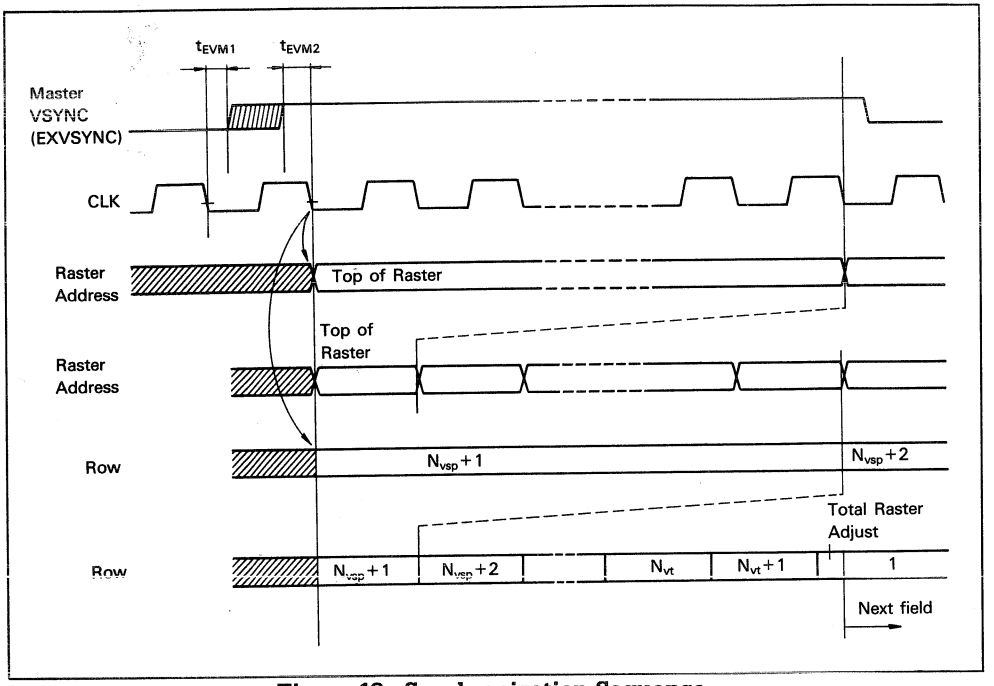


Figure 18 Synchronization Sequence

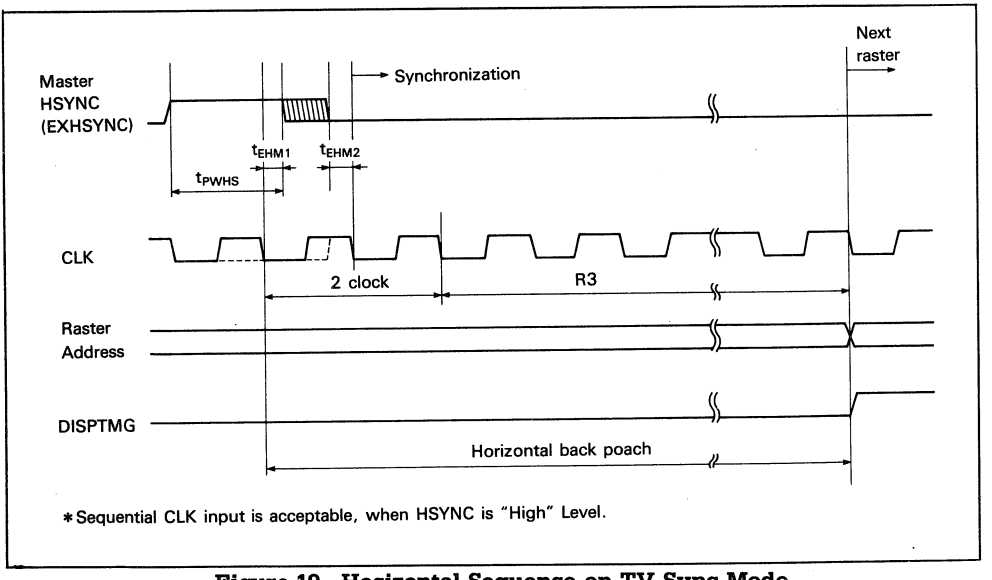
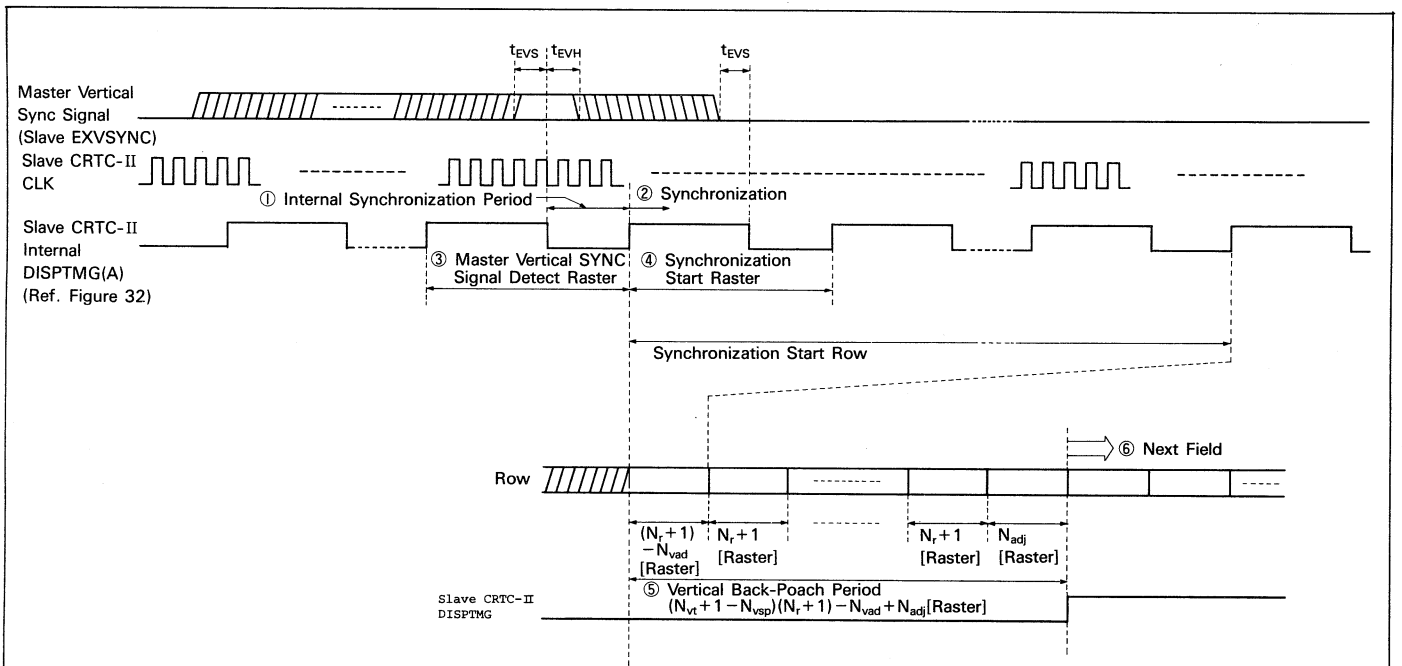


Figure 19 Hosizontal Sequence on TV Sync Mode



N_{vsw} : Setting value of sync width register (R3)
N_{vt} : Setting value of vertical total rows register (R4)
N_{adj} : Setting value of vertical total adjust (R5)
N_{vsp} : Setting value of vertical sync position register (R7)
N_r : Setting value of maximum raster address (R9)
N_{vad} : Setting value of vertical sync position adjust (R27)

Figure 20 Vertical Sequence on TV Sync Mode

INTERRUPT REQUEST

An interrupt request signal to the MPU is output in the timing shown in Figure 21. Interrupt request is generated by the vertical retrace period, or the light pen input.

Reading the status register (R31) clears interrupt request signal. Thus, if the MPU does not read the status register (R31) when an interrupt request is generated, an interrupt request signal is output during all the horizontal and vertical retrace periods.

In the MPRAM mode, an interrupt request signal is not output.

An interrupt request is controlled by the bits IB and IL of the control 1 register (R30).

Table 6 Interrupt Control

IB	IL	Source of Interrupt Request
0	0	None
0	1	Light pen strobe
1	0	Vertical retrace
1	1	Light pen strobe and/or vertical retrace

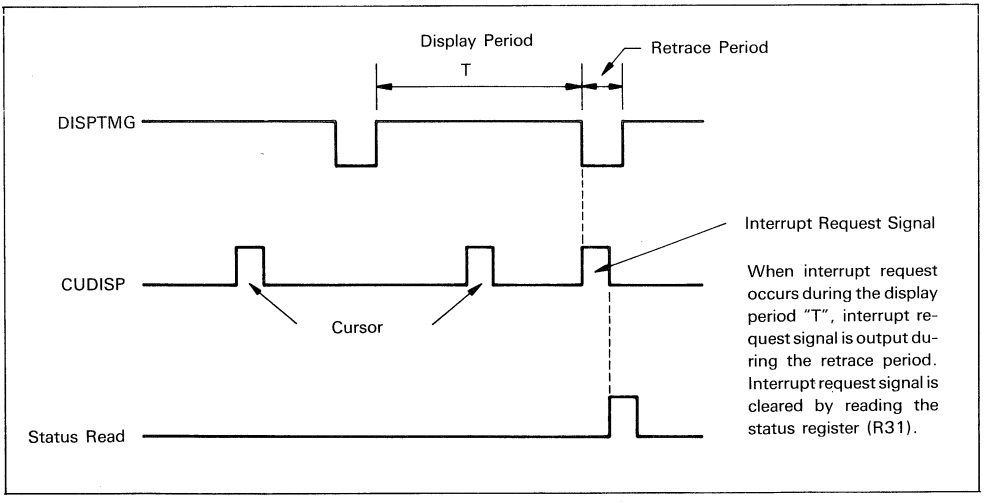


Figure 21 Interrupt Timing

THREE-STATE CONTROL OF MA/RA

Memory address (MA) and raster address (RA) outputs can be three-stated, using the TSC input pin. Three-state control is enabled by setting the TC bit of the control 3 register (R32).

When three-state control is used, a multiplexer (MPX) to select address lines from the MPU and the CRTC-II for refresh memory is not required, as shown in Figure 22.

MPRAM MODE

When the MPRAM mode is selected (DR=1), the HD6445 generates a programmable timing signal from the access inhibit pin. This signal, shown in Figure 23 as access inhibit period, provides the timing for the MPU to access to multi-port memory.

In the MPRAM mode, an interrupt request signal is not output, and the cursor 2 is not displayed.

This timing signal is controlled by the DR bit of the control 3 register (R32), and the cursor 2 width register (R39).

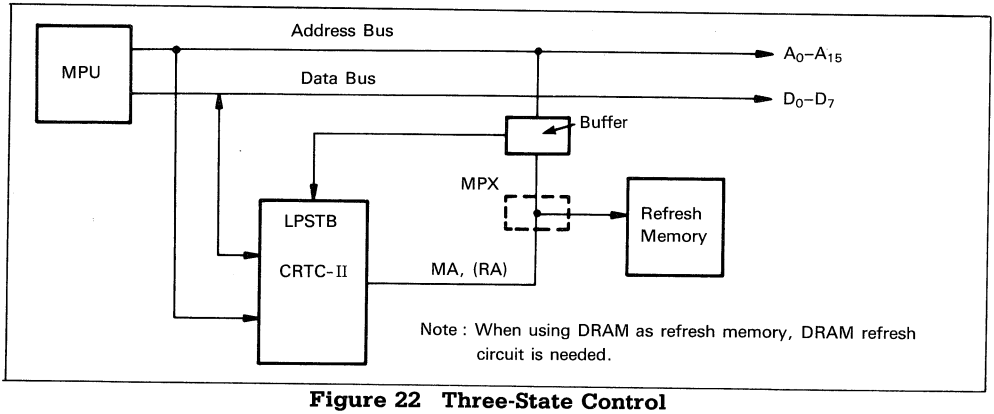


Figure 22 Three-State Control

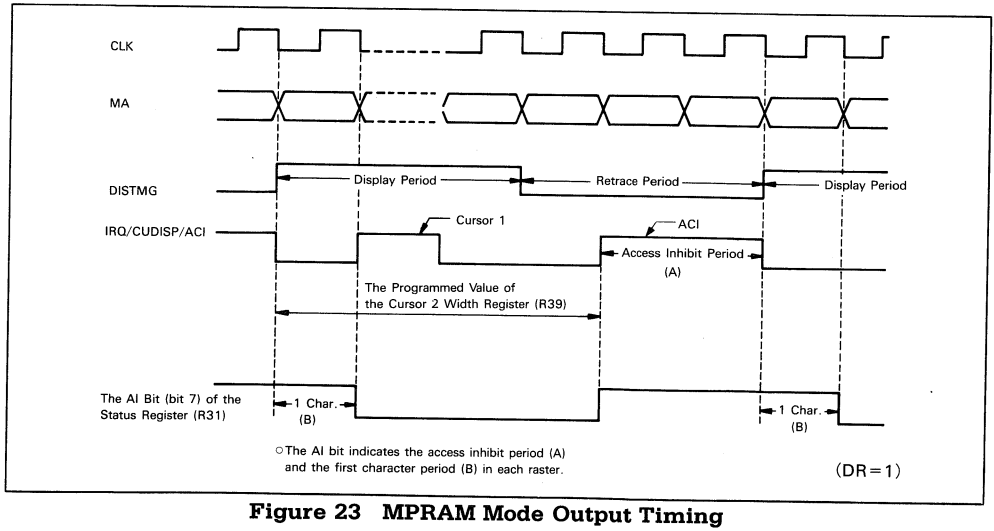


Figure 23 MPRAM Mode Output Timing

SKEW

D_1	D_0	DISPTMG
0	0	No skew
0	1	One character skew
1	0	Two character skew
1	1	Not available ("Low" fixing)

C_1	C_0	CUDISP
0	0	No skew
0	1	One character skew
1	0	Two character skew
1	1	Not available ("Low" fixing)

LIGHT PEN

The R16 and R17 registers latches the light pen detection address. R28 register latches the light pen detection raster address and the detection period. The DP bit is set to 1 when the LPSTB is detected during the display period; cleared 0 during the retrace period.

VERTICAL SYNC POSITION ADJUST

The R27 register performs a fine adjustment to the vertical sync signal output in units of rasters. The VSYNC signal is supplied after the delay of Nvad rasters. R27 register is enabled when 1 is set into the SY bit of the control 1 register (R30).

STATUS

E	Status
0	During odd field display
1	During even field display

SB	Status
0	Not during vertical retrace
1	During vertical retrace

SL	Status
0	Light pen strobe not detected
1	Light pen strobe detected

AI	Status
0	Refresh memory access allowed
1	Refresh memory access inhibited

INTERNAL REGISTER ASSIGNMENT

CS	RS	Register Address 5 4 3 2 1 0	Reg. No.	Register Name	Program Unit	Symbol	R/W	Data Bit 7	6	5	4	3	2	1	0
1	×	× × × × × ×	–	–	–	–	–								
0	0	× × × × × ×	AR	ADDRESS REGISTER	–	–	W								
0	1	0 0 0 0 0 0	R0	HORIZONTAL TORAL CHARACTERS	character	Nht	W								
0	1	0 0 0 0 0 1	R1	HORIZONTAL DISPLAYED CHARACTERS	character	Nhd	W								
0	1	0 0 0 0 1 0	R2	HORIZONTAL SYNC POSITION	character	Nhsp	W								
0	1	0 0 0 0 1 1	R3	SYNC WIDTH	*	Nvsw, Nhsw	W	Wv_3	Wv_2	Wv_1	Wv_0	Wh_3	Wh_2	Wh_1	Wh_0
0	1	0 0 0 1 0 0	R4	VERTICAL TORAL ROWS	row	Nvt	W								
0	1	0 0 0 1 0 1	R5	VERTICAL TORAL ADJUST	raster	Nadj	W								
0	1	0 0 0 1 1 0	R6	VERTICAL DISPLAYED ROWS	row	Nvd	W								
0	1	0 0 0 1 1 1	R7	VERTICAL SYNC POSITION	row	Nvsp	W								
0	1	0 0 1 0 0 0	R8	INTERLACE MODE AND SKEW	–	–	W	C_1	C_0	D_1	D_0			V	S
0	1	0 0 1 0 0 1	R9	MAX RASTER ADDRESS	raster	Nr	W								
0	1	0 0 1 0 1 0	R10	CURSOR 1 START	raster	Ncs_1	W		B_1	P_1					
0	1	0 0 1 0 1 1	R11	CURSOR 1 END	raster	Nce_1	W								
0	1	0 0 1 1 0 0	R12	SCREEN 1 START ADDRESS (H)	memory address	–	R/W								
0	1	0 0 1 1 0 1	R13	SCREEN 1 START ADDRESS (L)	memory address	–	R/W								
0	1	0 0 1 1 1 0	R14	CURSOR 1 ADDRESS (H)	memory address	–	R/W								
0	1	0 0 1 1 1 1	R15	CURSOR 1 ADDRESS (L)	memory address	–	R/W								
0	1	0 1 0 0 0 0	R16	LIGHT PEN (H)	–	–	R								
0	1	0 1 0 0 0 1	R17	LIGHT PEN (L)	–	–	R								
0	1	0 1 0 0 1 0	R18	SCREEN 2 START POSITION	row	–	R/W								
0	1	0 1 0 0 1 1	R19	SCREEN 2 START ADDRESS (H)	memory address	–	R/W								
0	1	0 1 0 1 0 0	R20	SCREEN 2 START ADDRESS (L)	memoey address	–	R/W								
0	1	0 1 0 1 0 1	R21	SCREEN 3 START POSTION	row	–	R/W								
0	1	0 1 0 1 1 0	R22	SCREEN 3 START ADDRESS (H)	memory address	–	R/W								
0	1	0 1 0 1 1 1	R23	SCREEN 3 START ADDRESS (L)	memory address	–	R/W								
0	1	0 1 1 0 0 0	R24	SCREEN 4 START POSITION	row	–	R/W								
0	1	0 1 1 0 0 1	R25	SCREEN 4 START ADDRESS (H)	memory address	–	R/W								
0	1	0 1 1 0 1 0	R26	SCREEN 4 START ADDRESS (L)	memory address	–	R/W								
0	1	0 1 1 0 1 1	R27	VERTICAL SYNC POSITION ADJUST	raster	Nvad	W								
0	1	0 1 1 1 0 0	R28	LIGHT PEN RASTER	–	–	R	DP							
0	1	0 1 1 1 0 1	R29	SMOOTH SCROLLING	raster	Nss	R/W								
0	1	0 1 1 1 1 0	R30	CONTROL 1	–	–	W	VE	VS	IB	IL	SY	TV	SP_1	SP_0
0	1	0 1 1 1 1 1	R31	CONTROL 2	–	–	W	SS_4	SS_3	SS_2	SS_1	RI			
				STATUS	–	–	R	AI					E	SB	SL
0	1	1 0 0 0 0 0	R32	CONTROL 3	–	–	W	CM	C_2	CW_1	CW_2	MW	TC	DR	

Note 1) *: Vertical: raster/Horizontal: character.

2) ▨ : "0" is to be set, since these bits may be used in the future.

CS	RS	Register Address 5 4 3 2 1 0	Reg. No.	Register Name	Program Unit	Symbol	R/W	Data Bit 7	6	5	4	3	2	1	0
0	1	1 0 0 0 0 1	R33	MEMORY WIDTH OFFSET	character	Nof	R/W								
0	1	1 0 0 0 1 0	R34	CURSOR 2 START	raster	Ncs_2	W	▨	B_2	P_2					
0	1	1 0 0 0 1 1	R35	CURSOR 2 END	raster	Nce_2	W	▨	▨	▨					
0	1	1 0 0 1 0 0	R36	CURSOR 2 ADDRESS (H)	memory address	–	R/W	▨	▨	▨	▨	▨	▨	▨	▨
0	1	1 0 0 1 0 1	R37	CURSOR 2 ADDRESS (L)	memory address	–	R/W								
0	1	1 0 0 1 1 0	R38	CURSOR 1 WIDTH	character	Ncw_1	R/W								
0	1	1 0 0 1 1 1	R39	CURSOR 2 WIDTH	character	Ncw_2	R/W								

Note 1) *: Vertical: raster/Horizontal: character.
2) ▨ : "0" is to be set, since these bits may be used in the future.

RESET

The $\overline{RES}$ functions as a reset input signal only while the LPSTB is "L". "Reset" is definable in two stages.

(1) "During a reset state" indicates the period that the $\overline{RES}$ remains "L".

(2) "After a reset state" indicates the state after the $\overline{RES}$ transition from "L" to "H".

The pin status during a reset state is in Table 7.

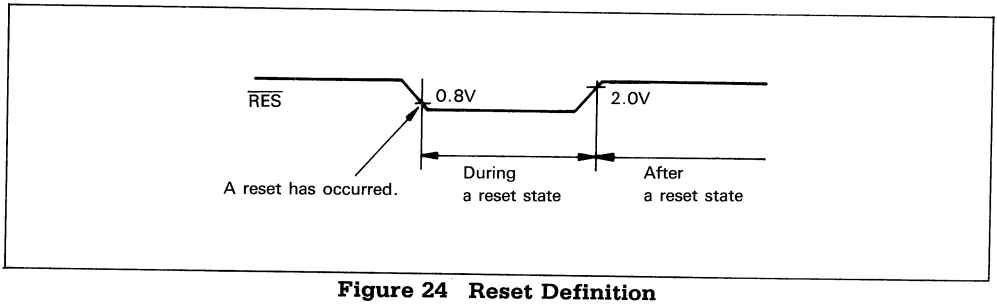


Figure 24 Reset Definition

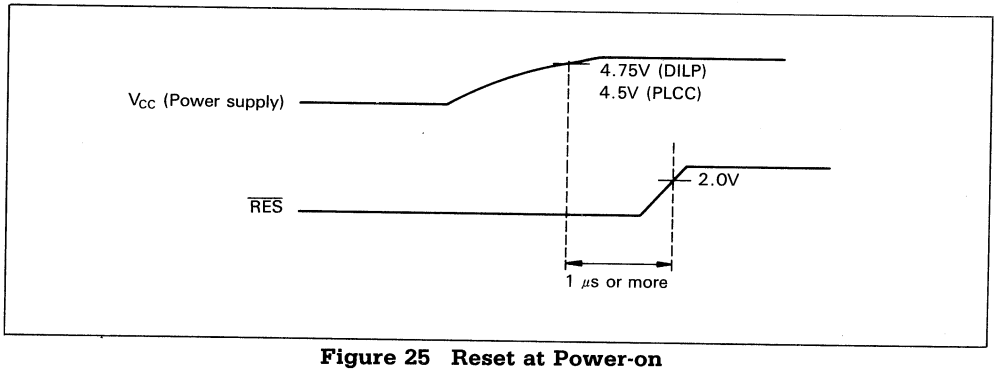


Figure 25 Reset at Power-on

Table 7 Pin Status during a Reset State

Pin No. DP-40	Pin No. CP-44	Symbol	Pin Name	Input/ Output	Pin Status
1	1, 2	V_{SS} ($V_{SS}1$, $V_{SS}2$)**	V_{SS}	–	–
2	3	$\overline{RES}$	RESET	Input	–
3	4	LPSTB	LIGHT PEN STROBE	Input	"L" level signal requested to be supplied
		TSC	THREE STATE CONTROL	Input	
4-17	5-11 13-19	MA0-MA13	MEMORY ADDRESS 0-13	Output	Goes "L" immediately after reset
18	20	DISPTMG	DISPLAY TIMING	Output	Goes "L" immediately after reset
19	21	CUDISP	CURSOR DISPLAY	Output	Goes "L" immediately after reset
		ACI	ACCESS INHIBIT	Output	
		IRQ	INTERRUPT REQUEST	Output	
20	22, 23	V_{CC} ($V_{CC}1$, $V_{CC}2$)**	V_{CC}	–	–
21	24	CLK	CHARACTER CLOCK	Input	Not affected
22	25	R/$\overline{W}$ ($\overline{WR}$)*	READ/WRITE (WRITE)*	Input	Not affected
23	26	E ($\overline{RD}$)*	ENABLE (READ)*	Input	Not affected
24	27	RS	REGISTER SELECT	Input	Not affected
25	28	$\overline{CS}$	CHIP SELECT	Input	Not affected
33-26	37-35 33-29	D0-D7	DATA BUS 0-7	Input/ Output	Not affected
38-34	42-38	RA0-RA4	RASTER ADDRESS 0-4	Output	Goes "L" immediately after reset
39	43	HSYNC	HORIZONTAL SYNC	Output	Outputs HSYNC signal until external sunch mode is set into the control 1 register (R29) after reset
		EXHSYNC	EXTERNAL HORIZONTAL SYNC	Input	
40	44	VSYNC	VERTICAL SYNC	Output	Outputs VSYNC signal until external sync mode is set into the control 1 register (R29) after reset
		EXVSYNC	EXTERNAL VERTICAL SYNC	Input	

Note : * marked pins are of the HD6445
** marked pins are of the CP-44

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Rating	Unit
Supply Voltage		V_{CC}*	−0.3 to +7.0	V
Input Voltage		V_{in}*	−0.3 to V_{CC} +0.3	V
Operating Temperature		T_{opr}	−20 to +75	°C
Storage Temperature		T_{stg}	−55 to +150	°C
Allowable Output Current	Data Bus	$\|I_O\|$**	5	mA
	Others		3	mA
Total Allowable Output Current		$\|\Sigma I_O\|$***	60	mA

* This value is in reference to V_{SS}=0V.
** The allowable output current is the maximum current that may be drawn from, of flow out to, one output pin or one input/output common pin.
*** The total allowable output current is the toral sum of currents that may be drawn from, or flow out to, output pins or input/output common pin.
Note: Using an LSI beyond its maximum ratings may result in its permanent destruction. LSI's should usually be under recommended operating conditions.
Exceeding any of these conditions may adversely affect its reliability.

RECOMMENDED OPERATING CONDITIONS

Item		Symbol	Min	Typ	Max	Unit
Power Supply Voltage	DP-40	V_{CC}*	4.75	5.0	5.25	V
	CP-44		4.5		5.5	
Input Low Level Voltage		V_{IL}*	−0.3	—	0.8	V
Input High Level Voltage		V_{IH}*	2.0	—	V_{CC}	V
Operating Temperature		T_{opr}	−20	25	75	°C

* This value is in reference to V_{SS}=0V.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(V_{CC}=5.0V ±5 % (DILP), 5.0 ±10 % (PLCC), V_{SS}=0V, T_a=−20 to +75°C (Normal) −40 to +85°C (J), unless otherwise noted)

Item		Symbol	Min	Typ*	Max	Unit	Test Conditions
Input High Level Voltage		V_{IH}	2.0	—	V_{CC}	V	
Input Low Level Voltage		V_{IL}	−0.3	—	0.8	V	
Input Leak Current	Input except D_0-D_7	I_{in}	−2.5	—	2.5	μA	V_{in}=0 to 5.25 V
Three-State (Off State) Input Current	D_0-D_7 Memory Address Raster Address	I_{TSI}	−10	—	10	μA	V_{in}=0.4 to 2.4 V V_{CC}=5.25 V
Output High Level Voltage	D_0-D_7	V_{OH}	2.4	—	—	V	I_{OH}=-205μA
	Others						I_{OH}=-100μA
Output Low Level Voltage		V_{OL}	—	—	0.4	V	I_{OL}=1.6mA
Input Capacity	D_0-D_7 EXVSYNC EXHSYNC	C_{in}	—	—	12.5	pF	V_{in}=0 V T_a=25°C f=1.0 MHz
	Others		—	—	10	pF	
Output Capacity		C_{out}	—	—	10	pF	V_{in}=0 V T_a=25°C f=1.0 MHz
Power Dissipation	No Load	P_D	—	50	100	mW	f_{CLK}=4.5 MHz f_E=2.0 MHz V_{CC}=max V_{IH}=V_{CC}-1.0 V V_{IL}=0.8 V
	Test Load			100	200		

* T_a=2.5°C, V_{CC}=5.0 V

AC CHARACTERISTICS

(V_{CC}=5.0V ±5 % (DILP), 5V ±10 % (PLCC), V_{SS}=0V, T_a=−20 to +75°C (Normal), −40 to +85°C (J), unless otherwise noted.)

1. Timing of CRT control signal

Item	Symbol	Min	Typ	Max	Unit	Reference Figure
Clock Cycle Time	tcycC	220	–	–	ns	Fig. 26
Clock High Pulse Width	PW_{CH}	100	–	–	ns	
Clock Low Pulse Width	PW_{CL}	100	–	–	ns	
Rise and Fall Time for Clock Input	tcr, tcf	–	–	20	ns	
Memory Address Delay Time	t_{MAD}	–	–	80	ns	
Raster Address Delay Time	t_{RAD}	–	–	80	ns	
DISPTMG Delay Time	t_{DTD}	–	–	120	ns	
CUDISP Delay Time	t_{CDD}	–	–	120	ns	
Horizontal Sync Delay Time	t_{HSD}	–	–	100	ns	
Vertical Sync Delay Time	t_{VSD}	15*	–	120	ns	
Light Pen Strobe Pulse Width	PW_{LPH}	60	–	–	ns	
Light Pen Strobe Uncertain Time of Acceptance	t_{LPD1}	–	–	70	ns	Fig. 28
	t_{LPD2}	–	–	0	ns	Fig. 29
Memory Address Three-State Off Time	t_{MAZ}	–	–	50	ns	Fig. 27
Raster Address Three-State Off Time	t_{RAZ}	–	–	50	ns	

Note*: Application after mark 7C1

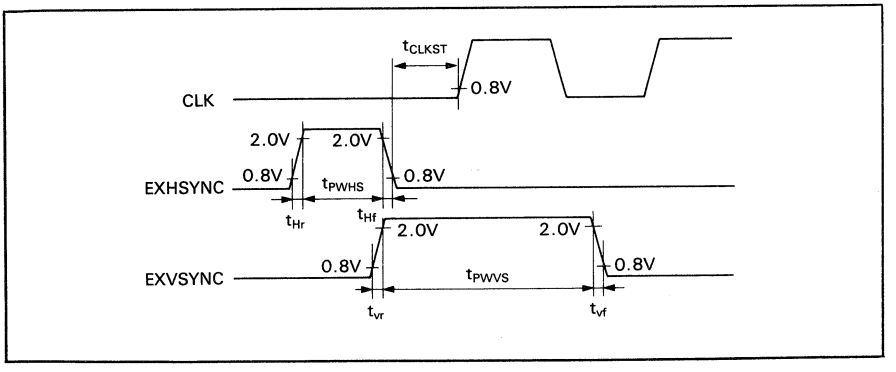
2. External sync timing

Item	Symbol	Min	Typ	Max	Unit	Reference Figure
External Vertical Sync Pulse Width*	t_{PWVS}	$2 \cdot t_{cyc}C$	–	–	ns	Fig. 32
External Vertical Sync Rise and Fall Time	t_{vr}	–	–	20	ns	
	t_{vf}	–	–	20	ns	
Master Slave Mode. EXVSYNC Uncertain Time of Acceptance	t_{EVM1}	10	–	–	ns	Fig.30
	t_{EVM2}	60	–	–	ns	
External Horizontal Sync Pulse Width	t_{PWHS}	$2 \cdot t_{cyc}C$	–	–	ns	Fig.31
External Horizontal Sync Rise and Fall Time	t_{Hr}	–	–	20	ns	Fig.32
	t_{Hf}	–	–	20	ns	
TV sync mode. EXHSYNC Uncertain Time of Acceptance	t_{EHT1}	30	–	–	ns	
	t_{EHT2}	50	–	–	ns	
TV Sync mode. EXVSYNC set-up Time	t_{EVS}	50	–	–	ns	
TV Sync mode. EXVSYNC Hold Time	t_{EVH}	50	–	–	ns	

Note * : Normal application add input over 1H (One raster period)
The above specification is applied after mark 7C1.
The following specification is applied before it.
The above specification is upward-compatible with the following specification.

External sync timing

Item	Symbol	Min	Typ	Max	Unit
Clock Halt Time	t_{CLKST}	100	–	–	ns
External Horizontal Sync Pulse Width	t_{PWHS}	1000	–	–	ns
External Horizontal Sync Rise and Fall Time	t_{Hr}	–	–	20	ns
	t_{Hf}	–	–	20	ns
External Vertical Sync Pulse Width	t_{PWVS}	1660	–	–	ns
External Vertical Sync Rise and Fall Time	t_{Vr}	–	–	20	ns
	t_{Vf}	–	–	20	ns



3. MP Bus Timing

(1) HD6345 MPU bus timing

Item	Symbol	6345 Min	6345 Max	63A45 Min	63A45 Max	63B45 Min	63B45 Max	Unit	Reference Figure
Enable Cycle Time	$tcyc_E$	1000	–	666	–	500	–	ns	Fig. 33
Enable High Pulse Width	PW_{EH}	450	–	280	–	220	–	ns	Fig. 34
Enable Low Pulse Width	PW_{EL}	400	–	280	–	210	–	ns	
Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	20	–	20	–	20	ns	
Address Setup Time	t_{AS}	80	–	80	–	40	–	ns	
Data Setup Time	t_{DSW}	195	–	80	–	60	–	ns	
Data Delay Time	t_{DDR}	–	200	–	140	–	120	ns	
Data Hold Time	t_H	10	–	10	–	10	–	ns	
Address Hold Time	t_{AH}	10	–	10	–	10	–	ns	
Data Access Time	t_{ACC}	–	280	–	220	–	160	ns	
Input Signal Rise and Fall Time ($\overline{RES}$, LPSTB, RS, $\overline{CS}$, R/$\overline{W}$)	tr, tf	–	100	–	100	–	100	ns	

(2) HD6445 MPU bus timing

Item	Symbol	Min	Typ	Max	Unit	Reference Figure
Read Address Setup Time	t_{AR}	0	–	–	ns	Fig. 35
Read Low Level Time	t_{RR}	160	–	–	ns	Fig. 36
Read Address Hold Time	t_{RA}	0	–	–	ns	
Write Address Setup Time	t_{AW}	0	–	–	ns	
Write Low Level Time	t_{WW}	190	–	–	ns	
Write Address Hold Time	t_{WA}	0	–	–	ns	
Data Delay Time	t_{RD}	–	–	120	ns	
Data Hold Time (Read)	t_{DF}	10	–	–	ns	
Data Setup Time	t_{DW}	60	–	–	ns	
Data Hold Time (Write)	t_{WD}	0	–	–	ns	
Access Inhibit Time	t_{DIS}	210	–	–	ns	
Input Signal Rise Time, Fall Time ($\overline{RES}$, LPSTB, RS, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$)	t_r t_f	–	–	100	ns	

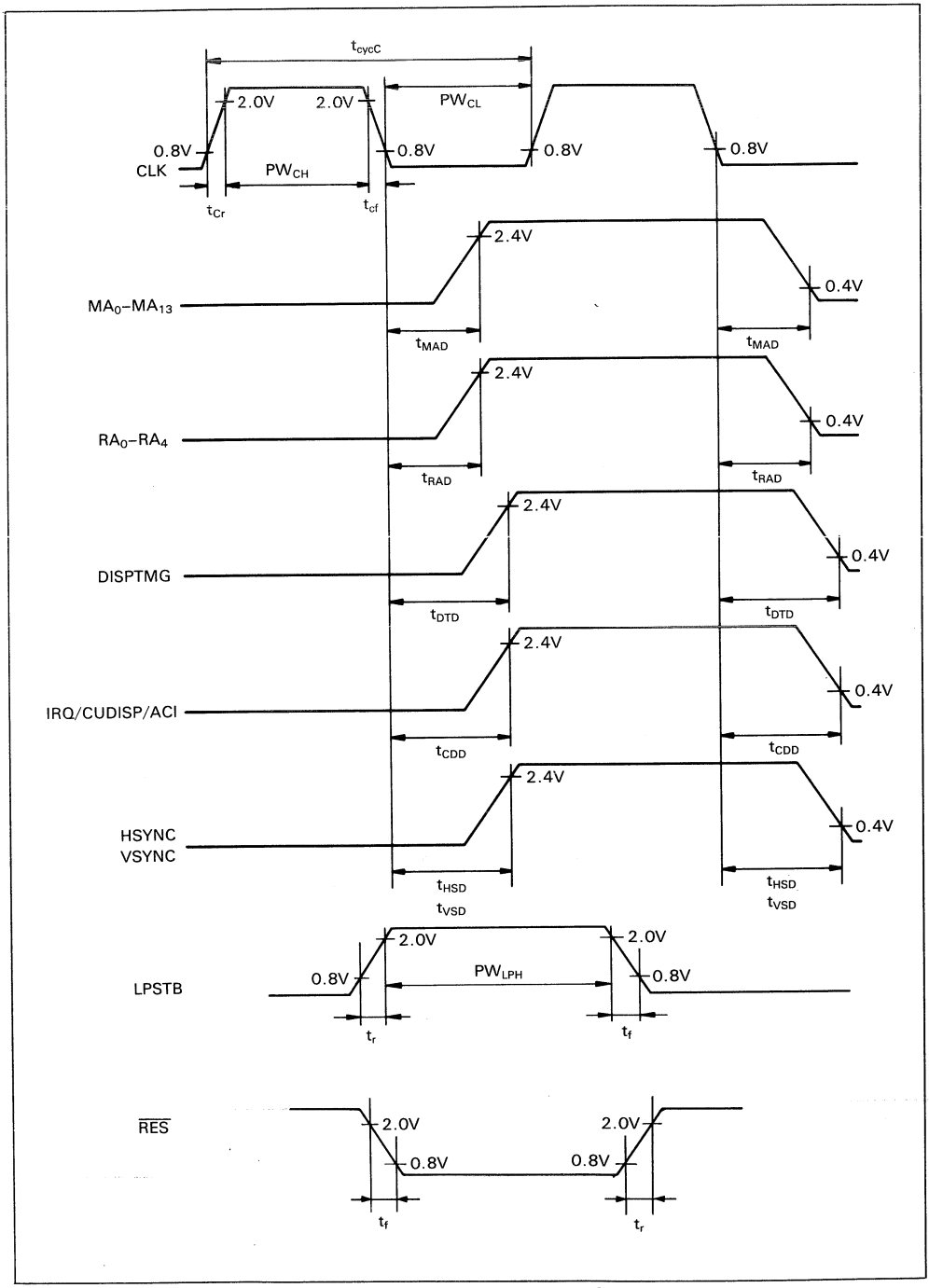


Figure 26 CRTC-II Timing Chart

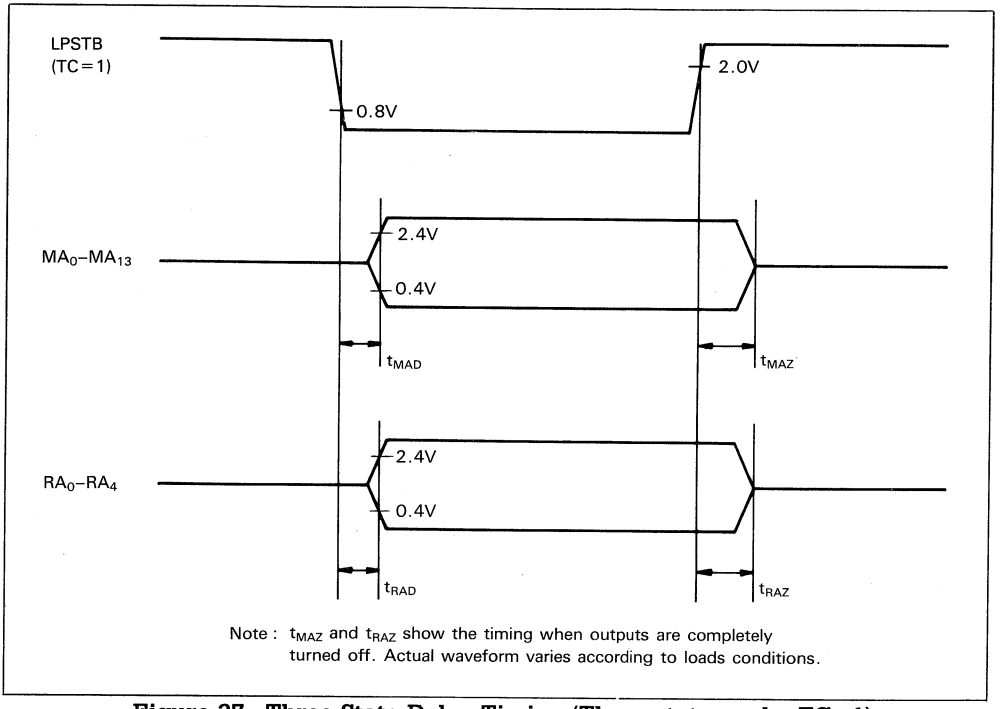


Figure 27 Three-State Delay Timing (Three-state mode: TC=1)

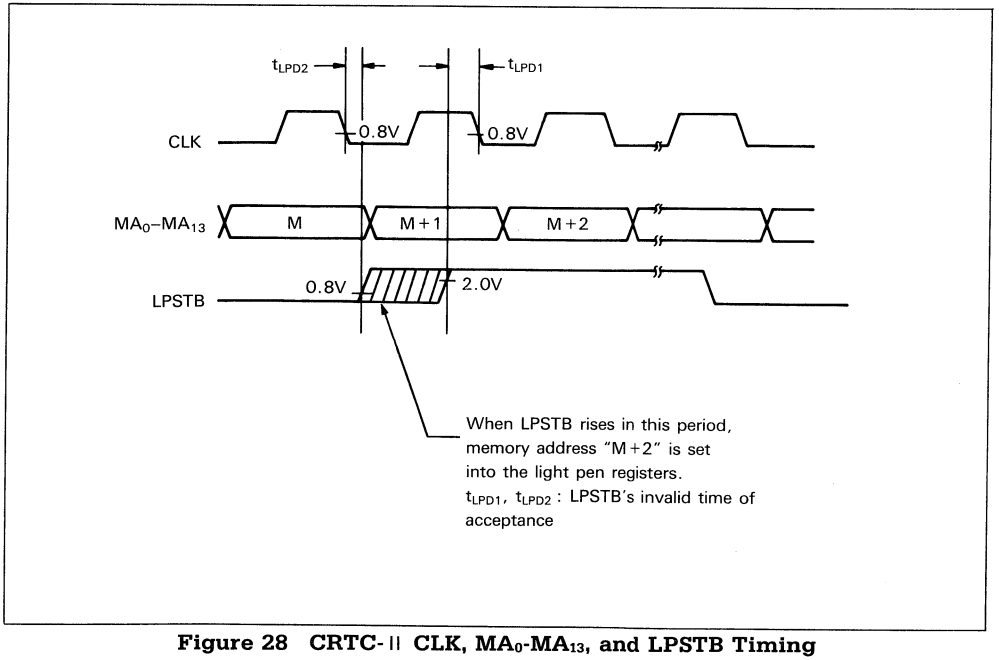


Figure 28 CRTC-II CLK, MA0-MA13, and LPSTB Timing

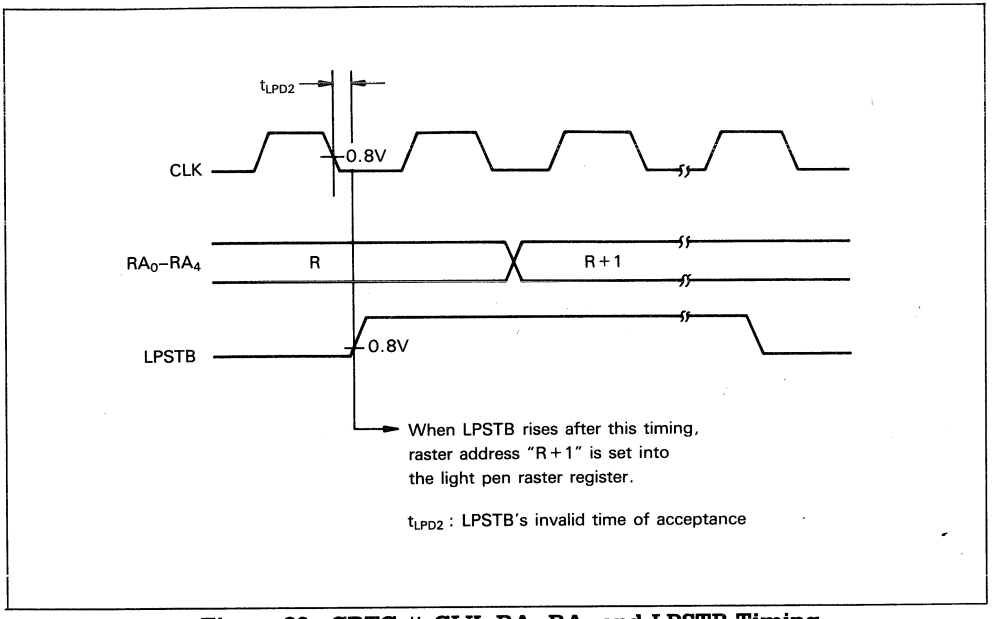


Figure 29 CRTC-II CLK, RA_0-RA_4 and LPSTB Timing

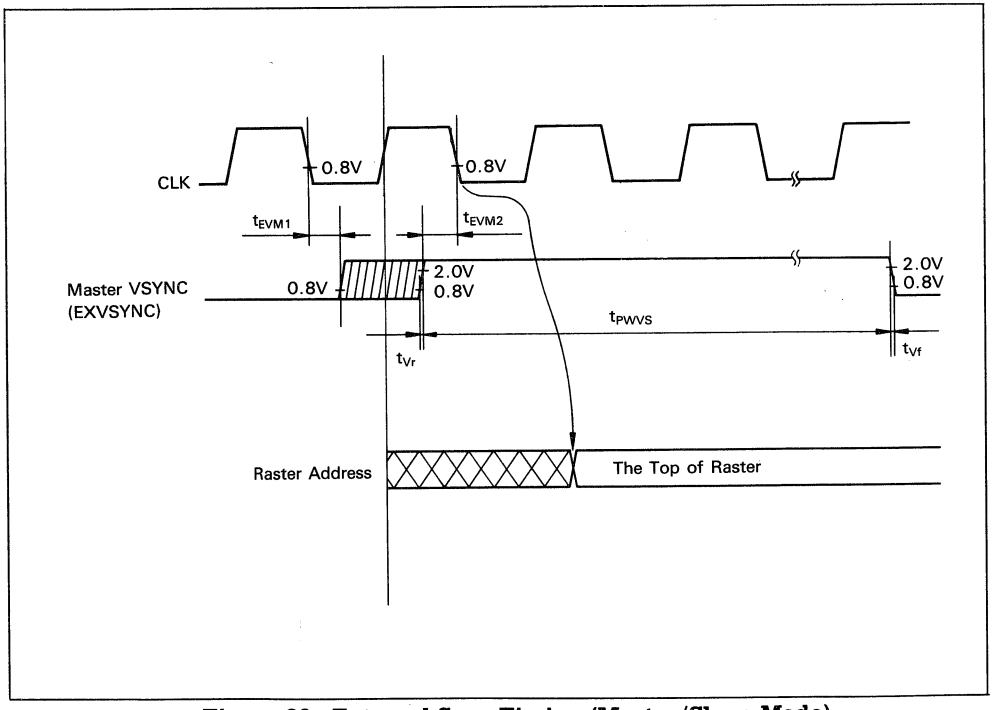


Figure 30 External Sync Timing (Master/Slave Mode)

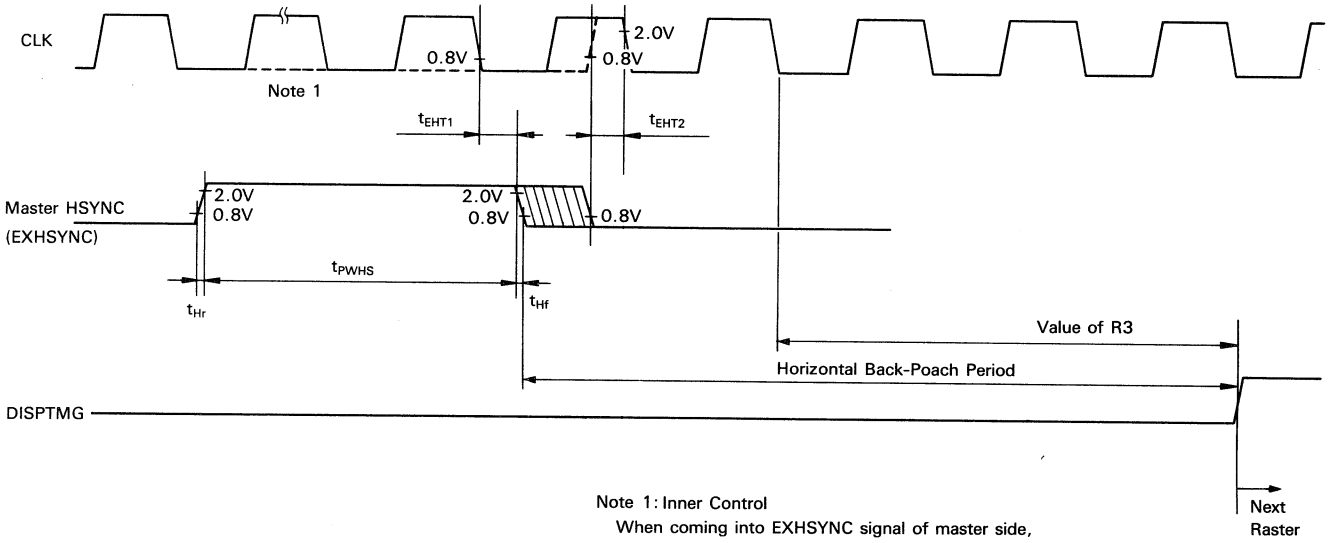
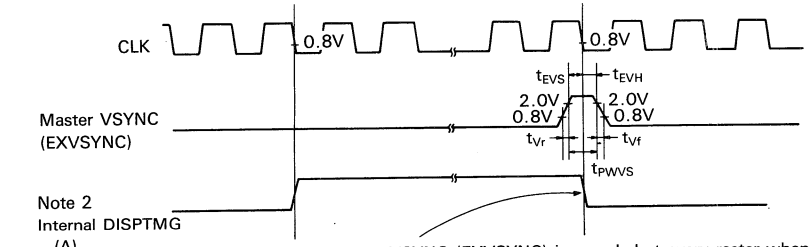
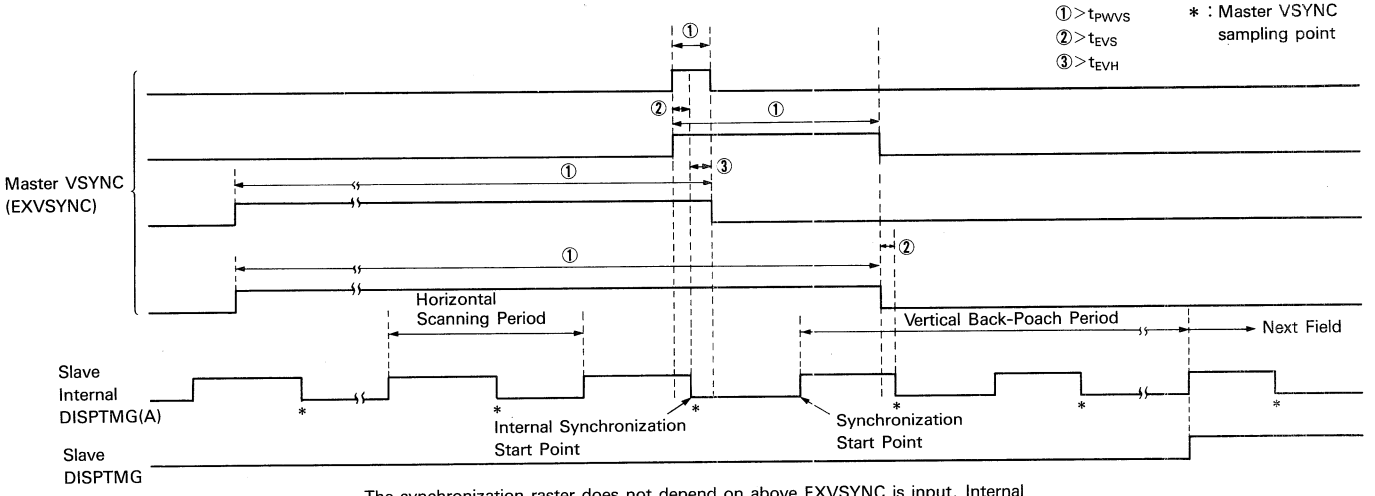


Figure 31 External Sync Timing (TV Sync Mode: EXHSYNC)



Master VSYNC (EXVSYNC) is sampled at every raster when internal DISPTMG(A) is falling. Whether the data is to be latched at current raster or at the next raster is determined at the negative edge of internal DISPTMG(A).



The synchronization raster does not depend on above EXVSYNC is input. Internal DISPTMG (A) signal is no output out of LSI in vertical retrace period, rise by starting horizontal display period, fall by ending it. Normal application add input the EXVSYNC over 1H (One raster period).

Figure 32-(a) External Sync Timing (TV Sync Mode: EXVSYNC)

Note : Internal DISPTMG
Internal DISPTMG (A) : The internal DISPTMG (A) show the display signal of the horizontal direction in circuit.
Internal DISPTMG (B) : The internal DISPTMG (B) show the display signal of the vertical direction in circuit.

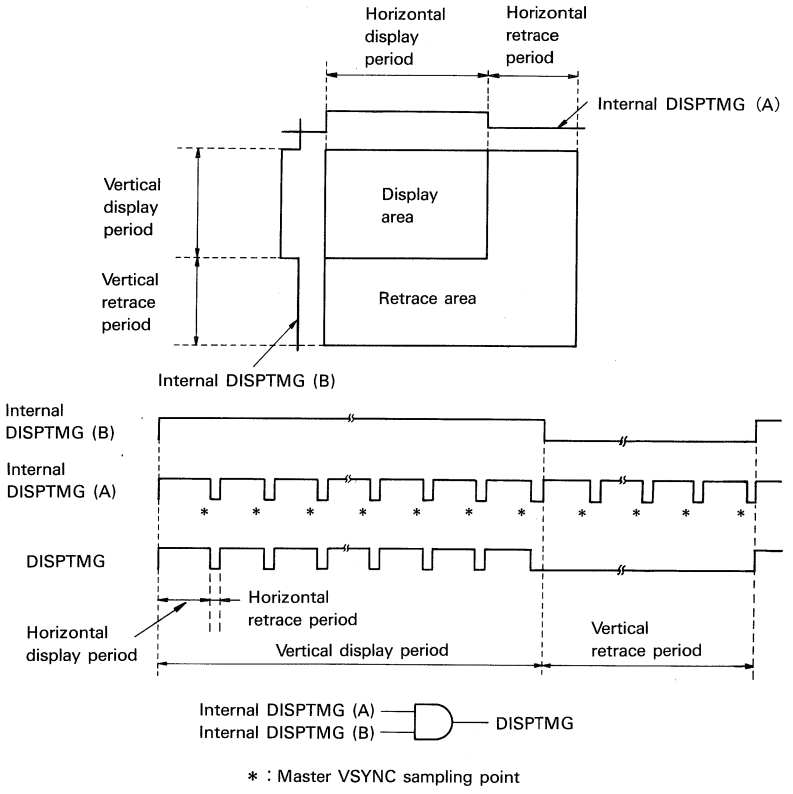


Figure 32-(b) External Sync Timing (TV Sync Mode: EXVSYNC)

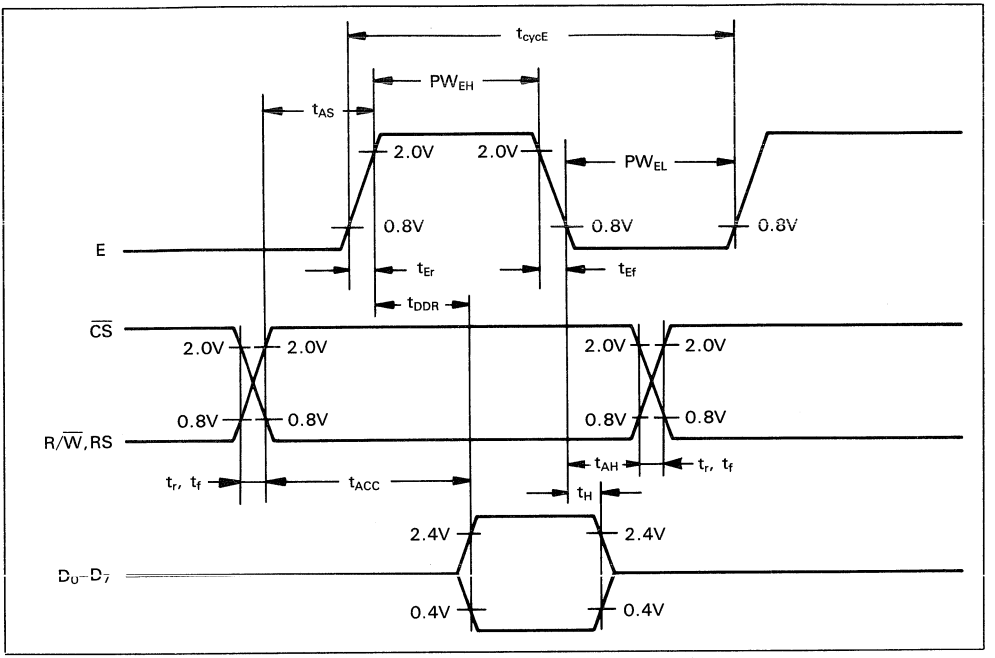


Figure 33 Read Sequence (HD6345)

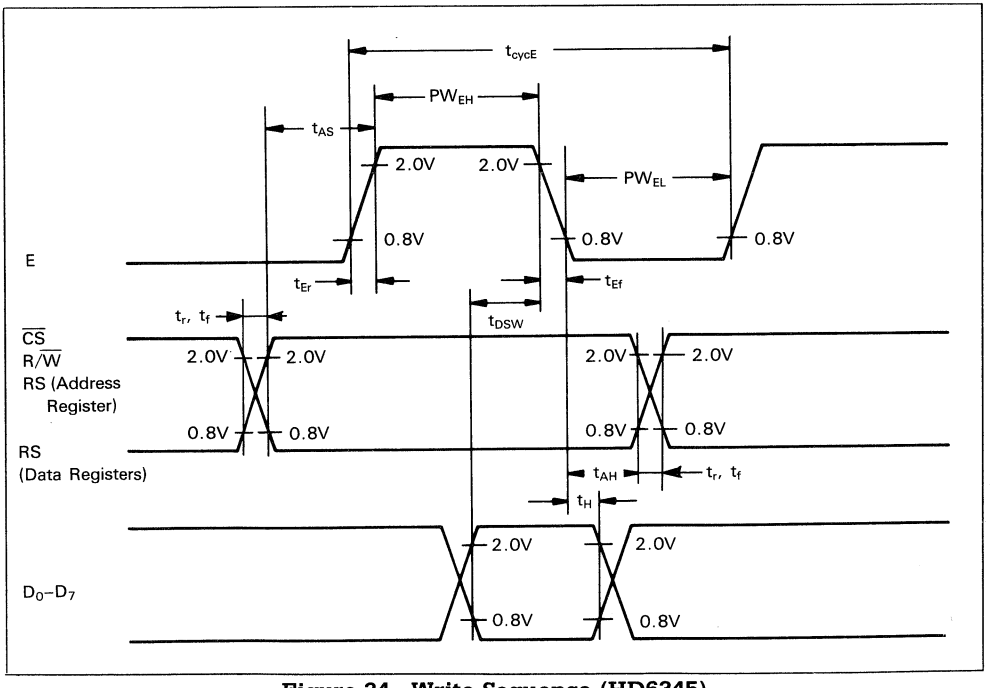


Figure 34 Write Sequence (HD6345)

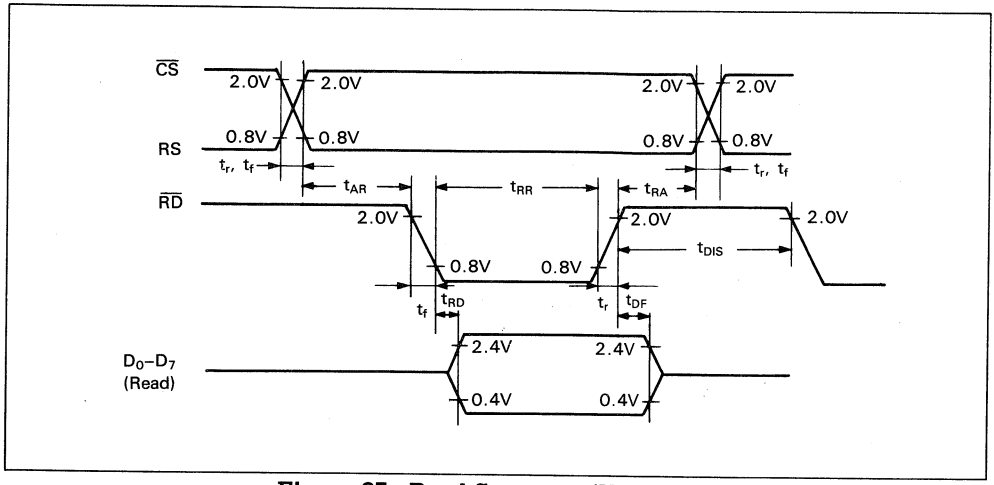


Figure 35 Read Sequence (HD6445)

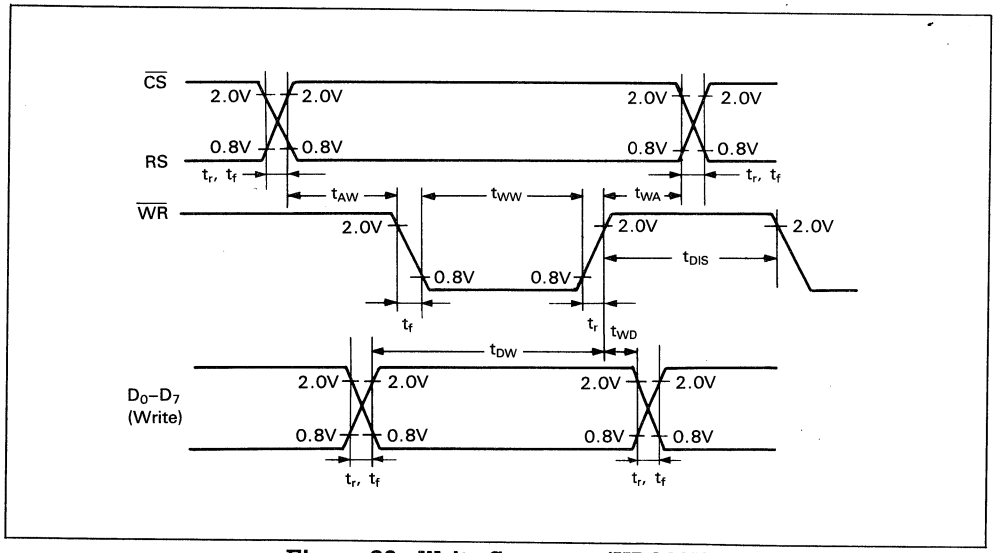


Figure 36 Write Sequence (HD6445)

TEST LOAD

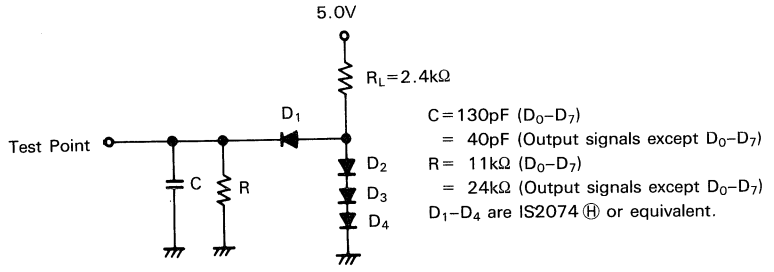


Figure 37 Test Load

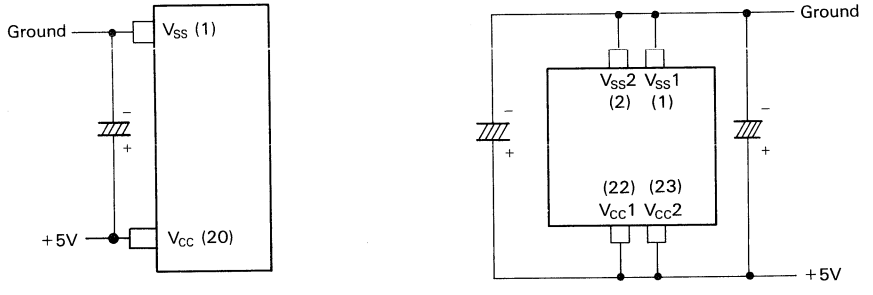


Figure 38 Note on Power Line Example

J SPECIFICATION

There is J specification in PLCC-44 of CRTC - II (HD6345/HD6445). J specification operating temperature is wider than normal specification operating temperature.

(1) Absolute maximum ratings

Item	Symbol	Rating	Unit
Operating temperature	T_{opr}	−40 to +85	°C

(2) Recommended operating conditions

		HD6345 CPJ			HD6445 CPJ			
Item	**Symbol**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**
Input high level voltage	V_{IH}*	CLK 2.2	–	V_{CC}	CLK, $\overline{WR}$ $\overline{RD}$ 2.2	–	V_{CC}	V
		Other 2.0	–	V_{CC}	Other 2.0	–	V_{CC}	V
Operating temperature	T_{opr}	−40	25	85	−40	25	85	°C

* This value is in reference to V_{SS} = 0 V.

(3) Electrical characteristics

		HD6345 CPJ			HD6445 CPJ			
Item	**Symbol**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**
Input high level voltage	V_{IH}	CLK 2.2	–	V_{CC}	CLK, $\overline{WR}$ $\overline{RD}$ 2.2	–	V_{CC}	V
		Other 2.0	–	V_{CC}	Other 2.0	–	V_{CC}	V

(4) Other item is the same normal specification items (Absolute Maximum Ratings, Recommended Operating Conditions, Electrical Characteristics).

CHARACTERISTICS DIFFERENCES BETWEEN HD6345 AND HD6845S

NO.	Item	Symbol	HD6345 Min	Typ	Max	HD6845S Min	Typ	Max	Unit
1	Power Dissipation	P_D	–	50	–	–	600	1000	mW
2	Clock Cycle Time	$tcyc_C$	220	–	–	270	–	–	ns
3	Clock High Pulse Width	PW_{CH}	100	–	–	130	–	–	ns
4	Clock Low Pulse Width	PW_{CL}	100	–	–	130	–	–	ns
5	Memory Address Delay Time	t_{MAD}	–	–	80	–	–	160	ns
6	Raster Address Delay Time	t_{RAD}	–	–	80	–	–	160	ns
7	Display Timing Delay Time	t_{DTD}	–	–	120	–	–	250	ns
8	Horizontal Sync Delay Time	t_{HSD}	–	–	100	–	–	200	ns
9	Vertical Sync Delay Time	t_{VSD}	–	–	120	–	–	250	ns
10	Cursor Display Delay Time	t_{CDD}	–	–	120	–	–	250	ns
11	Enable Cycle Time	$tcyc_E$	500	–	–	1000	–	–	ns
12	Enable High Pulse Width	PW_{EH}	220	–	–	450	–	–	ns
13	Enable Low Pulse Width	PW_{EL}	210	–	–	400	–	–	ns
14	Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	–	20	–	–	–	ns
15	Address Set Up Time	t_{AS}	40	–	–	140	–	–	ns
16	Data Set Up Time	t_{DSW}	80	–	–	195	–	–	ns
17	Data Delay Time	t_{DDR}	–	–	120	–	–	320	ns
18	Data Access Time	t_{ACC}	–	–	160	–	–	460	ns
19	Input Signal Rise and Fall Time	t_r, t_f	–	–	100	–	–	–	ns

CHARACTERISTICS DIFFERENCES BETWEEN HD6445 AND HD6845S

NO.	Item	Symbol	HD6445 Min	Typ	Max	HD6845S Min	Typ	Max	Unit
1	Power Dissipation	P_D	–	50	–	–	600	1000	mW
2	Clock Cycle Time	$tcyc_C$	220	–	–	270	–	–	ns
3	Clock High Pulse Width	PW_{CH}	100	–	–	130	–	–	ns
4	Clock Low Pulse Width	PW_{CL}	100	–	–	130	–	–	ns
5	Memory Address Delay Time	t_{MAD}	–	–	80	–	–	160	ns
6	Raster Address Delay Time	t_{RAD}	–	–	80	–	–	160	ns
7	Display Timing Delay Time	t_{DTD}	–	–	120	–	–	250	ns
8	Horizontal Sync Delay Time	t_{HSD}	–	–	100	–	–	200	ns
9	Vertical Sync Delay Time	t_{VSD}	–	–	120	–	–	250	ns
10	Cursor Display Delay Time	t_{CDD}	–	–	120	–	–	250	ns

Refer to user's manual (No. ADE-602-006A), application note (No. ADE-502-004) for detail of this product.

HD64460

Preliminary

CRT Controller Plus (CRTC+)

The CRTC+ is a single-chip CRT controller implementing graphic and character display functions which correspond to the VGA (Video Graphics Adapter™) for IBM personal computers.

Since the CRTC+ combines a video signal generator using a color palette, the graphics functions of the IBM-VGA, and control functions for a dynamic RAM frame buffer into a single chip, it provides the total system control required to implement graphic and character display with one chip.

In addition, the CPU can access the frame buffer up to four times faster with the CRTC+ than with the IBM-VGA. Graphics can therefore be created faster and CPU wait time is reduced.

In addition to the VGA features, the CRTC+ includes additional extended features, and it also has enhanced 6845 modes which correspond to the IBM-CGA (Color Graphics Adapter™), IBM-MDA (Monochrome Display Adapter™), or HGA (Hercules Graphics Adapter™).
These features enable the design of a multi-function personal computer graphic system using one CRTC+ chip.

In addition to the VGA functions, the CRTC+ supports many extended functions, including 132-column text display, frame buffer bank switching, additional text fonts, monochrome reverse video, and non-wait display/CPU access (smart access) for more efficient graphics drawing. These extended functions greatly simplify support for future products.

Notes:
1. IBM-PC, IBM-PS/2, VGA, CGA, and MDA are registered trademarks of International Business Machines Corporation.
2. Hercules Graphics is a registered trademark of Hercules Computer Technologies Corporation.

Features

Compatibility

- Hardware-and software-compatible with the IBM-VGA board
- Software-compatible with the IBM-MDA, IBM-CGA, and HGA modes*
- Compatible with IBM-EGA at the BIOS level**

* Functions provided by the CRTC+ but not by the VGA.
** EGA software can be used via BIOS (Basic Input Output System) software.

Display Control Functions

- Both bit-mapped graphics and code refresh supported
- Variety of resolutions supported:
  640 × 480 (VGA), 640 × 200 and 320 × 200 (CGA), 720 × 350 (MDA), 720 × 348 (HGA), 640 × 350 (EGA), and 800 × 600 (extended function)
- Dot clock speeds of up to 37 MHz (132-column text display mode)
- 2-partition screen splitting
- Programmable underlining, programmable cursor display (underline and cursor control by hardware)
- Flashless vertical smooth scroll, flashless horizontal panning scroll
- Interrupt generated at the start of the vertical retrace period

Ordering Information

Type	Clock Frequency [MHz]	Package
HD64460F28	32.0	FP-136
HD64460F37	37.0	

Graphics Assist Functions

- Bit shift and color logic operations on graphics data in the frame buffer
- Programmable bit masking and memory plane masking
- Copying of graphics using byte-boundary data in the frame buffer
- Writing of a specified color in the frame buffer
- Color data comparison in the frame buffer

Frame Buffer Access

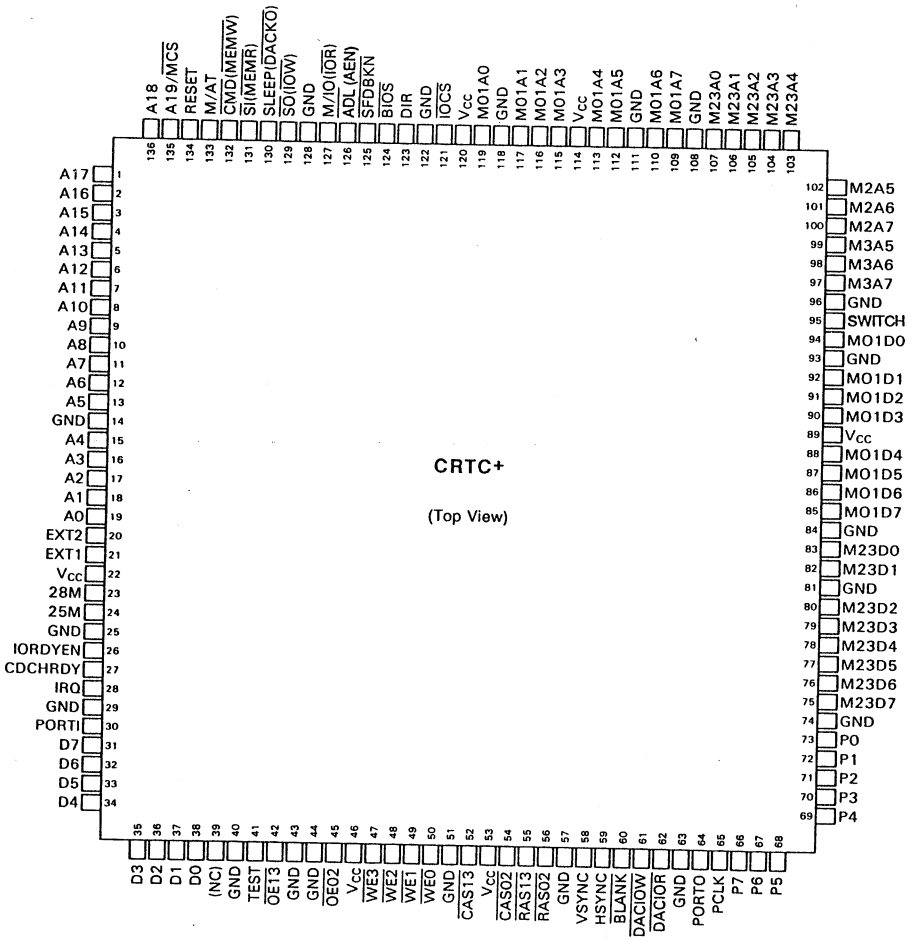
- Direct interface with a 256-kbyte memory using 64k × 4-type dynamic RAM chips (HM50464 or equivalent)
- Generation of dynamic RAM control signals ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)
- Generation of dynamic RAM refresh addresses
- Improved efficiency in CPU graphics drawing access through non-wait display/CPU access (smart access)

Other Features

- Switching to HD6845 (CRTC) compatible register configurations (MDA, CGA, and HGA modes)*
- 132-column text display (7 dots per character)* (available only in the HD64460F37 version.)
- Frame buffer bank switching*
- Additional text fonts*
- BIOS ROM bank switching*
- BIOS signal output masking*
- Three-state control of video pins*
- Monochrome reverse video (in MDA and HGA modes)*
- Port input*

* Functions provided by the CRTC+ but not by the VGA.

Pin Arrangement



Note: Connect (NC) [pin 39] to Vcc or ground

Pin Description

Power

Signal	Pin No.	Input/Output	Function
Vcc	22, 46, 53, 89, 114, 120	—	Power supply for the CRTC+: 5 V ±5%
Vss	14, 25, 29, 40, 43, 44, 51,57, 63, 74, 81, 84, 93, 96, 108, 111, 118, 122, 128	—	Ground for the CRTC+

Note: Connect all 25 Vcc and Vss power pins of the CRTC+ to the power supply or ground. Connect a bypass capacitor across Vcc and Vss as close to the pins as possible, as a noise killer.

CPU Interface

Signal	Pin No.	Input/Output	Function
A_{19}/$\overline{MCS}$	135	I	A_{19}/$\overline{MCS}$ is used to input the A_{19} address signal or the $\overline{MCS}$ signal derived from a higher address decoder when the frame buffer is acessed. A_{19}/$\overline{MCS}$ is switched to A_{19} when bit 3 of extended register 2 is 0, and to $\overline{MCS}$ when bit 3 of extended register 2 is 1.
A_{18}-A_0	136,1-13, 15-19	I	A_{18}-A_0 are the address input signals from the system bus. Address information input to these pins is used to access the frame buffer, BIOS ROM, color palette, and internal registers.
D_7-D_0	31-38	I/O	D_7-D_0 are used to transfer data between the CPU system and the CRTC+. The frame buffer and CRTC+ registers can be accessed through these lines.
$\overline{IOCS}$	121	I	$\overline{IOCS}$ selects the I/O address mapping function of the CRTC+. If $\overline{IOCS}$ is high when reset input is negated, the A_{15}-A_0 lines are used for accessing the I/O address. If $\overline{IOCS}$ is low when reset is negated, $\overline{IOCS}$ functions as I/O chip select after the reset. In this case, I/O addresses can be mapped to the area specified by the $\overline{IOCS}$ in place of the A_{15}-A_8 lines.
DIR	123	O	DIR indicates the data transfer direction on the system bus. Data is transferred from the system bus to the CRTC+ when DIR is high, and is transferred from the CRTC+ to the system bus when DIR is low.
M/$\overline{IO}$ ($\overline{IOR}$)	127	I	M/$\overline{IO}$ switches between I/O access and frame buffer access in the micro channel bus mode. High indicates frame buffer access; low indicates I/O access. $\overline{IOR}$ controls reading of the CRTC+ registers (I/O read command) in the I/O channel bus mode.

Signal	Pin No.	Input/Output	Function
$\overline{S0}$ ($\overline{IOW}$)	129	I	$\overline{S0}$ indicates access status 0 when the micro channel bus mode is used: **M/IO** **$\overline{S0}$** **$\overline{S1}$** **Status** 0 0 0 Reserved A 0 0 1 I/O write 0 1 0 I/O read 0 1 1 Reserved B 1 0 0 Reserved C 1 0 1 Memory write 1 1 0 Memory read 1 1 1 Reserved D 0: Low level 1: High level $\overline{IOW}$ controls writing to the CRTC+ registers in the I/O channel bus mode.
$\overline{S1}$ ($\overline{MEMR}$)	131	I	$\overline{S1}$ indicates access status 1 in the micro channel bus mode (see description of $\overline{S0}$). $\overline{MEMR}$ controls the reading of frame buffer data and BIOS ROM in the I/O channel bus mode.
$\overline{CMD}$ ($\overline{MEMW}$)	132	I	$\overline{CMD}$ indicates that valid data is present on the data bus (D_7-D_0) in the micro channel bus mode. $\overline{MEMW}$ controls the writing of frame buffer data in the I/O channel bus mode.
$\overline{ADL}$ (AEN)	126	I	$\overline{ADL}$ is the latch command for address signals on the address bus (A_{19}-A_0) in the micro channel bus mode. When AEN is asserted in the I/O channel bus mode, I/O access to the CRTC+ is ignored in the I/O channel bus mode. AEN assertion indicates that DMA transfer is being performed on the system bus.
SLEEP ($\overline{DACK0}$)	130	I	SLEEP disables both I/O access and memory access in the micro channel bus mode. $\overline{DACK0}$ inhibits the system from accessing the frame buffer in I/O channel bus mode.
$\overline{SFDBKN}$	125	O	$\overline{SFDBKN}$ indicates that either an I/O address or memory address mapped by the CRTC+ has ben accessed in the micro channel bus mode. $\overline{SFDBKN}$ must be left disconnected in I/O channel bus mode.
CDCHRDY	27	O	CDCHRDY indicates the data transfer completion/wait status between the system and the CRTC+. The CRTC+ performs the CPU wait control by driving the CDCHRDY pin low when the CPU attempped to access the frame buffer during the CRTC+ display access.

Signal	Pin No.	Input/Output	Function
CDCHRDY	27	O	The CRTC+ performs the CPU wait control against the I/O access when the IORDYEN pin is high. The wait control function for I/O access can be disabled by driving the IORDYEN pin low when the CPU does not need high-speed operation.
IRQ	28	O	IRQ is an interrupt request to the system.
$\overline{\text{BIOS}}$	124	O	$\overline{\text{BIOS}}$ output is used to access the BIOS ROM in the I/O channel bus mode (M/AT pin = low). $\overline{\text{BIOS}}$ output is kept to be High in the micro channel bus mode.

Operation Mode Interface

Signal	Pin No.	Input/Output	Function
RESET	134	I	RESET initializes the internal status of the CRTC+.
25M	24	I	25M is the input pin for a 25.175-MHz clock source. 25M is used to display a horizontal 640-dot screen.
28M	23	I	28M is the input pin for a 28.322-MHz clock source. 28M is used to display a horizontal 720-dot screen.
EXT1	21	I	An external clock other than 25 MHz, 28 MHz, and EXT2 can be input to EXT1. The EXT1 clock is selected when the CRTC+ is in external clock mode1, and also in the CGA mode.
EXT2	20	I	An external clock other than 25 MHz, 28 MHz, and EXT1 can be input to EXT2. The EXT2 clock is selected when the CRTC+ is in external clock mode2, and also in the MDA or HGA mode.
M/AT	133	I	M/AT selects either the micro channel bus mode or I/O channel bus mode. High selects the micro channel bus mode; low selects the I/O channel bus mode.
IORDYEN	26	I	IORDYEN determines whether wait control for CPU access is enabled or disabled when I/O access is performed. When IORDYEN is low, CDCHRDY stays in the high inpedance state. When IORDYEN is high, CDCHRDY goes low (not ready) in order to make the system wait.
SWITCH	95	I	Input to SWITCH sets bit 4 in the input status register 0. Normally, SWITCH is used to indicate either monochrome or color monitor.
PORT0, PORT1	64, 30	I	Inputs to port0 and port1 set bits 0 and 1 in the port register (POT).

Signal	Pin No.	Input/Output	Function
TEST	41	I	TEST is used for chip testing. The TEST pin must always be low.

Frame Buffer Interface

Signal	Pin No.	Input/Output	Function
$\overline{\text{RAS02}}$	56	O	$\overline{\text{RAS02}}$ outputs the row address strobe to memory planes 0 and 2.
$\overline{\text{RAS13}}$	55	O	$\overline{\text{RAS13}}$ outputs the row address strobe to memory planes 1 and 3.
$\overline{\text{CAS02}}$	54	O	$\overline{\text{CAS02}}$ outputs the column address strobe to memory planes 0 and 2.
$\overline{\text{CAS13}}$	52	O	$\overline{\text{CAS13}}$ outputs the column address strobe to memory planes 1 and 3.
$\overline{\text{OE02}}$	45	O	$\overline{\text{OE02}}$ outputs the read enable signal to memory planes 0 and 2.
$\overline{\text{OE13}}$	42	O	$\overline{\text{OE13}}$ outputs the read enable signal to memory planes 1 and 3.
$\overline{\text{WE0}}$-$\overline{\text{WE3}}$	50-47	O	$\overline{\text{WE0}}$-$\overline{\text{WE3}}$ output write enable signals to memory planes 0-3, respectively.
M01A0 - M01A7	119, 117-115, 113, 112, 110, 109	O	M01A0-M01A7 provide row and column addresses to memory planes 0 and 1 in a time-sharing manner.
M23A0 - M23A4	107-103	O	M23A0-M23A4 provide the 5 low-order bits of row and column addresses to memory planes 2 and 3 in a time-sharing manner.
M2A5 - M2A7	102-100	O	M2A5-M2A7 provide the 3 high-order bits of row and column addresses to memory plane 2 in a time-sharing manner.
M3A5 - M3A7	99-97	O	M3A5-M3A7 provide the 3 high-order bits of row and column addresses to memory plane 3 in a time-sharing manner.
M01D0 - M01D7	94, 92-90 88-85	I/O	M01D0-M01D7 transfer display data between memory planes 0 and 1 in a time-sharing manner.
M23D0 - M23D7	83, 82, 80-75	I/O	M23D0-M23D7 transfer display data between memory planes 2 and 3 in a time-sharing manner.

Video Interface

Signal	Pin No.	Input/Output	Function
P7-P0	66-73	O	P7-P0 output video signals. These are TTL-level outputs.
$\overline{\text{DACIOR}}$	62	O	$\overline{\text{DACIOR}}$ controls reading of the external color palette DAC.
$\overline{\text{DACIOW}}$	61	O	$\overline{\text{DACIOW}}$ controls writing to the external color palette DAC.
PCLK	65	O	PCLK provides the dot clock to the external color palette DAC.
$\overline{\text{BLANK}}$	60	O	$\overline{\text{BLANK}}$ provides the blanking signal to the external color palette DAC.
HSYNC	59	O	HSYNC provides the horizontal synchronization timing signal required by the CRT display. The polality of HSYNC is programmable in the VGA mode, and always active-high in the other modes.
VSYNC	58	O	VSYNC provides the vertical synchronization timing signal required by the CRT display. The polality of VSYNC is programmable in the VGA mode, and active-high in the CGA mode, and active-low in the other modes.

Internal Block Diagram

Figure 1 is the CRTC+ internal block diagram.

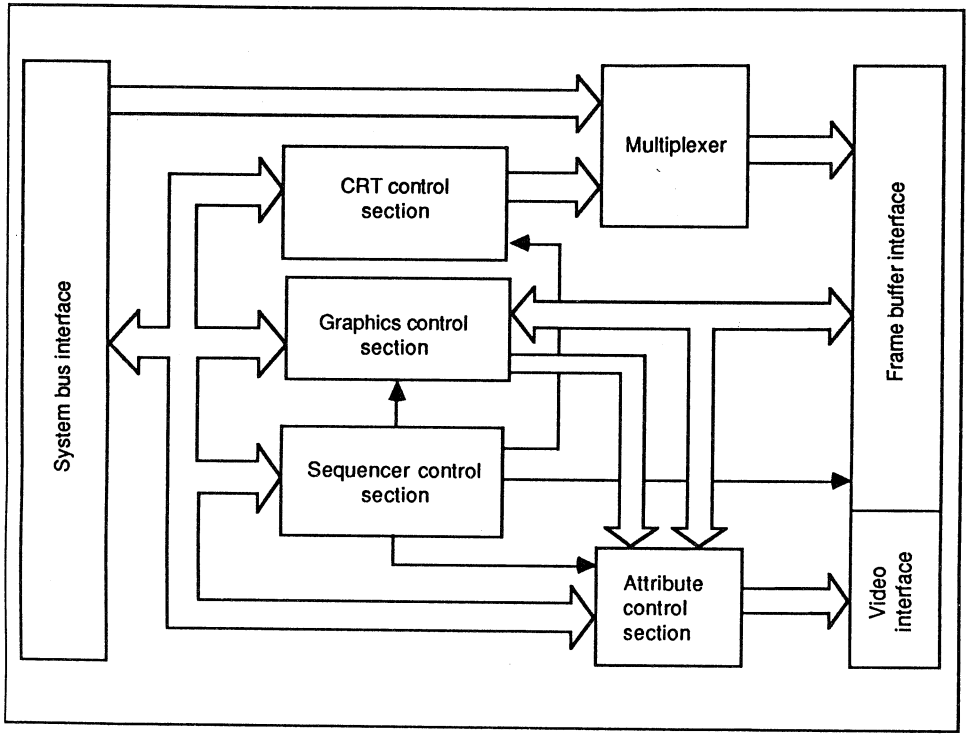


Figure 1 Internal Structure of the CRTC+

CRT Control Section: generates CRT control timing signals, frame buffer addresses, raster addresses, and refresh addresses. It also controls cursor and underline output.

Graphics Control Section: performs logic operations on graphics data, bit rotation and bit masking, memory plane masking, and other functions to support the CPU in creating graphics in the frame buffer. (CRTC+ does not support these functions in MDA, CGA, and HGA modes)

Sequencer Control Section: controls the timing of access to the frame buffer.

Attribute Control Section: controls the color palette, horizontal panning scroll, and other video functions.

Multiplexer: multiplexes the CPU address (the frame buffer address received from the CPU) and the frame buffer address generated by the CRT control section in the CRTC+.

System bus Interface: controls the interface with the system bus. The interface is easy to set up because it is compatible with both the I/O channel bus of the IBM-PC and the micro channel bus of the IBM-PS/2.

Frame Buffer Interface: direct interface to eight 64k × 4-type dynamic RAM (HM50464 or equivalent) chips.

Video Interface: outputs a TTL-level video signal and an external color palette control signal.

System Configuration

Figure 2 shows the configuration of a VGA system using the CRTC+. The CPU interface is compatible with both the I/O channel bus of the IBM-PC and the micro channel bus of the IBM-PS/2 and has an eight-bit data width, so there should be no interfacing problems. The bus type selection is made with the M/AT pin.

The frame buffer interface can directly control eight 64k × 4-type dynamic RAM (HM50464) chips, so a 256-kbyte frame buffer can be interfaced without going through an external circuit. The frame buffer consists of four memory planes (numbered 0 to 3), so the CPU can write 32 bits to the frame buffer at a time.

Use of the CRTC+ enables the parts count on a VGA graphics board to be greatly reduced.

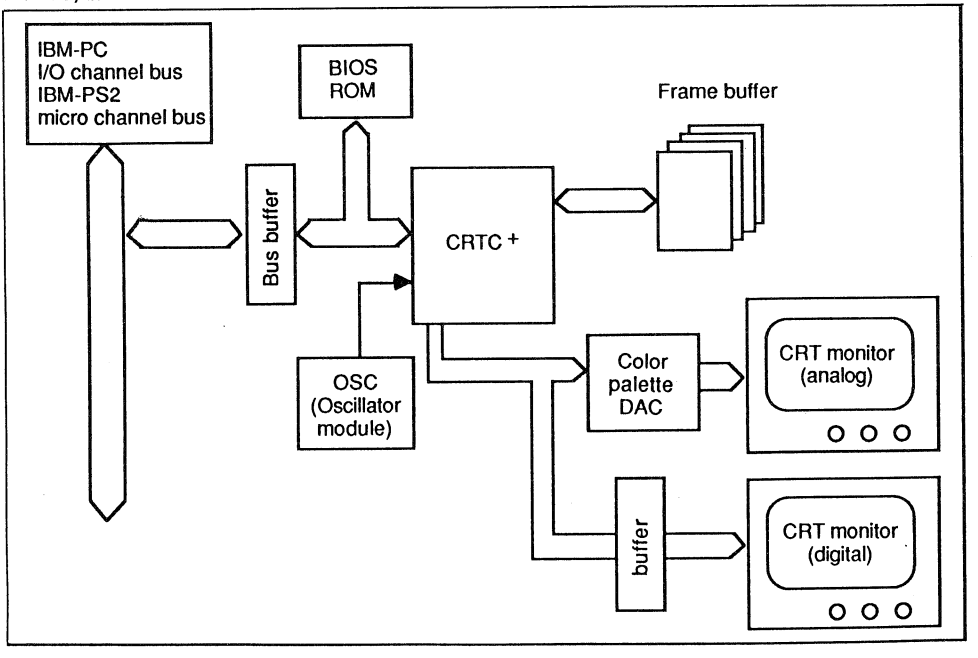


Figure 2 System Configuration

VGA-Mode Register Configuration

(1) General Control Registers

The general control registers of the VGA mode can be accessed directly by I/O port addresses.

Table 1 General Control Registers

Port *1 Address	Index Address	Register No.	Register Name	R/W	Data Bits *2							
					7	6	5	4	3	2	1	0
3C2 (3CC)	——	OR0	Output operation register	R/W								
3XA (3CA)	——	OR1	Feature control register	R/W								
3C2	——	OR2	Input status register 0	R								
3XA	——	OR3	Input status register 1	R								
3C3	——	OR4	Chip enable register	R/W								

*1 X is B in monochrome mode and D in color mode. The addresses in parentheses are read addresses.

*2 The shaded data bits are always read as 0, regardless of what value is written in them, except that bit 2 of OR3 is read as 1.

*3 The Chip enable register (OR4) is available only in the micro channel bus mode.

(2) CRT Control Registers

Table 2 CRT Control Registers

Port*1 Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3X4	—	CRA	CRT address	R/W								
3X5	00	CR0	Horizontal total characters	R/W								
3X5	01	CR1	Horizontal displayed characters	R/W								
3X5	02	CR2	Horizontal blanking start position	R/W								
3X5	03	CR3	Horizontal blanking stop position	R/W								
3X5	04	CR4	Horizontal sync pulse start position	R/W								
3X5	05	CR5	Horizontal sync pulse stop position	R/W								
3X5	06	CR6	Vertical total rasters	R/W								
3X5	07	CR7	MSB	R/W								
3X5	08	CR8	First raster address	R/W								
3X5	09	CR9	Maximum raster address	R/W								
3X5	0A	CR10	Cursor start raster	R/W								
3X5	0B	CR11	Cursor end raster	R/W								
3X5	0C	CR12	Start address (H)	R/W								
3X5	0D	CR13	Start address (L)	R/W								
3X5	0E	CR14	Cursor (H)	R/W								
3X5	0F	CR15	Cursor (L)	R/W								

Table 2 CRT Control Registers (cont)

Port*1 Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3X5	10	CR16	Vertical sync pulse start position	R/W								
3X5	11	CR17	Vertical sync pulse stop position	R/W								
3X5	12	CR18	Vertical displayed rasters	R/W								
3X5	13	CR19	Memory width	R/W								
3X5	14	CR20	Underline	R/W								
3X5	15	CR21	Vertical blanking start position	R/W								
3X5	16	CR22	Vertical blanking stop position	R/W								
3X5	17	CR23	CRTC mode control	R/W								
3X5	18	CR24	Screen split postion	R/W								

*1 X is B in monochrome mode and D in color mode.

(3) Graphics Control Registers

Table 3 Graphics Control Registers

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3CE	—	GRA	Graphics address	R/W								
3CF	00	GR0	Set/reset	R/W								
3CF	01	GR1	Enable set/reset	R/W								
3CF	02	GR2	Color compare	R/W								
3CF	03	GR3	Data rotate	R/W								
3CF	04	GR4	Read plane select	R/W								
3CF	05	GR5	Graphic mode control	R'W								
3CF	06	GR6	Graphics	R/W								
3CF	07	GR7	Color compare enable	R/W								
3CF	08	GR8	Bit mask	R/W								
3CF	09	GR9*1	Processor latch 0	R								
3CF	0A	GR10*1	Processor latch 1	R								
3CF	0B	GR11*1	Processor latch 2	R								
3CF	0C	GR12*1	Processor latch 3	R								

*1 The processor latch 0-3 are the extended registers of CRTC+.

(4) Sequencer Control Registers

Table 4 Sequencer Control Registers

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3C4	——	SRA	Sequencer address	R/W								
3C5	00	SR0	Reset	R/W								
3C5	01	SR1	Clock mode	R/W								
3C5	02	SR2	Memory plane mask	R/W								
3C5	03	SR3	Character font select	R/W								
3C5	04	SR4	Memory mode	R/W								

(5) Attribute Control Registers

Table 5 Attribute Control Registers

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3C0	——	ARA	Attribute address	R/W								
3C0(3C1)	00-0F	AR0-AR15	Palette	R/W								
3C0(3C1)	10	AR16	Attribute mode control	RW								
3C0(3C1)	11	AR17	Border color	R/W								
3C0(3C1)	12	AR18	Color plane enable	R/W								
3C0(3C1)	13	AR19	Horizontal panning scroll	R/W								
3C0(3C1)	14	AR20	Color select	R/W								

Note: The addresses in parentheses are read addresses.

(6) Extended Registers

The extended registers listed in table 6 support the extended functions of the CRTC+. These registers are internal registers of the CRT control section, and are each accessed by an index address placed in the CRT address register (CRA).

Table 6 Extended Registers

Port* Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3X5	FD	EM0	Extended register 1	R/W								
3X5	FE	EM1	Extended register 2	R/W								
3X5	FC	POT	Port register	R/W								

*: X is B in monochrome mode and D in color mode.

(7) External Palette DAC Control

External palette DAC control is provided at the port addresses listed in table 7. External Palette DAC Control Registers, for details of the register functions.

Table 7 External Palette DAC Control Registers

Port Address*1	Register No.	Register Name	R/W
3C8	DCWA	DAC write address*1	R/W
3C7	DCRA	DAC read address*1	W
3C7	DC0	DAC status*2	R
3C9	DC1	DAC data*1	R/W
3C6	DC2	DAC pel mask*1	R/W

*1 DAC write address registers, the DAC read address register, DAC data registers, and DAC pel mask register are located in the external palette DAC. The CRTC+ outputs the $\overline{\text{DACIOR}}$, $\overline{\text{DACIOW}}$ control signals by decoding the port address given above.

*2 The DAC status register is located in the CRTC+.

6845-Mode Register Configuration

(1) 6845-Mode Registers

Table 8 lists the 6845-mode registers, which are used in all three modes: MDA, HGA, and CGA. Although they are not listed in the table, the extended registers are also accessed by specifying an index address in the CRT address register, as in the VGA mode.

Table 8 6845-Mode Registers (Used in CGA, MDA, and HGA Modes)

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3X4	—	CRA	CRT address register	R/W								
3X5	00	CR0	Horizontal total characters register	R/W								
3X5	01	CR1	Horizontal displayed characters register	R/W								
3X5	02	CR62	Horizontal sync position register	R/W								
3X5	03	CR63	Sync pulse width register	R/W								
3X5	04	CR64	Vertical total characters register	R/W								
3X5	05	CR65	Total raster adjust register	R/W								
3X5	06	CR66	Vertical displayed characters register	R/W								
3X5	07	CR67	Vertical sync position register	R/W								
3X5	08	CR68	Skew register *2	R/W								
3X5	09	CR9	Maximum raster address register	R/W								
3X5	0A	CR10	Cursor start raster address *3	R/W								
3X5	0B	CR11	Cursor end raster address	R/W								
3X5	0C	CR12	Start address register (H) *4	R/W								
3X5	0D	CR13	Start address register (L)	R/W								
3X5	0E	CR14	Cursor register (H) *4	R/W								
3X5	0F	CR15	Cursor register (L)	R/W								

*1 X is [B] in the MDA and HGA modes and [D] in the CGA mode.
*2 The CRTC+ supports only the noninterlaced mode.
*3 The CRTC+ does not support cursor blinking.
*4 In the CRTC+, the start address register and cursor address register are 16-bit registers.

(2) MDA- and HGA-Compatible Registers

The MDA- and HGA-compatible registers are provided to make the 6845 modes of the CRTC+ compatible with MDA and HGA.

Table 9 MDA- and HGA-Compatible Registers

Port Address	Index Address	Register No.	Register Name		R/W	Data Bits							
						7	6	5	4	3	2	1	0
3B8	—	MH0	Mode control register	MDA	R/W								
				HGA									
3BA	—	MH1	CRT status register	MDA	R								
				HGA									
3BF*	—	MH2	Hercules configuration register		R/W								

* The Hercules configuration register [3BF] is used only in the HGA mode.

(3) CGA-Compatible Registers

The CGA-compatible registers are provided to make the 6845 modes of the CRTC+ compatible with CGA.

Table 10 CGA-Compatible Registers

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3D8	—	CG0	Mode control register	R/W								
3D9	—	CG1	Color select register	R/W								
3DA	—	CG2	CRT status register	R								

(4) Extended Registers

Extended registers 1 and 2 (EM0 and EM1) and the port register (POT) are used in the 6845 modes as well as the VGA mode. These registers have the same functions in the 6845 modes as in the VGA mode.

Absolute Maximum Ratings

Table 11 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC} *1	-0.3 to +6.7	V
Input voltage	V_{in} *1	-0.3 to (V_{CC} + 0.3)	V
Allowable output current	$\lvert I_0 \rvert$ *2	5	mA
Total allowable output current	$\lvert \Sigma I_0 \rvert$ *3	200	mA
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

*1 This value is referenced to V_{SS} = 0 V.
*2 Allowable output current is the maximum current that may be drawn from or sunk into one output pin or one input/output pin.
*3 Total allowable output current is the total sum of the currents that may be drawn from or sunk into all the output and input/output pins.

Notes 1. Using this chip beyond its maximum ratings may degrade its reliability or permanently destroy it. Use this chip under the conditions recommended in Recommended Operating Conditions.
2. Unused input pins should be pulled up.

Recommended Operating Conditions

Table 12 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}*	4.75	5.0	5.25	V
Low input level	V_{IL}*	0	–	0.7	V
High input level	V_{IH}*	2.2	–	V_{CC}	V
Reset low input level	V_{ILR}*	0	–	0.5	V
Reset high input level	V_{IHR}*	2.5	–	V_{CC}	V
Operating temperature	T_{opr}	0	25	70	C°

* This value is referenced to V_{SS} = 0 V.

■ Timing measurements

- The timing measurement point for low output levels in these specifications is defined to be 0.8 V.
- The low output level for stable conditions (DC characteristics) is defined to be 0.5 V.
- The high output level is defined to be V_{CC} - 2.0 V.

DC Characteristics

Table 13 DC Characteristics

(V_{CC} = 5.0 V ±5%, V_{SS} = 0 V, Ta = 0 to 70°C, unless otherwise noted)

Item	Symbol	Min	Max	Unit	Test Conditions
Input high level (except RESET)	V_{IH}	2.2	V_{CC}	V	
Input low level (except RESET)	V_{IL}	-0.3	0.7	V	
Reset input high level	V_{IHR}	2.5	V_{CC}	V	
Reset input low level	V_{ILR}	-0.3	0.5	V	
Input leakage current	I_{IN}	-2.5	+2.5	µA	V_{in} = 0 - V_{CC}
Three-state input current	I_{TSI}	-10	+10	µA	V_{in} = 0.4 - V_{CC}
Output high level	V_{OH}	3.5*4	–	V	I_{OH} = -350 µA
		–	–	–	–
Output low level	V_{OL}	–	0.5*3	V	I_{OL} = 2.2 mA*1
		–	0.5*3	V	I_{OL} = 1.6 mA*2
Input capacity	C_{in}	–	15	pF	V_{in} = 0 V, T_a =25°C, f = 1 MHz
Current consumption	I_{CC}	–	280	mA	f = 32 MHz

*1 CDCHRDY, IRQ, and $\overline{\text{SFDBKN}}$ pins
*2 Other pins
*3 The AC timing measurement point for output low levels is defined to be 0.8 V.
*4 The AC timing measurement point for output high level is defined to be V_{CC} - 2.0 V.

AC Characteristics

(1) Clock Timing

Table 14 Clock Timing

(Vcc = 5.0 V ±5%, Vss = 0 V, Ta = 0 to 70°C, unless otherwise noted)

			F28		F37			
No.	**Item**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Reference**
1	Operating frequency	f_C	5	32	5	37	MHz	Figure 3
2	Clock cycle	T_C	31	200	27	200	ns	
3	Clock high pulse width	t_{CH}	13	–	11	–	ns	
4	Clock low pulse width	t_{CL}	13	–	11	–	ns	
5	Clock rise time	t_{CR}	–	6	–	5	ns	
6	Clock fall time	t_{CF}	–	6	–	5	ns	

(2) CPU Read/Write Cycle Timing

Table 15 (1) to (3) gives the CPU read/write cycle timing for I/O channel bus mode.

Table 15 (1) CPU Read/Write Cycle Timing (I/O Channel Bus Mode)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
11	$\overline{IOR}$ low pulse width	t_{IRLW}	$3M_c$	–	$3M_c$	–	Cycles*1	Figure 4 (a),
12	$\overline{IOR}$ high pulse width	t_{IRHW}	$2M_c$	–	$2M_c$	–	Cycles*1	Figure 4 (b)
13	$\overline{IOW}$ low pulse width	t_{IWLW}	$3M_c$	–	$3M_c$	–	Cycles*1	
14	$\overline{IOW}$ high pulse width	t_{IWHW}	$2M_c$	–	$2M_c$	–	Cycles*1	
15	$\overline{IOR}$ input inhibit time	t_{IRIH}	$2M_c$	–	$2M_c$	–	Cycles*1	
16	$\overline{IOW}$ input inhibit time	t_{IWIH}	$2M_c$	–	$2M_c$	–	Cycles*1	
17	Address setup time (from $\overline{IOR}$)	t_{ASIR}	0	–	0	–	ns	
18	Address hold time (from $\overline{IOR}$)	t_{AHIR}	10	–	10	–	ns	
19	Address setup time (from $\overline{IOW}$)	t_{ASIW}	0	–	0	–	ns	
20	Address hold time (from $\overline{IOW}$)	t_{AHIW}	10	–	10	–	ns	
21	I/O read data access time	t_{IRAC}	–	70	–	70	ns	
22	I/O read data hold time	t_{IRDH}	5	–	5	–	ns	
23	I/O read data turnoff time 1	t_{IRTF1}	–	35	–	35	ns	
24	I/O write data setup time 1	t_{IWDS1}	0	–	0	–	ns	
25	I/O write data hold time 1	t_{IWDH1}	0	–	0	–	ns	

*1 M_c: Clock cycle on the 28M pin

Table 15 (1) CPU Read/Write Cycle Timing (I/O Channel Bus Mode) (cont)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
31	I/O read data setup time	t_{IRDS}	$1M_C$	–	$1M_C$	–	Cycles*1	Figure 4 (b)
36	CDCHRDY low delay (from IOR)	t_{RDIR}	0	70	0	70	ns	
37	CDCHRDY low delay (from IOW)	t_{RDIW}	0	70	0	70	ns	

*1 M_C: Clock cycle on the 28M pin

Table 15 (2) CPU Read/Write Cycle Timing (I/O Channel Bus Mode)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
41	$\overline{\text{MEMR}}$ low pulse width							Figure 5
	Text, graphics	t_{MRLW}	$10T_c$	–	$10T_c$	–	Cycles*2	
	132-column mode	t_{MRLW}	$12T_c$	–	$12T_c$	–	Cycles*2	
42	$\overline{\text{MEMR}}$ high pulse width	t_{MRHW}	$2M_c$	–	$2M_c$	–	Cycles*1	
43	$\overline{\text{MEMW}}$ low pulse width							
	Text, graphics	t_{MWLW}	$10T_c$	–	$10T_c$	–	Cycles	
	132-column mode	t_{MWLW}	$12T_c$	–	$12T_c$	–	Cycles	
44	$\overline{\text{MEMW}}$ high pulse width	t_{MWHW}	$2M_c$	–	$2M_c$	–	Cycles*1	
45	$\overline{\text{MEMR}}$ input inhibit time	t_{MRIH}	$2M_c$	–	$2M_c$	–	ns*1	
46	$\overline{\text{MEMW}}$ input inhibit time	t_{MWIH}	$2M_c$	–	$2M_c$	–	ns*1	
47	$\overline{\text{MEMR}}$ hold time (from CDCHRDY)	t_{MRH}	0	–	0	–	ns	
48	$\overline{\text{MEMW}}$ hold time (from CDCHRDY)	t_{MWH}	0	–	0	–	ns	
49	Address hold time (from CDCHRDY)	t_{AHRD}	0	–	0	–	ns	
50	Address hold time (from MEMR)	t_{AHMR}	10	–	10	–	ns	
51	Address hold time (from $\overline{\text{MEMW}}$)	t_{AHMW}	10	–	10	–	ns	
52	Address setup time (from MEMR)	t_{ASMR}	0	–	0	–	ns	
53	Address setup time (from MEMW)	t_{ASMW}	0	–	0	–	ns	

*1 M_c: Clock cycle on the 28M pin
*2 T_c: Clock cycle used as pixel clock

Table 15 (2) CPU Read/Write Cycle Timing (I/O Channel Bus Mode) (cont)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
54	Memory read data setup time	t_{MRDS}	$1T_c$	–	$1T_c$	–	Cycles	Figure 5
55	Memory read data hold time	t_{MRDH}	5	–	5	–	ns	
56	Memory read data turnoff time	t_{MRDT}	–	35	–	35	ns	
57	Memory write data setup time	t_{MWDS}	0	–	0	–	ns	
58	Memory write data hold time	t_{MWDH}	0	–	0	–	ns	
59	CDCHRDY low delay (from $\overline{MEMR}$)	t_{RDMR}	0	70	0	70	ns	
60	CDCHRDY low delay (from $\overline{MEMW}$)	t_{RDMW}	0	70	0	70	ns	
61	CDCHRDY low pulse width							
	Memory access	t_{RDLW}	$10T_c$	–	$10T_c$	–	Cycles*2	
	I/O or BIOS access	t_{RDLW}	$2M_c$	–	$2M_c$	–	Cycles*1	
62	CDCHRDY high hold time	t_{RDHH}	0	–	0	–	ns	

*1 M_c: Clock cycle on the 28M pin
*2 T_c: Clock cycle used as pixel clock

Table 15 (3) CPU Read/Write Cycle Timing (I/O Channel Bus Mode)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
71	AEN setup time (from $\overline{IOR}$)	t_{AESR}	20	–	20	–	ns	Figure 6
72	AEN setup time (from $\overline{IOW}$)	t_{AESW}	20	–	20	–	ns	
73	AEN hold time (from $\overline{IOR}$)	t_{AEHR}	5	–	5	–	ns	
74	AEN hold time (from $\overline{IOW}$)	t_{AEHW}	5	–	5	–	ns	
75	$\overline{DACK0}$ setup time (from $\overline{MEMR}$)	t_{DKSR}	20	–	20	–	ns	
76	$\overline{DACK0}$ setup time (from $\overline{MEMW}$)	t_{DKSW}	20	–	20	–	ns	
77	$\overline{DACK0}$ hold time (from $\overline{MEMR}$)	t_{DKHR}	5	–	5	–	ns	
78	$\overline{DACK0}$ hold time (from $\overline{MEMW}$)	t_{DKHW}	5	–	5	–	ns	
79	$\overline{BIOS}$ delay (from $\overline{MEMR}$)	t_{BSMR}	0	50	0	50	ns	
80	DIR delay (from $\overline{IOR}$ and $\overline{MEMR}$)	t_{DRIM}	0	55	0	55	ns	

Table 16 gives the CPU read/write cycle timing for micro channel bus mode.

Table 16 CPU Read/Write Cycle Timing (Micro Channel Bus Mode)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
91	Address setup time (from S0 or S1)	t_{ASST}	5	–	5	–	ns	Figure 7
92	Status setup time (from CMD)	t_{SSCM}	50	–	50	–	ns	
99	Address hold time (from CMD)	t_{AHCM}	25	–	25	–	ns	
100	Status hold time (from CMD)	t_{STHC}	25	–	25	–	ns	
101	$\overline{\text{SFDBKN}}$ delay	t_{SFDD}	–	50	–	50	ns	
102	Address setup time (from CMD)	t_{ASCM}	80	–	80	–	ns	
103	$\overline{\text{CMD}}$ low pulse width	t_{CMLW}	90	–	90	–	ns	

Table 16 CPU Read/Write Cycle Timing (Micro Channel Bus Mode) (cont)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
104	Write data setup time	t_{WDSC}	0	–	0	–	ns	Figure 7
105	Write data hold time	t_{WDHC}	25	–	25	–	ns	
106	Read data access time (from S0 or S1)	t_{ACST}	–	100	–	100	ns	
107	Read data access time (from CMD)	t_{ACCM}	–	45	–	45	ns	
108	Read data access time (from CDCHRDY)	t_{ACRD}	–	45	–	45	ns	
109	Read data hold time (from CMD)	t_{RDHC}	0	–	0	–	ns	
110	$\overline{\text{CMD}}$ input inhibit time 1	t_{CIH1}	180	–	180	–	ns	
111	$\overline{\text{CMD}}$ input inhibit time 2	t_{CIH2}	$1.5M_C$	–	$1.5M_C$	–	Cycles*1	
113	Status input inhibit time	t_{STIH}	35	–	35	–	ns	
114	$\overline{\text{CMD}}$ negate time (to next S0 or S1)	t_{CMNG}	–	5	–	5	ns	
115	CDCHRDY low delay (from address)	t_{RDAD}	–	60	–	60	ns	
116	CDCHRDY low delay (from S0 or S1)	t_{RDSD}	0	30	0	30	ns	
117	Read data turnoff time	t_{RDTF}	–	35	–	35	ns	

*1 M_C: Clock cycle on the 28M pin

Table 16 CPU Read/Write Cycle Timing (Micro Channel Bus Mode) (cont)

			F28		F37		
No. Item	Symbol	Min	Max	Min	Max	Unit	Reference
123 DIR delay (from $\overline{CMD}$)	t_{DRCM}	0	35	0	35	ns	Figure 7
124 SLEEP setup time	t_{SLS}	5	–	5	–	ns	
125 SLEEP hold time	t_{SLH}	10	–	10	–	ns	

(3) IRQ and RESET Timing

Table 17 IRQ and RESET Timing

		F28		F37			
No. Item	Symbol	Min	Max	Min	Max	Unit	Reference
131 IRQ delay 1 (Hi-Z to low)	t_{IQD1}	–	80	–	70	ns	Figure 8
132 IRQ delay 2 (low to high)	t_{IQD2}	–	80	–	70	ns	
133 RESET pulse width	t_{RSTW}	$10T_C$	–	$10T_C$	–	Cycles	
134 RESET rise time	t_{RSTR}	–	100	–	100	ns	
135 RESET fall time	t_{RSTF}	–	100	–	100	ns	

(4) Frame Buffer Memory Interface Timing

Table 18 (1) Frame Buffer Memory Interface Timing

No.	Item		Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
141	$\overline{RAS}$ delay		t_{RD}	10	80	10	65	ns	Figure 9 (a),
142	$\overline{RAS}$ low pulse width *1	Text, graphics (CPU)	t_{RSLW}	$(4T_c-10)$	$(4T_c+10)$	$(4T_c-10)$	$(4T_c+10)$	ns	Figure 9 (b)
		Graphics (display) 25M, 28M		$(4T_c-10)$	$(125T_c+10)$	$(4T_c-10)$	$(125T_c+10)$		
		Graphics (display) EXT1, EXT2		$(4T_c-10)$	$(253T_c+10)$	$(4T_c-10)$	$(253T_c+10)$		
		132-column (CPU)		$(5T_c-10)$	$(5T_c+10)$	$(5T_c-10)$	$(5T_c+10)$		
		132-column (display) 25M, 28M		$(5T_c-10)$	$(125T_c+10)$	$(5T_c-10)$	$(125T_c+10)$		
		132-column (display) EXT1, EXT2		$(5T_c-10)$	$(253T_c+10)$	$(5T_c-10)$	$(253T_c+10)$		
143	$\overline{RAS}$ high pulse width	Text, graphics	t_{RSHW}	$(3T_c-10)$	$(3T_c+10)$	$(3T_c-10)$	$(3T_c+10)$	ns	
		132-column		$(4T_c-10)$	$(4T_c+10)$	$(4T_c-10)$	$(4T_c+10)$		
144	$\overline{CAS}$ delay		t_{CD}	$(2T_c-10)$	$(2T_c+10)$	$(2T_c-10)$	$(2T_c+10)$	ns	
145	$\overline{CAS}$ low pulse width	Text, graphics	t_{CSLW}	$(3T_c-10)$	$(3T_c+10)$	$(3T_c-10)$	$(3T_c+10)$	ns	
		132-column		$(4T_c-10)$	$(4T_c+10)$	$(4T_c-10)$	$(4T_c+10)$		
146	$\overline{CAS}$ high pulse width	Text, graphics	t_{CSHW}	$(4T_c-10)$	$(4T_c+10)$	$(4T_c-10)$	$(4T_c+10)$	ns	
		Graphics (display)		$(2T_c-10)$	$(2T_c+10)$	$(2T_c-10)$	$(2T_c+10)$		
		132-column (CPU)		$(5T_c-10)$	$(5T_c+10)$	$(5T_c-10)$	$(5T_c+10)$		
		132-column (display)		$(3T_c-10)$	$(3T_c+10)$	$(3T_c-10)$	$(3T_c+10)$		

*1: Page mode access is used for graphics display and 132-column text display. t_{RSLW} differs according to the master clock selection (specified in the output operation register).

Table 18 (2) Frame Buffer Memory Interface Timing

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
151	Row address setup time	t_{RAS}	0	–	0	–	ns	Figure 9 (a),
152	Row address hold time	t_{RAH}	$1/2T_C-5$	–	$1/2T_C-5$	–	ns	Figure 9 (b)
153	Column address setup time	t_{CAS}	0	–	0	–	ns	
154	Column address hold time	t_{CAH}	T_C-10	–	T_C-10	–	ns	
155	RAM read data setup time	t_{RRS}	10	–	10	–	ns	
156	RAM read data hold time	t_{RRH}	5	–	5	–	ns	
157	$\overline{OE}$ delay	t_{OED}	$(t_{RD}-10)(t_{RD}+10)$		$(t_{RD}-10)(t_{RD}+10)$*1		ns	
158	$\overline{OE}$ low pulse width — Text, graphics	t_{OEW}	$(2T_C-10)(2T_C+10)$		$(2T_C-10)(2T_C+10)$		ns	
	132-column		$(3T_C-10)(3T_C+10)$		$(3T_C-10)(3T_C+10)$			
159	RAM write data setup time	t_{RWS}	0	–	0	–	ns	
160	RAM write data hold time	t_{RWH}	$(1.5T_C-10)$	–	$(1.5T_C-5)$	–	ns	
161	$\overline{WE}$ delay	t_{WED}	$(t_{RD}-10)(t_{RD}+10)$		$(t_{RD}-10)(t_{RD}+10)$*1		ns	
162	$\overline{WE}$ low pulse width — Text, graphics	t_{WEW}	$(2T_C-10)(2T_C+10)$		$(2T_C-10)(2T_C+10)$		ns	
	132-column		$(3T_C-10)(3T_C+10)$		$(3T_C-10)(3T_C+10)$			

*1 t_{RD} : No. 141 $\overline{RAS}$ delay time.

(5) Video Interface Timing

Table 19 Video Interface Timing

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
171	$\overline{\text{DACIOR}}$ delay (from $\overline{\text{IOR}}$)	t_{DRIR}	–	55	–	55	ns	Figure 10 (a), Figure 10 (b)
172	$\overline{\text{DACIOR}}$ delay (from $\overline{\text{CMD}}$)	t_{DRCM}	–	45	–	45	ns	
173	$\overline{\text{DACIOW}}$ delay (from $\overline{\text{IOW}}$)	t_{DWIW}	–	55	–	55	ns	
174	$\overline{\text{DACIOW}}$ delay (from $\overline{\text{S0}}$ or $\overline{\text{S1}}$)	t_{DWST}	–	45	–	45	ns	
175	$\overline{\text{DACIOW}}$ low pulse width	t_{DWLI}	$1M_C$–10	–	$1M_C$–10	–	ns*1	
176	PCLK delay	t_{PCD}	–	45	–	45	ns	Figure 11
177	Video data setup time	t_{PDS}	6	–	6	–	ns	
178	Video data hold time	t_{PDH}	6	–	6	–	ns	
179	$\overline{\text{BLANK}}$ delay time	t_{BLD}	–	60	–	55	ns	
181	HSYNC delay	t_{HSD}	–	60	–	55	ns	
182	VSYNC delay	t_{VSD}	–	60	–	55	ns	

*1 M_C: Clock cycle on the 28M pin

Timing Charts

(1) Clock Timing

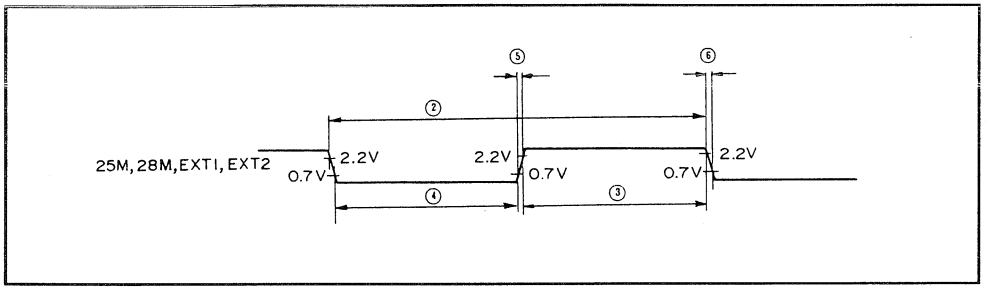


Figure 3 Clock Timing

(2) I/O Access Timing (I/O Channel Bus Mode)

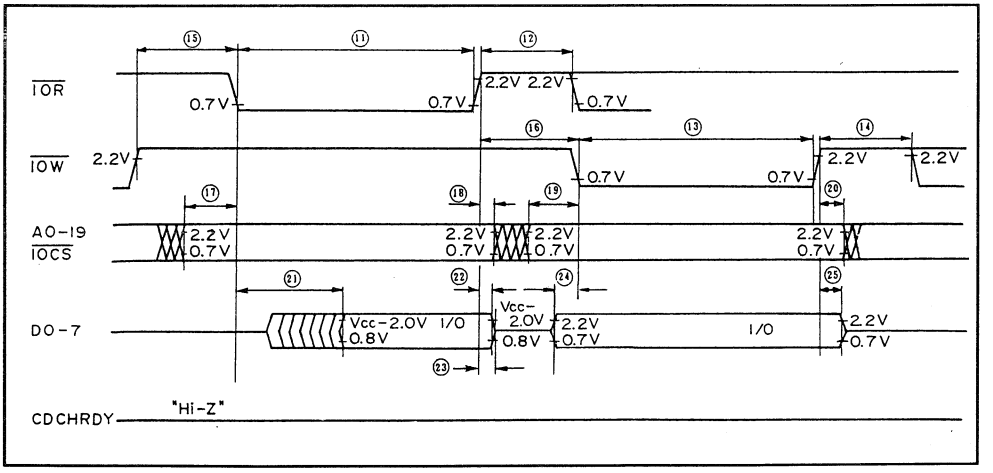


Figure 4 (a) I/O Access Timing (IORDYEN Pin Low)

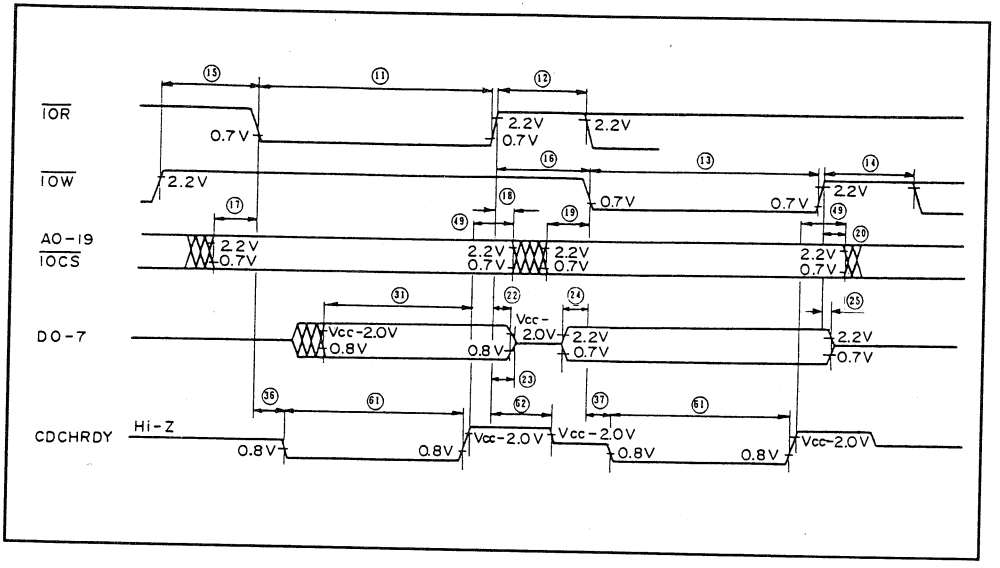


Figure 4 (b) I/O Access Timing (IORDYEN Pin High)

(3) Memory Access Timing (I/O Channel Bus Mode)

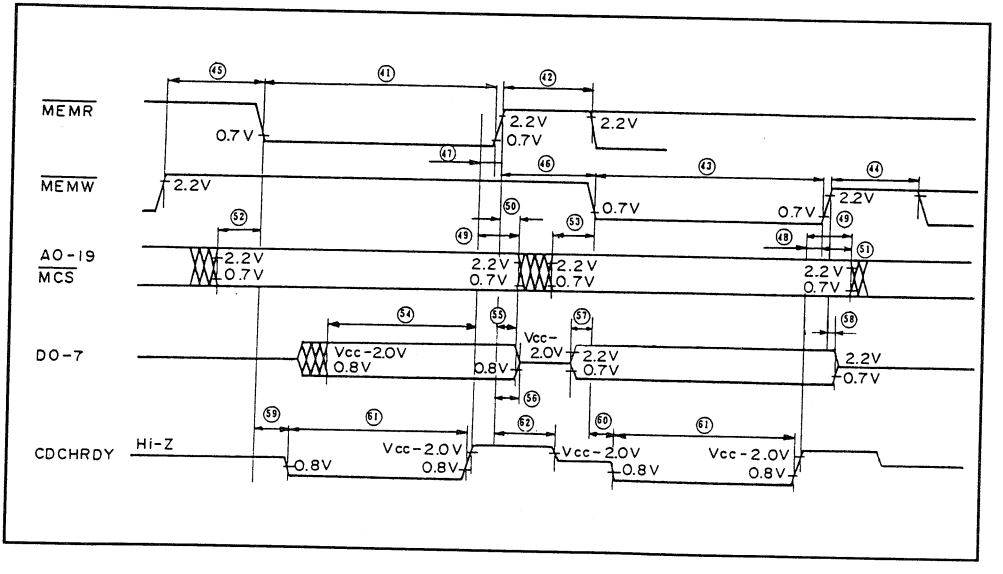


Figure 5 Memory Access Timing

(4) System Bus Interface Timing (I/O Channel Bus Mode)

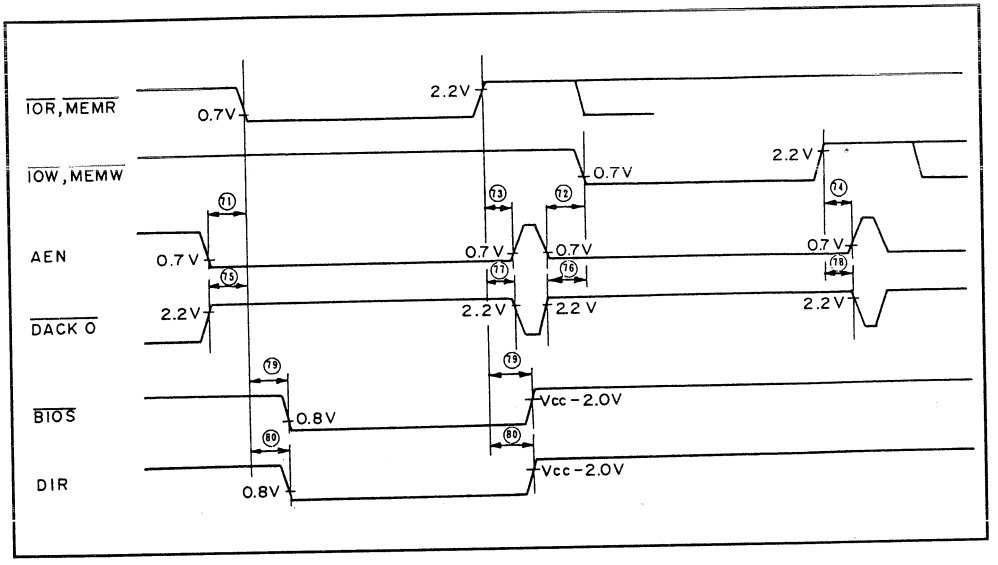


Figure 6 I/O Channel Bus Control Signal Timing

(5) Micro Channel Access Timing (Micro Channel Bus Mode)

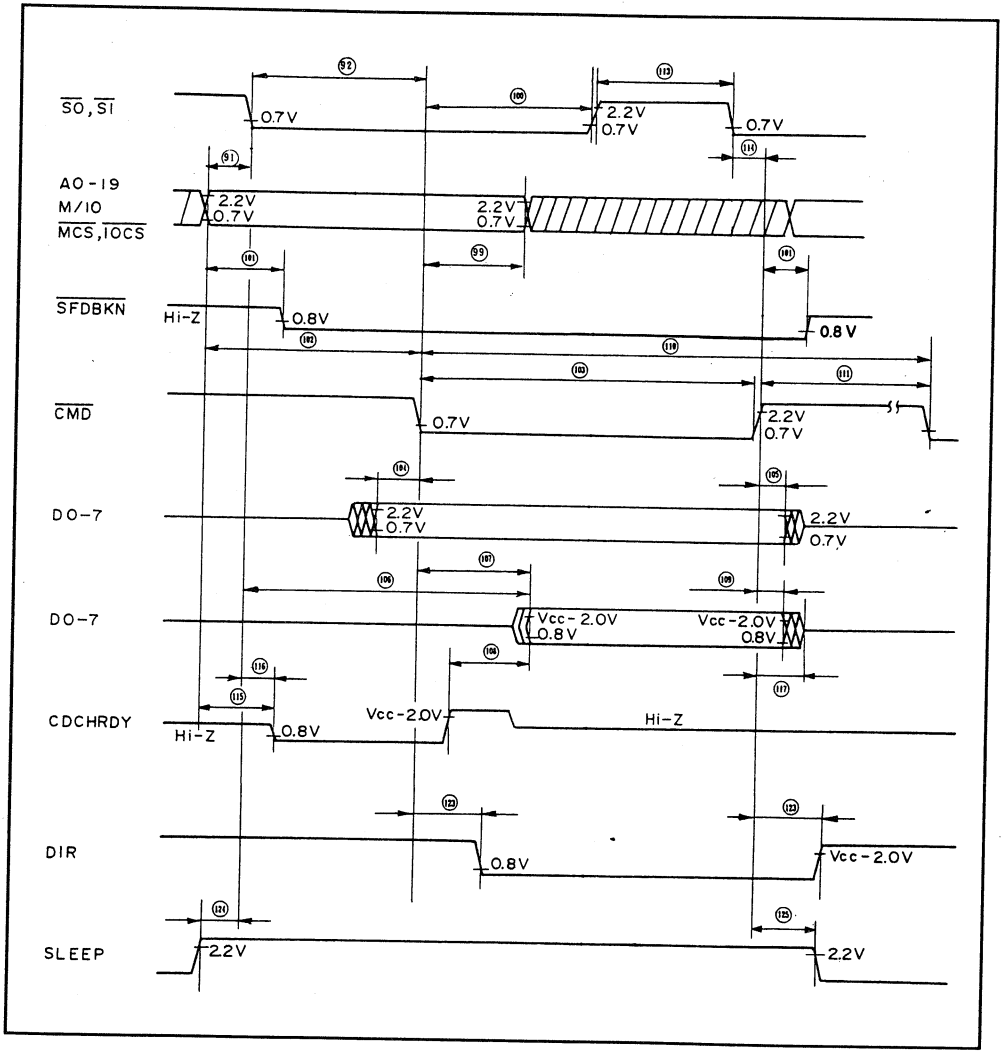


Figure 7 Micro Channel Bus Access Timing

(6) IRQ and RESET Timing

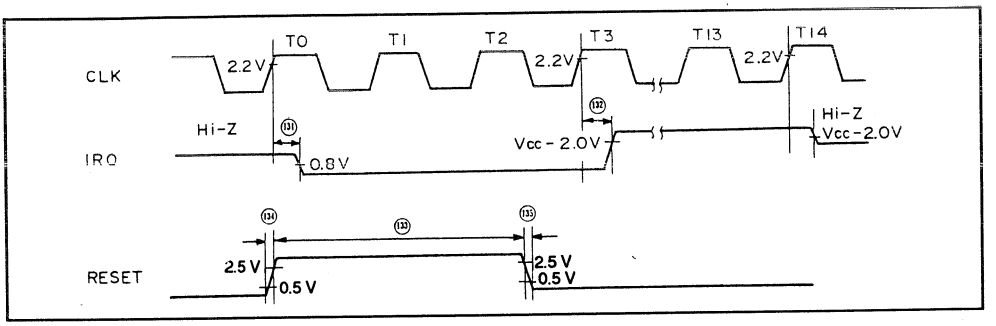


Figure 8 IRQ and RESET Timing

(7) Display Memory Read/Write Cycle Timing

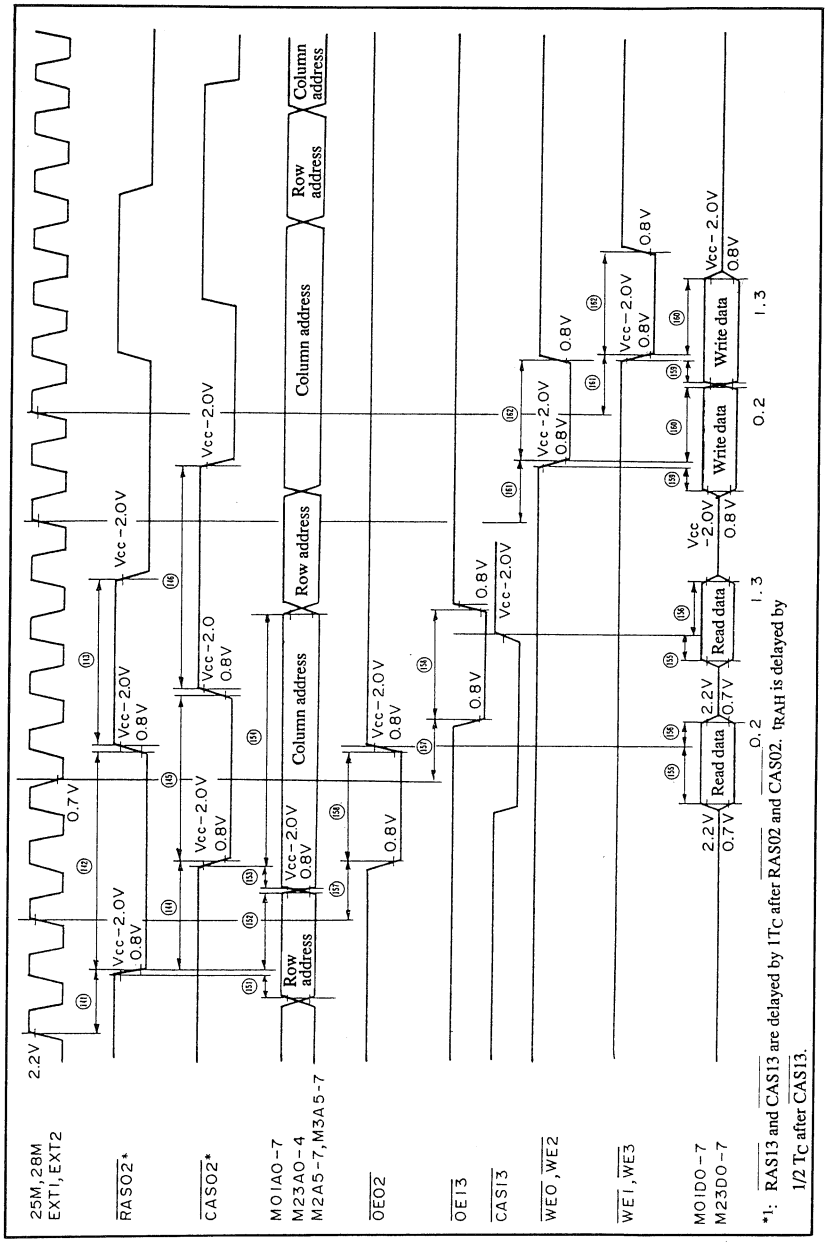


Figure 9 (a) Display Memory Normal Read/Write Timing
(Display or CPU access in non-132-column text mode
CPU access in graphics mode (smart access)
CPU access in 132-column text mode

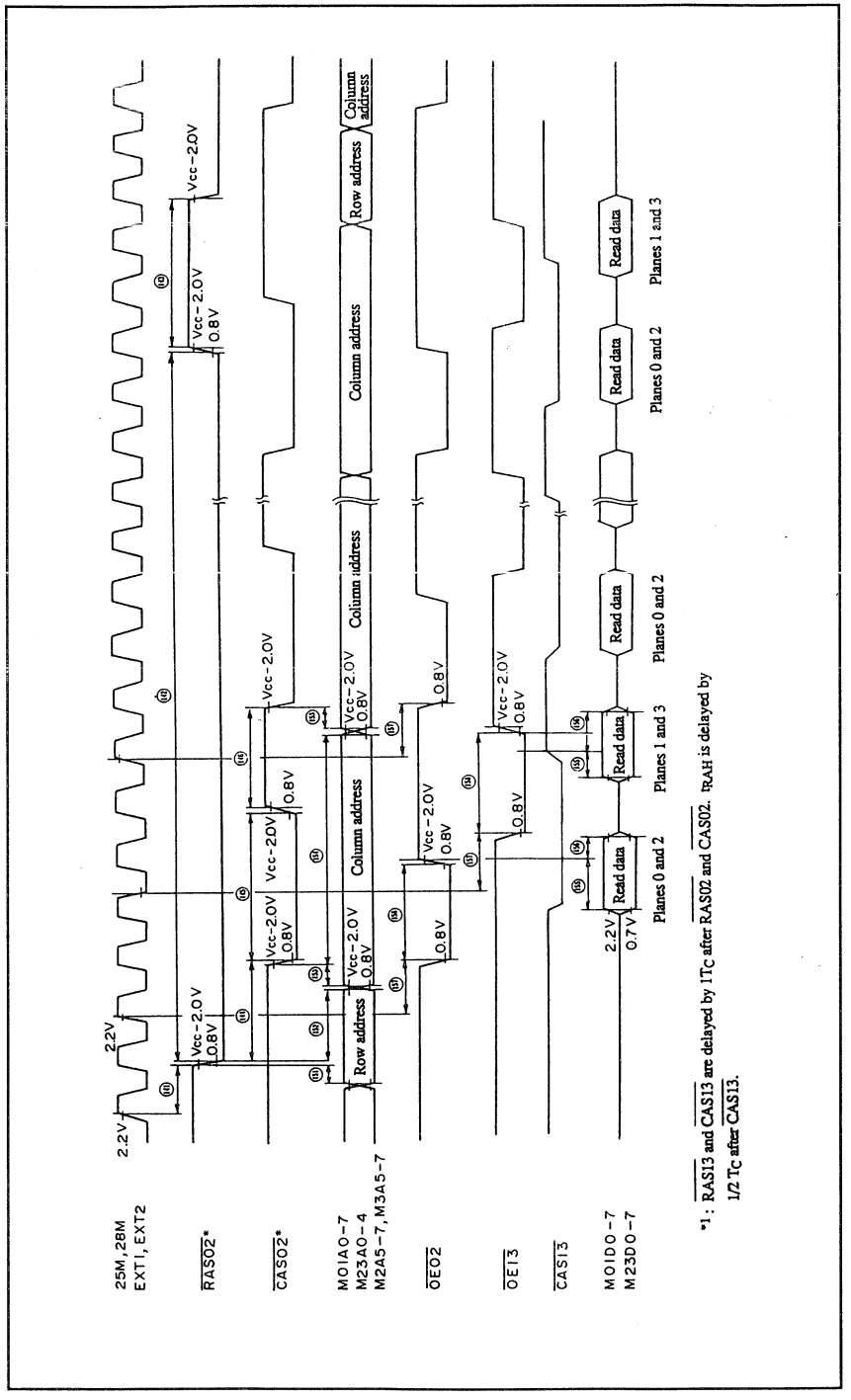


Figure 9 (b) Display Memory Page-Mode Read Timing
(Display access in graphics mode (smart access) and 132-column text mode)

(8) $\overline{\text{DACIOR}}$ and $\overline{\text{DACIOW}}$ Timing

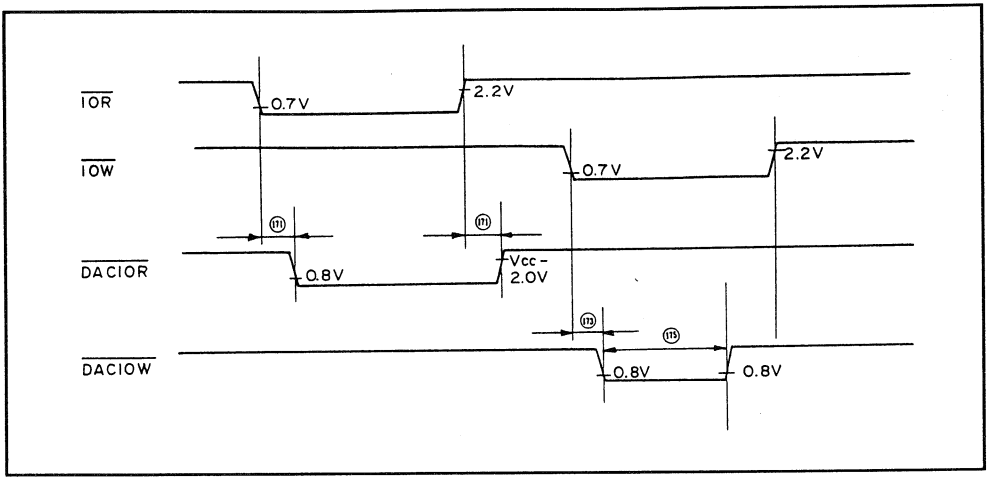


Figure 10 (a) $\overline{\text{DACIOR}}$ and $\overline{\text{DACIOW}}$ Timing (I/O Channel Bus Mode)

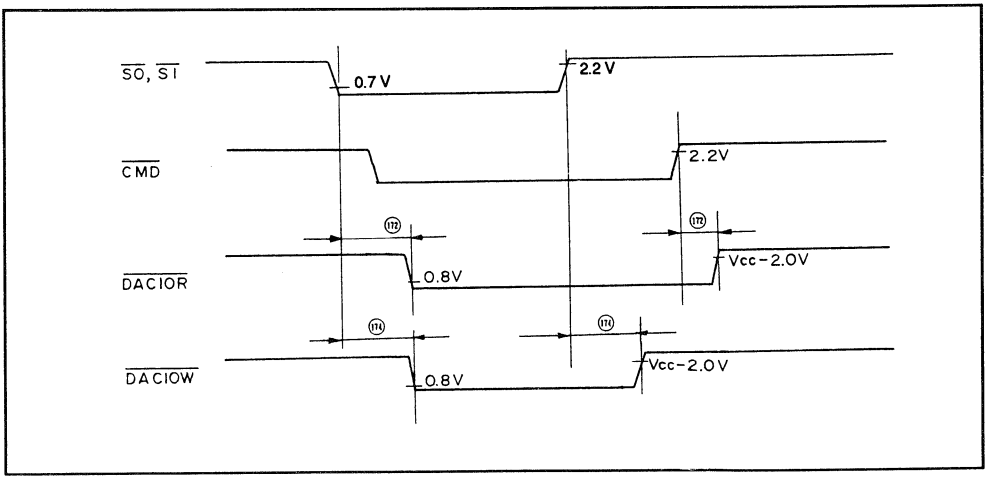


Figure 10 (b) $\overline{\text{DACIOR}}$ and $\overline{\text{DACIOW}}$ Timing (Micro Channel Bus Mode)

(9) Video Interface Timing

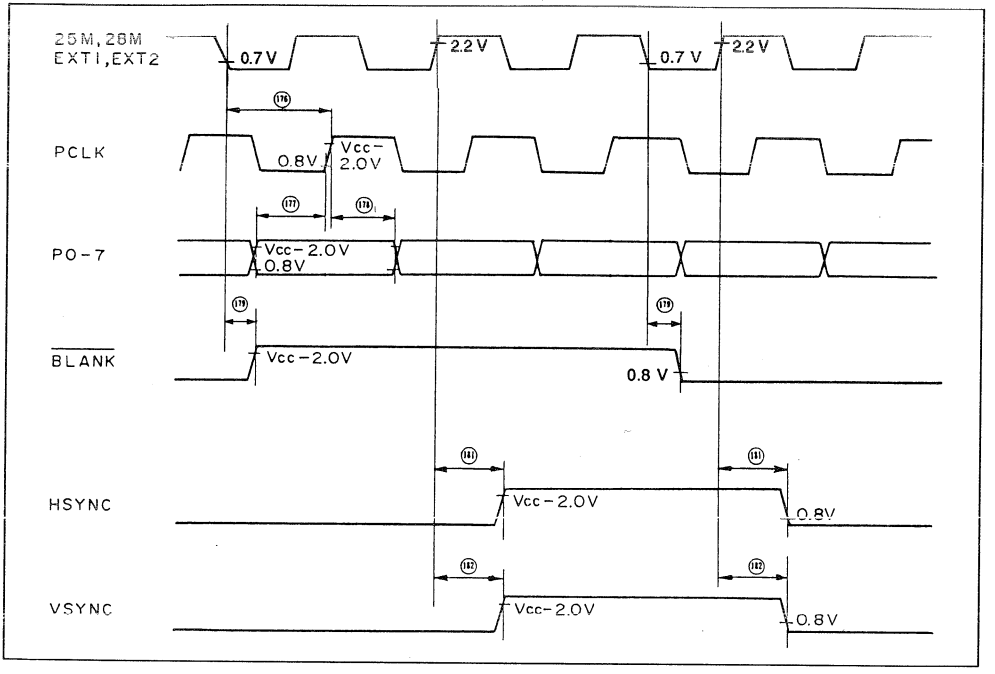


Figure 11 Video Interface Timing

Test Load Conditions

Load	Pin	Condition	Unit
R_L	$\overline{\text{SFDBKN}}$, CDCHRDY, IRQ	1.8	kΩ
	Other pins	2.4	kΩ
C	$\overline{\text{SFDBKN}}$, CDCHRDY, IRQ	100	pF
	Other pins	40	pF
R	$\overline{\text{SFDBKN}}$, CDCHRDY, IRQ	10	kΩ
	Other pins	10	kΩ

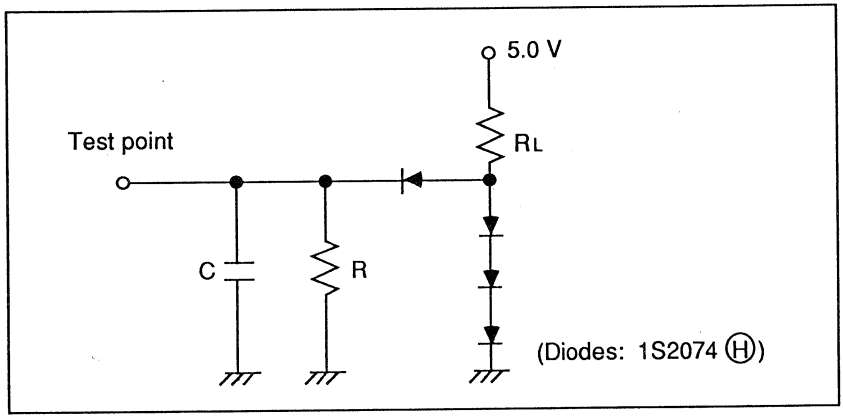


Figure 12 Test Load Conditions

Refer to user's manual (No. ADE-602-013A) for detail of this product.

HD64400 GDP

Graphic Data Processor

Description

The HD64400 is a graphic data processing chip with high-speed drawing functions and an extensive set of display functions.

It can control a wide range of raster-scan CRT displays, ranging from low to high resolution, and can display up to four overlapping hardware windows.

Drawing commands include commands for drawing high-speed graphics, for text drawing on bit-mapped displays, for high-speed bit block transfers (BitBlt), and for enlarging, shrinking, and rotating images by arbitrary amounts.

Features

Display Functions

- Hardware windowing: up to four overlapping windows, one of which can be superimposed
- Multiport DRAM interface functions, supporting realtime read transfer
- Smooth scrolling, with independent vertical and horizontal direction
- Graphic cursor and cross-hair cursor
- Two memory access modes: single access and dual access
- Three scan modes: noninterlace, interlace sync, interlace sync & video
- External synchronization: master/slave, or TV sync
- Laser printer interface

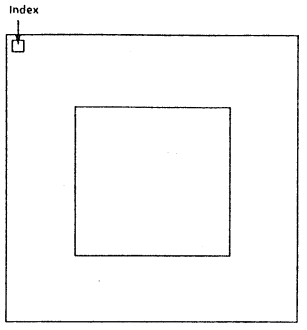
Drawing Functions

- High-speed drawing. Speeds of representative commands at 4 bits/pixel are listed below (frame buffer data bus width—32 bits; clock rate—20 MHz):
  - — Line: 200 ns/pixel (any direction)
  - — Fill: 25 ns/pixel (single color)
  - — Text: 37.5 ns/pixel
  - — Copy (BitBlt): 75 ns/pixel (copy)
- Drawing versatility
  - — Thick lines can be drawn using arbitrary pel shapes (up to 32 × 32 pixels).
  - — Line style information can be stored on-chip RAM (up to 1024 bits).
  - — Areas can be tiled with arbitrary (binary or color) patterns. Patterns can be stored in on-chip RAM (for fast access) or the frame buffer (for large patterns), or in both locations.
  - — Raster operations: 20 arithmetic and logic operations; 20 enable/disable conditions.
  - — Hardware converts between binary and color data.
  - — Drawing area control: area detect, clipping, picking.
- High-level command language
  - — The command language conforms to VDI (CGI: ISO TC97/SC21 N1179, May 1986) and provides 11 line drawing commands, 7 fill commands, 5 text commands, 3 image commands, 17 interface commands, and 7 auxiliary commands.
  - — Characters can be rotated, enlarged, or modified for proportional spacing, kerning, italics, etc.
  - — Image commands include enlargement and shrinking with interpolation to preserve true shapes.

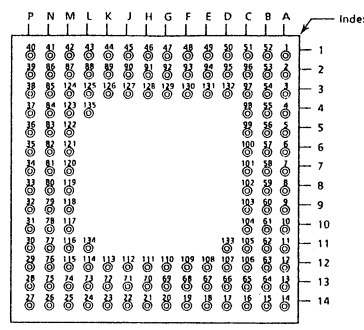
System Interface Functions

- The MPU can access the frame buffer directly.
- The bus interface supports both 68000/68020 and 80286/80386 MPUs.
- Large frame buffer address space (maximum 512 Mbytes).
- The GDP can draw graphics in system memory.
- Fifteen interrupt factors; interrupt vector output; on-chip bus-error handling.
- Color plane features: read/write masks, plane-to-plane copy

Pin Arrangement



(Top View)



(Bottom View)

135-Pin Ceramic PGA (PC-135)

Pin Configuration

Signal	Pin Code	Signal	Pin Code	Signal	Pin Code	Signal	Pin Code
D_0	D–2	$\overline{DREQ}$	G–1	MD_0	H–2	$\overline{AFBR}$	N–10
D_1	E–3	$\overline{DACK}$	H–1	MD_1	H–3	$\overline{HALT}$	P–11
D_2	B–1	$\overline{DONE}$	J–1	MD_2	J–2	$\overline{HALTA}$	N–11
D_3	A–1			MD_3	K–1	$\overline{SBREQ}$	M–11
D_4	C–2	MA_0	A–13	MD_4	K–2	$\overline{SBACK}$	P–12
D_5	B–2	MA_1	B–13	MD_5	L–1	$\overline{RETRY}$	N–12
D_6	A–2	MA_2	A–14	MD_6	L–2	$\overline{BERR}$	M–12
D_7	C–3	MA_3	D–12	MD_7	M–1		
D_8	B–3	MA_4	C–13	MD_8	N–1	CLKIN	B–9
D_9	A–3	MA_5	B–14	MD_9	M–2	SCLK	A–10
D_{10}	B–4	MA_6	D–13	MD_{10}	L–3	MCYC1	A–11
D_{11}	A–4	MA_7	C–14	MD_{11}	L–4	MCYC2	B–10
D_{12}	B–5	MA_8	F–12	MD_{12}	P–1		
D_{13}	A–5	MA_9	E–13	MD_{13}	N–2	$\overline{STB}$	A–9
D_{14}	C–6	MA_{10}	D–14	MD_{14}	P–2	FBS0	P–13
D_{15}	B–6	MA_{11}	F–13	MD_{15}	M–3	FBS1	N–13
		MA_{12}	E–14	MD_{16}	N–3	FBS2	P–14
$\overline{RES}$	A–8	MA_{13}	F–14	MD_{17}	P–3	FBS3	L–11
CS	C–1	MA_{14}	G–13	MD_{18}	N–4		
RS1	E–2	MA_{15}	G–14	MD_{19}	P–4	$V_{CC}1$, $V_{CC}2$	F–3, C–4
$\overline{RS2}$	D–1	MA_{16}	H–14	MD_{20}	M–5	$V_{CC}3$, $V_{CC}4$	A–6, C–10
$\overline{R/W}$	F–2	MA_{17}	J–14	MD_{21}	N–5	$V_{CC}5$, $V_{CC}6$	E–12, J–12
$\overline{DTACK}$	F–1	MA_{18}	H–13	MD_{22}	P–5	$V_{CC}7$, $V_{CC}8$	L–12, P–10
$\overline{IRQ}$	E–1	MA_{19}	H–12	MD_{23}	M–6	$V_{CC}9$, $V_{CC}10$	M–7, K–3
$\overline{IACK}$	G–2	MA_{20}	J–13	MD_{24}	N–6	GND 1, GND 2	G–3, D–3
		MA_{21}	K–14	MD_{25}	P–6	GND 3, GND 4	C–5, A–7
$\overline{HSYNC}$/$\overline{EXHSYNC}$	B–8	MA_{22}	K–13	MD_{26}	P–7	GND 5, GND 6	B–7, C–7
$\overline{VSYNC}$	B–11	MA_{23}	L–14	MD_{27}	N–7	GND 7, GND 8	C–9, C–11
$\overline{EXVSYNC}$/$\overline{ACT}$	C–8	MA_{24}	L–13	MD_{28}	P–8	GND 9, GND 10	D–11, G–12
$\overline{DISP1}$/EXDISP	C–12	MA_{25}	M–14	MD_{29}	N–8	GND 11, GND 12	K–12, M–10
$\overline{DISP2}$	B–12	MA_{26}	N–14	MD_{30}	P–9	GND 13, GND 14	M–9, M–8
$\overline{CUD}$	A–12	MA_{27}	M–13	MD_{31}	N–9	GND 15, GND 16	M–4, J–3

Pin Description

Type	Symbol	Pin Name	I/O	Function
Power	V_{CC}	Power Supply	—	+5 V power supply
	GND	Ground	—	Connected to system ground
Clock	CLKIN	Clock In	I	Max. 40 MHz clock input (50% duty ratio)
	SCLK	S Clock	O	Reference clock output
	MCYC1	Memory Cycle 1	O	Indicates frame buffer memory access timing
	MCYC2	Memory Cycle 2	O	90° phase delay with respect to MCYC1
MPU Bus Interface	D_0 — D_{15}	Data Bus	3-state I/O	Used for data transfer between the GDP and MPU
MPU Bus Control	$\overline{RES}$	Reset	I	External input that resets the GDP. (1) The entire internal state of the GDP is reset. Display and drawing operations both abort. (2) During $\overline{RES}$ input the GDP outputs DRAM refresh addresses at the MA pins specified in the refresh address output position (RAP) field. $\overline{HSYNC}$ remains low during this interval. (3) The following registers are affected by $\overline{RES}$ input.

Register	Effect of Reset
Address/Write FIFO Count Register (AWFCR)	WFC is reset to "100000," indicating write FIFO is empty.
Status Register (SR)	UDP, CED, WFR, and WFE are set to "1;" other bits are cleared to "0." SR value is H'8023.
FIFO	FIFO is entirely cleared. Commands, parameters, and data in write FIFO and data in read FIFO are all lost.
Command Control Registers (CCR0, CCR1)	SRES is set to "1;" all other bits are cleared to "0."
Interrupt Enable Register (IER)	All bits are cleared to "0."
Operation Mode Registers (OMR0, OMR1)	EXS is cleared to "00;" STR, LBP, and EXSP are cleared to "0." Other bits are not affected.
Display Control Registers (DCR0, DCR1)	DSPE is cleared to "0;" other bits are not affected.
Interrupt Vector Register (IVR)	Initialized to H'000F.

Pin Description (cont)

Type	Symbol	Pin Name	I/O	Function
MPU Bus Control	$\overline{RES}$	Reset	I	(4) Registers other than those listed above are not affected by $\overline{RES}$ input.
	$\overline{CS}$	Chip Select	I	Used by the MPU and other system devices to select the GDP. The GDP's internal registers can be written and read only when $\overline{CS}$ is low.
	RS1, RS2	Register Select 1 & 2	I	Input signals that select internal registers in the GDP. Registers are accessed as indicated below.

RS2	RS1	R/$\overline{W}$	Register
L	L	L	Address register
L	L	H	Address/write FIFO counter register
L	H	L	Status register clear register
L	H	H	Status register
H	L	—	FIFO entry
H	H	—	Control registers

	R/$\overline{W}$	Read/Write	I	Indicates direction of data transfer between GDP and MPU. (1) Read: When R/$\overline{W}$ is high, GDP transfers data to MPU. (2) Write: When R/$\overline{W}$ is low, MPU transfers data to GDP.
	$\overline{DTACK}$	Data Transfer Acknowledge	3-state output	Indicates completion of data transfer. Used for data transfer control with HD68000 and other devices having an asynchronous bus interface.
	$\overline{IRQ}$	Interrupt Request	Open-drain output	Notifies MPU of command termination, undefined commands, etc.
	$\overline{IACK}$	Interrupt Acknowledge	I	Notifies GDP that current system bus cycle is an interrupt acknowledge cycle. When it receives this signal, the GDP sends its interrupt vector number to the MPU.
DMA Control	$\overline{DREQ}$	DMA Request	O	Requests a DMA controller to perform a DMA transfer of commands or data.
	$\overline{DACK}$	DMA Acknowledge	I	Reply from DMA controller to $\overline{DREQ}$
	$\overline{DONE}$	Done	Open-drain I/O	Indicates end of DMA transfer.

Pin Description (cont)

Type	Symbol	Pin Name	I/O	Function
Display Control	$\overline{\text{HSYNC}}$ or EXHSYNC	Horizontal Sync or External Horizontal Sync	I/O	Horizontal synchronization output signal (master or slave mode) Horizontal synchronization input signal (TV synchronization or laser printer mode)
	$\overline{\text{VSYNC}}$	Vertical Sync	O	Vertical synchronization signal
	$\overline{\text{EXVSYNC}}$ or ACT	External Vertical Sync or Active	I/O	Vertical synchronization signal. When the GDP operates in master mode, EXVSYNC is an output pin. The shape of the EXVSYNC output depends on the scan mode as follows: (1) Non-interlace mode Same output waveform as $\overline{\text{VSYNC}}$. (2) Interlaced sync or interlaced sync and video mode Odd fields of $\overline{\text{VSYNC}}$, output separately. If the active (ACT) bit in command control register 0 (CCR0) is set to "1," this pin outputs a signal notifying external devices of the operating status of the drawing processor.
	$\overline{\text{DISP1}}$ or EXDISP	Display Timing 1 or External Display Timing	I/O	In CRT display mode, an output signal indicating the display timing. In laser printer interface mode an input signal requesting display address output.
	$\overline{\text{DISP2}}$	Display Timing 2	O	Output during display of the superimpose window.
	$\overline{\text{CUD}}$	Cursor Display	O	Displays a cursor on the CRT.
Frame Buffer Control	MD_0 to MD_{31}	Frame Buffer Data Bus	3-state I/O	Data bus between GDP and frame buffer or system memory.
	MA_0 to MA_{27}	Frame Buffer Address Bus	3-state output	Address output for access from GDP to frame buffer.
Frame Buffer Bus Control	$\overline{\text{STB}}$	Strobe	O	Strobe for frame buffer address and status signals. Output even while the GDP is halted (while $\overline{\text{HALT}}$ is asserted).

Pin Description (cont)

Type	Symbol	Pin Name	I/O	Function
Frame Buffer Bus Control	FBS0 to FBS3	Frame Buffer Bus Status	3-state output	Output signals indicating frame buffer status in each cycle as follows.

FBS3	FBS2	FBS1	FBS0	Description
0	0	0	0	Not accessing frame buffer
0	0	0	1	Memory write with pixel address in write-only mode
0	0	1	0	Undefined
0	0	1	1	Executing ADOUT instruction
0	1	0	0	Drawing cycle: reading 16-bit word
0	1	0	1	Drawing cycle: writing 16-bit word
0	1	1	0	Drawing cycle: reading 32-bit longword
0	1	1	1	Drawing cycle: writing 32-bit longword
1	0	0	0	DRAM refresh address output
1	0	0	1	DRAM refresh output with common attribute output on MD pins
1	0	1	0	Undefined
1	0	1	1	Undefined
1	1	0	0	Display address output for base window
1	1	0	1	Display address output for superimpose window
1	1	1	0	Undefined
1	1	1	1	Undefined

Pin Description (cont)

Type	Symbol	Pin Name	I/O	Function
Bus Switching Control	$\overline{AFBR}$	Advanced Frame Buffer Request	O	Output signal notifying other devices of request for use of frame buffer bus.
	$\overline{HALT}$	Halt	I	Input signal that halts drawing and other operations by GDP.
	$\overline{HALTA}$	Halt Acknowledge	O	Output signal notifying bus requester that GDP has released frame buffer bus.
	$\overline{SBREQ}$	System Bus Request	O	Signal output by GDP to request use of bus for system memory access.
	$\overline{SBACK}$	System Bus Acknowledge	I	Input signal that notifies GDP when system bus is released.
	$\overline{RETRY}$	Retry	I	Input signal requesting repetition of drawing cycle when system memory access time is slower than GDP's memory cycle.
	$\overline{BERR}$	Bus Error	I	Input signal that notifies GDP of bus errors occurring during system memory access.

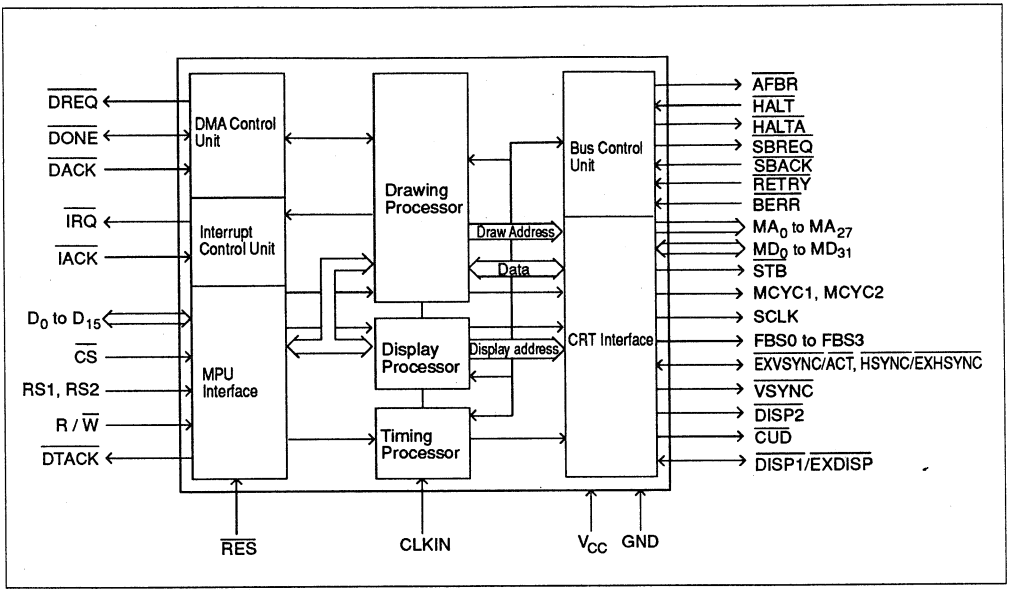
Functional Description

Item			Description	
Clock Frequency			20 MHz (max) or 16 MHz (max)	
Frame Buffer Space (full bit-mapped)			512 Mbytes (max)	
Display Functions	Hardware windows		Max. 4 overlapping windows (specified priorities), 1-window superimpose	
	Display control	Frame buffer access	Single access, dual access	
		Smooth scroll	Supported in any direction	
		Graphic cursor	Graphic or cross-hair cursor position signals	
		CRT scanning system	Non-interlace scan, interlace sync, interlace sync & video	
	Multiport DRAM interface		Realtime data transfer supported	
	DRAM refresh		10-bit address	
	External synchronization		Master-slave, TV sync	
	Laser printer interface		On-chip printer synchronization functions	
Drawing Functions	Command set	Line	11	Command set conform to GKS (CGI)
		Fill	7	
		Text	5	
		Image	3	
		Interface	17	
		Auxiliary	7	
	Drawing speed (Max.) (4 bits/pixel)	Line	200 ns/pixel (any direction)	
		Fill	25 ns/pixel (solid-color fill)	
		Text	37.5 ns/pixel	
		BitBlt	75 ns/pixel (copy)	
	Coordinate systems		X-Y addresses (3 independent coordinate systems definable) and physical addresses	
	Color representation		Monochrome (binary) and color (1, 2, 4, 8, or 16 bits/pixel)	

Functional Description (cont)

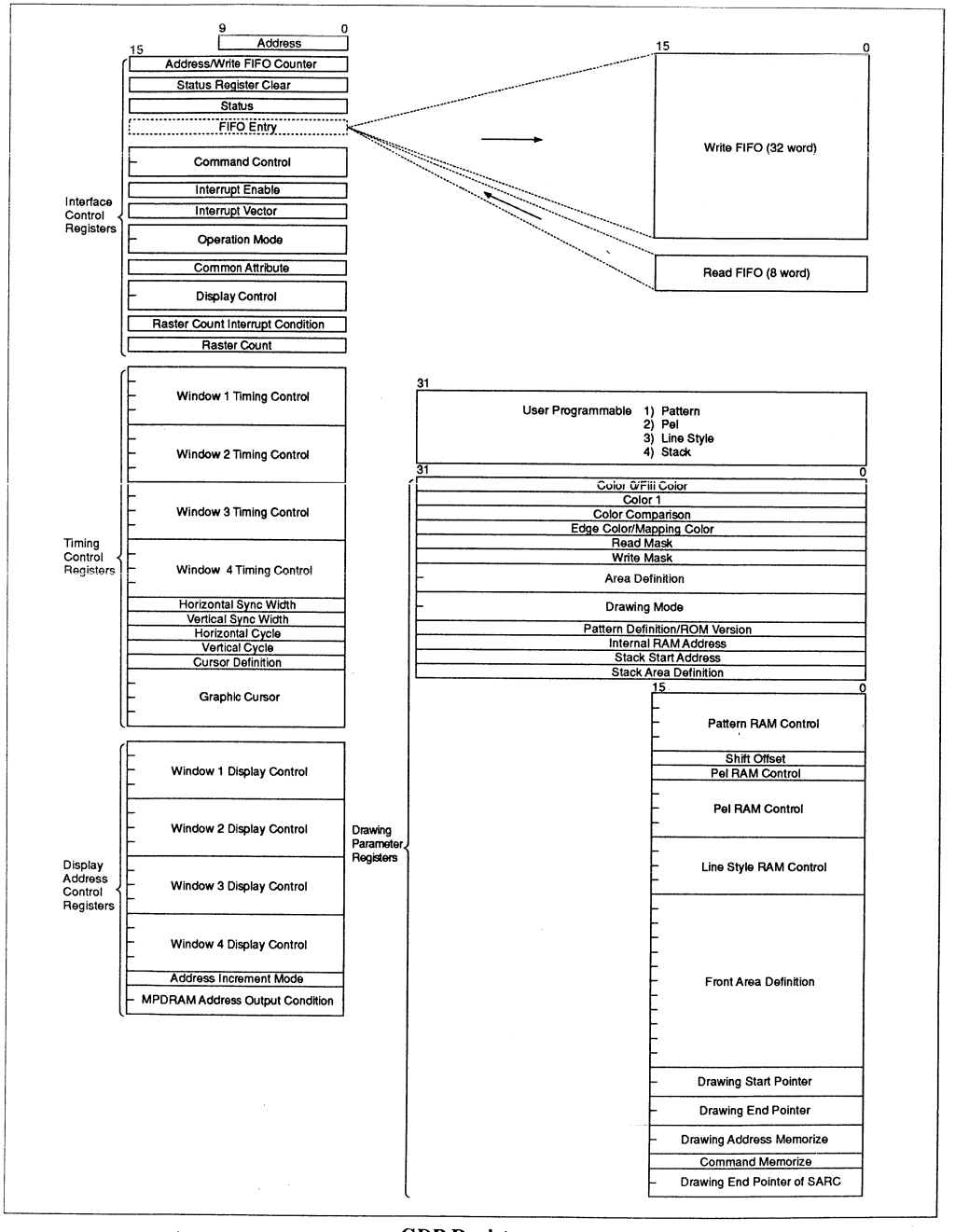
Item			Description
Drawing Functions	Drawing modes	Mapping condition modes	8 modes (color → binary)
		Color modes	4 modes (binary → color)
		Operation modes	16 logic operations, +4 arithmetic operations
		Color comparison modes	14 register comparisons, +6 transparent modes
		Logical pel modes	2 modes, pel definable up to 32 × 32 pixels
		Area modes	2 modes (graphic clipping, area detect)
		Character area modes	3 modes (character clipping, area detect)
		Pick mode	1 mode (picks graphics and text)
	Tiling		Tiling pattern can be stored in on-chip RAM or frame buffer
	Line style information		Up to 1024 bits specifiable in on-chip RAM
	Image operations		Enlargement and shrinking with any zoom ratio (with interpolation), rotation through any angle
	Character attribution		Proportional spacing, italic, enlargement, text path
System Interface	MPU interface (16-bit)		Supports H16/H32, 8086, and 68000 families
	MPU access to frame buffer		On-chip halt function
	GDP access to system memory		Font handling etc. (bus attribution functions)
	DMA transfer		PUT/GET commands
	Command transfer methods		3 methods (program I/O, DMA, batch transfer)
	Interrupts		15 factors, generates interrupt vector
	Error handling		Saves address information and command code
	Color plane features		Read and write masks, plane-to-plane copy
Process			1.0 μm CMOS
Supply Voltage			Single +5 V supply voltage
Package			135-pin PGA

Block Diagram



Block Diagram

Registers



GDP Registers

Address Registers and Interface Control Registers

$\overline{CS}$	RS2	RS1	R/$\overline{W}$	Register No.	Register Name	Register Abbr.	Data 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Setting CRT	Setting LBP
1	–			–	–	–	–																–	–
0	0	0	0	AR	Address	AR							INC	ADDRESS								0	✇	✇
			1	AWFCR	Address/write FIFO counter	AWFCR	WFC						INC	ADDRESS									R	R
		1	0	SRCR	Status register clear	SRCR	UDCL	RCCL		WDCL	DECL	BECL	XECL	STCL	CECL	ARCL		FOCL					O	O
			1	SR	Status	SR	UDP	RCD		WDC	DER	BER	XER	STP	CER	ARD	CED	FOR	RFF	RFR	WFR	WFE	R	R
	1	0	1/0	FE	FIFO entry	FE	FE																✇	✇
		1		r002	Command control	CCR0	SRES	SHLT		ACT	IVM	GBM			WDM	WDRC			DDM	DDRC		DTSEL	✇	✇
				r004		CCR1								WTR		DTP		SMA	WTM		BSZ		✇	✇
				r006	Interrupt enable	IER	UDE	RCE		WDE	DEE	BEE	XEE	STE	CRE	ARE	CEE	FOE	RFE	RRE	WRE	WEE	O	O
				r008	Interrupt vector	IVR	IV																O	O
				r00A	Operation mode	OMR0	STR	EXS		LBP	EXSP	ACP	CSK		DSK		RAM	MPM	ACM	RSM		VRP	O	O
				r00C		OMR1	RAP					RCYN			MATS	CATP	WATP						O	O
				r00E	Common attribute	CATRR									CATR								O	O
				r010	Display control	DCR0		PR4				PR3				PR2				PR1			O	X
				r012		DCR1	DSPE											SIE		SWD			O	X
				r014	Raster counter interrupt condition	RCCR		RCC															O	O
			1	r016	Raster count	RCR		RC															R	R
1	–			r018 to r0FE	Reserved																		–	–

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)

2. Do not read or write registers r018 to r0FE. (These registers have undetermined values when read.)

3. Meaning of symbols:

   ✇ : Must always be set (although this does not mean the value is always necessary)

   O: Must be set if the corresponding function is used.

   X: The laser printer mode uses window 4, regardless of the setting.

   R: Read-only

Timing Control Registers

$\overline{CS}$	RS2	RS1	R/$\overline{W}$	Register No.	Register Name		Abbr.	Data 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Setting CRT	LBP
0	1	1	1/0	r100	Window 1	Horizontal display start 1	HDSR1							HDS1										○[1]	×
				r102		Horizontal display width 1	HDWR1							HDW1											
				r104		Vertical display start 1	VDSR1			VDS1															
				r106		Vertical display width 1	VDWR1			VDW1															
				r108	Window 2	Horizontal display start 2	HDSR2							HDS2										○[1]	×
				r10A		Horizontal display width 2	HDWR2							HDW2											
				r10C		Vertical display start 2	VDSR2			VDS2															
				r10E		Vertical display width 2	VDWR2			VDW2															
				r110	Window 3	Horizontal display start 3	HDSR3							HDS3										○[1]	×
				r112		Horizontal display width 3	HDWR3							HDW3											
				r114		Vertical display start 3	VDSR3			VDS3															
				r116		Vertical display width 3	VDWR3			VDW3															
				r118	Window 4	Horizontal display start 4	HDSR4							HDS4										○[1]	×
				r11A		Horizontal display width 4	HDWR4							HDW4											
				r11C		Vertical display start 4	VDSR4			VDS4															
				r11E		Vertical display width 4	VDWR4			VDW4															
1	–			r120 to r13E	Reserved																			–	–
0	1	1	1/0	r140	Horizontal sync width		HSWR												HSW					✪	×
				r142	Vertical sync width		VSWR												VSW						
				r144	Horizontal cycle		HCR							HC											○[2]
				r146	Vertical cycle		VCR			VC															
				r148	Cursor definition		CDR	CM	CCM		CDA							CON				COFF			✪	×
				r14A	Graphic cursor		GCR							CXS										▲[1]	
				r14C										CXE											
				r14E						CYS															
				r150						CYE															
1	–			r152 to r17E	Reserved																			–	–

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)

2. Do not read or write registers r120 to r13E or r152 to r17E. (These registers have undetermined values when read.)

3. Meaning of symbols:
   - ✪ : Must always be set
   - × : Need not be set
   - ▲[1]: Must be set if the cursor is used
   - ○[1]: Need not be set for undisplayed windows (If there is no display, no settings are required.)
   - ○[2]: Need not be set if static memory is used

Display Address Control Registers

$\overline{CS}$	RS2	RS1	R/$\overline{W}$	Register No.	Name		Abbr.	Data 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Setting CRT	LBP
0	1	1	1/0	r180	Window 1	Window attribute control signal 1	WATRR1									WATR1								○[1]	×
				r182		Memory width 1	MWR1									MW1									
				r184		Start address 1	SAR1									SAH1									
				r186												SAL1									
				r188	Window 2	Window attribute control signal 2	WATRR2									WATR2								○[1]	×
				r18A		Memory width 2	MWR2									MW2									
				r18C		Start address 2	SAR2									SAH2									
				r18E												SAL2									
				r190	Window 3	Window attribute control signal 3	WATRR3									WATR3								○[1]	×
				r192		Memory width 3	MWR3									MW3									
				r194		Start address 3	SAR3									SAH3									
				r196												SAL3									
				r198	Window 4	Window attribute control signal 4	WATRR4									WATR4								○[1]	⊛
				r19A		Memory width 4	MWR4									MW4									
				r19C		Start address 4	SAR4									SAH4									
				r19E												SAL4									
1	–			r1A0 to r1BE	Reserved																			–	–
0	1	1	1/0	r1C0	Address increment mode		ADIR									SDA							DAI	⊛	⊛
				r1C2	MPDRAM display address output condition	Base window display address output condition	BDCR									BDC								▲[2]	×
				r1C4		Superimpose window display address output condition	SDCR									SDC								▲[3]	
1	–			r1C6 to r1FE	Reserved																			–	–

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)

2. Do not read or write registers r1A0 to r1BE or r1C6 to r1FE. (These registers have undetermined values when read.)

3. Meaning of symbols:
   - ⊛ : Must always be set
   - × : Need not be set
   - ○[1]: Need not be set for undisplayed windows (If there is no display, no settings are required.)
   - ▲[2]: Must be set if multiport memory is used
   - ▲[3]: Must be set if multiport memory and superimpose window are used

Drawing Parameter Control Registers (1)

Register No.	Read/Write	Register Name	Register Abbr.	Data 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	R, W	Color 0/fill color	CLOR/FCLR	CL0H/FCLH															
01				CL0L/FCLL															
02	R, W	Color 1	CLIR	CL1H															
03				CL1L															
04	R, W	Color comparison	CCMPR	CCMPH															
05				CCMPL															
06	R, W	Edge color/mapping color	EDGR/MAPCLR	EDGH/MAPCLH															
07				EDGL/MAPCLL															
08	R, W	Read mask	RMASKR	RMASKH															
09				RMASKL															
0A	R, W	Write mask	WMASKR	WMASKH															
0B				WMASKL															
0C	R, W	Area definition	ADR	XMIN															
0D				YMIN															
0E				XMAX															
0F				YMAX															
10	R, W	Drawing mode	DMR	PICK		AREA		CAM					PEL				COL		
11				MAP				CCMPM					OPM						
12				DM	DMW														
13				SM	SMW														
14	R, W	Pattern definition	PDR	PM	PMW														
15	R	ROM version	RVR	RV															
16	R, W	Internal RAM address	IRAR	IRAH															
17				IRAL															
18	R, W	Stack — Start address	SSAR	SSAH															
19				SSAL															
1A		Stack — Area definition	SADR	SADH															
1B				SADL															
1C to 21	Reserved																		

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)

2. Do not write to register No. 15 (which is a read-only register). Do not read or write register Nos. 1C to 21. (These registers have undetermined values when read.)

Drawing Parameter Control Registers (2)

Register No.	Read/Write	Register		Data															
		Name	Abbr.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
22	R, W	Pattern RAM control	PRCR	PSX															
23				PSY															
24				PEX															
25				PEY															
26	Reserved																		
27																			
28	R, W	Shift offset	SOFSR									SOFS							
29	Reserved																		
2A	R, W	Pel RAM address	PLAR						PLA						(PLD)				
2B	Reserved																		
2C	R, W	Pel RAM control	PLCR												PLX1				
2D															PLX2				
2E															PLY1				
2F															PLY2				
30	R, W	Line style RAM control	LSCR							LSP									
31										LSS									
32										LSE									
33								LSZC								LSZ			
34	R, W	Font area definition	FADR	FSAH															
35				FSAL															
36																FBNH			
37				FBNL															
38					FAMW														
39				IOFS															
3A				FSX															
3B				FSY															
3C				DX															
3D				DY															
3E				CSX															
3F				CSY															

Notes: 1. In setting these registers, write "0" in the shaded bits. (These bits have undetermined values when read.)

2. Do not read or write register Nos. 26, 27, 29, and 2B. (These registers have undetermined values when read.)

Drawing Parameter Control Registers (3)

Register No.	Read/Write	Register Name	Register Abbr.	Data 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40 to 47	Reserved																		
48	R	Drawing start pointer	DSPR	DSPX															
49				DSPY															
4A	R	Drawing end pointer	DEPR	DEPX															
4B				DEPY															
4C	R	Drawing address memorize	DRADR	DRADH															
4D				DRADL															R/W
4E	R	Command memorize	CMDR	CMD															
4F to 51	Reserved																		
52	R	Drawing end pointer of SARC	DEPSR	DEPSX															
53				DEPSY															
54 to 57	Reserved																		
58 to FF	Undefined																		

Notes: 1. Shaded bits have undetermined values when read.

2. Do not write to register Nos. 48 to 4E or 52 to 53.

3. Do not read or write register Nos. 40 to 47, 4F to 51, or 54 to FF. (These registers have undetermined values when read.)

4. An execution error occurs if register Nos. 40 to FF are written or register Nos. 58 to FF are read.

Commands (1)

	Mnemonic	Command	Operation Code				Parameters	Words
Line	LINE	Line	1000	0000	0000	000B	Xs, Ys, Xe, Ye	5
	RCT	Rectangle	1000	0010	0000	000B	X_1, Y_1, X_2, Y_2	5
	PLL	Polyline	1000	1000	0000	000B	n, X_1, Y_1 ... Xn, Yn	2+2n
	DPLL	Disjoint Polyline	1000	1010	0000	000B	n, X_1, Y_1 ... Xn, Yn	2+2n
	SPLL	Short Polyline	1001	0010	0000	000B	n, X, Y, {(dX1, dY1), ... (dXn, DYn)}	②
	PLG	Polygon	1001	0000	0000	000B	n, X_1, Y_1 ... Xn, Yn	2+2n
	CRCL	Circle	1010	1000	0000	000B	Xc, Yc, A, B	5
	ARC	Arc	1010	1010	0000	000B	Xc, Yc, A, B, DXs, DYs, DXe, DYe	9
	ARCC	Arc Close	1011	100CT	0000	000B	Xc, Yc, A, B, DXs, DYs, DXe, DYe	9
	SARC	Single-stroke Arc	1011	101C	0000	000B	Xc, Yc, a, b, Xs, Ys, DXe, DYe	9
	DOT	Dot	1001	1000	0000	000B	X, Y	3
Fill	FRCT	Filled Rectangle	1000	0110	P000	000B	X_1, Y_1, X_2, Y_2	5
	FCRCL	Filled Circle	1010	1100	P000	000B	Xc, Yc, A, B	5
	FFAN	Filled Fan	1011	110CT	P000	000B	Xc, Yc, A, B, DXs, DYs, DXe, DYe	9
	PAINT	Paint	1001	110E	P000	000B	Xs, Ys	3
	SEARCH	Search	1000	110①E	0000	000B	Xs, Ys	3
	FTRAP	Filled Trapezoid	1001	0100	PS00	000B	X_1, Y_1, X_2, Y_2, X_3, Y_3, X_4, Y_4, Ys, Ye	11
	FHLINE	Filled Horizontal Line	1000	0100	P000	000B	Y, n, X_1 ... Xn	3+n

Notes: ①: DIR: Search right if DIR = 0, left if DIR = 1
②: $4 + (n/2)\uparrow$
Words: Number of words in command and parameters
B: Breakpoint bit
CT: Sector if CT = 0, segment if CT = 1
P: Tiling pattern if P = 0, solid color fill if P = 1
E: If E = 0, boundary color is color in edge color register
If E = 1, boundary color is color other than color in edge color register
C: Counterclockwise if C = 0, clockwise if C = 1
S: Fill sides if S = 0, do not fill sides if S = 1

Commands (2)

	Mnemonic	Command	Operation Code				Parameters	Words
Text	TEXT	Text	0111	0SD0	0000	000B	X, Y, n, CN_1 ... CNn	4+n
	ATEXT	Append Text	0111	1SD0	0000	000B	n, CN_1 ... CNn	2+n
	TEXTSP	Text with Space	0110	1SD0	0000	000B	X, Y, n, CN_1, DX_1, DY_1 ... CNn, DXn, DYn	4+3n
	ATEXTSP	Append Text with Space	1101	1SD0	0000	000B	n, CN_1, DX_1, DY_1 ... CNn, DXn, DYn	2+3n
	CHR	Character	0110	0SD0	0000	000B	CN	2
Image	COPY	Copy	111③	DSD0	0000	000B	Xs, Ys, DX, DY, Xd, Yd	7
	ZOOM	Zoom	1101	0010	0000	000B	Xs, Ys, LSX, LSY, Xd, Yd, LDX, LDY	9
	ROT	Rotation	1101	0100	0000	000B	Xs, Ys, LSX, LSY, Xd, Yd, LDXx, LDXy, LDYx, LDYy	11
Inter-face	PUT	Put	0101	110M	0000	000B	X, Y, DX, DY, D_1 ... Dn	5+α
	GET	Get	0101	111M	0000	000B	X, Y, DX, DY	5
	ORGD	Origin of Drawing	0000	0110	0000	000B	AH, AL, X, Y	5
	ORGS	Origin of Source	0000	1000	0000	000B	AH, AL, X, Y	5
	ORGP	Origin of Pattern	0000	1010	0000	000B	AH, AL, X, Y	5
	LDPR	Load Parameter Register	0001	1100	0000	000B	RN, AH, AL, n	5
	STPR	Store Parameter Register	0001	1110	0000	000B	RN, AH, AL, n	5
	WPR	Write Parameter Register	0001	0110	0000	000B	RN, D_1 ... Dn, n	3+n
	RPR	Read Parameter Register	0001	1010	0000	000B	RN, n	3

Notes: ③: SSD: Horizontal if SSD = 0; vertical if SSD = 1
Words: Number of words in command and parameters
B: Breakpoint bit
SD: Left-to-right if SD = 00, up if SD = 01 (rotated 90°), right-to-left if SD = 10 (rotated 180°), down if SD = 11 (rotated 270°)
DSD: Right-up if DSD = 000, right-down if DSD = 001, left-up if DSD = 010, left-down if DSD = 011, up-right if DSD = 100, down-right if DSD = 101, up-left if DSD = 110, down-left if DSD = 111
M: Normal transfer if M = 0, convert if M = 1 (PUT—convert binary to color; GET—convert color to binary)
I: No interpolation if I = 0, interpolate if I = 1

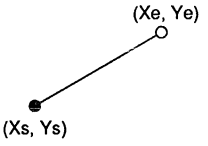
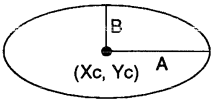
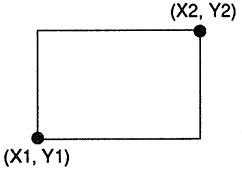
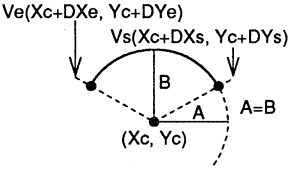
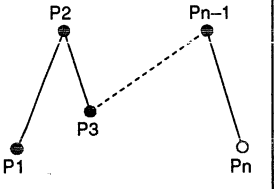
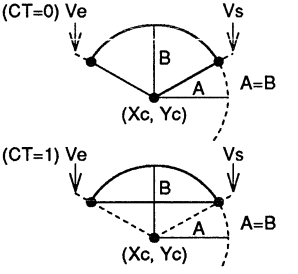
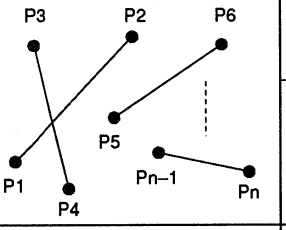
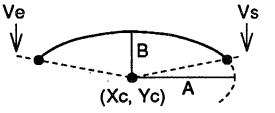
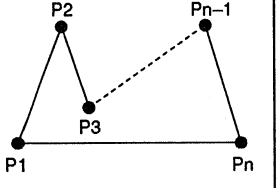
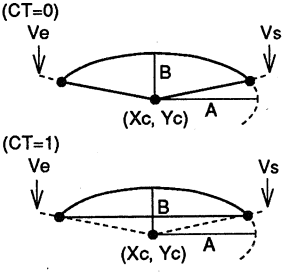
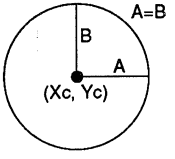
Commands (3)

	Mnemonic	Command	Operation Code				Parameters	Words
Inter-face	BWT	Block Write	0101	0000	0000	000B	AH, AL, n, $D_1 \cdots D_{2n}$	4+2n
	BRD	Block Read	0101	0010	0000	000B	AH, AL, n	4
	BCOPY	Block Copy	0101	01ID0	0000	000B	ASH, ASL, ADH, ADL, n	6
	DISPON	Display On	0001	0000	0000	000B		1
	DISPOFF	Display Off	0001	0010	0000	000B		1
	NOP	No Operation	0000	0010	0000	000B		1
	ADOUT	Address/Data Out	0000	1100	0000	000B	AH, AL, DH, DL	5
	WDEND	Write DMA End	0000	0100	0000	000B		1
Auxil-iary	TERM	Terminator	1001	1010	0000	000B		1
	CLINE	Current Line	1001	0110	0000	000B	Xe, Ye	3
	CHRBGN	Character Begin	0100	1000	0000	000B	X, Y	3
	CHRSPC	Character Space	0100	1010	0000	000B	dX, dY	3
	NOP3	No Operation 3	0000	0000	0000	000B	H'0, H'0	3
	BATCH	Batch	0100	0000	0000	0000	AH, AL	3
	BTEND	Batch End	0100	0010	0000	0000		1

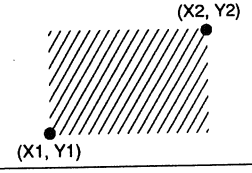
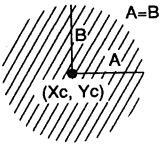
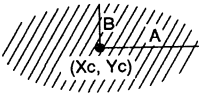
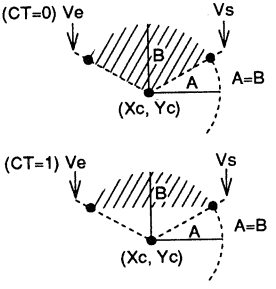
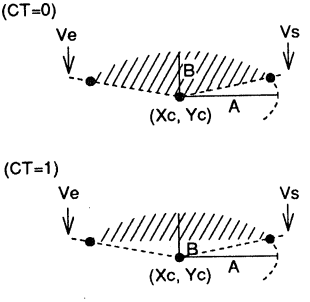
Notes: Words: Number of words in command and parameters
B: Breakpoint bit
ID: Increment if ID = 0, decrement if ID = 1

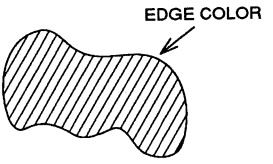
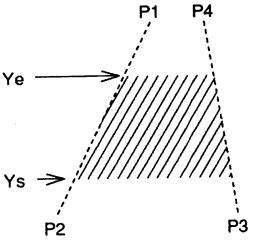
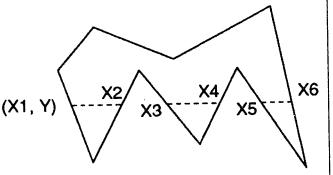
Examples of Principal Drawing Commands

1. Line Drawing Commands

Command	Example	Command	Example
LINE (draw line)		CRCL (draw ellipse)	
RCT (draw rectangle)		ARC (draw circular arc)	
PLL (draw polyline) SPLL (draw polyline with short segments)		ARCC (draw circular sector or segment)	
DPLL (draw disjoint polyline)		ARC (draw elliptical arc)	
PLG (draw polygon)		ARCC (draw elliptical sector or segment)	
CRCL (draw circle)		DOT (draw one dot)	

2. Filling Commands

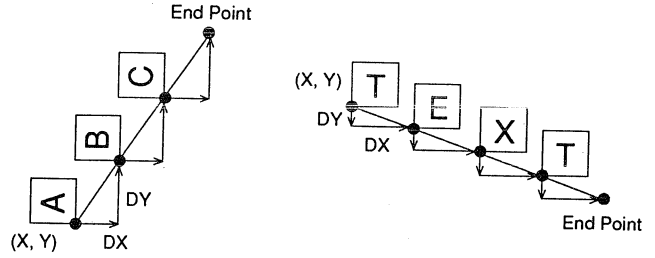
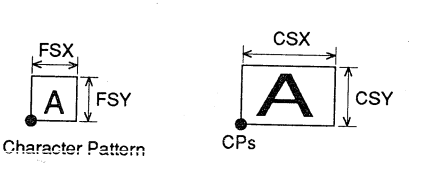
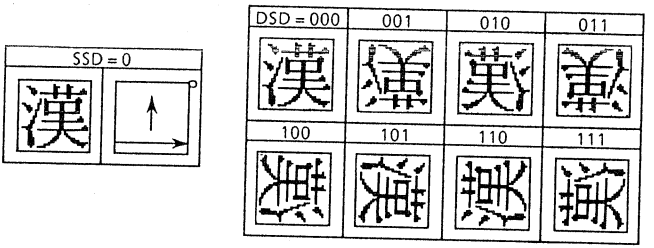
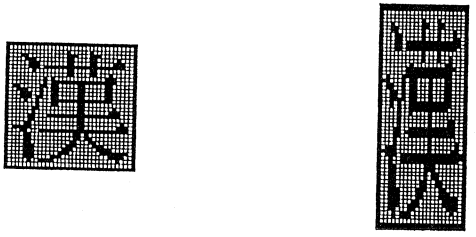
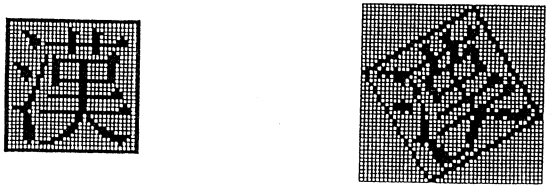
Command	Example
FRCT (draw filled rectangle)	
FCRCL (draw filled circle)	
FCRCL (draw filled ellipse)	
FFAN (draw filled circular sector or segment)	
FFAN (draw filled elliptical sector or segment)	

Command	Example
PAINT (fill arbitrary area)	
FTRAP (draw filled trapezoid)	
FHLINE (fill horizontal line segments)	

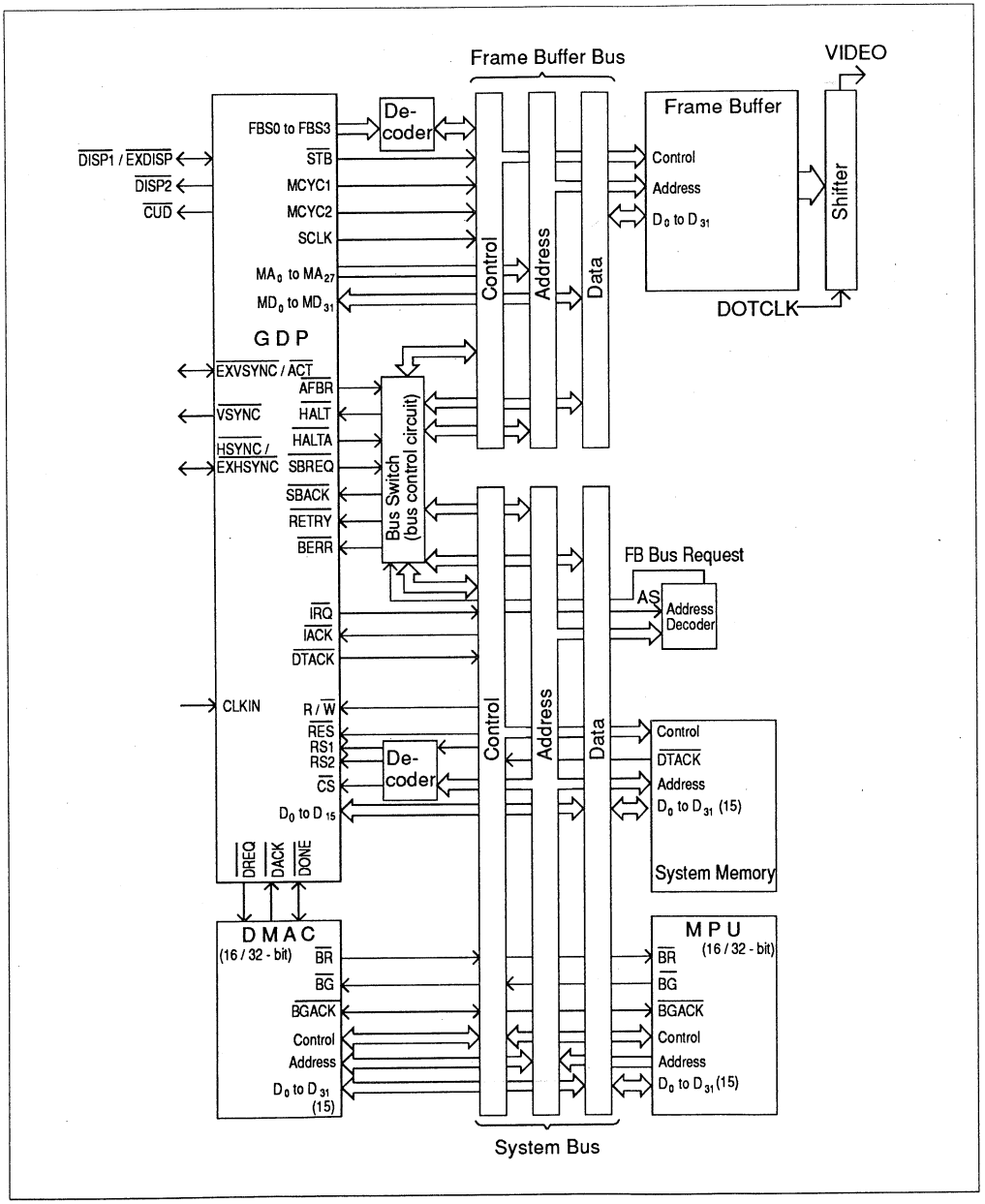


Pattern (example)

3. Character or Image Drawing Commands

Command	Example
TEXT /ATEXT (draw character string)	
CHR (draw character)	
COPY (copy image data)	
ZOOM (copy with enlargement or shrinking)	
ROT (copy with rotation)	

System Overview



Graphic Processing System Configuration Using GDP (example)

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}*	–0.3 to +7.0	V
Input Voltage	V_{in}*	–0.3 to V_{CC} + 0.3	V
Allowable Output Current	|Io|**	5	mA
Total Allowable Output Current	|ΣIo|***	240	mA
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	–55 to +150	°C

* Based on GND = 0 V

** Allowable output current refers to the maximum current that may be sourced or sinked at a single output pin or input/output pin.

*** Total allowable output current refers to the sum of all currents sourced or sinked at all output and input/output pins.

Note: Permanent damage to the GDP chip can result if it is used outside its absolute maximum ratings. The chip should preferably be used in the recommended operating conditions given next. Use in conditions outside the recommended conditions may adversely affect the reliability of the chip.

Recommended Operating Conditions

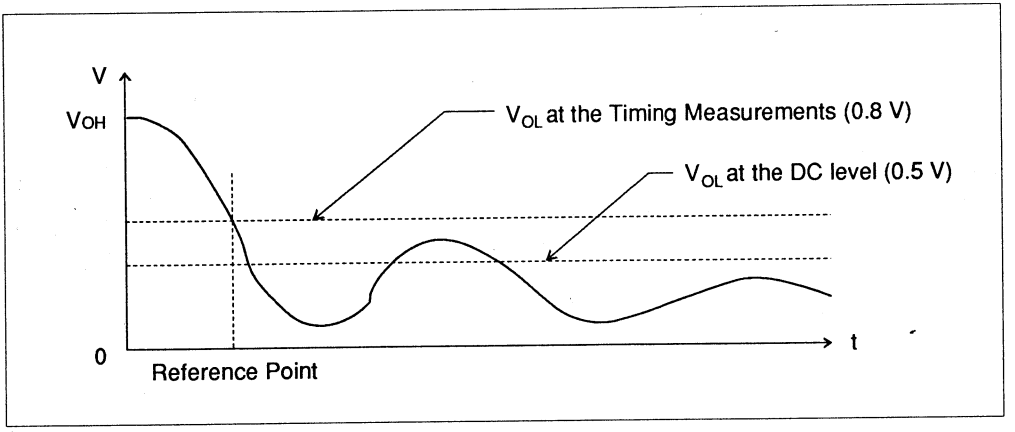
1. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}*	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}*	0	—	0.7	V
Input High Voltage	V_{IH}*	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

* Based on GND = 0 V

2. Timing Measurements

The output low voltage for timing measurements is 0.8 V. The normal output low voltage remains 0.5 V as listed in the DC characteristics. The high voltage level for timing measurements is V_{CC} – 2.0 V. (For $\overline{DTACK}$ measurements the high level is 2.4 V.)



V_{OL} for Timing Measurement

DC Characteristics at V_{CC} = 5.0 V ±5%, GND = 0 V, Ta = 0 to +70°C

Item	Pins	Symbol	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit	Conditions
Input High Voltage	○, △, □	V_{IH}	2.2	V_{CC}	2.2	V_{CC}	V	
Input Low Voltage		V_{IL}	–0.3	0.7	–0.3	0.7		
Input Leakage Current	○	I_{in}	–2.5	2.5	–2.5	2.5	µA	V_{in} = 0 to V_{CC}
Three-State Input Current (Off-State)	△	I_{TSI}	–10	10	–10	10		V_{in} = 0.4 to V_{CC}
Output High Voltage	△, ◇	V_{OH}	V_{CC} –1.0	—	V_{CC} –1.0	—	V	I_{OH} = –400µA
	◎		2.4	—	2.4	—		
Output Low Voltage	△, ◇, ◎	V_{OL}	—	0.5	—	0.5		I_{OL} = 2.2mA
	□, ☆		—	0.5	—	0.5		I_{OL} = 2.5mA
Output Leakage Current (Off-State)		I_{LOD}	—	10	—	10	µA	V_{OH} = V_{CC}
Input Capacitance	△	C_{in}	—	20	—	20	pF	V_{in} = 0V
	○		—	20	—	20		Ta = 25°C
Output Capacitance	□, ☆	C_{out}	—	18	—	18		f = 1.0MHz
Current Dissipation		I_{CC}	—	480	—	380	mA	• Chip not selected • Display on
			—	480	—	380		• During data bus read/write • Display on • During command execution

Notes: ○: Input — $\overline{RES}$, $\overline{CS}$, RS1, RS2, R/$\overline{W}$, $\overline{IACK}$, $\overline{DACK}$, $\overline{HALT}$, $\overline{SBACK}$, $\overline{RETRY}$, $\overline{BERR}$, CLKIN

△: Input/output (including 3-state) — D_0 to D_{15}, HSYNC/$\overline{EXHSYNC}$, $\overline{EXVSYNC}$/$\overline{ACT}$, DISP1/$\overline{EXDISP}$, MD_0 to MD_{31}

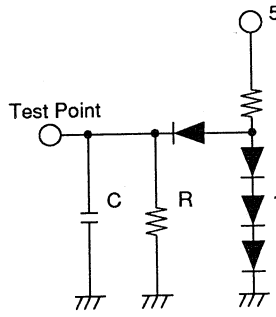
□: Open-drain input/output — $\overline{DONE}$

◇: Output (including 3-state) — $\overline{DREQ}$, $\overline{VSYNC}$, $\overline{DISP2}$, $\overline{CUD}$, MA_0 to MA_{27}, $\overline{STB}$, $\overline{FBS_0}$ to $\overline{FBS_3}$, $\overline{AFBR}$, $\overline{HALTA}$, $\overline{SBREQ}$, SCLK, MCYC1, MCYC2

◎: Output (3-state) — $\overline{DTACK}$

☆: Open-drain output — $\overline{IRQ}$

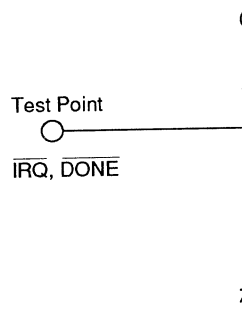
Test Load Circuit A



RL=1.8k Ω
C=40pF
R=10k Ω
All diodes are 1S2074 Ⓗ or equivalent.

Signal
D_0-D_{15}, $\overline{HSYNC}$/$\overline{EXHSYNC}$, $\overline{EXVSYNC}$/$\overline{ACT}$, $\overline{DISP1}$/$\overline{EXDISP}$, MD_0-MD_{31}, $\overline{DTACK}$, $\overline{DREQ}$, $\overline{VSYNC}$, $\overline{DISP2}$, $\overline{CUD}$, MA_0-MA_{27}, $\overline{STB}$, FBS0-FBS3, $\overline{AFBR}$, $\overline{HALTA}$, $\overline{SBREQ}$, SCLK, MCYC1, MCYC2

Test Load Circuit B



RL=1.8k Ω
C=40pF

AC Characteristics at V_{CC} = 5.0 V ±5%, GND = 0 V, Ta = 0 to +70°C

Clock and Reset Input

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
	Input Clock Frequency	f		4	40	4	32	MHz
1	Clock Cycle Time	t_{cyc}		25	250	32	250	ns
2	Clock "High" Level Pulse Width	t_{PWCH}		8	125	10	125	ns
3	Clock "Low" Level Pulse Width	t_{PWCL}	Fig. 1	8	125	10	125	ns
4	Clock Rise Time	t_{Cr}		–	8	–	8	ns
5	Clock Fall Time	t_{Cf}		–	8	–	8	ns
6	$\overline{RES}$ Input Pulse Width	t_{RESW}		20	–	20	–	t_{cyc}
7	$\overline{RES}$ Hold Time	t_{RESH}	Fig. 2	8	–	12	–	ns
8	$\overline{RES}$ Setup Time	t_{RESS}		4	–	8	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

MPU Read/Write

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
20	R/$\overline{W}$ Setup Time	t_{RWS}		0	–	0	–	ns
21	R/$\overline{W}$ Hold Time	t_{RWH}		0	–	0	–	ns
22	RS1, RS2 Setup Time	t_{RSS}		0	–	0	–	ns
23	RS1, RS2 Hold Time	t_{RSH}		0	–	0	–	ns
24	$\overline{CS}$ Setup Time	t_{CSS}		30	–	40	–	ns
25	$\overline{CS}$ "High" Level Width	t_{WCSH}		50	–	60	–	ns
26	Data Bus 3 state Recovery Time 1	t_{DBRT1}		0	–	0	–	ns
27	Read Data Access Time	t_{RDAC}		–	45	–	55	ns
28	Read Data Hold Time	t_{RDH}		5	–	5	–	ns
29	Read Data Turn Off Time	t_{RDZ}	Fig. 3	–	45	–	55	ns
30	$\overline{DTACK}$ Delay Time (Z to L)	t_{DTKZL}		–	45	–	55	ns
31	$\overline{DTACK}$ Delay Time (D to L)	t_{DTKDL}	Fig. 4	0	–	0	–	ns
32	$\overline{DTACK}$ Release Time (L to H)	t_{DTKLH}		–	45	–	55	ns
33	$\overline{CS}$ High to $\overline{DTACK}$ High Impedance	t_{CDTKZ}		–	50	–	60	ns
34	MPU Wait Time	t_{MWAT}		0	–	0	–	ns
35	Write Data Setup Time	t_{WDS}		0	–	0	–	ns
36	Write Data Hold Time	t_{WDH}		0	–	0	–	ns
38	$\overline{DACK}$, $\overline{IACK}$ Setup Time to $\overline{CS}$	t_{DICSS}		50	–	60	–	ns
39	$\overline{DACK}$, $\overline{IACK}$ Hold Time to $\overline{CS}$	t_{DICSH}		50	–	60	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

DMA Read/Write

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
41	$\overline{\text{DREQ}}$ Delay Time 1	t_{DRQD1}		–	60	–	70	ns
42	$\overline{\text{DREQ}}$ Delay Time 2	t_{DRQD2}		–	60	–	70	ns
46	$\overline{\text{DACK}}$ Setup Time	t_{DAKS}		30	–	40	–	ns
47	$\overline{\text{DACK}}$ "High" Level Width	t_{WDAKH}		50	–	60	–	ns
48	Data Bus 3 state Recovery Time 2	t_{DBRT2}		0	–	0	–	ns
49	DMA Read Data Access Time	t_{DRDAC}		–	45	–	55	ns
50	DMA Read Data Hold Time	t_{DRDH}		5	–	5	–	ns
51	DMA Read Data Turn Off Time	t_{DRDZ}		–	45	–	55	ns
52	DMA $\overline{\text{DTACK}}$ Delay Time (Z to L)	t_{DDTZL}		–	45	–	55	ns
53	DMA $\overline{\text{DTACK}}$ Delay Time (D to L)	t_{DDTDL}	Fig. 5	0	–	0	–	ns
54	DMA $\overline{\text{DTACK}}$ Release Time (L to H)	t_{DDTLH}		–	45	–	55	ns
55	$\overline{\text{DACK}}$ High to $\overline{\text{DTACK}}$ High Impedance	t_{DDTKZ}	Fig. 6	–	50	–	60	ns
56	DMA Wait Time	t_{DWAT}		0	–	0	–	ns
58	$\overline{\text{DONE}}$ Output Delay Time	t_{DND}		–	60	–	70	ns
59	$\overline{\text{DONE}}$ Output Turn Off Time (L to Z)	t_{DNLZ}		–	70	–	80	ns
60	$\overline{\text{DONE}}$ Input Pulse Width	t_{WDNL}		4	–	4	–	t_{cyc}
61	DMA Write Data Setup Time 1	t_{DWDS1}		30	–	40	–	ns
62	DMA Write Data Hold Time 1	t_{DWDH1}		0	–	0	–	ns
65	DMA Write Data Setup Time 2	t_{DWDS2}		0	–	0	–	ns
66	DMA Write Data Hold Time 2	t_{DWDH2}		0	–	0	–	ns
67	$\overline{\text{CS}}$, $\overline{\text{IACK}}$, Setup Time to $\overline{\text{DACK}}$	t_{CIDKS}		50	–	60	–	ns
68	$\overline{\text{CS}}$, $\overline{\text{IACK}}$, Hold Time to $\overline{\text{DACK}}$	t_{CIDKH}		50	–	60	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

Frame Buffer Read/Write

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
70	SCLK Delay Time 1 (L to H)	t_{SCKD1}		–	25	–	27	ns
71	SCLK Delay Time 2 (H to L)	t_{SCKD2}		–	23	–	27	ns
72	MCYC1, MCYC2 Delay Time from SCLK	t_{MYSD}		0	10	0	15	ns
73	MCYC Phase Difference	t_{MPHS}		40	60	45	80	ns
74	Memory Address Turn On Time	t_{MAZA}		0	–	0	–	ns
75	Memory Address Delay Time	t_{MAD}		0	25	0	25	ns
76	Memory Address Hold Time	t_{MAH}		0	–	0	–	ns
77	Memory Address Turn Off Time	t_{MAAZ}		0	25	0	30	ns
78	FBS Turn On Time	t_{FBSZF}		0	–	0	–	ns
79	FBS Delay Time	t_{FBSD}	Fig. 7	0	20	0	23	ns
80	FBS Hold Time	t_{FBSH}		0	–	0	–	ns
81	FBS Turn Off Time	t_{FBSFZ}	Fig. 8	0	25	0	30	ns
82	MA, FBS, Setup Time 1	t_{MAFBS1}		0	–	0	–	ns
83	$\overline{STB}$ Delay Time	t_{STBD}	Fig. 9	0	19	0	19	ns
84	MA, FBS Hold Time 2	t_{MAFBS2}		0	–	0	–	ns
85	Memory Read Data Setup Time	t_{MRDS}		30	–	30	–	ns
86	Memory Read Data Hold Time	t_{MRDH}		0	–	0	–	ns
87	Memory Write Data Turn On Time	t_{MWDZD}		0	–	0	–	ns
88	Memory Write Data Delay Time	t_{MWDD}		–	25	–	30	ns
89	Memory Write Data Setup Time	t_{MWDS}		0	–	0	–	ns
90	Memory Write Data Hold Time	t_{MWDH}		5	–	5	–	ns
91	Memory Write Data Turn Off Time	t_{MWDDZ}		–	25	–	30	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

System Interface

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
100	$\overline{\text{HALT}}$ Setup Time	t_{HLTS}		25	–	35	–	ns
101	$\overline{\text{HALT}}$ Hold Time	t_{HLTH}		0	–	0	–	ns
102	$\overline{\text{HALT}}$A Delay Time	t_{HLTD}		0	25	0	30	ns
104	$\overline{\text{AFBR}}$ Delay Time	t_{AFD}		0	20	0	20	ns
105	$\overline{\text{SBREQ}}$ Delay Time	t_{SBRD}	Fig. 10	0	20	0	30	ns
106	$\overline{\text{SBACK}}$ Setup Time	t_{SBKS}		25	–	35	–	ns
107	$\overline{\text{SBACK}}$ Hold Time	t_{SBKH}		0	–	0	–	ns
108	$\overline{\text{RETRY}}$ Setup Time	t_{RTYS}		25	–	35	–	ns
109	$\overline{\text{RETRY}}$ Hold Time	t_{RTYH}		0	–	0	–	ns
110	$\overline{\text{BERR}}$ Setup Time	t_{BERS}		25	–	35	–	ns
111	$\overline{\text{BERR}}$ Hold Time	t_{BERH}		0	–	0	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

Display Control Signals and External Synchronization

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
119	MCYC1, MCYC2 Delay Time from CLKIN	t_{MYCKD}		–	33	–	40	ns
120	$\overline{\text{HSYNC}}$ Output Delay Time from CLKIN	t_{HSDCK}		–	45	–	60	ns
121	$\overline{\text{VSYNC}}$ Delay Time from CLKIN	t_{VSDCK}		–	45	–	60	ns
122	$\overline{\text{EXVSYNC}}$ Output Delay Time from CLKIN	t_{EXVDCK}		–	33	–	40	ns
123	$\overline{\text{DISP1}}$, $\overline{\text{DISP2}}$ Output Delay Time from CLKIN	t_{DSPDCK}		–	45	–	60	ns
124	$\overline{\text{CUD}}$ Delay Time from CLKIN	t_{CUDDCK}		–	45	–	60	ns
125	$\overline{\text{EXVSYNC}}$ Output Hold Time from SCLK	t_{EXVHSK}		18	–	25	–	ns
126	$\overline{\text{EXVSYNC}}$ Output Setup Time from SCLK	t_{EXVSSK}		2	–	5	–	ns
127	$\overline{\text{EXVSYNC}}$ Input Pulse Width	t_{WEXV}	Fig. 11	24	–	24	–	t_{cyc}
128	$\overline{\text{EXVSYNC}}$ Input Hold Time from CLKIN	t_{EXVHCK}		12	–	15	–	ns
129	$\overline{\text{EXVSYNC}}$ Input Setup Time from CLKIN	t_{EXVSCK}		12	–	15	–	ns
130	$\overline{\text{EXHSYNC}}$ Input Pulse Width	t_{WEXH}	Fig. 12	24	–	24	–	t_{cyc}
131	$\overline{\text{EXHSYNC}}$ Input Hold Time from CLKIN	t_{EXHHCK}		12	–	15	–	ns
132	$\overline{\text{EXHSYNC}}$ Input Setup Time from CLKIN	t_{EXHSCK}		12	–	15	–	ns
133	$\overline{\text{HSYNC}}$ Output Delay Time from SCLK	t_{HSDSK}		0	25	0	35	ns
134	$\overline{\text{VSYNC}}$ Delay Time from SCLK	t_{VSDSK}		0	25	0	35	ns
135	$\overline{\text{DISP1}}$, $\overline{\text{DISP2}}$ Output Delay Time from SCLK	t_{DSPDSK}		0	25	0	35	ns
136	$\overline{\text{CUD}}$ Delay Time from SCLK	t_{CUDDSK}		0	25	0	35	ns
138	$\overline{\text{EXDISP}}$ Input Setup Time	t_{EXDS}		25	–	30	–	ns
139	$\overline{\text{EXDISP}}$ Input Hold Time	t_{EXDH}		0	–	0	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

Interrupts

No.*	Item	Symbol	Ref. Fig.*	20 MHz Version Min	20 MHz Version Max	16 MHz Version Min	16 MHz Version Max	Unit
140	$\overline{\text{IRQ}}$ Delay Time 1	t_{IRQ1}		–	60	–	70	ns
141	$\overline{\text{IRQ}}$ Delay Time 2	t_{IRQ2}		–	300	–	300	ns
142	$\overline{\text{IACK}}$ Setup Time	t_{IKS}		30	–	40	–	ns
144	$\overline{\text{IACK}}$ "High" Level Width	t_{WIKH}		50	–	60	–	ns
145	Data Bus 3 state Recovery Time 3	t_{DBRT3}		0	–	0	–	ns
146	Interrupt Vector Delay Time	t_{IVD}		–	45	–	55	ns
147	Interrupt Vector Hold Time	t_{IVH}		5	–	5	–	ns
148	Interrupt Vector Turn Off Time	t_{IVTZ}			45	–	55	ns
149	Interrupt $\overline{\text{DTACK}}$ Delay Time (Z to L)	t_{IDTZL}	Fig. 13	–	45	–	55	ns
150	Interrupt $\overline{\text{DTACK}}$ Delay Time (D to L)	t_{IDTDL}		0	–	0	–	ns
151	Interrupt $\overline{\text{DTACK}}$ Release Time (L to H)	t_{IDTLH}		–	45	–	55	ns
152	$\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High Impedance	t_{IDTKZ}		–	50	–	60	ns
153	Interrupt Cycle Wait Time	t_{ICWAT}		0	–	0	–	ns
156	$\overline{\text{CS}}$, $\overline{\text{DACK}}$ Setup Time to $\overline{\text{IACK}}$	t_{CDKIS}		50	–	60	–	ns
157	$\overline{\text{CS}}$, $\overline{\text{DACK}}$ Hold Time to $\overline{\text{IACK}}$	t_{CDKIH}		50	–	60	–	ns

Note: * Reference figures (see Timing Charts) indicate measurement conditions. Numbers in the left-hand column (No.) match numbers in these timing charts.

Timing Charts

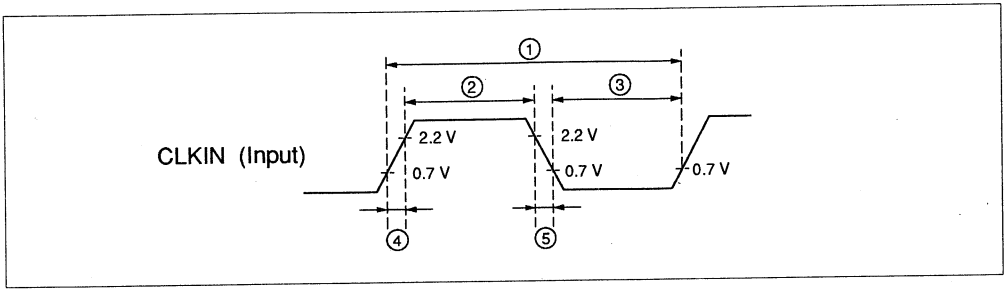


Figure 1. Clock Input (CLKIN) Waveform

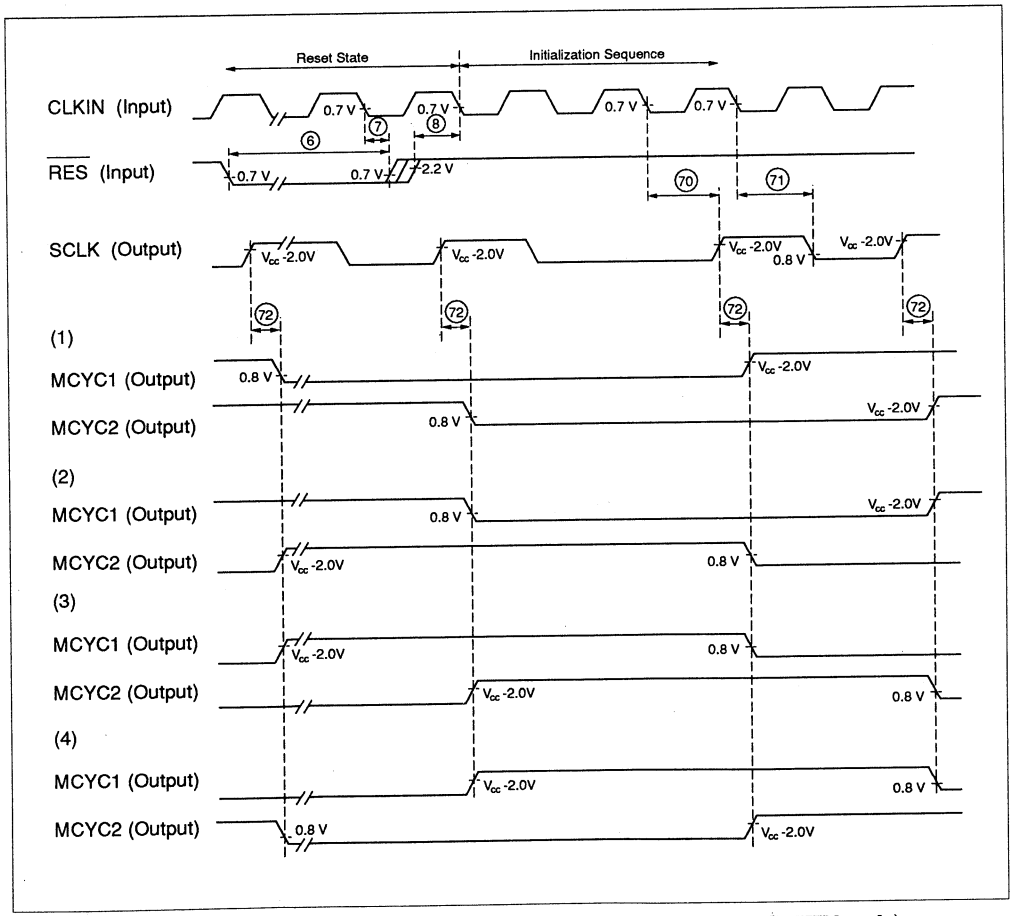


Figure 2. (a) Reset Timing (when SCLK phase is lengthened by 1 CLKIN cycle)

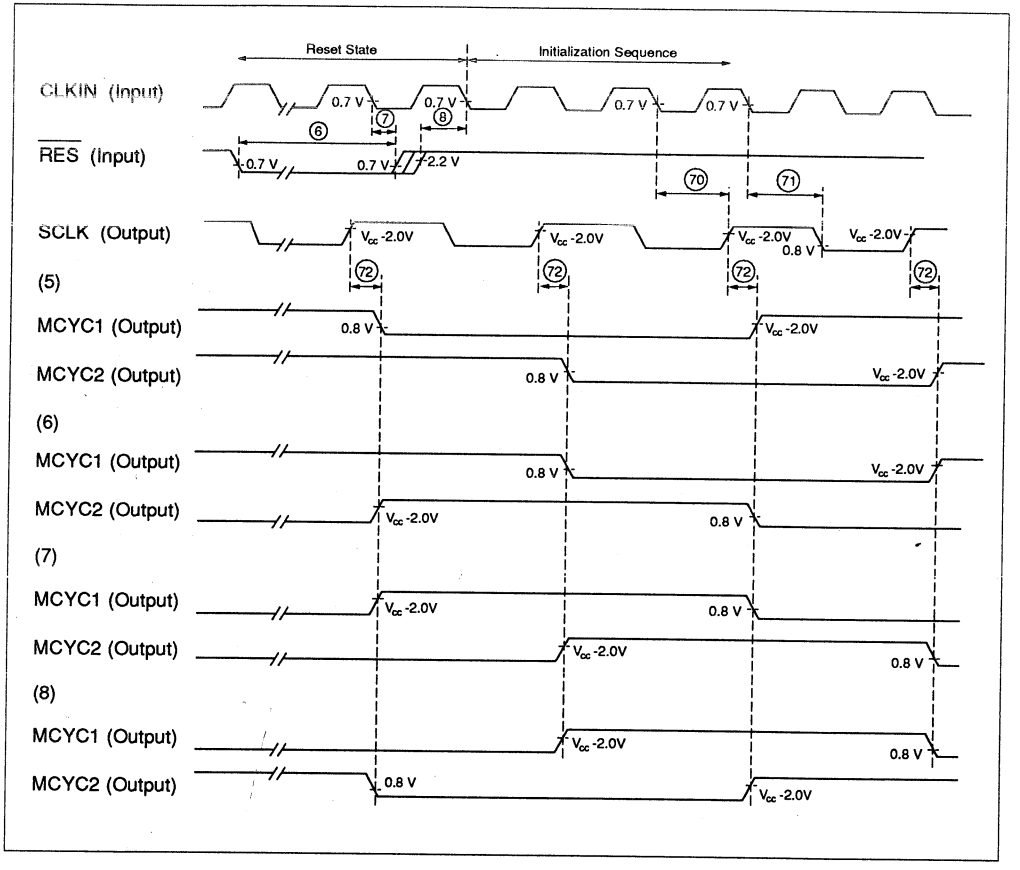


Figure 2. (b) Reset Timing (when SCLK phase is not changed)

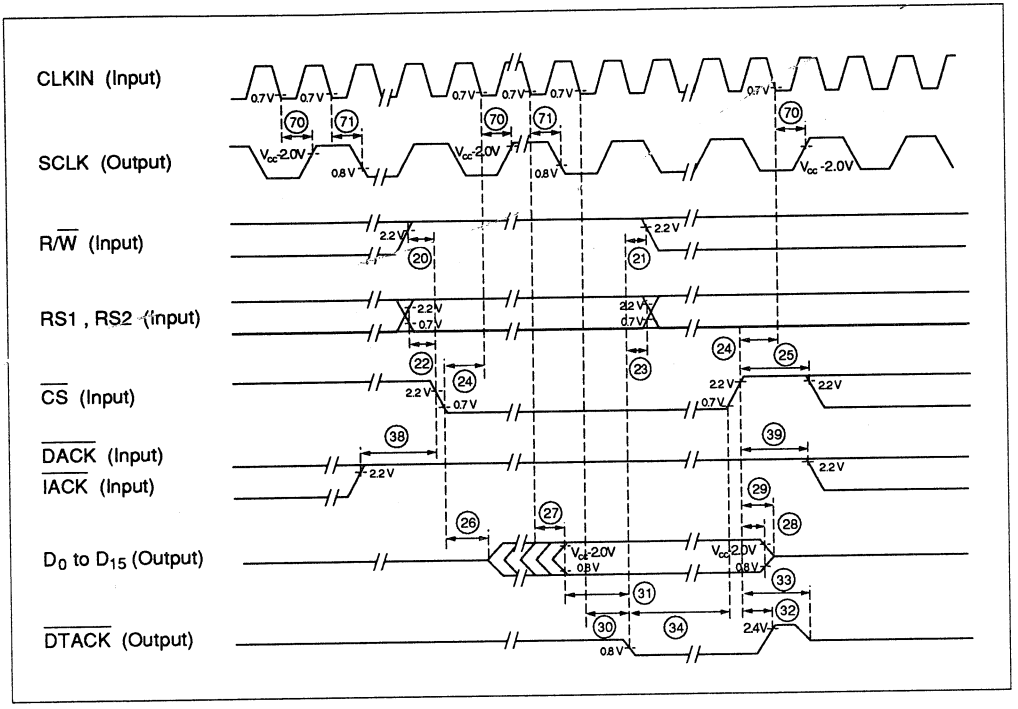


Figure 3. MPU Read Cycle Timing (MPU ← GDP)

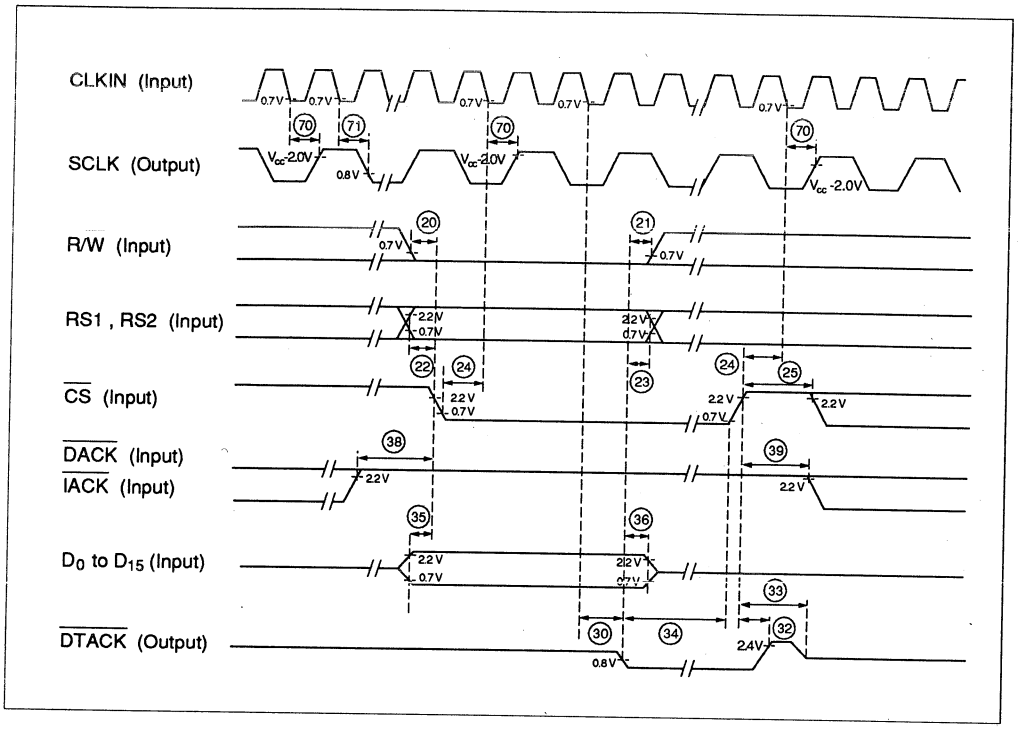


Figure 4. MPU Write Cycle Timing (MPU → GDP)

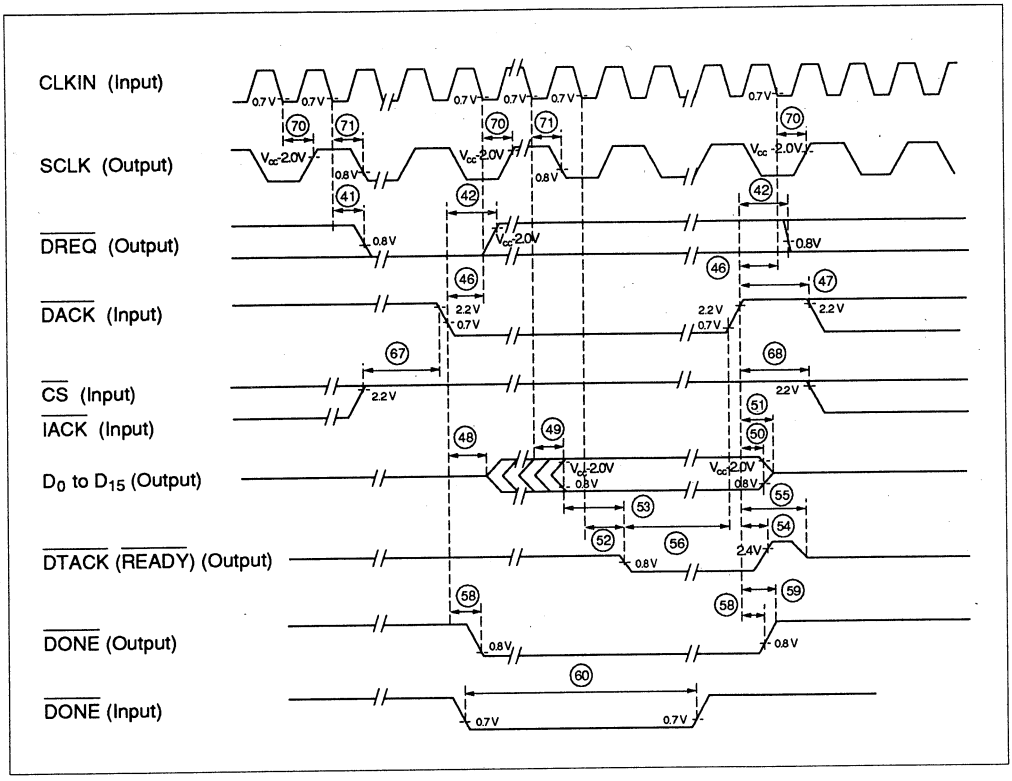


Figure 5. (a) DMA Read Cycle Timing (single address mode)

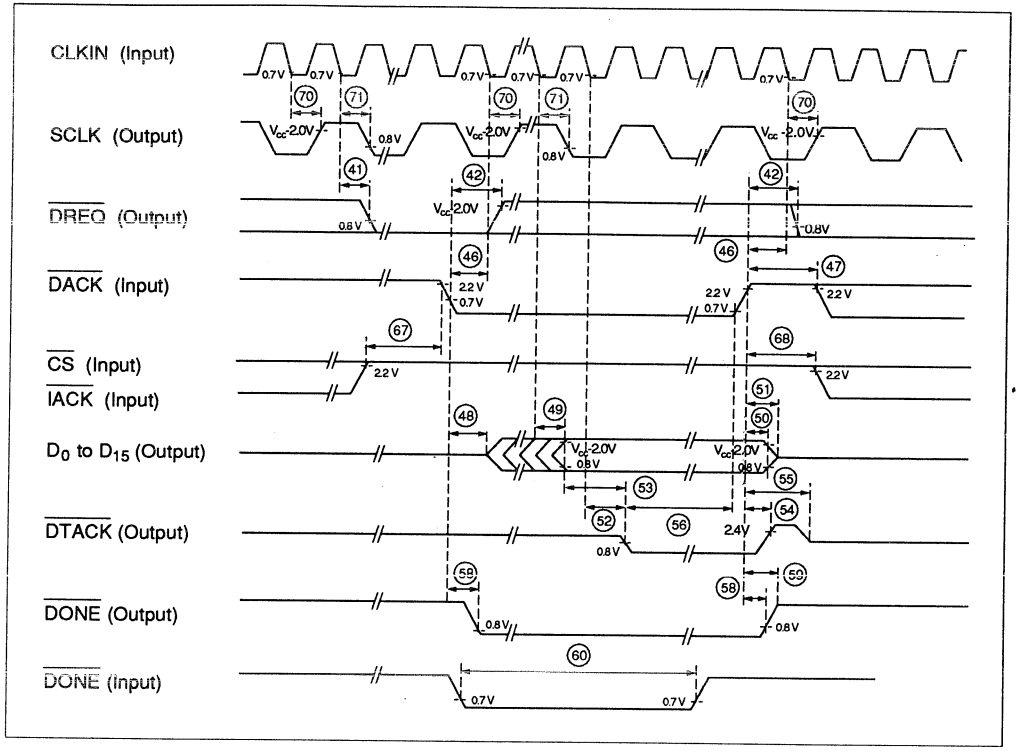


Figure 5 .(b) DMA Read Cycle Timing (dual address mode)

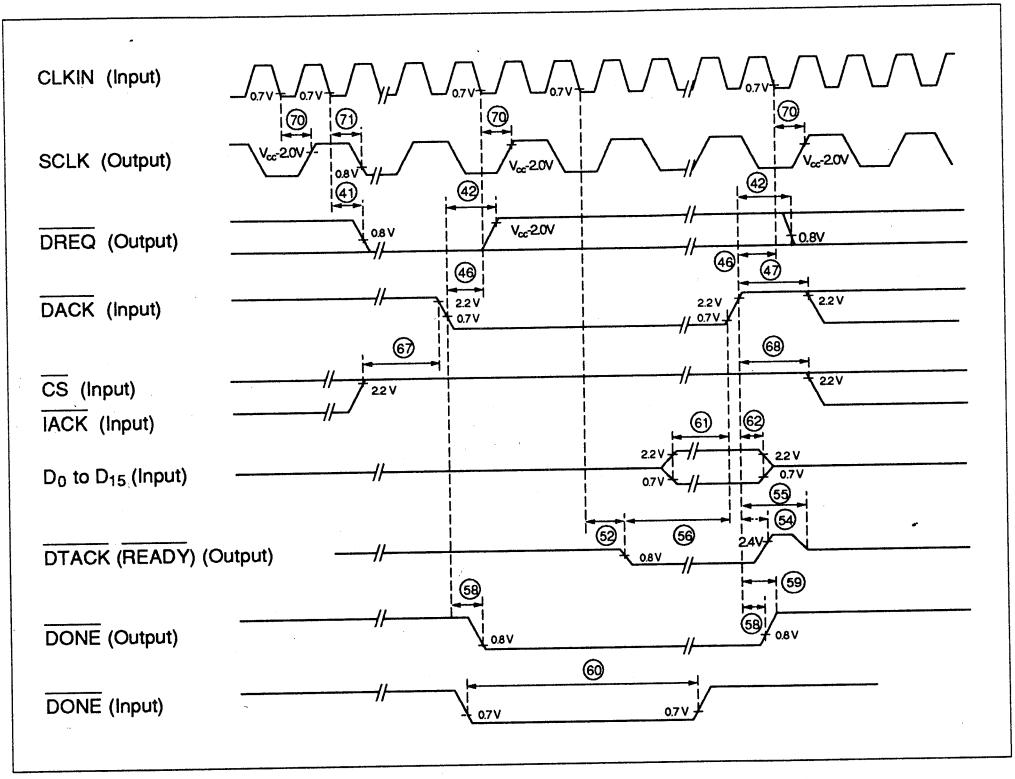


Figure 6. (a) DMA Write Cycle Timing (single address mode)

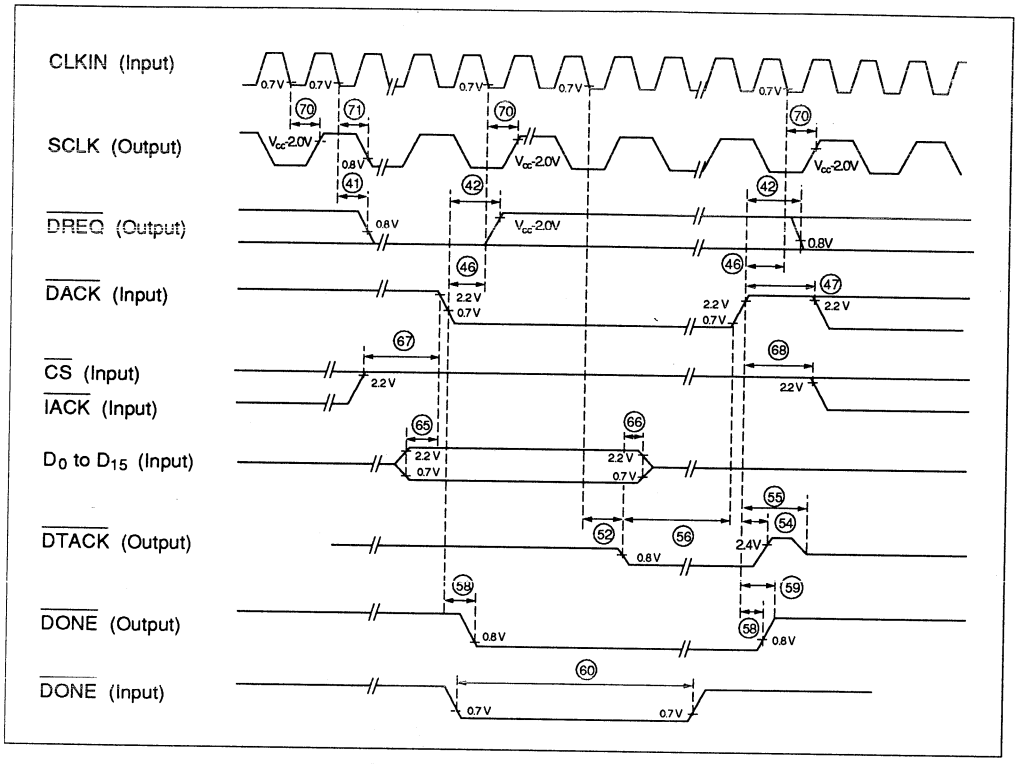


Figure 6. (b) DMA Write Cycle Timing (dual address mode)

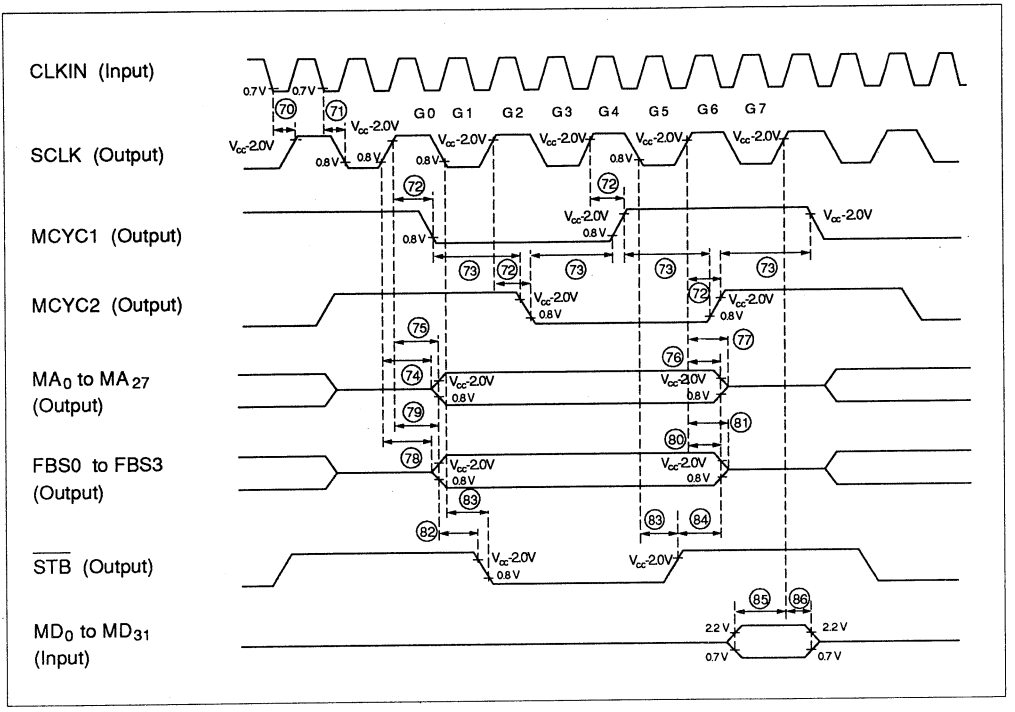


Figure 7. (a) Frame Buffer Read Cycle Timing (MA output three-state mode: MATS = "0")

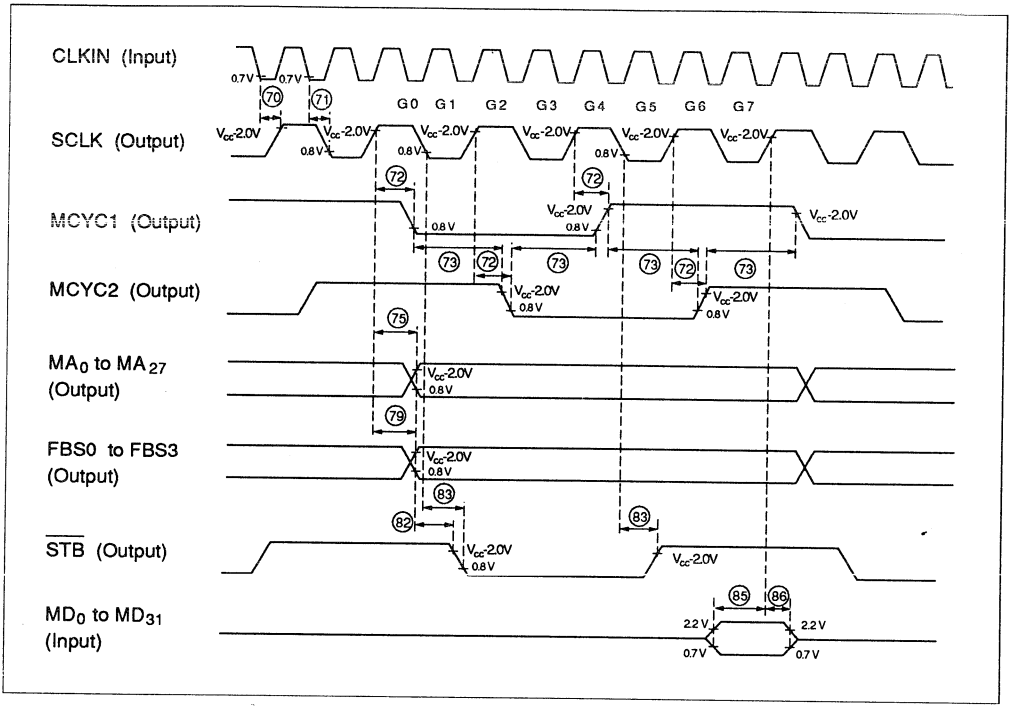


Figure 7. (b) Frame Buffer Read Cycle Timing (MA output non-three-state mode: MATS = "1")

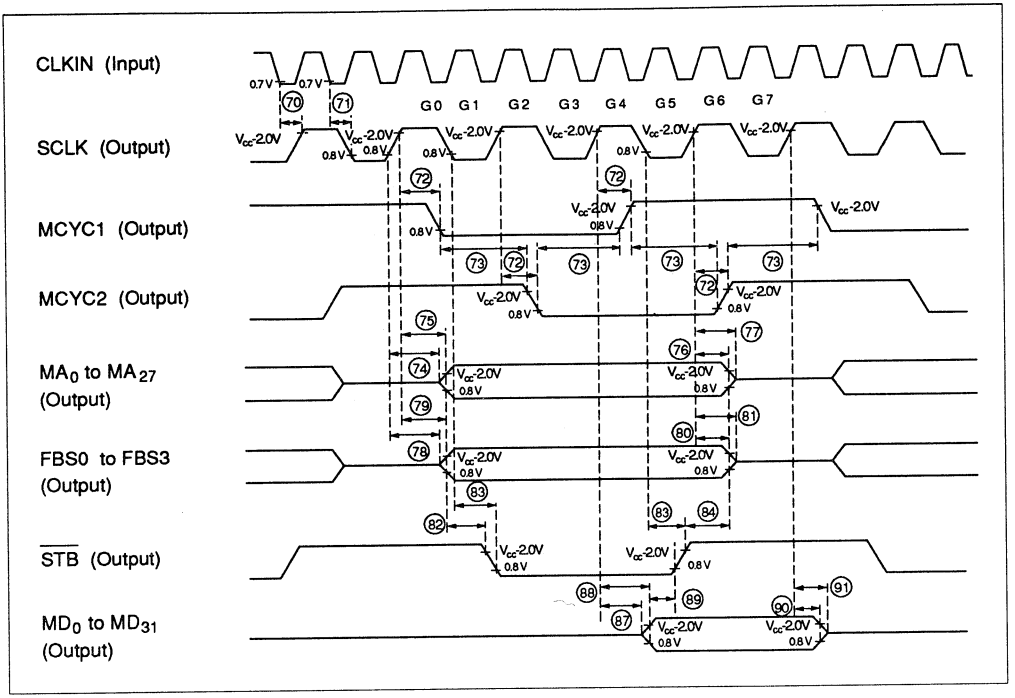


Figure 8. (a) Frame Buffer Write Cycle Timing (MA output three-state mode: MATS = "0")

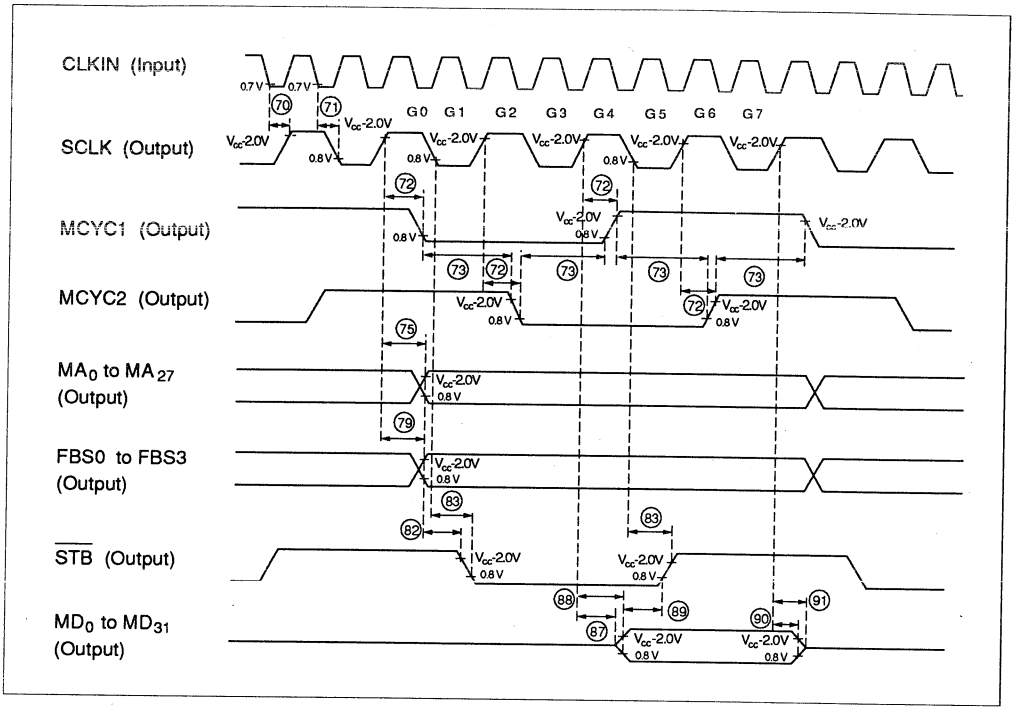


Figure 8. (b) Frame Buffer Write Cycle Timing (MA output non-three-state mode: MATS = "1")

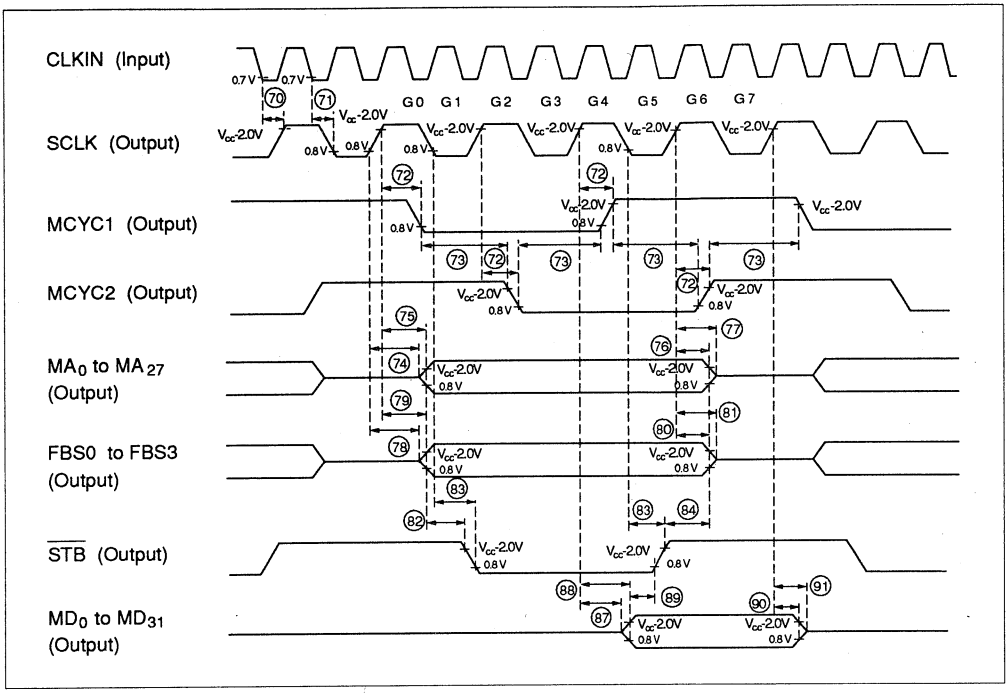


Figure 9. (a) Display Address, Refresh Address, and Attribute Control Information Output Cycle Timing (MA output three-state mode: MATS = "0")

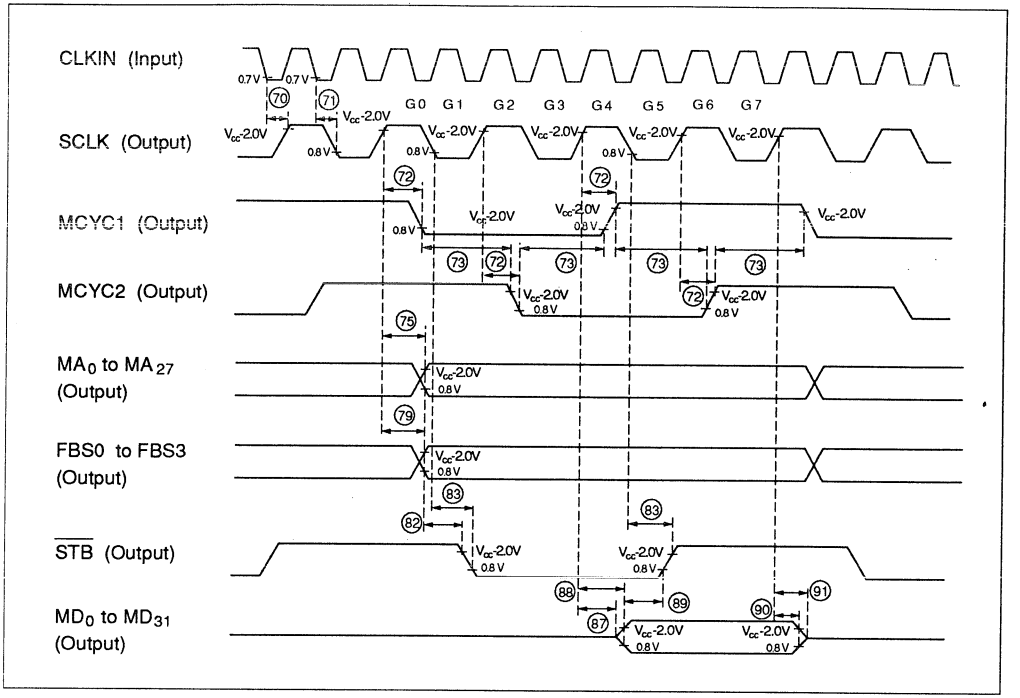


Figure 9. (b) Display Address, Refresh Address, and Attribute Control Information Output Cycle Timing (MA output non-three-state mode: MATS = "1")

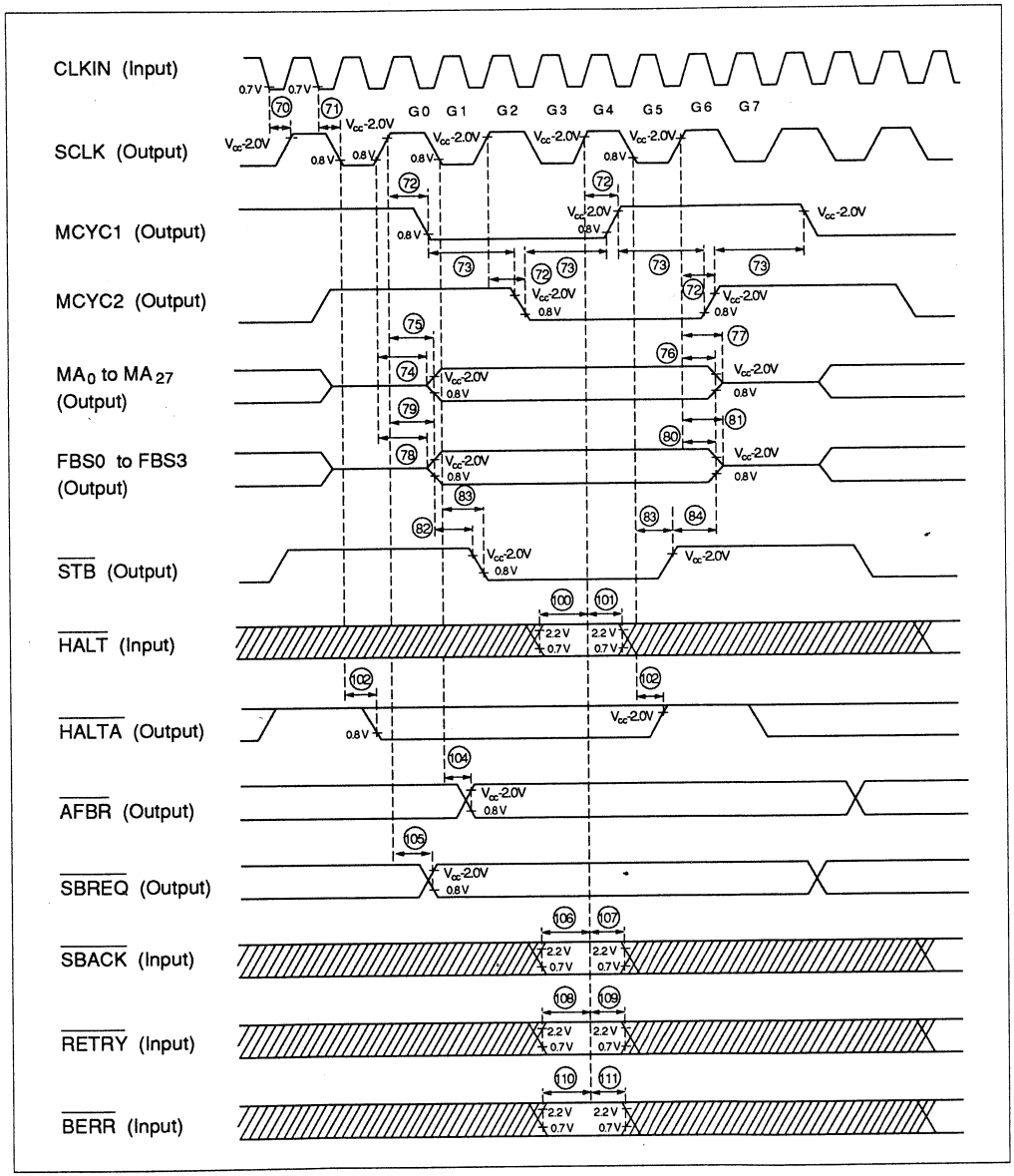


Figure 10. System Interface Timing (MA output three-state mode: MATS = "0")

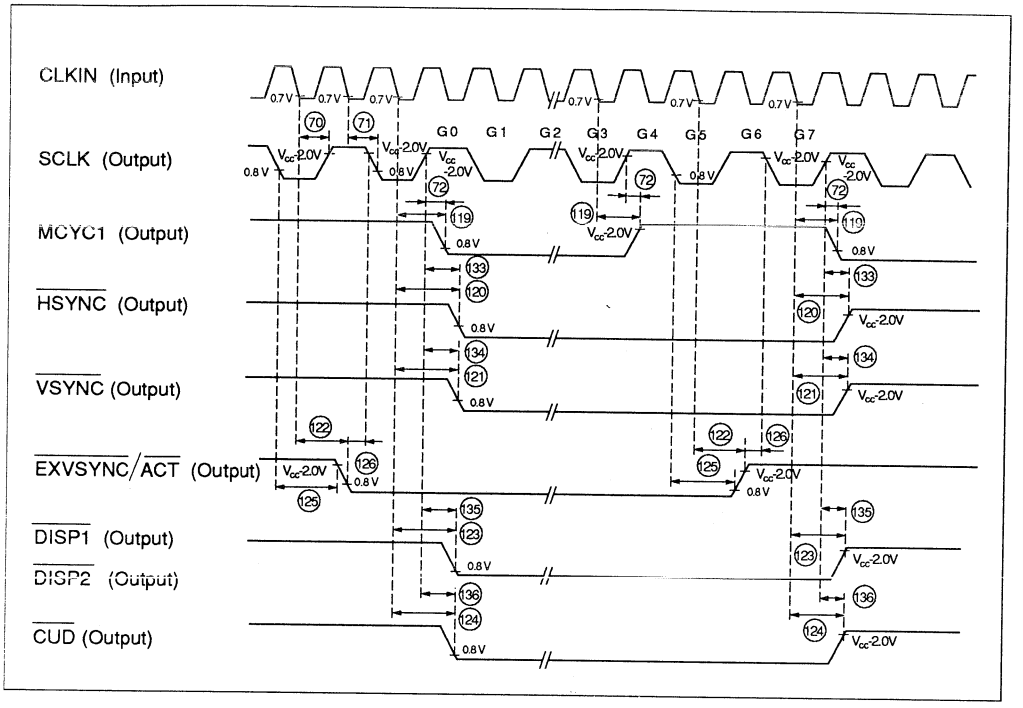


Figure 11 Display Control Signal Output Timing

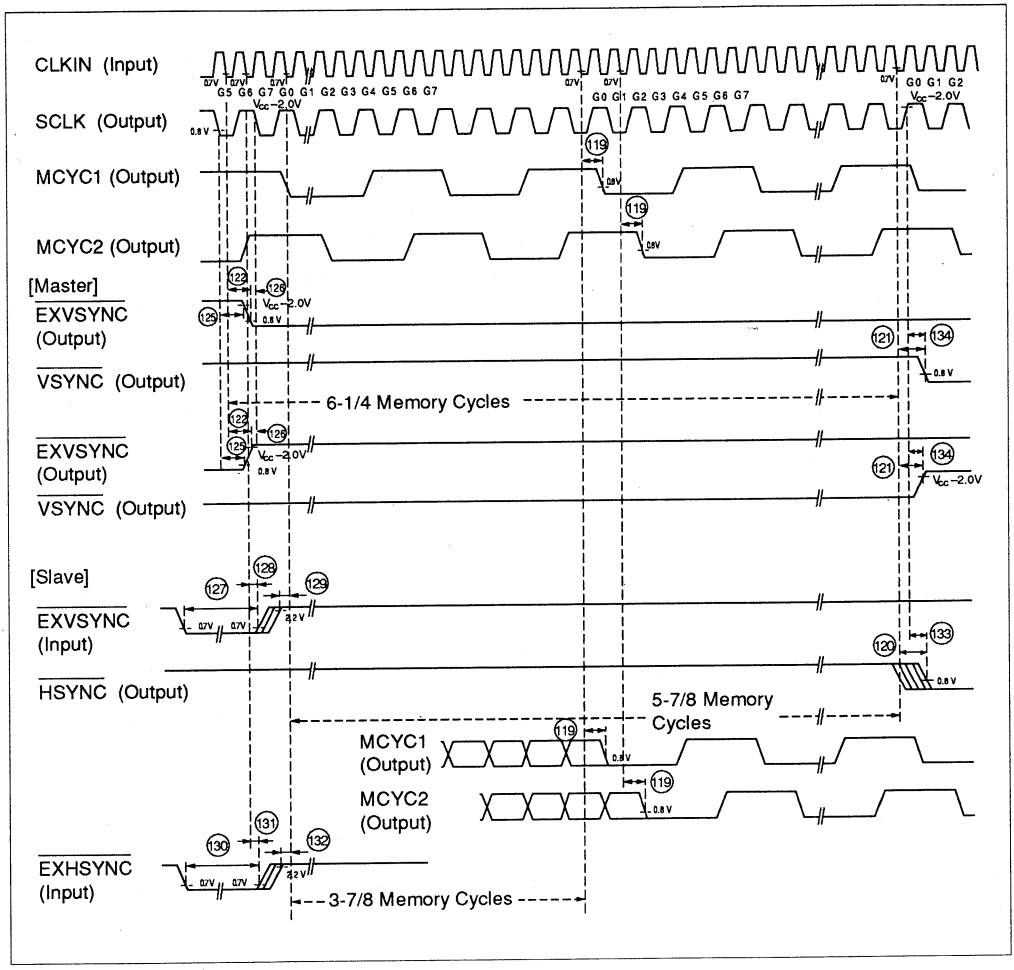


Figure 12. (a) External Synchronization Timing

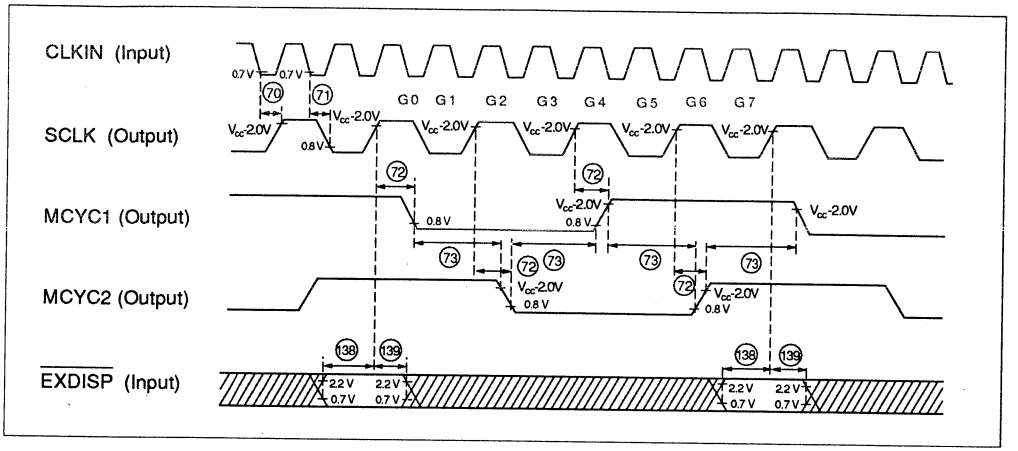


Figure 12. (b) External Synchronization Timing (laser printer mode)

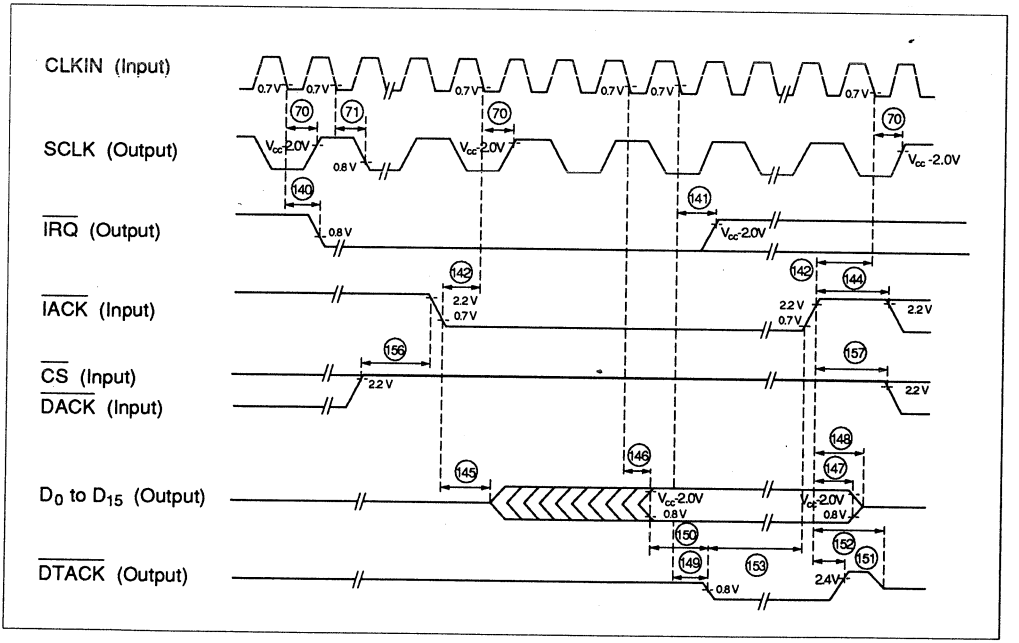


Figure 13. Interrupt Cycle Timing

HD63484

Advanced CRT Controller (ACRTC)

The advanced CRT controller (ACRTC) CMOS VLSI microcomputer peripheral device can display both graphics and characters on raster-scan displays. It is a new generation CRT controller based on bitmapped technology. It executes high-level commands, like Line, Ellipse, Paint, Pattern, and Copy, issued by the MPU in screen X-Y coordinates, and performs the address translation necessary to draw into frame memory. It can draw in up to 64k colors, on three split screens and an independent window, and perform area clipping and hitting.

The ACRTC controls a CRT in one of three modes: character only, graphics only, and multiplexed character/graphics modes. Therefore, the ACRTC has many applications, from character-only displays to large full-graphics systems.

The ACRTC reduces CPU software overhead and enhances system throughput.

Features

- High-speed graphics
  - —Drawing rate: 408 ns/pixel max (color drawing)
  - —Commands: 38 commands including 23 graphic drawing commands
    Dot, Line, Rectangle, Poly-line, Polygon, Circle, Ellipse, Paint, Copy, etc.
  - —Colors: 16 bits/word
    1, 2, 4, 8, 16 bits/pixel (5 types)
    Monochrome to 64k colors max
  - —Pattern RAM: 32 bytes
  - —Converts logical X-Y coordinates to physical address
  - —Color operation and conditional drawing
  - —Drawing area control for hardware clipping and hitting
- Large frame-memory space
  - —Maximum 2 Mbytes graphic memory and 128 kbytes character memory separate from the MPU memory
  - —Maximum resolution: 4096×4096 pixels (1 bit/pixel mode)
- CRT display control
  - —Split screens: three displays and one window
  - —Zoom: 1 to 16 times
  - —Scroll: vertical and horizontal
- Interleaved access mode for flashless display and superimposition
- External synchronization between ACRTCs or between ACRTC and external device (TV system or other controller)
- DMA interface
- Two programmable cursors
- Three scan modes
  - —Non-interlaced
  - —Interlace sync
  - —Interlace sync and video
- Interrupt request to MPU
- 256 characters/line 32 raster/line, 4096 rasters/screen
- Maximum clock frequency: 9.8 MHz
- CMOS, single +5 V power supply

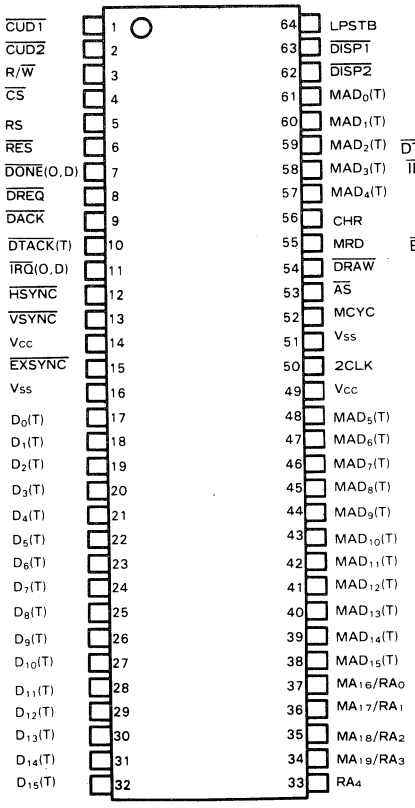
Ordering Information

Part No.	Clock Frequency (2CLK)	Package
HD63484-4	4 MHz	DC-64
HD63484-6	6 MHz	(64-pin ceramic DIP)
HD63484-8	8 MHz	
HD63484-98	9.8 MHz	
HD63484P4	4 MHz	DP-64
HD63484P6	6 MHz	(64-pin plastic DIP)
HD63484P8	8 MHz	
HD63484P98	9.8 MHz	
HD63484CP4	4 MHz	CP-68
HD63484CP6*	6 MHz	(68-pin plastic PLCC)
HD63484CP8	8 MHz	
HD63484CP98	9.8 MHz	
HD63484Y4	4 MHz	PC-68
HD63484Y6	6 MHz	(68-pin PGA)
HD63484Y8	8 MHz	
HD63484Y98	9.8 MHz	
HD63484PS4	4 MHz	DP-64S
HD63484PS6	6 MHz	(64-pin plastic shrink DIP)
HD63484PS8	8 MHz	
HD63484PS98	9.8 MHz	

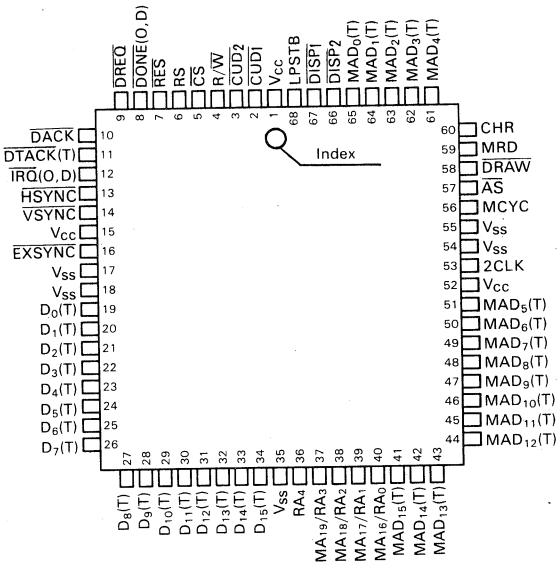
Note: Wide temperature range (−40C° to +80C°) version is available.

Pin Arrangement

HD63484, HD63484P, HD63484PS

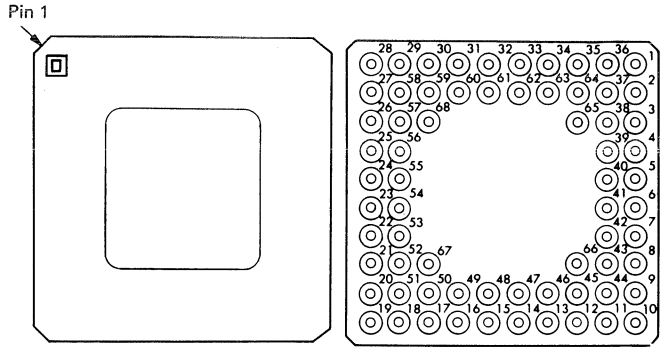


HD63484CP



O,D: Open drain
T: Three state

HD63484Y



(Top View) (Bottom View)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	MAD_{14} (T)	18	RS	35	MA_{18}/RA_2	52	$\overline{DREQ}$
2	MAD_{11} (T)	19	$\overline{DTACK}$ (T)	36	MA_{16}/RA_0	53	$\overline{HSYNC}$
3	MAD_9 (T)	20	$\overline{IRQ}$ (O,D)	37	MAD_{13} (T)	54	$\overline{EXSYNC}$
4	MAD_8 (T)	21	$\overline{VSYNC}$	38	MAD_{10} (T)	55	D_0 (T)
5	MAD_6 (T)	22	V_{CC}	39	MAD_7 (T)	56	D_4 (T)
6	V_{CC}	23	V_{SS}	40	MAD_5 (T)	57	D_3 (T)
7	V_{SS}	24	V_{SS}	41	2CLK	58	D_6 (T)
8	V_{SS}	25	D_1 (T)	42	MCYC	59	D_9 (T)
9	$\overline{AS}$	26	D_2 (T)	43	$\overline{DRAW}$	60	D_{11} (T)
10	MRD	27	D_5 (T)	44	MAD_4 (T)	61	D_{14} (T)
11	MAD_3 (T)	28	D_8 (T)	45	MAD_2 (T)	62	RA_4
12	MAD_1 (T)	29	D_{10} (T)	46	MAD_0 (T)	63	MA_{17}/RA_1
13	$\overline{DISP_2}$	30	D_{12} (T)	47	$\overline{DISP_1}$	64	MAD_{15} (T)
14	LPSTB	31	D_{13} (T)	48	$\overline{CUD_1}$	65	MAD_{12} (T)
15	V_{CC}	32	D_{15} (T)	49	$\overline{CS}$	66	CHR
16	$\overline{CUD_2}$	33	V_{SS}	50	$\overline{RES}$	67	$\overline{DACK}$
17	R/$\overline{W}$	34	MA_{19}/RA_3	51	$\overline{DONE}$ (O,D)	68	D_7

Pin Description

Group	Mnemonic	Pin Number DIP	PLCC	PGA	I/O	Function
MPU Interface	$\overline{RES}$	6	7	50	I	ACRTC reset
	D_0-D_{15}*	17-32	19-34	25-32 55-61 68	I/O	Data bus (three state)
	R/$\overline{W}$	3	4	17	I	Read/write strobe
	$\overline{CS}$	4	5	49	I	Chip select
	RS	5	6	18	I	Register select
	$\overline{DTACK}$	10	11	19	O	Data transfer acknowledge (three state)
	$\overline{IRQ}$	11	12	20	O	Interrupt request (open drain)
DMAC Interface	$\overline{DREQ}$	8	9	52	O	DMA request
	$\overline{DACK}$	9	10	67	I	DMA acknowledge
	$\overline{DONE}$	7	8	51	I/O	DMA done (open drain)
CRT Interface	2CLK	50	53	41	I	ACRTC clock
	MAD_0-MAD_{15}*	61-57, 48-38	65-61, 51-41	1-5, 11,12 37-40,44-46, 64, 65	I/O	Multiplexed frame buffer address/data bus
	$\overline{AS}$	53	57	9	O	Adress strobe
	MA_{16}/RA_0-* MA_{19}/RA_3	37-34	40-37	34-36	O	Higher-order address bits/ character screen raster address
	RA_4	33	36	62	O	High-order character screen raster address bit
	CHR	56	60	66	O	Graphic or character screen access
	MCYC	52	56	42	O	Frame buffer memory access timing signal
	MRD	55	59	10	O	Frame buffer memory read
	$\overline{DRAW}$	54	58	43	O	Draw/refresh signal
	$\overline{DISP1}$, $\overline{DISP2}$	63, 62	67, 66	47, 13	O	Display enable
	$\overline{CUD1}$, $\overline{CUD2}$	1,2	2,3	48,16		Cursor display
	$\overline{VSYNC}$	13	14	21	O	CRT vertical sync pulse
	$\overline{HSYNC}$	12	13	53		CRT horizontal sync pulse
	$\overline{EXSYNC}$	15	16	54	I/O	External sync
	LPSTB	64	68	14	I	Lightpen strobe
Power Supply	V_{CC}	14, 49	1, 15, 52	6, 15, 22		+5 V
	V_{SS}	16, 51	17, 18, 35, 54, 55	7, 8, 23 24, 33		Ground

*: PGA pin numbers don't correspond to D_0-D_{15}, MAD_0-MAD_{15}, MA_{16}/RA_0-MA_{19}/RA_3. Please refer to the pin arrangement.

MPU Interface

$\overline{RES}$ (Reset): $\overline{RES}$ is the MPU hardware reset.

D_0-D_{15} (Data Bus): D_0-D_{15} are the bidirectional data bus to/from the host MPU or DMAC. D_0-D_7 are used in 8-bit data bus mode.

R/W (Read/Write): R/$\overline{W}$ input controls the direction of host/ACRTC transfers.

$\overline{CS}$ (Chip Select): $\overline{CS}$ input enables transfers between the host and the ACRTC.

RS(Register Select): RS input selects the ACRTC register to be accessed. It is usually connected to the least significant bit of the host address bus.

$\overline{DTACK}$ (Data Transfer Acknowledge): $\overline{DTACK}$ output provides asynchronous bus cycle timing. It is compatible with the HD68000 MPU $\overline{DTACK}$ output.

$\overline{IRQ}$ (Interrupt Request): $\overline{IRQ}$ output generates interrupt service requests to the host MPU.

DMAC Interface

$\overline{DREQ}$ (DMA Acknowledge): $\overline{DACK}$ receives DMA acknowledge timing from the host DMAC.

$\overline{DONE}$ (DMA Done): $\overline{DONE}$ terminates DMA transfer. It is compatible with the HD68450 DMAC DONE signal.

CRT Interface

2CLK (Dot Clock): 2CLK is the basic ACRTC operating clock, twice the frequency of the dot clock.

MAD_0-MAD_{15} (Frame Memory Address/ Data Bus): MAD_0-MAD_{15} are the multiplexed frame buffer address/data bus.

AS (Address Strobe): The $\overline{AS}$ output demultiplexes the address/data bus (MAD_0-MAD_{15}).

MA_{16}/RA_0-MA_{19}/RA_3 (Memory Address/ Raster Address): MA_{16}/RA_0-MA_{19}/RA_3 are the upper bits of the graphics screen address multiplexed with the lower bits of the character screen raster address.

RA_4 (Raster Address): RA_4 is the high bit of the character screen raster address (up to 32 rasters).

CHR (Character): CHR output indicates whether a graphic or character screen is being accessed.

MCYC (Memory Cycle): MCYC is the frame buffer memory access timing output, one-half the frequency of 2CLK.

MRD (Memory Read): MRD output controls the frame buffer data bus direction.

$\overline{DRAW}$ (Draw): $\overline{DRAW}$ output differentiates between drawing and CRT display refresh cycles.

$\overline{DISP1}$, $\overline{DISP2}$ (Display 1, 2): The $\overline{DISP1}$ and $\overline{DISP2}$ programmable display enable outputs can enable, disable, and blank logical screens.

$\overline{CUD1}$, $\overline{CUD2}$ (Cursor Display 1, 2): $\overline{CUD1}$ and $\overline{CUD2}$ outputs provides cursor timing programmed by ACRTC parameters such as cursor definition, cursor mode, cursor address, etc.

$\overline{VSYNC}$ (Vertical Sync): $\overline{VSYNC}$ outputs the CRT vertical synchronization pulse.

$\overline{HSYNC}$ (Horizontal Sync): $\overline{HSYNC}$ outputs the CRT horizontal synchronization pulse.

$\overline{EXSYNC}$ (External Sync): $\overline{EXSYNC}$ allows synchronization between multiple ACRTCs and other video signal generators.

LPSTB (Lightpen Strobe): LPSTB is the lightpen input.

Block Diagrams

ACRTC Functions

The ACRTC consists of 5 major functional blocks (figure 1). They operate in parallel to achieve maximum performance.

MPU Interface: The MPU interface interfaces asynchronously with the host MPU. Its functions include programmable interrupts handling, and DMA handshaking control.

CRT Interface: The CRT interface manages the frame buffer bus and the CRT timing input and output control signals. It also selects display refresh or drawing address outputs.

Drawing Processor: The drawing processor interprets commands and command parameters issued by the host bus (MPU and/or DMAC) and performs drawing operations on the frame buffer memory. It executes ACRTC drawing algorithms and converts logical X-Y addresses to physical frame buffer addresses.

It communicates with the host bus via separate 16-byte read and write FIFOs.

Display Processor: The display processor manages frame buffer refresh addressing based on the user-specified display screen organization. It combines and displays as many as 4 independent screen segments (3 horizontal split screens and 1 window) using an internal high-speed address calculation unit. It controls display refresh outputs in graphic (physical frame buffer address) or character (physical refresh memory address + row address) modes.

Timing Processor: The timing processor generates the CRT synchronization signals and signals used internally by the ACRTC.

Registers: The ACRTC registers that are visible to software are partitioned in the same way. They reside in the internal processor appropriate to their function. The registers in the display and timing processors are loaded with the basic display parameters during system initialization. During operation, the host communicates primarily with the ACRTC's drawing processor via the on-chip FIFOs.

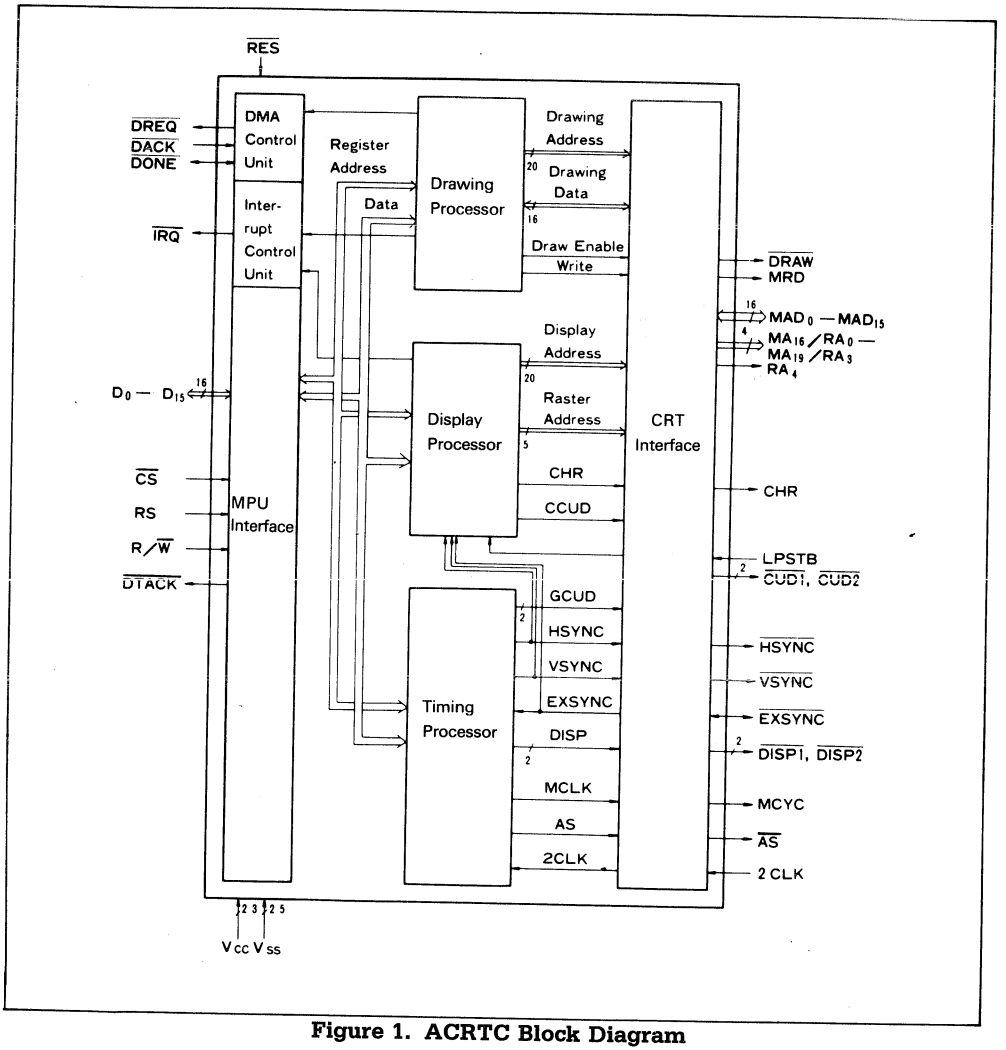


Figure 1. ACRTC Block Diagram

System Configuration

Current CRT controllers provide a single bus interface to the frame buffer that must be shared with the host MPU. However, refreshing large frame buffers, and accessing the frame buffer for drawing operations can quickly saturate the shared bus.

As shown in figure 2, the ACRTC uses separate host MPU and frame buffer interfaces. This allows the ACRTC full access to the frame buffer for display refresh and drawing operations and minimizes the ACRTC's use of the MPU system bus. A related benefit is that a large frame buffer (2 Mbyte for each ACRTC) can be used, even if the host MPU has a smaller address space or segment size restriction.

The ACRTC can use an external DMA controller. A DMA controller increases system throughput when many commands, parameters, and data must be transferred to the ACRTC. Advanced DMAC features, such as the HD68450 "chaining" modes can be used to develop powerful graphics system architectures.

However, more cost-sensitive or less performance-sensitive applications do not require a DMAC. The interface to the ACRTC can be handled under MPU software control.

While both ACRTC bus interfaces (host MPU and frame buffer) are 16 bits wide, the ACRTC also offers an 8-bit MPU mode for easy connection to popular 8-bit busses.

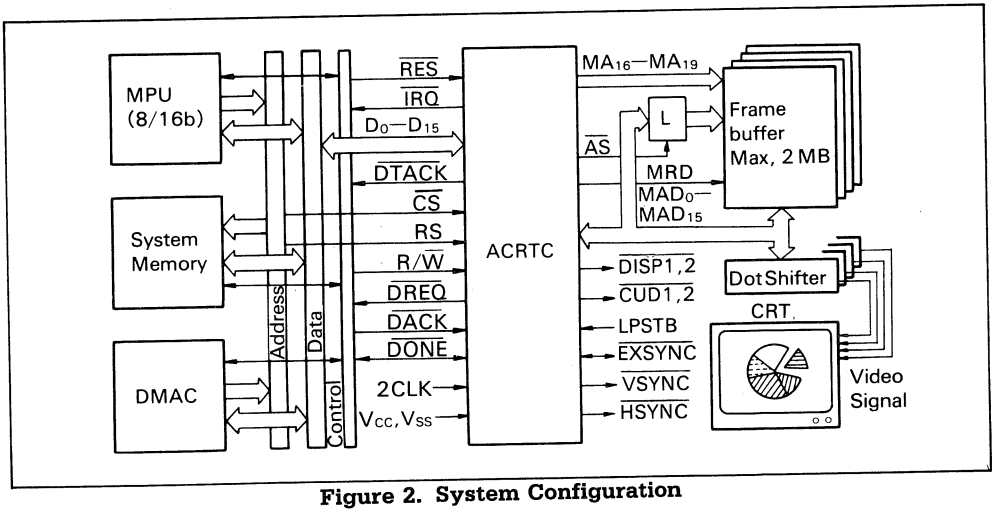


Figure 2. System Configuration

Programming Model

Address Space

The ACRTC allows the host to issue commands in logical X-Y coordinates. The ACRTC converts these physical linear word addresses with bit field offsets in the frame buffer. Figure 3 shows the relationship between the logical X-Y screen address and the frame buffer memory, which is organized as sequential 16-bit words. The host may specify logical pixels of 1, 2, 4, 8, or 16 physical bits in the frame buffer. The system in figure 3 uses 4-bit logical pixels, allowing 16 colors or tones to be selected.

Up to four logical screens (upper, base, lower, and window) are mapped onto the ACRTC physical address space. The host specifies a logical screen physical start address, logical screen physical memory width (memory words per raster), logical pixel physical memory width (bit per pixel), and the logical origin physical address. Then the ACRTC converts logical pixel X-Y addresses issued by the host MPU or the ACRTC drawing processor to physical frame buffer addresses. The ACRTC also performs bit extraction and masking to map logical pixel operations (for example, 4 bits), to 16-bit word frame buffer addresses.

Registers

The ACRTC has over 200 bytes of accessible registers (figures 4, 5 and table 1). They are organized as hardware access, direct access, and FIFO access.

Hardware Access: The ACRTC is connected to the host MPU as a standard memory-mapped peripheral that occupies two word locations of the host's address space. The RS (register select) pin selects one of these two locations. When RS = 0 (low), read operations access the status register, and write operations access the address register.

The status register summarizes the ACRTC state. It monitors the overall state of the ACRTC for the host MPU.

When the MPU wants to access a direct access register, it puts the register's address

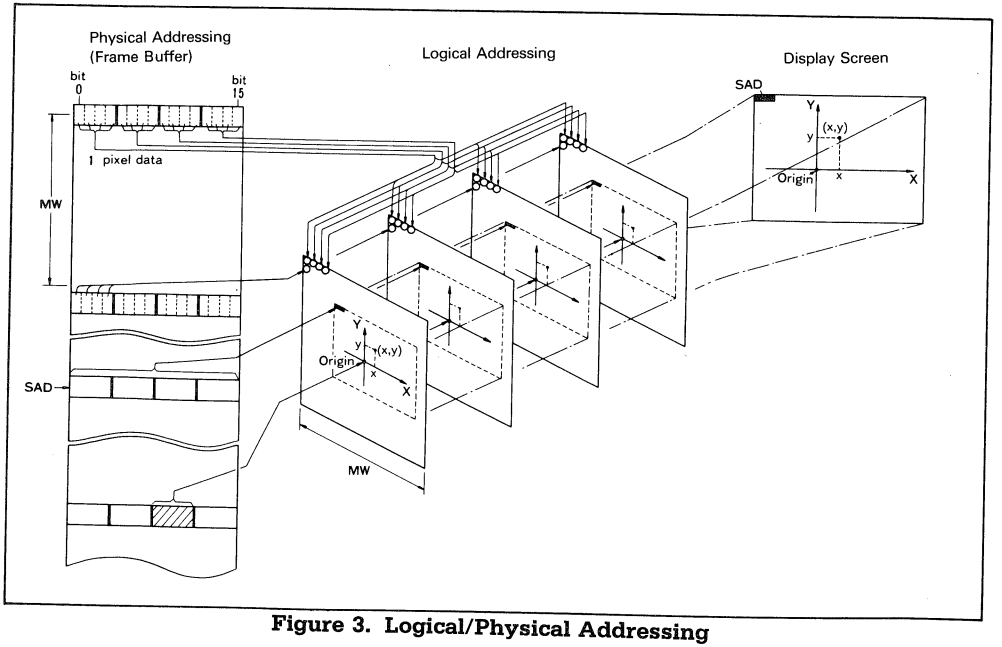


Figure 3. Logical/Physical Addressing

into the ACRTC address register.

Direct Access: The MPU accesses the direct access registers by first loading the register address into the address register. Then, when the MPU accesses the ACRTC with RS = 1 (high), the chosen register is accessed.

The FIFO entry register enables the MPU to access FIFO access registers using the ACRTC read and write FIFOs.

The command control register controls overall ACRTC operations, such as aborting or pausing commands, defining DMA protocols, and enabling/disabling interrupt sources.

The operation mode register defines basic parameters of ACRTC operation, such as frame buffer access mode, display or drawing priority, cursor and display timing skew factors, and raster scan mode.

The display control register independently enables and disables the four ACRTC logical address screens (upper, base, lower, and window). It also contains 8 user-defined video attribute bits.

The timing control RAM registers define ACRTC timing, including timing specifications for CRT control signals ($\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, etc), logical display screen size and display period, and blink period.

The display control RAM contains registers which define logical screen display parameters, such as start address, raster address, and memory width. It also includes the cursor(s) definition, zoom factor, and lightpen registers.

FIFO Access: For high-performance drawing, key drawing processor registers are coupled to the host MPU via the ACRTC's 16-byte read and write FIFOs.

ACRTC commands are sent from the MPU via the write FIFO to the command register. As the ACRTC completes a command, the next command is automaticaly fetched from the write FIFO and put into the command register.

The pattern RAM defines drawing and painting patterns. It is accessed with the ACRTC's Read Pattern RAM (RPTN) and Write Pattern RAM (WPTN) register access commands.

The drawing parameter registers define detailed parameters of the drawing process, such as color data, area control (hitting/clipping), and pattern RAM pointers. The drawing parameter registers are accessed using the ACRTC's Read Parameter Register (RPR) and Write Parameter Register (WPR) commands.

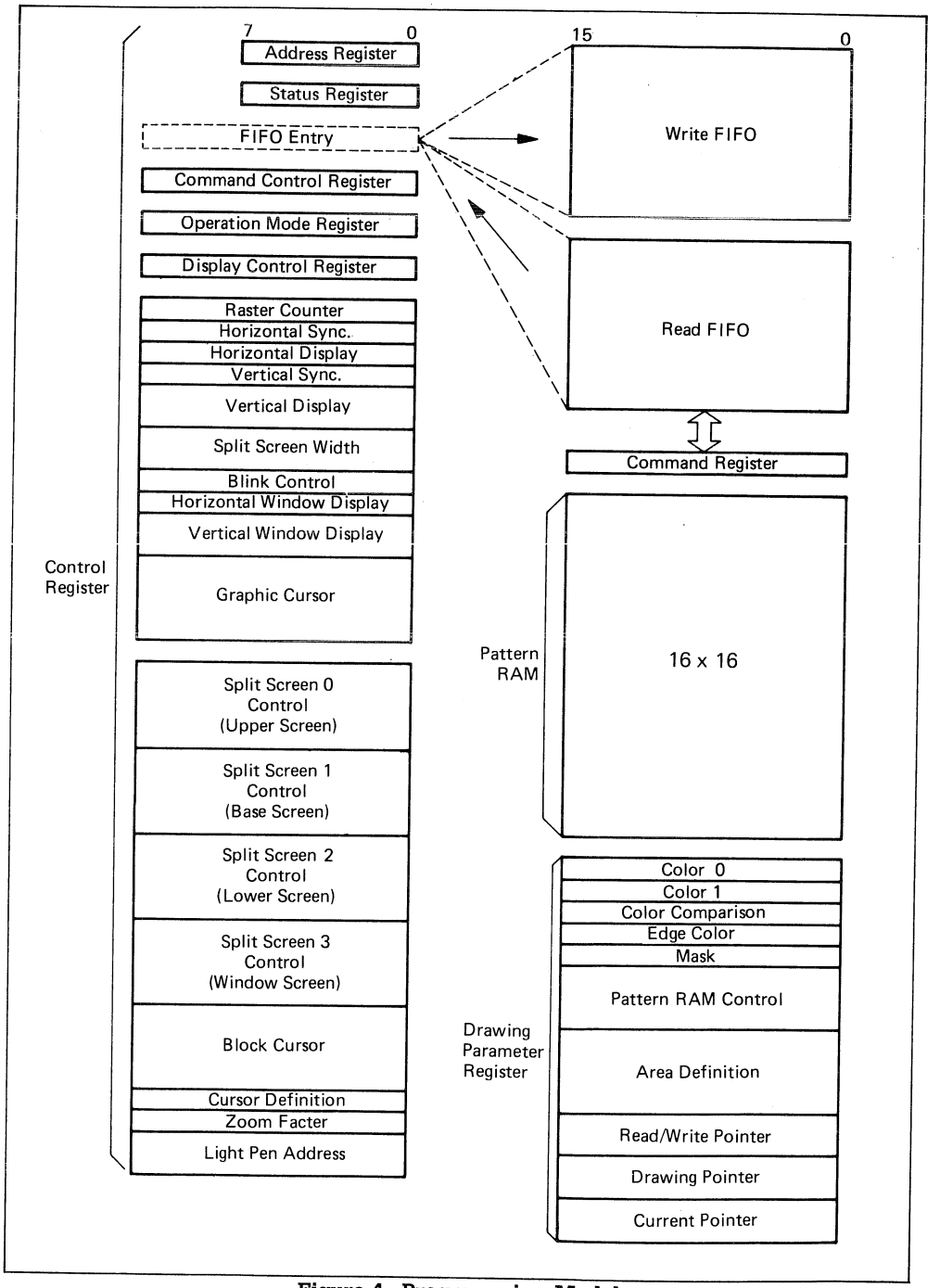


Figure 4. Programming Model

Data High								Data Low							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Address Register — Register No.=AR — $\overline{CS}$=0, RS=0, R/$\overline{W}$=0

—	Address

Status Register — Register No.=AR — $\overline{CS}$=0, RS=0, R/$\overline{W}$=0

	CER	ARD	CED	LPD	RFF	RFR	WFR	WFE

FIFO Entry (FE) — Register No.=r00 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

FIFO Entry

Command Control (CCR) — Register No.=r02 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

ABT	PSE	DDM	CDM	DRC	GBM	CRE	ARE	CEE	LPE	RFE	RRE	WRE	WEE

Operation Mode (OMR) — Register No.=r04 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

M/S	STR	ACP	WSS	$\overline{CSK}$	DSK	RAM	GAI	ACM	RSM

Display Control (DCR) — Register No.=r06 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

DSP	SE1	SE0	SE2	SE3	ATR

(Undefined) — Register No.=r08-R7E — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—

Raster Count (RCR) — Register No.=r80 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=1

—	RC

Horizontal Sync (HSR) — Register No.=r82 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

HC	—	HSW

Horizontal Display (HDR) — Register No.=r84 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

HDS	HDW

Vertical Sync (VSR) — Register No.=r86 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	VC

Vertical Display (VDR) — Register No.=r88 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

VDS	—	VSW

Figure 5. Hardware Access and Direct Access Registers

Split Screen Width (SSW) Register No.=8A, 8C, 8E $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	SP1
—	SP0
—	SP2

Blink Control (BCR) Register No.=r90 $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

BON1	BOFF1	BON2	BOFF2

Horizontal Window Display (HWR) Register No.=r92 $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

HWS	HWW

Vertical Window Display (VDR) Register No.=r94, 96 $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	VWS
—	VWW

Graphic Cursor (GCR) Register No.=r98, 9A, 9C $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

CXE	CXS
—	CYS
—	CYE

(Underfined) Register No.=r9E-BE $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—

Upper Screen

Raster Address 0 (RAR0) Register No.=rC0 $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	LRA0	—	FRA0

Memory Width 0 (MWR0) Register No.=C2 $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

CHR	—	MW0

Start Address 0 (SAR0) Register No.=rC4, C6 $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	SDA0	—	SA0H/SRA0
SA0L			

Figure 5. Hardware Access and Direct Access Registers (cont)

Base Screen

Raster Address 1 (RAR1) — Register No.=rC8 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	LRA1	—	FRA1

Memory Width 1 (MWR1) — Register No.=rCA — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

CHR	—	MW1

Start Address 1 (SAR1) — Register No.=rCC, rCE — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	SDA1	—	SA1H/SRA1
SA1L			

Lower Screen

Raster Address 2 (RAR2) — Register No.=rD0 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	LRA2	—	FRA2

Memory Width 0 (MWR2) — Register No.=rD2 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

CHR	—	MW2

Start Address 0 (SAR2) — Register No.=rD4, D6 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	SDA2	—	SA2H/SRA2
SA2L			

Window Screen

Raster Address 3 (RAR3) — Register No.=rD8 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	LRA3	—	FRA3

Memory Width 0 (MWR3) — Register No.=rDA — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

CHR	—	MW3

Start Address 0 (SAR3) — Register No.=rDC, rDE — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	SDA3	—	SA3H/SRA3
SA3L			

Block Cursor 1 (BCUR1) — Register No.=rE0, rE2 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

BCW1	$\overline{BCS}$R1	—	BCER1
BCA1			

Block Cursor 2 (BCUR2) — Register No.=rE4, rE6 — $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

BCW2	$\overline{BCS}$R2	—	BCER2
BCA2			

Figure 5. Hardware Access and Direct Access Registers (cont)

Cursor Definition (CDR) Register No.=rE8 $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

CM	CON1	COFF1	—	CON2	COFF2

Zoom Factor (ZFR) Register No.=rEA $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

HZF	VZF	—

Lightpen Address (LPAR) Register No.=rEC, rEE $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—	CHR	—	LPAH
LPAL			

(Underfined) Register No.=rF0-rFE $\overline{CS}$=0, RS=1, R/$\overline{W}$=0/1

—

ABT: Abort
ACM:Access Mode
ACP: Access Priority
Address: Control Register number
ARD: Area Detect
ARE: Area Detect Interrupt Enable
ATR: Attribute Control
CDM: Command DMA Mode
CED: Command End
CEE: Command End Interrupt Enable
CER: Command Error
CRE: Command Error Interrupt Enable
CSK: Cursor Display Skew
DDM: Data DMA Mode
DRC: DMA Request Control
DSK: $\overline{DISP}$ Skew
DSP: $\overline{DISP}$ Signal Control
FE: FIFO Entry
GAI: Graphic Address Increment Mode
GBM: Graphic Bit Mode
HC: Horizontal Cycle
HDS: Horizontal Display Start
HDW: Horizontal Display Width
HSW: Horizontal Sync Width
LPD: Light Pen Strobe Detect
LPE: Light Pen Strobe Interrupt Enable
M/S: Master/Slave
PSE: Pause
RAM: RAM Mode
RC: Raster Count
RFE: Read FIFO Full Interrupt Enable
RFF: Read FIFO Full
RFR: Read FIFO Ready
RRE: Read FIFO Ready Interrupt Enable
RSM: Raster Scan Mode
SE0: Split Enable 0
SE1: Split Enable 1
SE2: Split Enable 2
SE3: Split Enable 3
STR: Start
VC: Vertical Cycle
VDS: Vertical Display Start
VSW: Vertical Sync Width
WEE: Write FIFO Empty Interrupt Enable
WFE: Write FIFO Empty
WFR: Write FIFO Ready
WRE: Write FIFO Ready Interrupt Enable
WSS: Window Smooth Scroll
SP0, SP1, SP2: Split Screen 0 Width, Split Screen 1 Width, Split Screen 2 Width
BON1, BON2: Blink On 1, Blink On 2
BOFF1, BOFF2: Blink Off 1, Blink Off 2
HWS: Horizontal Window Start
HWW: Horizontal Window Width
VWS: Vertical Window Start
VWW: Vertical Window Width
CXS, CYS: Cursor X Start, Cursor Y Start
CXE, CYE: Cursor X End, Cursor Y End
FRA: First Raster Address
LRA: Last Raster Address
CHR: Character
MW: Memory Width
SDA: Start Dot Address
SAH/SRA: Start Address High/Start Raster Address
SAL: Start Address Low
BCW1, BCW2: Block Cursor Width 1, Block Cursor Width 2
BCSR1, BCSR2: Block Cursor Start Raster 1, Block Cursor Start Raster 2
BCER1, BCER2: Block Cursor End Raster 1, Block Cursor End Raster 2
BCA1, BCA2: Block Cursor Address 1, Block Cursor Address 2
CM: Cursor Mode
CON1, CON2: Cursor On 1, Cursor On 2
COFF1, COFF2: Cursor Off 1, Cursor Off 2
HZF, VZF: Horizontal Zoom Facter, Vertical Zoom Factor
LPAH: Light Pen Address High
LPAL: Light Pen Address Low

Figure 5. Hardware Access and Direct Access Registers (cont)

Table 1. Drawing Parameter Registers

Register No.	Read/ Write	Name of Register	Abbr.	Data (H) 15	14	13	12	11	10	9	8	Data (L) 7	6	5	4	3	2	1	0
Pr00	R/W	Color 0	CL0	CL0															
Pr01	R/W	Color 1	CL1	CL1															
Pr02	R/W	Color Comparison	CCMP	CCMP															
Pr03	R/W	Edge Color	EDG	EDG															
Pr04	R/W	Mask	MASK	MASK															
Pr05	R/W	Pattern RAM Control	PRC	PPY				PZCY				PPX				PZCX			
↓				PSY				—				PSX				—			
Pr07				PEY				PZY				PEX				PZX			
Pr08	R/W	Area Definition**	ADR	XMIN															
↓				YMIN															
				XMAX															
Pr08				YMAX															
Pr0C	R/W	Read Write Pointer	RWP	DN		—					RWPH								
Pr0D				RWPL														—	
Pr0E	—	Undefined	—	—															
Pr0F				—															
Pr010	R	Drawing Pointer	DP	DN		—					DPAH								
Pr11				DPAL														DPD	
Pr12	R	Current Pointer**	CP	X															
Pr13				Y															
Pr14	—	Undefined	—	—															
Pr15				—															

—: Always set to 0 .
**: Set two's complements for negative values of X and Y axis.

Drawing Parameter Register

R: Register which can be read by Read Parameter Register Command (RPR)
W: Register which can written into by Write Parameter Register Command (WPR)
—: Access is not allowed
CL0: Defines the color data used for the drawing when logical drawing data=0
CL1: Defines the color data used for the drawing when logical drawing data=1
CCMP: Defines the comparison color of the drawing operation
PSX, PSY: Pattern Start Point
PEX, PEY: Pattern End Point
PPX, PPY: Pattern Scan Start Point
PZX, PZY: Pattern Zoom
PZCX, PZCY: Pattern Zoom Count
XMIN, YMIN: Start point of Area definition
XMAX, YMAX: End point of Area definition
Dn: Screen Number
RWPH: High-order 8 bits of Read Write Pointer Address
RWPL: Low-order 12 bits of Read Write Pointer Address
DPAH: High-order 8 bits of Drawing Pointer Address
DPAL: Low-order 12 bits of Drawing Pointer Address
DPD: Drawing Pointer Dot Address
X, Y: Position indicated by Current Pointer on X-Y coodinate

Display Functions

Logical Display Screens

The ACRTC allows the frame buffer to be divided into four separate logical screens (table 2, figure 6).

In the simplest case, only the base screen parameters must be defined. Other screens may be selectively enabled, disabled, and blanked under software control.

The background screens (upper, base, and lower) split the screen into three horizontal partitions whose positions are fully programmable. A typical application might use the base screen for the bulk of user interaction, using the lower screen for a "status line(s)" and the upper screen for "pulldown menus".

The window screen is unique, since the ACRTC usually gives it higher priority than the background screens. Thus, when the window, whose size and position is completely programmable, overlaps a background screen, the window is displayed. The exception is in the ACRTC superimposed mode, in which the window has the same priority as the background screens. In this mode, the window and background screens are "superimposed" on the display.

Table 2. Logical Screen

Screen Number	Screen Name	Screen Group
0	Upper screen	Background screens
1	Base screen	
2	Low screen	
3	Window screen	

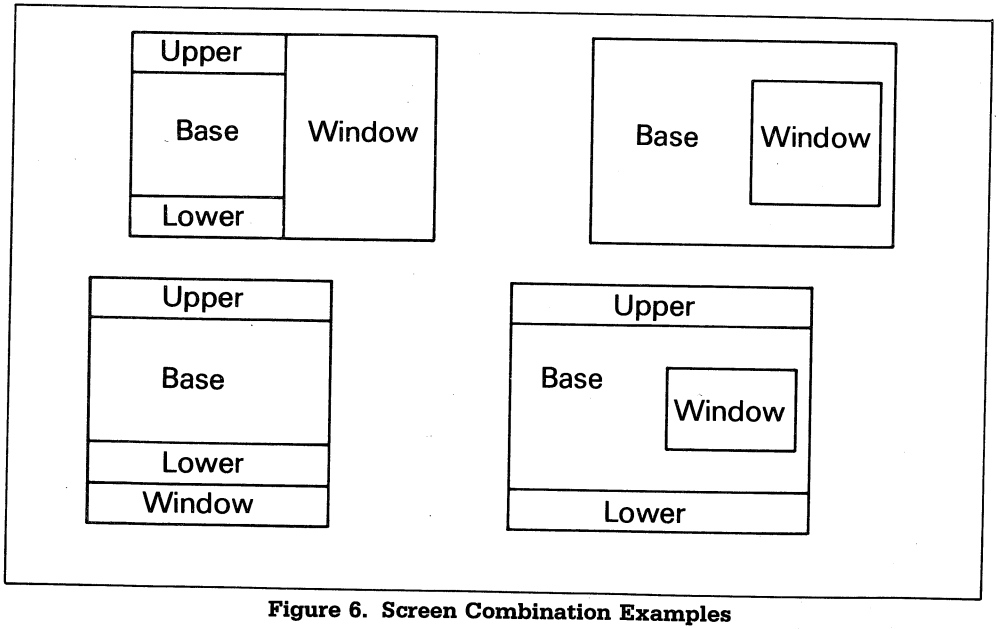


Figure 6. Screen Combination Examples

Frame Memory Setup

The ACRTC can have two independent frame memories, a 2-Mbyte frame buffer and a 128-kbyte refresh memory. The CHR output controls which memory is accessed.

Frame memory width is defined by setting up the memory width register (MWR). The horizontal width is independently defined by the horizontal display register (HDR). The memory area can therefore be specified bigger than the display area (figure 7).

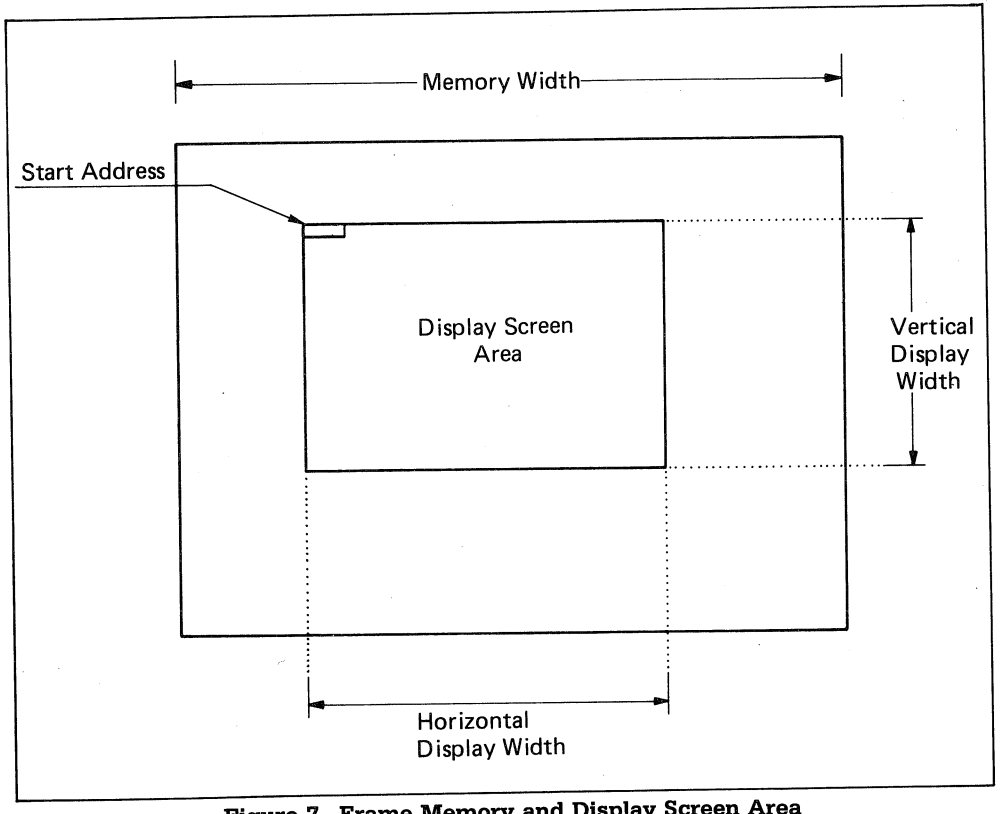


Figure 7. Frame Memory and Display Screen Area

Display Control

Figure 8 shows the relation between the frame memory and display screens. Each screen has its own memory width, vertical display width, and character/graphic attribution. These specifications are set by the control registers.

Horizontal display control registers are set in units of memory cycles. Vertical display control registers are set in units of rasters.

Note that display width of registers marked with an asterisk (*) in figure 9 is:

(Display width) = (Register value) + 1 memory cycles

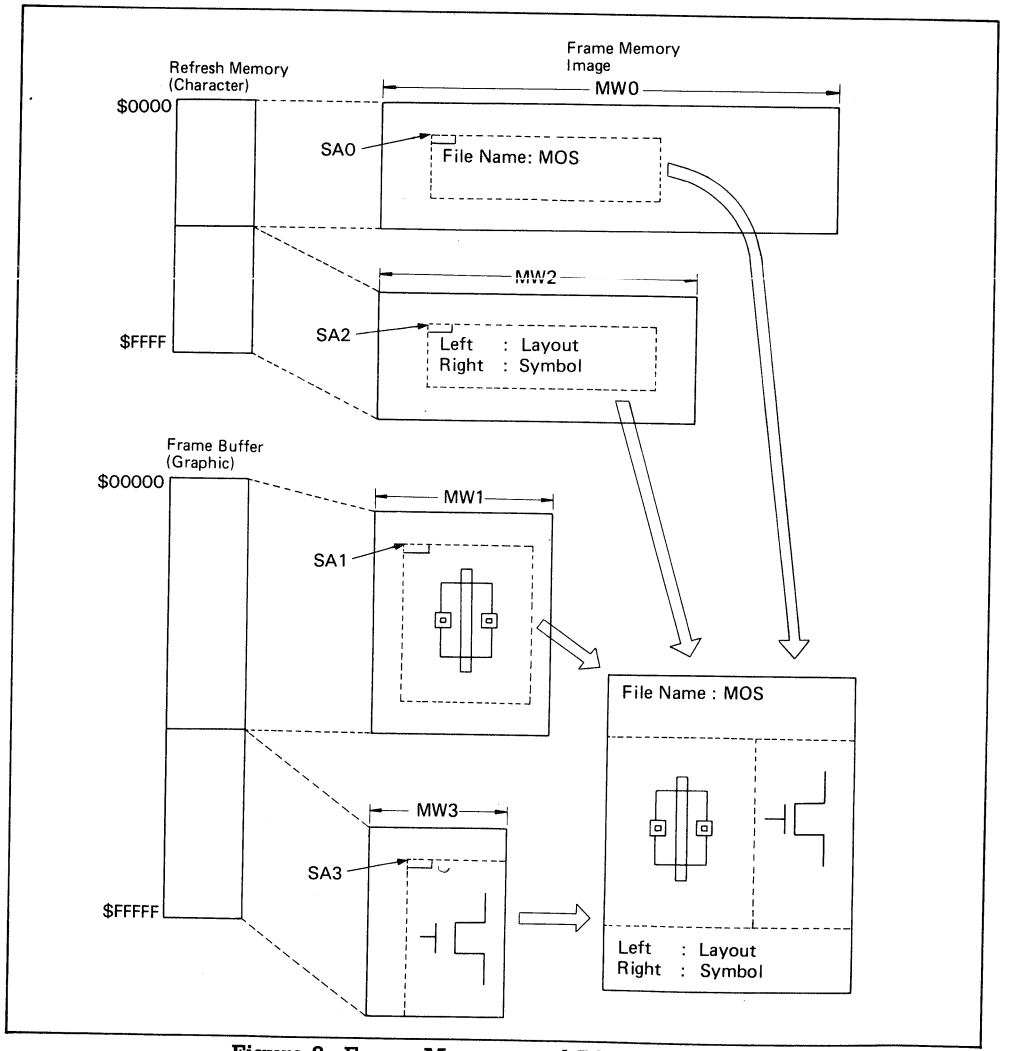


Figure 8. Frame Memory and Display Screens

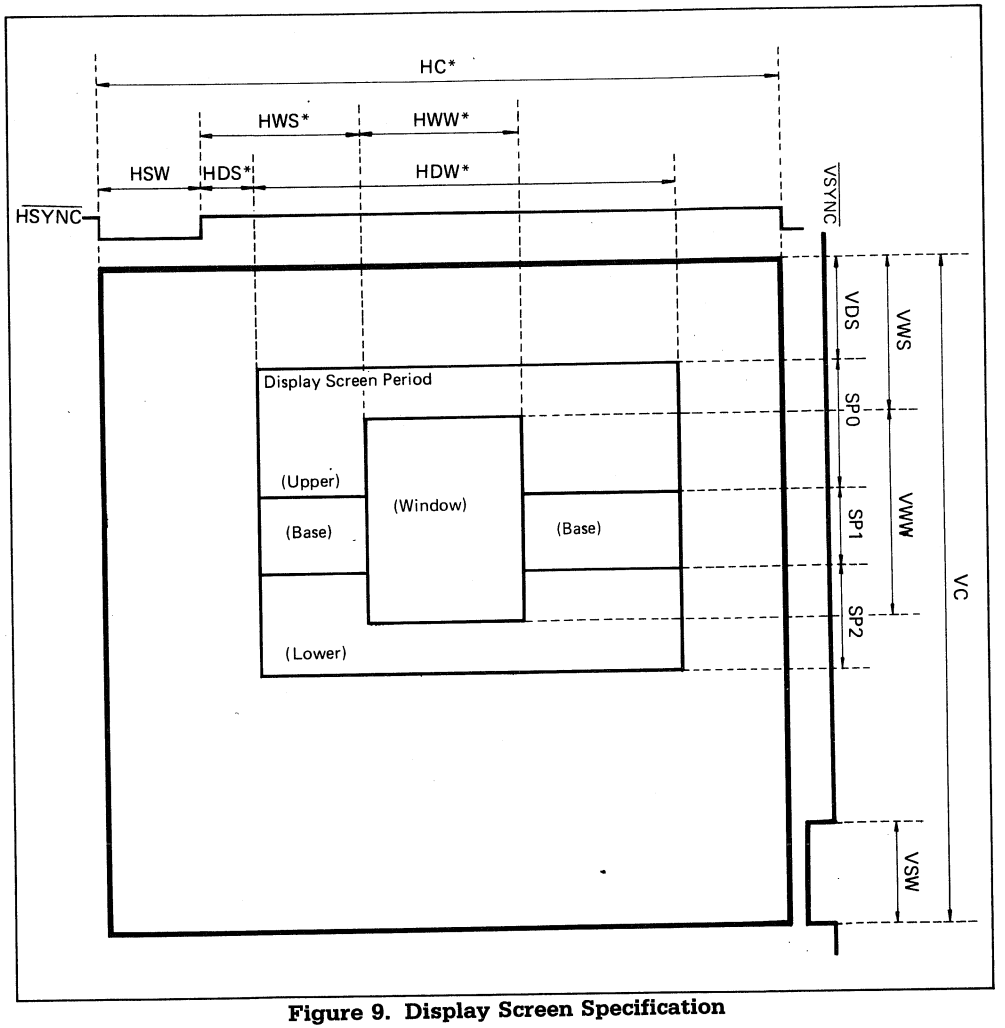


Figure 9. Display Screen Specification

Commands

The ACRTC has 38 commands classified into three groups (tables 3, 4):

- Register access
- Data transfer
- Graphic drawing

Five register access commands give the host MPU access to drawing processor drawing parameter registers and the pattern RAM.

Ten data transfer commands move data between the host system memory and the frame buffer, or within the frame buffer.

Twenty-three graphic drawing commands cause the ACRTC to draw. Parameters for these commands are specified using logical X-Y addressing.

All commands, parameters, and data are trasnferred via the ACRTC read and write FIFOs.

Assuming the ACRTC has been properly initialized, the MPU must perform two steps to make the ACRTC draw:

1. First the MPU must specify drawing parameters that define the details associated with the drawing. For example, to draw a figure or paint an area, the MPU must specify the drawing or painting pattern by initializing the ACRTC pattern RAM and related pointers. If clipping or hitting control are desired, the MPU must specify the area to be monitored during drawing by initilizing the area definition registers. Other drawing parameters include color, edge definition, etc.

2. After the drawing parameters have been specified, the MPU issues a drawing command and any required command parameters, such as the CRCL (circle) command with a radius parameter.

The ACRTC then performs the specified drawing operation by reading, modifying, and rewriting the contents of the frame buffer.

Table 3. ACRTC Command Table

Type	Mnemonic	Command Name	# (words)	Operation Cycles *1
Register Access Command	ORG	Origin	3	8
	WPR	Write Parameter Register	2	6
	RPR	Read Parameter Register	1	6
	WPTN	Write Pattern RAM	n+2	4n+8
	RPTN	Read Pattern RAM	2	4n+10
Data Transfer Command	DRD	DMA Read	3	(4x+8)y+12[x·y/8↑]+(62~68)
	DWT	DMA Write	3	(4x+8)y+16[x·y/8↑]+34
	DMOD	DMA Modify	3	(4x+8)y+16[x·y/8↑]+34
	RD	Read	1	12
	WT	Write	2	8
	MOD	Modify	2	8
	CLR	Clear	4	(2x+8)y+12
	SCLR	Selective Clear	4	(4x+6)y+12
	CPY	Copy	5	(6x+10)y+12
	SCPY	Selective Copy	5	(6x+10)y+12
Graphic Drawing Command	AMOVE	Absolute Move	3	56
	RMOVE	Relative Move	3	56
	ALINE	Absolute Line	3	P·L+18
	RLINE	Relative Line	3	P·L+18
	ARCT	Absolute Rectangle	3	2P(A+B)+54
	RRCT	Relative Rectangle	3	2P(A+B)+54
	APLL	Absolute Polyline	2n+2	Σ[P·L+16]+8
	RPLL	Relative Polyline	2n+2	Σ[P·L+16]+8
	APLG	Absolute Polygon	2n+2	Σ[P·L+16]+P·Lo+20
	RPLG	Relative Polygon	2n+2	Σ[P·L+16]+P·Lo+20
	CRCL	Circle	2	8d+66
	ELPS	Ellipse	4	10d+90
	AARC	Absolute Arc	5	8d+18
	RARC	Relative Arc	5	8d+18
	AEARC	Absolute Ellipse Arc	7	10d+96
	REARC	Relative Ellipse Arc	7	10d+96
	AFRCT	Absolute Filled Rectangle	3	(P·A+8)B+18
	RFRCT	Relative Filled Rectangle	3	(P·A+8)B+18
	PAINT	Paint	1	(18A+102)B-58 *2
	DOT	Dot	1	8
	PTN	Pattern	2	(P·A+10)B+20
	AGCPY	Absolute Graphic Copy	5	((P+2)A+10)B+70
	RGCPY	Relative Graphic Copy	5	((P+2)A+10)B+70

Notes: 1. 2CLK cycles.
2. Applies to rectangular figures. Time varies for other shapes.
3. Abbreviations
   - n: Number of read/write data words
   - x: Number of words in X direction
   - y: Number of words in Y direction
   - ↑: Round up
   - P: Operation cycles—P=4 cycles when OPM=000—011;
     P=6 cycles when OPM=100—111
   - L, Lo: Number of dots in a straight line
   - d: Total number of dots
   - A: Number of dots in main scan direction
   - B: Number of dots in sub scan direction

Table 4. Command Operation Codes and Parameters

Type	Mnemonic	Operation Code	Parameter
Register Access Command	ORG	0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	DPH DPL
	WPR	0 0 0 0 1 0 0 0 0 0 RN	D
	RPR	0 0 0 0 1 1 0 0 0 0 RN	
	WPTN	0 0 0 1 1 0 0 0 0 0 0 0 PRA	n $D_1, \ldots, D_n$
	RPTN	0 0 0 1 1 1 0 0 0 0 0 0 PRA	n
Data Transfer Command	DRD	0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0	AX AY
	DWT	0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0	AX AY
	DMOD	0 0 1 0 1 1 0 0 0 0 0 0 0 0 MM	AX AY
	RD	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0	
	WT	0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0	D
	MOD	0 1 0 0 1 1 0 0 0 0 0 0 0 0 MM	D
	CLR	0 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0	D AX AY
	SCLR	0 1 0 1 1 1 0 0 0 0 0 0 0 0 MM	D AX AY
	CPY	0 1 1 0 S DSD 0 0 0 0 0 0 0 0	SAH SAL AX AY
	SCPY	0 1 1 1 S DSD 0 0 0 0 0 0 0 MM	SAH SAL AX AY
Graphic Drawing Command	AMOVE	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	X Y
	RMOVE	1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	dX dY
	ALINE	1 0 0 0 1 0 0 0 AREA COL OPM	X Y
	RLINE	1 0 0 0 1 1 0 0 AREA COL OPM	dX dY
	ARCT	1 0 0 1 0 0 0 0 AREA COL OPM	X Y
	RRCT	1 0 0 1 0 1 0 0 AREA COL OPM	dX dY
	APLL	1 0 0 1 1 0 0 0 AREA COL OPM	n X1, Y1, . . Xn, Yn
	RPLL	1 0 0 1 1 1 0 0 AREA COL OPM	n dX1, dY1, . dXn, dYn
	APLG	1 0 1 0 0 0 0 0 AREA COL OPM	n X1, Y1, . . Xn, Yn
	RPLG	1 0 1 0 0 1 0 0 AREA COL OPM	n dX1, dY1,...dXn, dYn
	CRCL	1 0 1 0 1 0 0 C AREA COL OPM	r
	ELPS	1 0 1 0 1 1 0 C AREA COL OPM	a b DX
	AARC	1 0 1 1 0 0 0 C AREA COL OPM	Xc Yc Xe Ye
	RARC	1 0 1 1 0 1 0 C AREA COL OPM	dXc dYc dXe dYe
	AEARC	1 0 1 1 1 0 0 C AREA COL OPM	a b Xc Yc Xe Ye
	REARC	1 0 1 1 1 1 0 C AREA COL OPM	a b dXc dYc dXe dYe
	AFRCT	1 1 0 0 0 0 0 0 AREA COL OPM	X Y
	RFRCT	1 1 0 0 0 1 0 0 AREA COL OPM	dX dY
	PAINT	1 1 0 0 1 0 0 E AREA 0 0 000	
	DOT	1 1 0 0 1 1 0 0 AREA COL OPM	
	PTN	1 1 0 1 SL SD AREA COL OPM	SZ
	AGCPY	1 1 1 0 S DSD AREA 0 0 OPM	Xs Ys DX DY
	RGCPY	1 1 1 1 S DSD AREA 0 0 OPM	dXs dYs DX DY

Notes: 1. Register access commands abbreviations
RN: Drawing parameter register number ($0-$13)
PRA: Patterm RAM read/write operation starting address ($0-$F)
DPH: Drawing pointer register high word (figure 29)
DPL: Drawing pointer register low word (figure 29)
DPAH: Higher 8 bits of drawing pointer address
DPAL: Lower 12 bits of drawing pointer address
DPD: Dot position in memory address

2. Data transfer commands abbreviations
MM: Modify mode
S: Source scan direction (figure 30)
DSD: Destination scan direction (figure 31)
AX: Number of words in X direction — 1
AY: Number of words in Y direction — 1
D: Write data
SAH: Source start address high word (figure 32)

SAL: Source start address low word

3. Graphic drawing commands abbreviations
   AREA: Area mode
   COL: Color mode
   OPM: Operation mode
   C: Circle drawing direction—C=0 for counterclockwise;
   C=1 for clockwise
   E: Edge color definition—E=0, edge color is data in edge color register;
   E=1, edge color is any color except data in color register
   SL: Slant (figure 33)
   SD: Scan direction (figure 33)
   S: Source scan direction (figure 30)
   DSD: Destination scan direction (figure 31)
4. Parameter abbreviations
   X, X1, ..., Xn: Absolute X address from origin point
   Y, Y1, ..., Yn: Absolute Y address from origin point
   dX: Relative X address from current pointer
   dY: Relative Y address from current pointer
   n: Number of nodes
   dX1, ..., dXn: Relatve X address from each node
   dY1, ..., dYn: Relative Y address from each node
   r: Number of dots on radius
   a, b: ratio of dX squared to dY squared in ellipse—$a:b=dX^2:dY^2$
   DX: X-direction dot number
   DY: Y-direction dot number
   Xc: Absolute X address of center point of arc/ellipse
   Yc: Absolute Y address of center point of arc/ellipse
   dXc: Relative X address from current point to center point of arc/ellipse
   dYc: Relative Y address from current point to center point of arc/ellipse
   Xe: Absolute X address of end point of arc/ellipse
   Ye: Absolute Y address of end point of arc/ellipse
   dXe: Relative X address from current point to end point of arc/ellipse
   dYe: Relative Y address from current point to end point of arc/ellipse
   Xs: Absolute X address of start point of arc/ellipse
   Ys: Absolute Y address of start point of arc/ellipse
   dXs: Relative X address from current point to start point of arc/ellipse
   dYs: Relative Y address from current point to start point of arc/ellipse

Program Transfer

For program transfer, the MPU specifies the FIFO entry address and then writes commands/parameters to the write FIFO under program control (RS = high, R/$\overline{W}$, $\overline{CS}$ = low). The MPU writes are normally synchronized with FIFO status by software polling or interrupt.

Software Polling: WFR, WFE interrupts are disabled.

1. MPU program checks the SR (status register) for write FIFO ready flag (WFR) = 1, then writes 1 command/parameter word.
2. MPU program checks the SR (status register) for write FIFO empty flag (WFE) = 1, then writes 1 to 8 command/parameter words.

Interrupt Driven: WFR, WFE interrupts are enabled.

1. MPU WFR interrupt service routine writes 1 command/parameter word.
2. MPU WFE interrupt service routine writes 1 to 8 command/parameter words.

Register Access Commands: When writing register access commands to an initially empty write FIFO, the MPU does not have to synchronize to write FIFO status. The ACRTC can fetch and execute these commands faster than the MPU can issue them.

Command DMA Transfer

Commands and parameters can be transferred from the MPU system memory by an external DMAC. The MPU initiates and terminates command DMA transfer under software control (CDM bit of CCR). Command DMA transfer can also be terminated by asserting the ACRTC $\overline{DONE}$ signal. $\overline{DONE}$ is an input in command DMA transfer mode.

In command DMA transfer mode, the ACRTC issues cycle stealing DMA requests to the DMAC when the write FIFO is ready. The DMA data is automatically sent from system memory to the ACRTC write FIFO regardless of the contents of the address register.

Make sure that the write FIFO is empty and all previous commands are terminated before starting the command DMA transfer.

Data DMA transfer cannot be executed in command DMA transfer mode.

Register Access Commands

Registers associated with the drawing processor (pattern RAM and drawing parameter registers) are accessed throught the read and write FIFOs using register access commands (table 5).

Table 5. Register Access Commands

Command	Function
ORG	Initialize the relation between the origin point in the X-Y coordenates and the physical address
WPR	Write into parameter register
RPR	Read the parameter register
WPTN	Write into pattern RAM
RPTN	Read pattern RAM

Data Transfer Commands

Data transfer commands move blocks of data between the MPU system memory and the ACRTC frame buffer, or within the frame buffer itself (table 6). Before issuing these commands, a physical 20-bit frame buffer address must be specified in the RWP (read/write pointer) drawing parameter register.

Graphic Drawing Commands

The ACRTC has 23 graphic drawing commands (table 7). Graphic drawing is performed by modifying the contents of the frame buffer based on microcoded drawing algorithms in the ACRTC drawing processor.

Most drawing coordinate parameters are specified by logical pixel X-Y addresses. The ACRTC high-speed hardware performs the complex task of translating a logical pixel address to a linear frame buffer word address, and further, selecting the proper subfield of the word (for example, a 4-bit logical pixel might reside in bits 8-11 of a certain frame buffer word).

Many instructions allow specification in either absolute or relative X-Y coordinates (for example, ALINE and RLINE). In both cases, two's complement numbers represent both positive and negative values.

Table 6. Data Transfer Commands

Command	Function
DRD	Transfer data, by DMA transfer, from the frame buffer to the MPU system memory
DWT	Transfer data, by DMA transfer, from the MPU system memory to the frame buffer
DMOD	Transfer data, by DMA transfer, from the MPU system to the frame buffer subject to logical modification (bit maskable)
RD	Read one word of data from the frame buffer specified by the read/write pointer (RWP), and load the word into read FIFO
WT	Write one word of data to the frame buffer specified by the read/write pointer (RWP)
MOD	Perform logical operation on one word in the frame buffer specified by the read/write pointer (RWP) (bit maskable
CLR	Clear a rectangular area of the frame buffer with data in the command parameter
SCLR	Initialize a rectangular area of the frame buffer with 1-word data subject to logical operation (bit maskable)
CPY	Copy frame buffer data from one area (source area) to another area (destination area) specified by the read/write pointer (RWP)
SCPY	Copy frame buffer data from one area (source area) to another area (destination area) subject to logical modification by word. The source and destination areas must reside on the same screen (bit maskable)

Table 7. Graphic Drawing Commands

Command	Function
AMOVE	Move the current pointer (CP) to an absolute logical pixel X-Y address
RMOVE	Move the current pointer (CP) to a relative logical pixel X-Y address
ALINE	Draw a straight line from the current pointer (CP) to a command-specified end point in absolute coordinates
RLINE	Draw a straight line from the current pointer (CP) to a command-specified end point in relative corrdinates
ARCT	Draw a rectangle defined by the current pointer (CP) and a command-specified diagonal point in absolute coordinates
RRCT	Draw a rectangle defined by the current pointer (CP) and a command-specified diagonal point in relative coordinates
APLL	Draw a polyline (multiple contiguous segments) from the current pointer (CP) through command-specified points in absolute coordinates
RPLL	Draw a polyline (multiple contiguous segments) from the current pointer (CP) through command-specified points in relative coordinates
APLG	Draw a polygon which connects the current pointer (CP) and command-specified points in absolute coordinates
RPLG	Draw a polygon which connects the current pointer (CP) and command-specified points in relative coordinates
CRCL	Draw a circle of radius R placing the current pointer (CP) at the center
ELPS	Draw a ellipse whose shape is specifed by command parameters, placing the current pointer (CP) at the center
AARC	Draw an arc by using the current pointer (CP) as a start point with an end point and a center point in absolute coordinates
RARC	Draw an arc by using the current pointer (CP) as a start point with an end point and a center point in relative coordinates
AEARC	Draw an ellipse arc by using the current pointer (CP) as a start point with an end point and a center point in absolute coordinates
REARC	Draw an ellipse arc by using the current pointer (CP) as a start point with an end point and a center point in relative coordinates
AFRCT	Paint a rectangular area specifed by the current pointer (CP) and command parameters (absolute coordinates) according to a figure pattern stored in the pattern RAM (tiling)
RFRCT	Paint a rectangular area specifed by the current point (CP) and command parameters (relative coordinates) according to a figure pattern stored in the pattern RAM (tiling)
PAINT	Paint a closed area surrounded by edge color using a figure pattern stored in the pattern RAM (tiling)
DOT	Mark a dot on the coordinates indicated by the current pointer (CP)
PTN	Draw a graphic pattern defined in the pattern RAM onto a rectangular area specifed by the current point (CP) and by the pattern size (rotation angle: 45°)
AGCPY	Copy a rectangular area specifed by the absolute coordinates to the address specifed by the current pointer (CP) (rotation angle: 90°/mirror reflection)
RGCPY	Copy a rectangular area specified by the relative coordinates to the address specified by the current pointer (CP) (rotation angle: 90°/mirror reflection)

Notes on System Design

Power-On Sequence

The conditions in figure 10 must be satisfied at power-on.

Output Waveform

If excessive ringing (figure 11) occurs on CRT data buses, (MAD_0-MAD_{15}, MA_{16}/RA_0-MA_{19}/RA_4), damping resistors may be required as shown in figure 12.

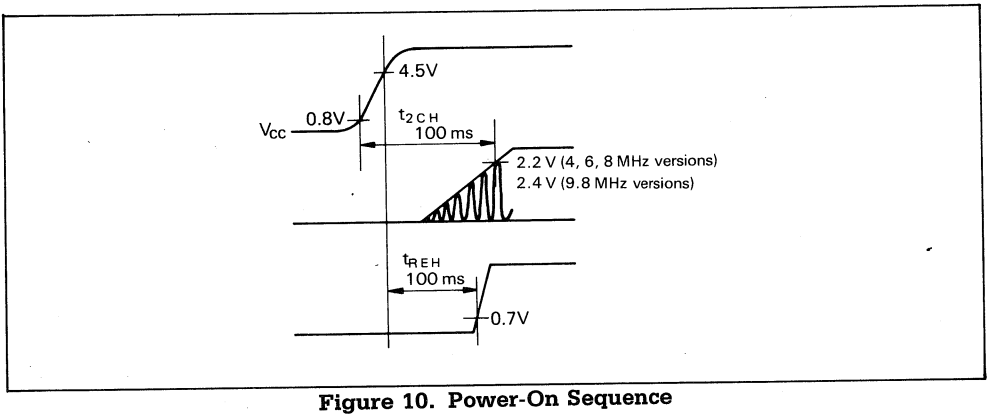


Figure 10. Power-On Sequence

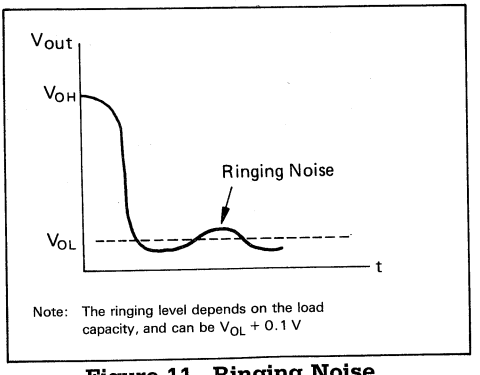


Figure 11. Ringing Noise

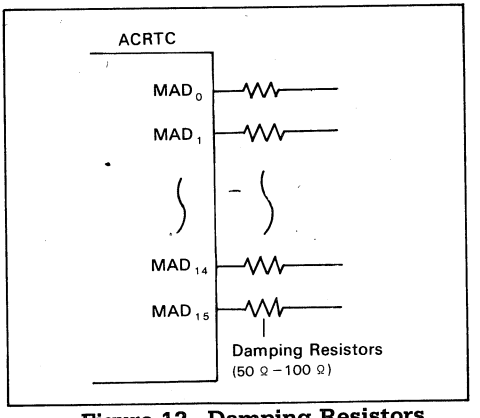


Figure 12. Damping Resistors

Power Supply Circuit

When laying out the V_{CC} and V_{SS} traces on the circuit board, locate capacitors as close as possible to each power supply pin (figures 13, 14, 15).

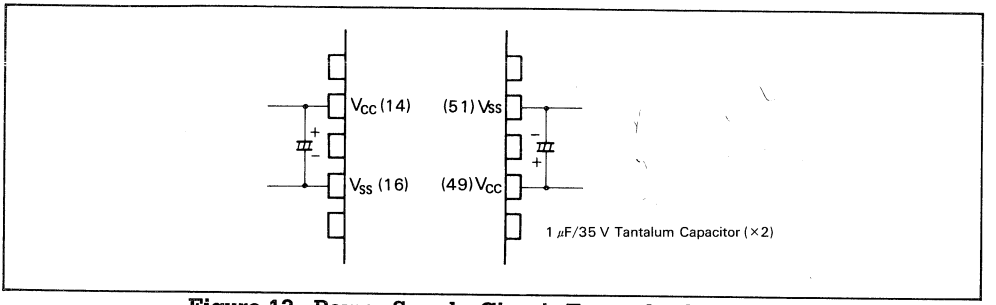


Figure 13. Power Supply Circuit Example, 64-Pin DIP

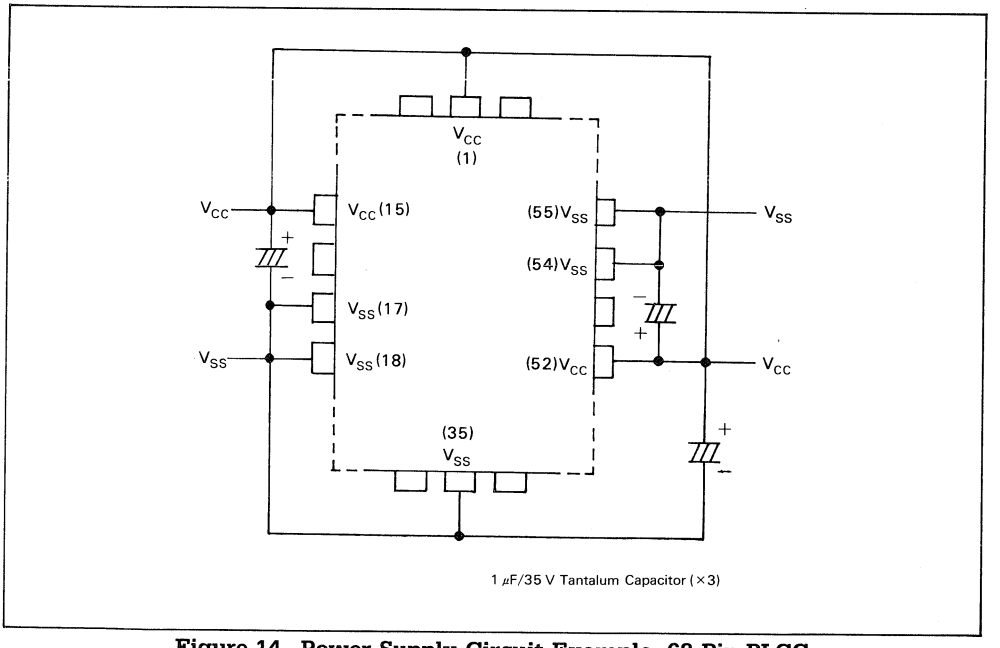


Figure 14. Power Supply Circuit Example, 68-Pin PLCC

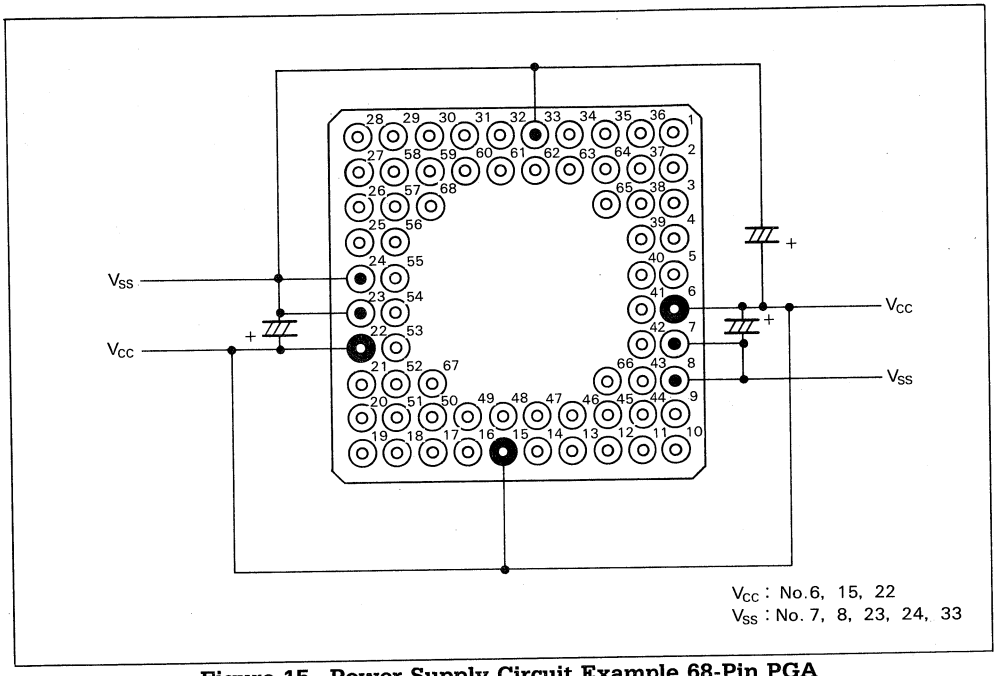


Figure 15. Power Supply Circuit Example 68-Pin PGA

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC} (Note 1)	−0.3 to +7.0	V
Input Voltage	V_{in} (Note 1)	−0.3 to V_{CC} +0.3	V
Allowable Output Current	$\|I_O\|$ (Note 2)	5	mA
Total Allowable Output Current	$\|\Sigma I_O\|$ (Note 3)	120	mA
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Notes: 1. Referenced to V_{SS} = 0 V.
2. The maximum current that may be drawn from, or flow out of, one output, or one common input/output terminal.
3. The total sum of currents that may be drawn from, or flow out of, all output or common input/output terminals.
4. Using an LSI beyond its maximum rating may result in its permanent destruction.
LSIs should usually be used under recommended operating conditions. Exceeding any of these conditions may adversely affect reliability.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{cc} (Note)	4.75	5.0	5.25	V
Input Low Voltage		V_{IL} (Note)	0		0.7	V
Input High Voltage	(4, 6, 8 MHz versions)	V_{IH} (Note)	2.2		V_{CC}	V
	(9.8 MHz version)	V_{IH} (Note)	2.4		V_{CC}	V
Operating Temperature		T_{opr}	0	25	75	°C

Note: Referenced to V_{SS} = 0 V

Electrical Characteristics
DC Characteristics
(V_{CC}=5.0V ± 5%, V_{SS}=0V, Ta=0°C to +70°C unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Condition
Input High Level Voltage	All inputs	V_{IH}	2.2	V_{CC}	V	4, 6, 8 MHz versions
			2.4	V_{CC}	V	9.8 MHz ★ version
Input Low Level Voltage	All inputs	V_{IL}	−0.3	0.7	V	
Input Leak Current	R/$\overline{W}$, $\overline{CS}$, RS, $\overline{RES}$, $\overline{DACK}$, 2CLK, LPSTB	I_{in}	−2.5	2.5	µA	V_{in}=0.4 to V_{CC}
Hi-Z Input Current	D_0-D_{15}, MAD_0-MAD_{15}, $\overline{EXSYNC}$	I_{TSI}	−10	10	µA	V_{in}=0.4 to V_{CC}
Output High Level Voltage	D_0-D_{15}, MAD_0-MAD_{15}, $\overline{CUD1}$, $\overline{CUD2}$, $\overline{DREQ}$, $\overline{DTACK}$, $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{EXSYNC}$, $\overline{MRD}$, $\overline{DRAW}$, $\overline{AS}$, $\overline{DISP1}$, $\overline{DISP2}$, CHR, MCYC, RA_4, MA_{16}/RA_0-MA_{19}/RA_3	V_{OH}	V_{CC} −1.0		µA	I_{OH}=−400µA
Output Low Level Voltage	D_0-D_{15}, MAD_0-MAD_{15}, $\overline{CUD1}$, $\overline{CUD2}$, $\overline{DREQ}$, $\overline{DTACK}$, $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{EXSYNC}$, $\overline{MRD}$, $\overline{DRAW}$, $\overline{AS}$, $\overline{DISP1}$, $\overline{DISP2}$, CHR, MCYC, RA_4, MA_{16}/RA_0-MA_{19}/RA_3	V_{OL}		0.5	V	I_{OL}=2.2mA
	$\overline{IRQ}$, $\overline{DONE}$	VO_L		0.5	V	I_{OL}=2.5 mA
Output Leak Current (Hi-Z)	$\overline{IRQ}$, $\overline{DONE}$	I_{LOD}		10	µA	V_{OH}=V_{CC}
Input Capacitance	D_0-D_{15}, MAD_0-MAD_{15}, $\overline{EXSYNC}$, R/$\overline{W}$, $\overline{CS}$, RS, $\overline{RES}$, $\overline{DACK}$, 2CLK, LPSTB	C_{in}		17	pF	V_{in}=0 V, Ta=25°C, f=1.0 MHz
Output Capacitance	$\overline{IRQ}$, $\overline{DONE}$	C_{out}		15	pF	V_{in}=0 V, Ta=25°C, f=1.0 MHz
Current Consumption		I_{CC}		60	mA	4 MHz version
				80	mA	6 MHz version
				100	mA	8 MHz version
				120	mA	9.8 MHz version

AC Characteristics (V_{CC}=5.0V ± 5%, V_{SS}=0V, Ta=0 to +70°C unless otherwise noted)

Clock Timing

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
	Operation Frequency of 2CLK	f	1	4	1	6	1	8	1	9.8	MHz	17
1	Clock Cycle Time	tcyc	250	1000	167	1000	125	1000	102	1000	ns	
2	Clock High Level Pulse Width	tPWCH	115	500	75	500	55	500	46	500	ns	
3	Clock Low Level Pulse Width	tPWCL	115	500	75	500	55	500	46	500	ns	
4	Clock Rise Time	tcr	–	10	–	10	–	10	–	5	ns	
5	Clock Fall Time	tcf	–	10	–	10	–	10	–	5	ns	

MPU Read/Write Cycle Timing

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
6	R/$\overline{W}$ Setup Time	tRWS	70	–	60	–	50	–	50	–	ns	18—20
7	R/$\overline{W}$ Hold Time	tRWH	0	–	0	–	0	–	0	–	ns	
8	RS Setup Time	tRSS	70	–	60	–	50	–	50	–	ns	
9	RS Hold Time	tRSH	0	–	0	–	0	–	0	–	ns	
10	$\overline{CS}$ Setup Time	tCSS	50	–	40	–	40	–	40	–	ns	
11	$\overline{CS}$ High Level Width	tWCSH	80	–	70	–	60	–	60	–	ns	18, 19
12												
13	Read Wait Time	tRWAI	0	–	0	–	0	–	0	–	ns	18, 20
14	Read Data Access Time	tRDAC	–	120	–	100	–	80	–	80	ns	
15	Read Data Hold Time	tRDH	10	–	10	–	10	–	10	–	ns	
16	Read Data Turn Off Time	tRDZ	–	60	–	60	–	60	–	60	ns	
17	$\overline{DTACK}$ Delay Time (Z to L)	tDTKZL	–	90	–	80	–	70	–	70	ns	18—20
18	$\overline{DTACK}$ Delay Time (D to L)	tDTKDL	0	–	0	–	0	–	0	–	ns	18, 20
19	$\overline{DTACK}$ Release Time (L to H)	tDTKLH	–	100	–	90	–	80	–	80	ns	18—20
20	$\overline{DTACK}$ Turn Off Time (H to Z)	tDTKZ	–	100	–	100	–	100	–	100	ns	
21	Data Bus 3-State Recovery Time 1	tDBRT1	0	–	0	–	0	–	0	–	ns	18, 20
22	Write Wait Time	tWWAI	0	–	0	–	0	–	0	–	ns	19,20
23	Write Data Setup Time	tWDS	80	–	60	–	40	–	40	–	ns	
24	Write Data Hold Time	tWDH	10	–	10	–	10	–	10	–	ns	

DMA Read/Write Cycle Timing

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
25	$\overline{DREQ}$ Delay Time 1	tDRQD1	–	150	–	130	–	110	–	110	ns	21—24
26	$\overline{DREQ}$ Delay Time 2	tDRQD2	–	90	–	80	–	70	–	70	ns	
27	DMA R/$\overline{W}$ Setup Time	tDMRWS	70	–	60	–	50	–	50	–	ns	
28	DMA R/$\overline{W}$ Hold Time	tDMRWH	0	–	0	–	0	–	0	–	ns	
29	$\overline{DACK}$ Setup Time	tDAKS	50	–	40	–	40	–	40	–	ns	
30	$\overline{DACK}$ High Level Width	tWDAKH	80	–	70	–	60	–	60	–	ns	
31												
32	DMA Read Wait Time	tDRW	0	–	0	–	0	–	0	–	ns	21, 22
33	DMA Read Data Access Time	tDRDAC	–	120	–	100	–	80	–	80	ns	
34	DMA Read Data Hold Time	tDRDH	10	–	10	–	10	–	10	–	ns	
35	DMA Read Data Turn Off Time	tDRDZ	–	60	–	60	–	60	–	60	ns	
36	DMA $\overline{DTACK}$ Delay Time (Z to L)	tDDTZL	–	90	–	80	–	70	–	70	ns	21—24
37	DMA $\overline{DTACK}$ Delay Time (D to L)	tDDTDL	0	–	0	–	0	–	0	–	ns	21, 22
38	DMA $\overline{DTACK}$ Release Time (L to H)	tDDTLH	–	100	–	90	–	80	–	80	ns	21—24
39	DMA $\overline{DTACK}$ Turn Off Time (H to Z)	tDDTHZ	–	100	–	100	–	100	–	100	ns	
40	$\overline{DONE}$ Output Delay Time	tDND	–	90	–	80	–	70	–	70	ns	
41	$\overline{DONE}$ Output Turn Off Time (L to Z)	tDNLZ	–	100	–	90	–	80	–	80	ns	
42	Data Bus 3-State Recovery Time 2	tDBRT2	0	–	0	–	0	–	0	–	ns	21, 22
43	$\overline{DONE}$ Input Pulse Width	tDNPW	2	–	2	–	2	–	2	–	tcyc	23, 24
44	DMA Write Wait Time	tDWW	0	–	0	–	0	–	0	–	ns	
45	DMA Write Data Setup Time	tDWDS	80	–	60	–	40	–	40	–	ns	
46	DMA Write Data Hold Time	tDWDH	10	–	10	–	10	–	10	–	ns	
47												

Frame Memory Read/Write Cycle Timing

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
48	$\overline{AS}$ "Low" Level Pulse Width	tPWASL	80	–	40	–	25	–	20	–	ns	25—28
49	Memory Address Hold Time 2	tMAH2	10	–	10	–	10	–	5	–	ns	
50	$\overline{AS}$ Delay Time 1	tASD1	–	90	–	75	–	60	–	50	ns	
51	$\overline{AS}$ Delay Time 2	tASD2	5	90	5	75	5	65	5	40	ns	
52	Memory Address Delay Time	tMAD	15	95	15	80	15	70	10	50	ns	
53	Memory Address Hold Time 1	tMAH1	25	–	25	–	25	–	15	–	ns	
54	Memory Address Turn Off Time (A to Z)	tMAAZ	–	50	–	50	–	50	–	35	ns	
55	Memory Read Data Setup Time	tMRDS	60	–	50	–	35	–	30	–	ns	26
56	Memory Read Data Hold Time	tMRDH	10	–	10	–	10	–	0	–	ns	
57	MA/RA Delay Time	tMARAD	–	100	–	90	–	80	–	60	ns	25—28
58	MA/RA Hold Time	tMARAH	10	–	10	–	10	–	5	–	ns	25—27
59	MCYC Delay Time	tMCYCD	5	60	5	50	5	50	5	40	ns	25—29
60	MRD Delay Time	tMRDD	–	90	–	80	–	70	–	50	ns	24—28
61	MRD Hold Time	tMRH	10	–	10	–	10	–	5	–	ns	
62	$\overline{DRAW}$ Delay Time	tDRWD	–	90	–	80	–	70	–	50	ns	
63	$\overline{DRAW}$ Hold Time	tDRWH	10	–	10	–	10	–	5	–	ns	
64	Memory Write Data Delay Time	tMWDD	–	90	–	80	–	70	–	50	ns	27
65	Memory Write Data Hold Time	tMWDH	10	–	10	–	10	–	5	–	ns	
110	Memory Address Setup Time 1	tMAS1	10	–	10	–	10	–	10	–	ns	25—28
112	Memory Address Setup Time 2	tMAS2	10	–	10	–	10	–	10	–	ns	

Notes: 1. Characteristic No.52 is independent of the 2CLK operation frequency (f) and timing of No.51 and No.110.
2. New characteristics No.50 and No.52 shown above are applicable only to lot numbers 5M*, 6*, 7**, and greater (* means don't care).

For the other lot numbers, applicable characteristics are as follows:

No.	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		Unit
		Min	Max	Min	Max	Min	Max	
50	tASD1	–	90	–	75	–	65	ns
52	tMAD	–	95	–	80	–	70	ns

Display Control Signal Output Timing

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
67	$\overline{\text{HSYNC}}$ Delay Time	tHSD	–	90	–	80	–	70	–	50	ns	28—30
68	$\overline{\text{VSYNC}}$ Delay Time	tVSD	–	90	–	80	–	70	–	50	ns	29
69	$\overline{\text{DISP1}}$, $\overline{\text{DISP2}}$ Delay Time	tDSPD	–	90	–	80	–	70	–	50	ns	
70	$\overline{\text{CUD1}}$, $\overline{\text{CUD2}}$ Delay Time	tCUDD	–	90	–	80	–	70	–	50	ns	
71	$\overline{\text{EXSYNC}}$ Output Delay Time	tEXD	20	90	20	80	20	70	15	50	ns	
72	CHR Delay Time	tCHD	–	90	–	80	–	70	–	50	ns	
73												
74												

$\overline{\text{EXSYNC}}$ Input Timing

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
75	$\overline{\text{EXSYNC}}$ Input Pulse Width	tEXSW	3	–	3	–	3	–	3	–	tcyc	30
76	$\overline{\text{EXSYNC}}$ Input Setup Time	tEXS	60	–	60	–	50	–	30	–	ns	
77	$\overline{\text{EXSYNC}}$ Input Hold Time	tEXH	15	–	15	–	15	–	10	–	ns	

LPSTB Input Timing

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
78	LPSTB Uncertain Time 1	tLPD1	70	–	70	–	70	–	45	–	ns	31, 32
79	LPSTB Uncertain Time 2	tLPD2	10	–	10	–	10	–	10	–	ns	
80	LPSTB Input Hold Time	tLPH	10	–	10	–	10	–	10	–	ns	
81	LPSTB Input Inhibit time	tLPI	4	–	4	–	4	–	4	–	tcyc	

$\overline{\text{RES}}$ and $\overline{\text{DACK}}$ Input Timing

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
82	$\overline{\text{DACK}}$ Setup Time for $\overline{\text{RES}}$	tDAKSR	100	–	100	–	100	–	100	–	ns	33
83	$\overline{\text{DACK}}$ Hold Time for $\overline{\text{RES}}$	tDAKHR	0	–	0	–	0	–	0	–	ns	
84	$\overline{\text{RES}}$ Input Pulse Width	tRES	10	–	10	–	10	–	10	–	tcyc	

$\overline{IRQ}$ and Attributes Output Cycle Timing

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
85	$\overline{IRQ}$ Delay Time 1	tIRQ1	–	250	–	200	–	150	–	150	ns	34, 35
86	$\overline{IRQ}$ Delay Time 2	tIRQ2	–	500	–	500	–	500	–	500	ns	
87	ATR Delay Time 1	tATRD1	–	100	–	90	–	80	–	60	ns	28
88	ATR Hold Time 1	tATRH1	10	–	10	–	10	–	5	–	ns	
89												
90	ATR Delay Time 2	tATRD2	–	100	–	90	–	80	–	60	ns	28
91	ATR Hold Time 2	tATRH2	10	–	10	–	10	–	5	–	ns	

Synchronous Bus Timing, MPU or DMA Read/Write Cycle

No.	Item	Symbol	4 MHz Version		6 MHz Version		8 MHz Version		9.8 MHz Version		Unit	Reference Figure Number
			Min	Max	Min	Max	Min	Max	Min	Max		
100	$\overline{CS}$ Cycle Time	tCSC	4	–	4	–	4	–	4	–	tcyc	18, 19
101	$\overline{CS}$ Low Level Width	tWCSL	2	–	2	–	2	–	2	–	tcyc	
102	$\overline{CS}$ High Level Width	tWCSH	2	–	2	–	2	–	2	–	tcyc	
104	$\overline{DACK}$ Cycle Time	tDACKC	4	–	4	–	4	–	4	–	tcyc	22, 24
105	$\overline{DACK}$ Low Level Width	tWDACKL	2	–	2	–	2	–	2	–	tcyc	
106	$\overline{DACK}$ High Level Width	tWDACKH	2	–	2	–	2	–	2	–	tcyc	

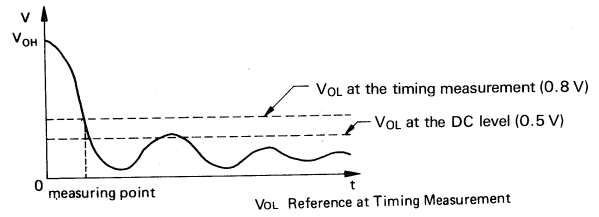
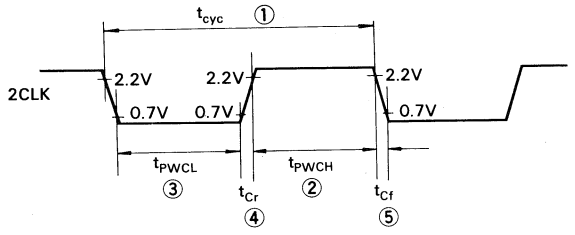
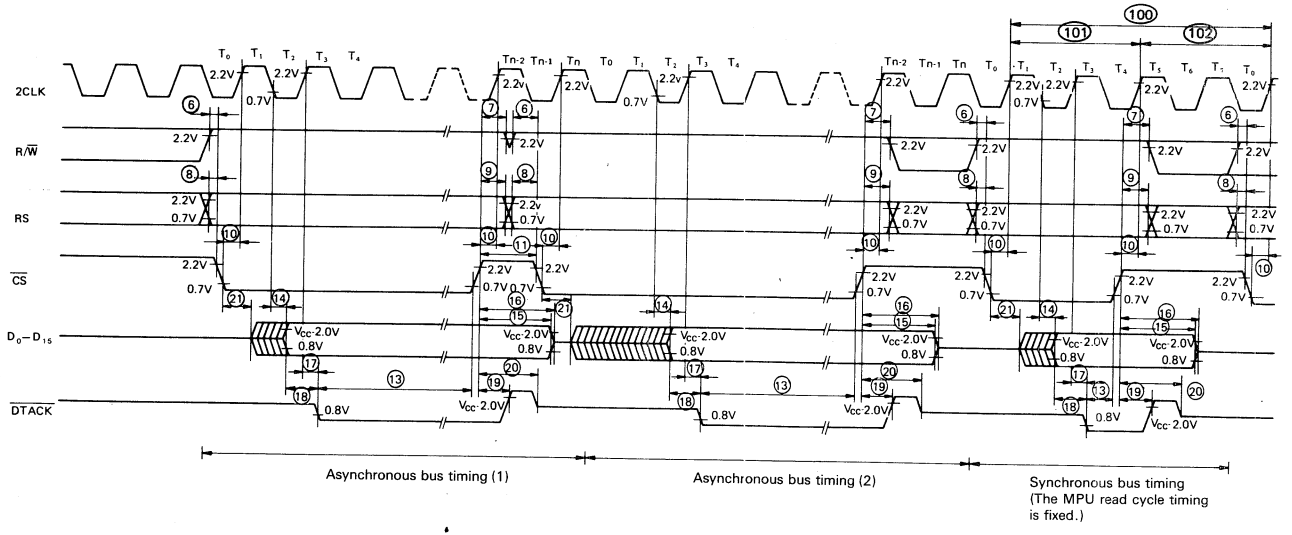


Figure 16. Test Points



Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

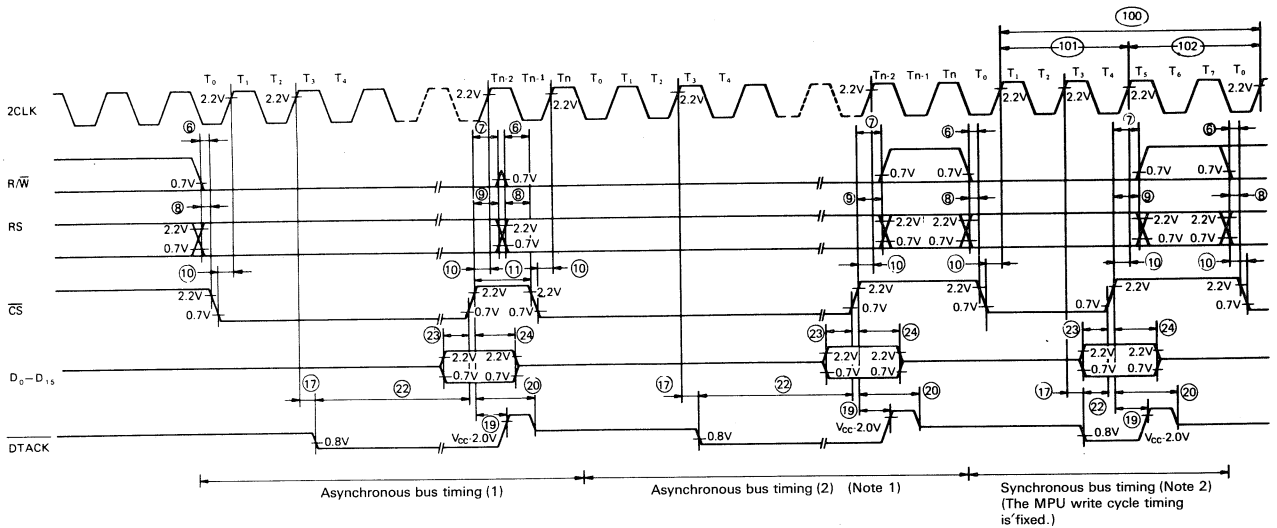
Figure 17. 2CLK Waveform



Notes: 1. $\overline{CS}$ high level width must satisfy specification (11).
Unless spec (102) is satisfied, $\overline{DTACK}$ and read data responses to the succeeding cycle are delayed.
2. (100), (101) and (102) are synchronous bus timing specifications.

Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

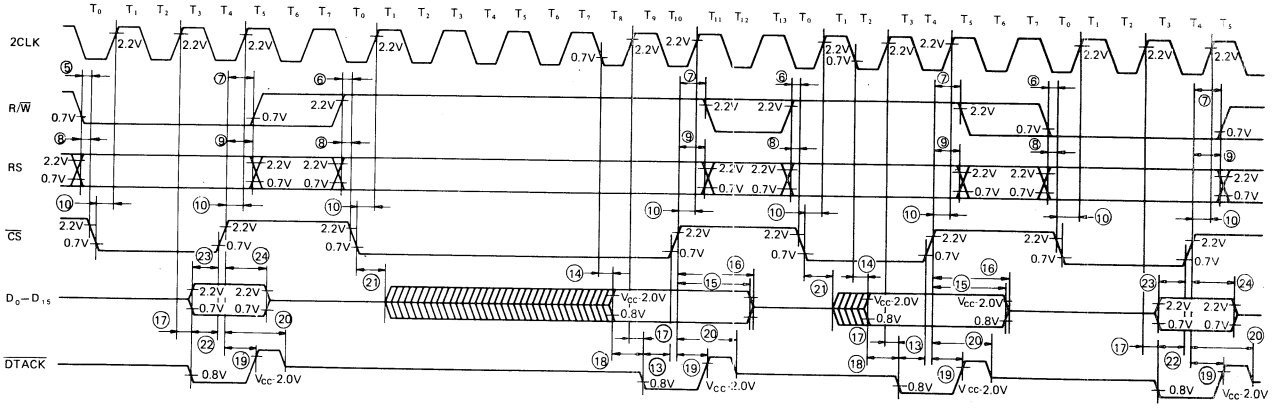
Figure 18. MPU Read Cycle Timing (MPU ← ACRTC)



Notes: 1. $\overline{CS}$ high width must satisfy the specification (11).
Unless spec. (102) is satisfied. $\overline{DTACK}$ response to the succeense to the succeeding cycle is delayed.
2. When the ACRTC is used with the synchronous bus timing, the specifications (100), (101) and (102) must be satisfied.

Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

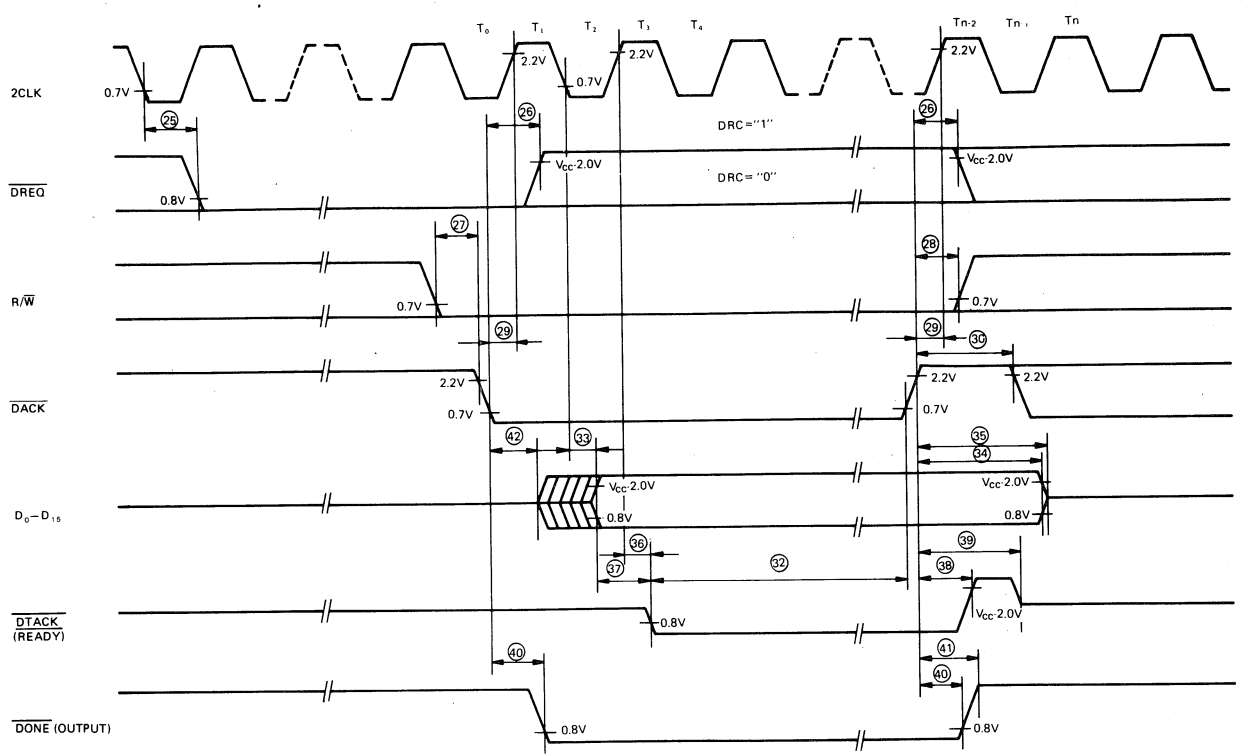
Figure 19. MPU Write Cycle Timing (MPU → ACRTC)



Note: When the MPU read cycle immediately follows the MPU wirte cycle execution, $\overline{\text{DTACK}}$ and the read data responses are delayed (by 3 cycles of 2CLK) even though spec. (102) is satisfied.

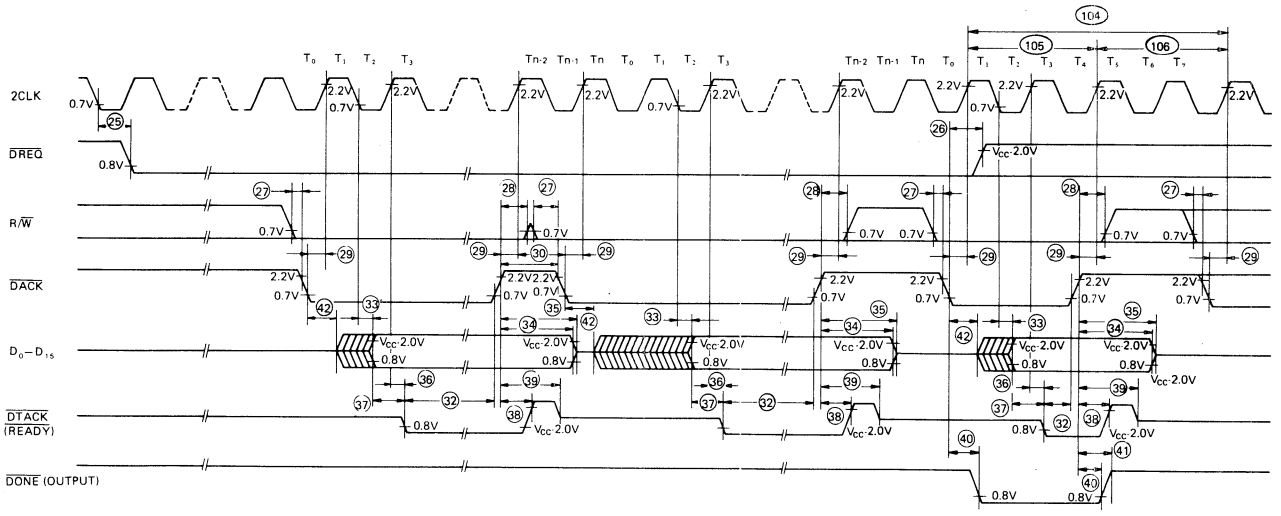
Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version. Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 20. MPU Read/Write Cycle Timing (MPU → ACRTC)



Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

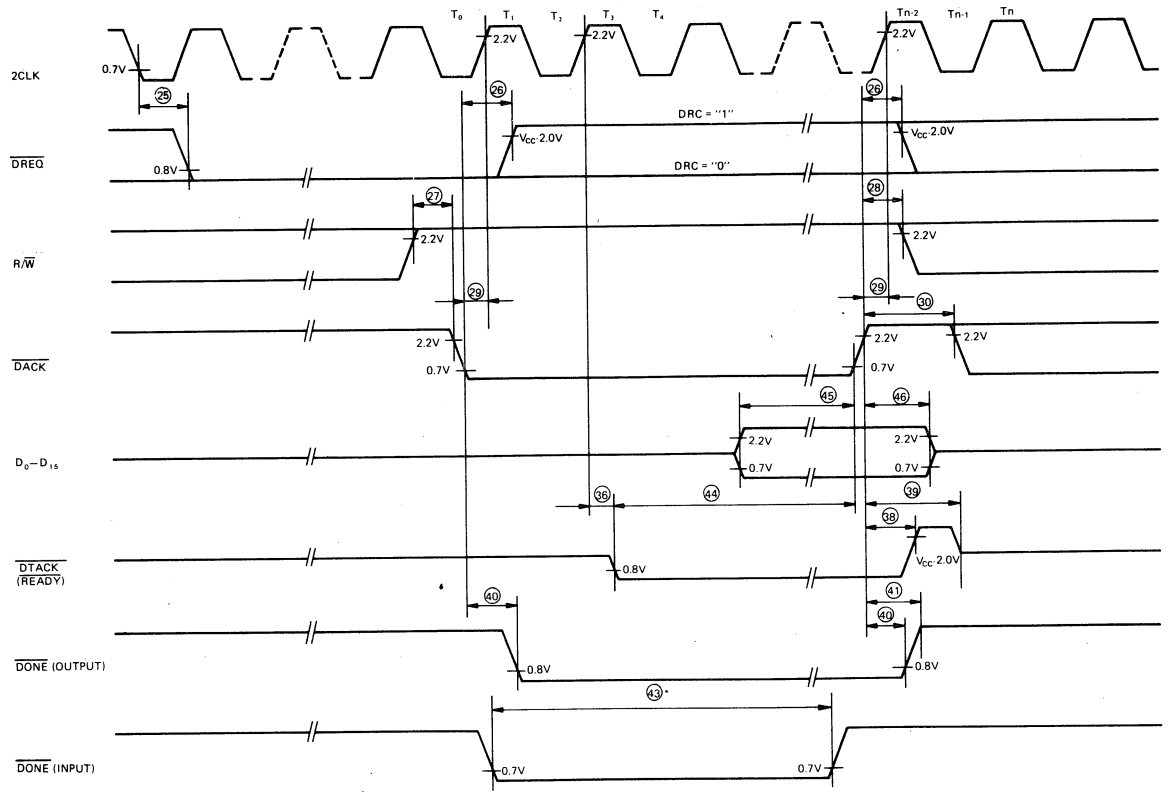
Figure 21. DMA Read Cycle Timing (Memory ← ACRTC)



Note: $\overline{\text{DACK}}$ high width must satisfy spec (30). Unless spec. (106) is satisfied, $\overline{\text{DTACK}}$ and the read data responses to the succeeding cycle are delayed. When the ACRTC is used with synchronous bus timing, the specifications (104), (105) and (106) must be satisfied.

Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version. Note that in 9.8 MHz version, V_{IH} is 2.4 V.

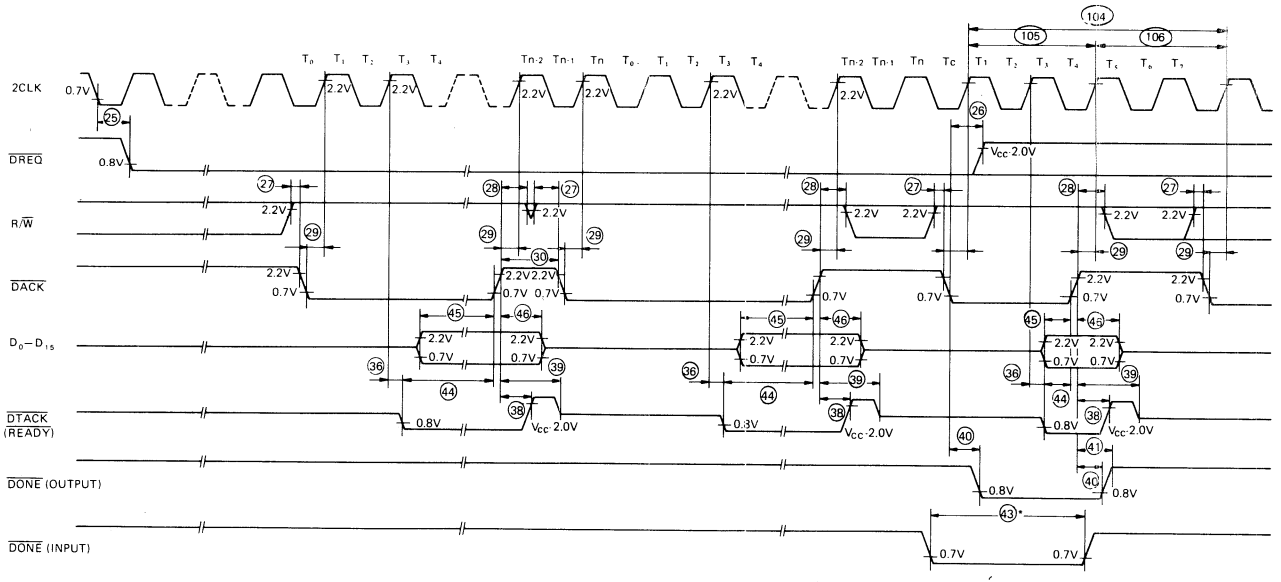
Figure 22. DMA Ready Cycle Timing (Memory ← ACRTC): Burst Mode



*$\overline{\text{DONE}}$ must be asserted low while $\overline{\text{DACK}}$ remains low. $\overline{\text{DONE}}$ low width must satisfy spec. (43)

Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version. Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 23. DMA Write Cycle Timing (Memory → ACRTC)

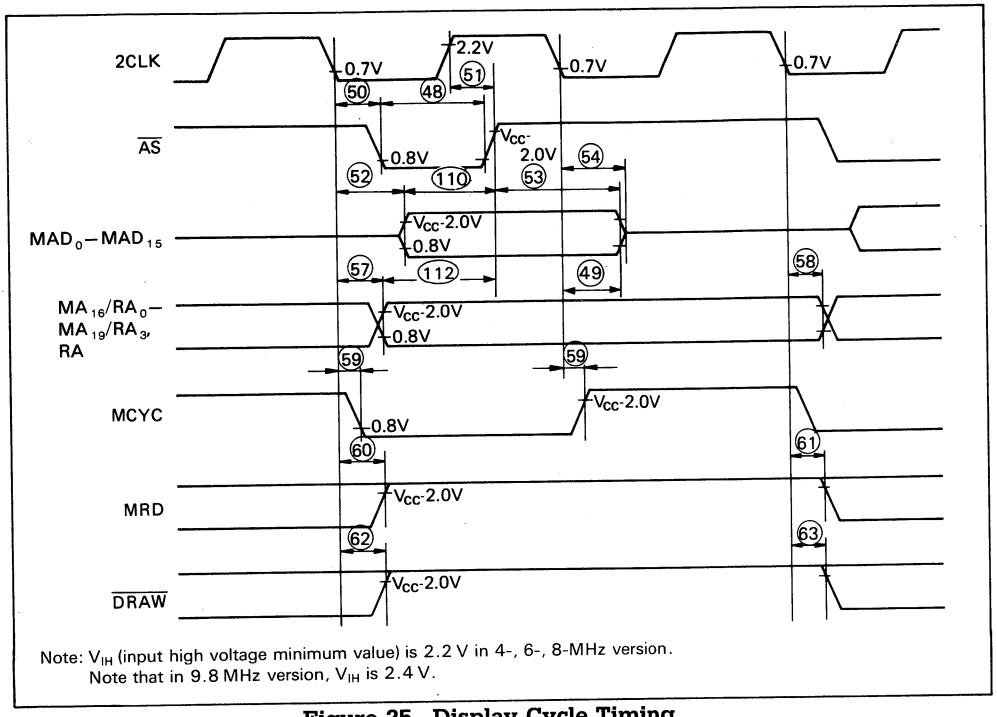


*DONE must be asserted low while DACK remains low.
DONE low width must satisfy the spec (43).

Note: DACK high width must satisfy the spec, (30). Unless spec. (106) is satisfied, DTACK response to the succeeding cycle is delayed.
When the ACRTC is used with the synchronous bus timing specifications (104), (105) and (106) must be satisfied.

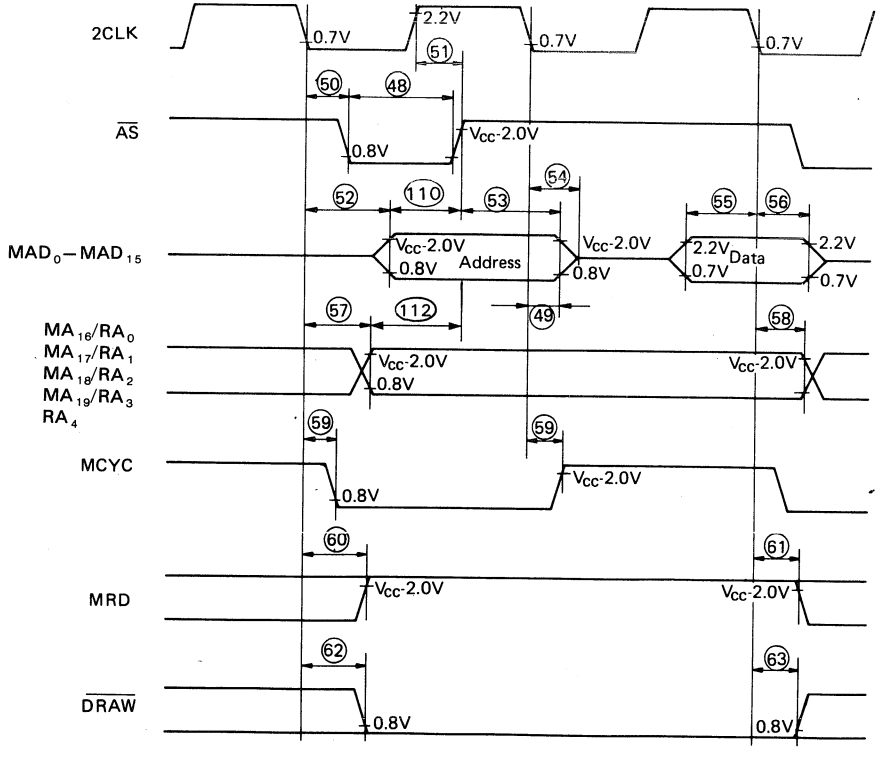
Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version. Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 24. DMA Write Cycle Timing (Memory → ACRTC): Burst Mode



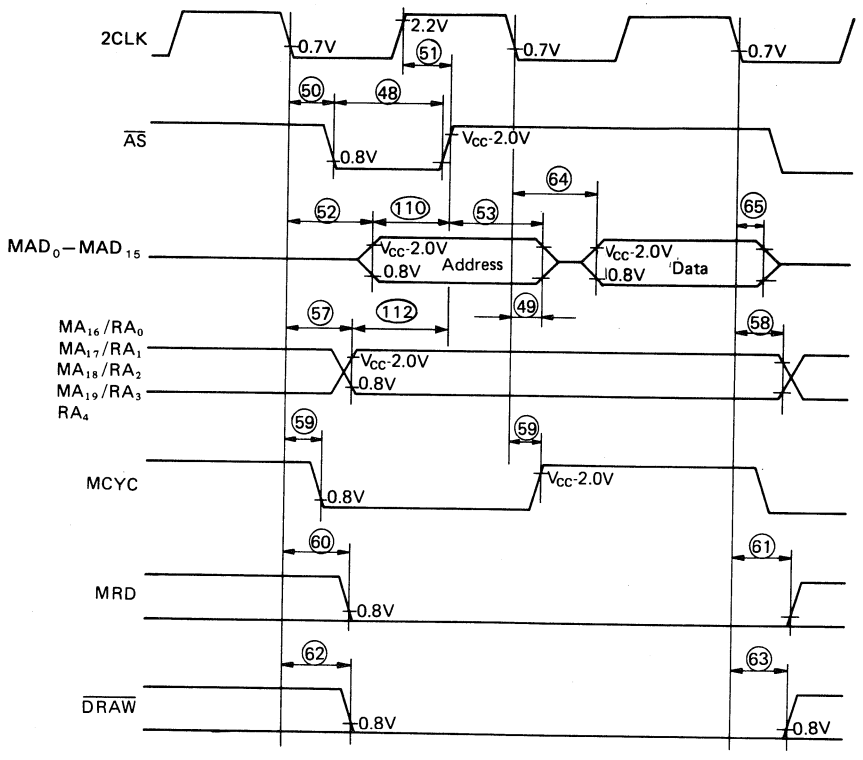
Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 25. Display Cycle Timing



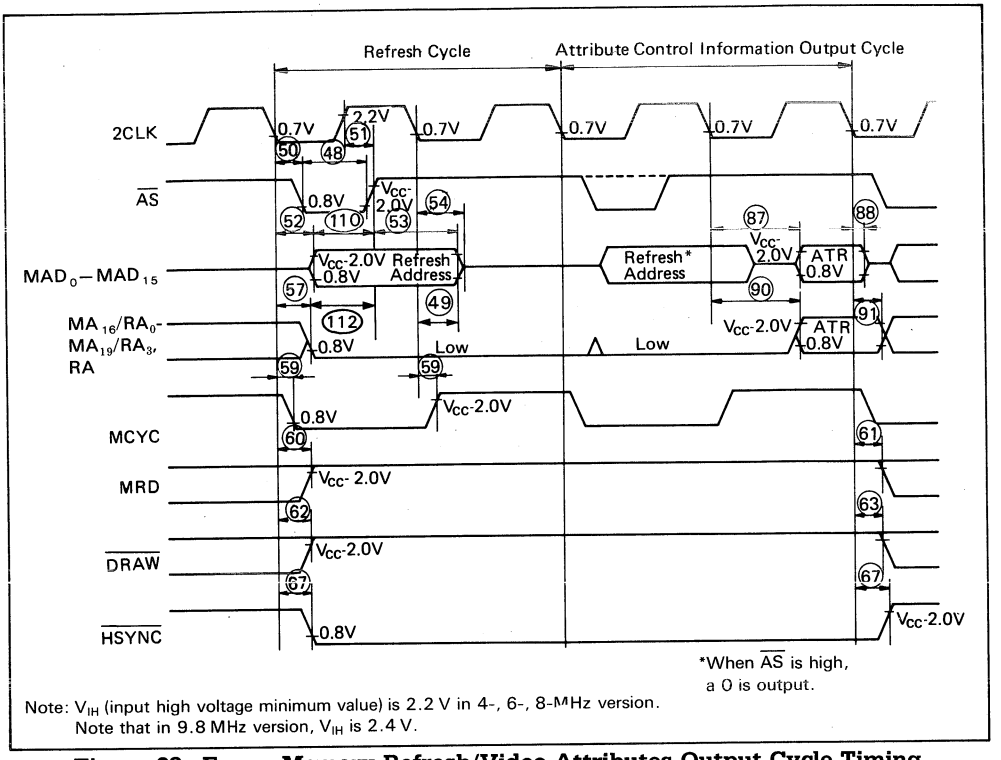
Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 26. Frame Memory Read Cycle Timing (ACRTC ← Frame Memory)



Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 27. Frame Memory Write Cycle Timing (ACRTC → Frame Memory)



Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 28. Frame Memory Refresh/Video Attributes Output Cycle Timing

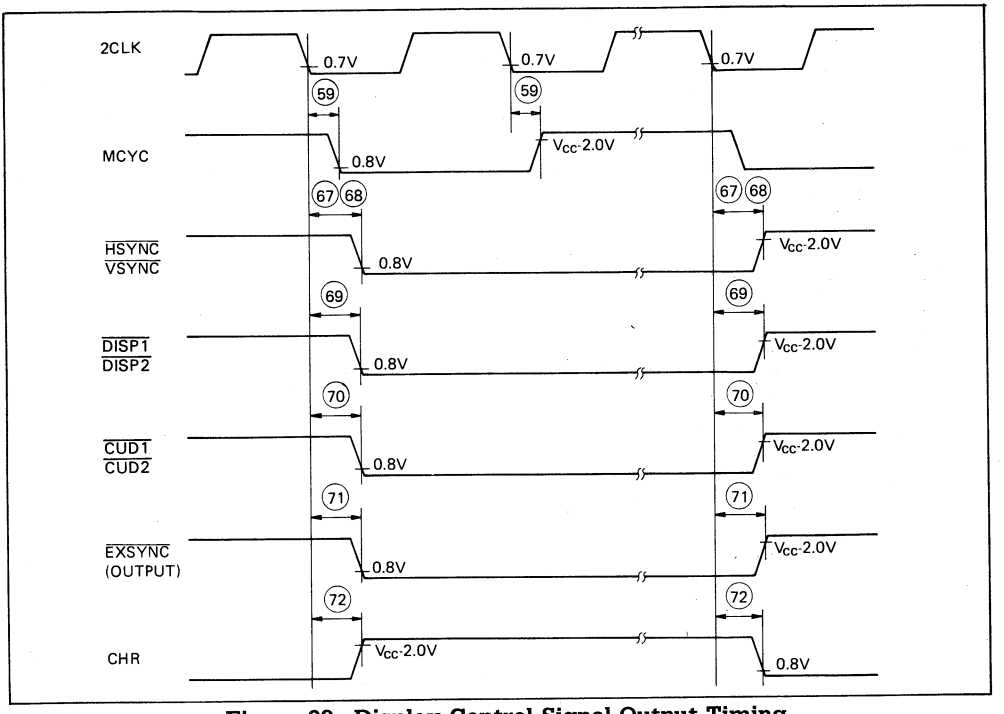
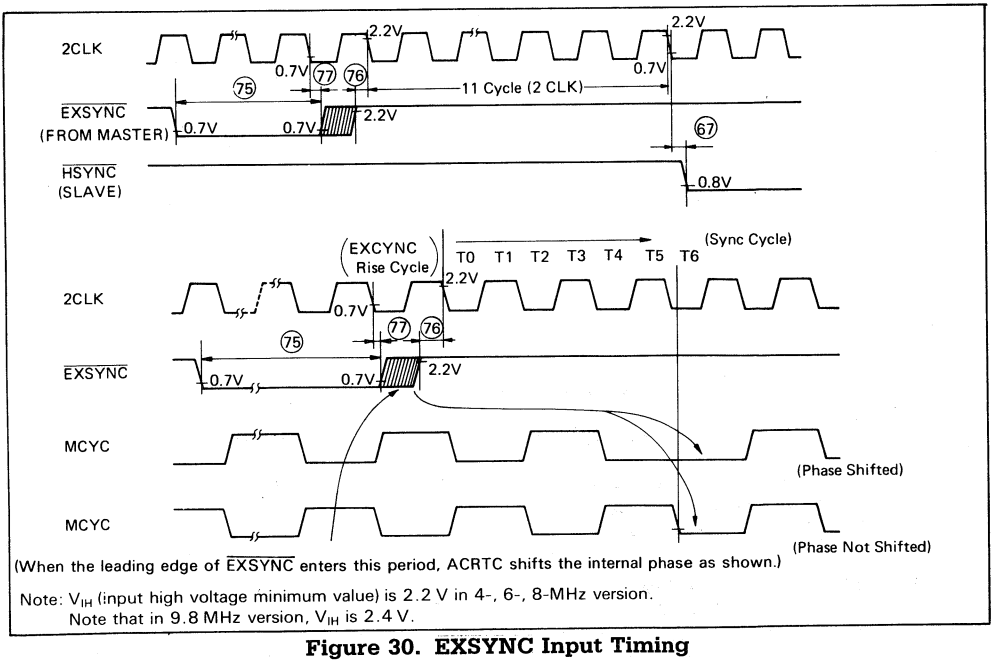


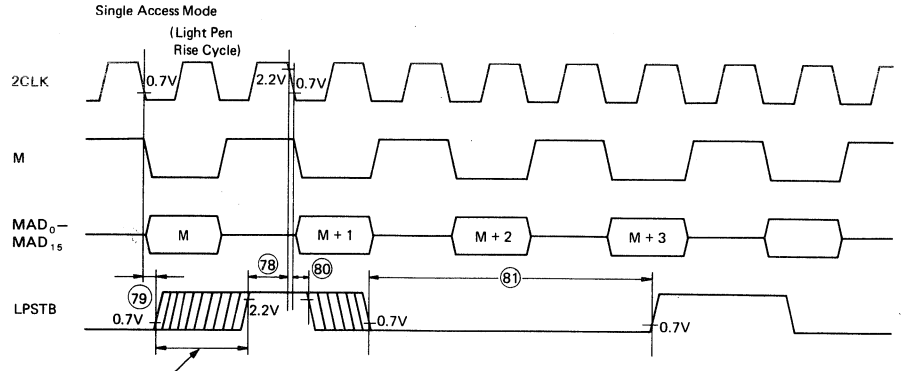
Figure 29. Display Control Signal Output Timing



(When the leading edge of $\overline{\text{EXSYNC}}$ enters this period, ACRTC shifts the internal phase as shown.)

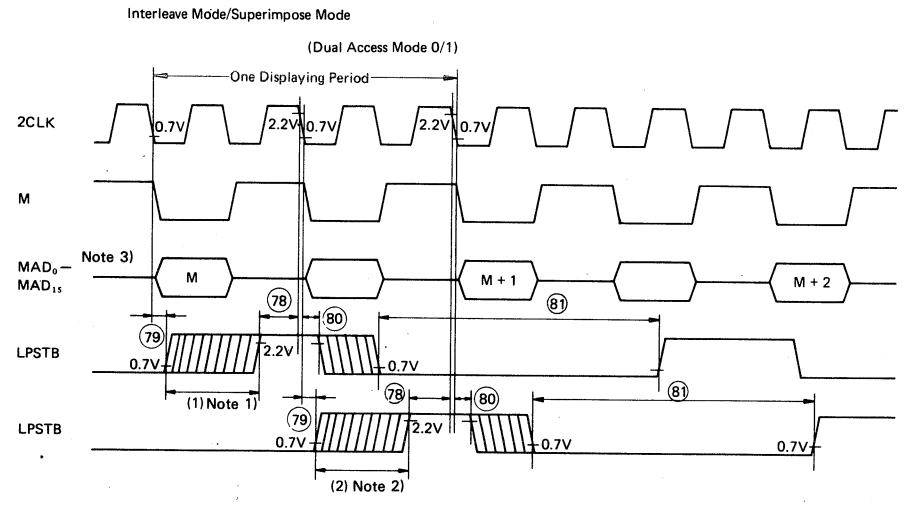
Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 30. $\overline{\text{EXSYNC}}$ Input Timing



Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 31. LPSTB Input Timing (Single Access Mode)



Note: 1. When LPSTB rises in the period (1), memory address M + 1 is set in the lightpen address register.
2. When LPSTB rises in the period (2), memory address M + 2 is set in the lightpen address register.
3. In the interleave mode, memory addresses M, M + 1, M + 2 denote the display address In the superimpose mode, memory addresses M, M + 1, M + 2 denote the display address of the background screen.

Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 32. LPSTB Input Timing (Dual Access Mode)

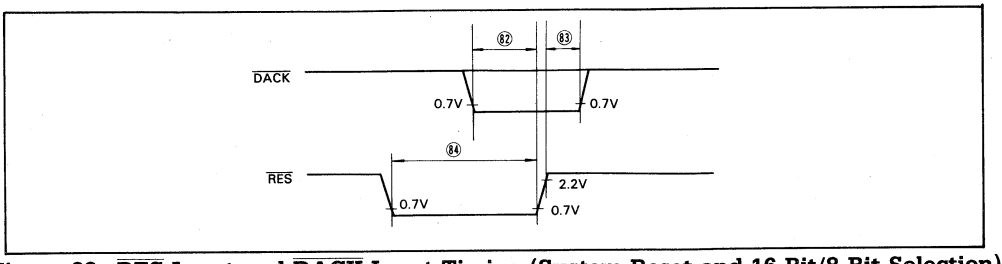
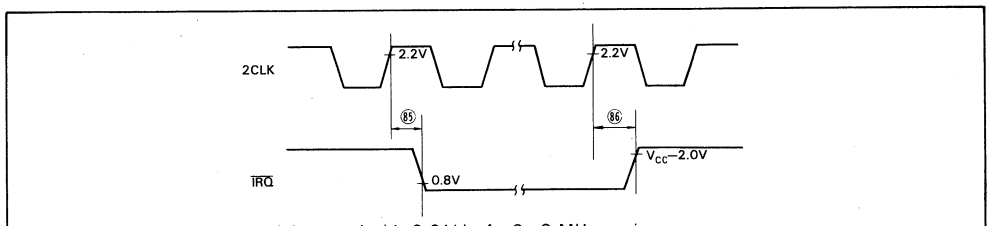
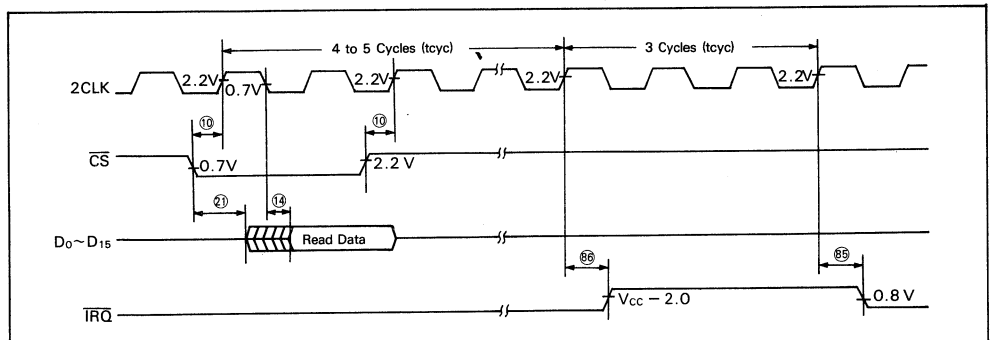


Figure 33. $\overline{RES}$ Input and $\overline{DACK}$ Input Timing (System Reset and 16-Bit/8-Bit Selection)



Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 34. $\overline{IRQ}$ Output Timing



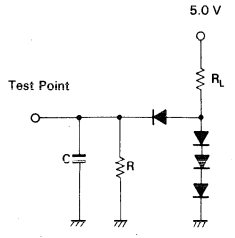
This is an $\overline{IRQ}$ output timing example. In this case, $\overline{IRQ}$ is generated by status flag RFF (Read FIFO Full).

When issuing read commands (RD) which transfer data exceeding Read FIFO space (8 words), the FIFO becomes full, and the command execution pauses (RFF: set, $\overline{IRQ}$: generated). By reading out 1-word data, spare occurs in the FIFO, and the ACRTC resets RFF flag and then negates $\overline{IRQ}$, while on the other hand the ACRTC resumes the internal operation (command execution) to fill the FIFO, and sets RFF flag and then asserts $\overline{IRQ}$ again.

In this case, the timing from $\overline{IRQ}$ negate to assert is 3 cycles (tcyc).

Note: V_{IH} (input high voltage minimum value) is 2.2 V in 4-, 6-, 8-MHz version.
Note that in 9.8 MHz version, V_{IH} is 2.4 V.

Figure 35. $\overline{IRQ}$ Output Timing (Example: Read FIFO Full Interrupt Enable)



Signal	Load Condition
$\overline{D_0}-\overline{D_{15}}$ $\overline{DTACK}$ $\overline{DREQ}$ MAD_0-MAD_{15} $MA_{16}/RA_0-MA_{19}/RA_3$ RA_4 $\overline{VSYNC}$, $\overline{HSYNC}$ $\overline{EXSYNC}$ $\overline{MCYC}$, $\overline{AS}$, MRD $\overline{DRAW}$, CHR $\overline{DISP1}$, $\overline{DISP2}$ $\overline{CUD1}$, $\overline{CUD2}$	R_L = 1.8 kΩ C = 40 pF R = 10 kΩ All diodes are 1S2074(H)'s or the equivalent.

Figure 36. Test Load Circuit A

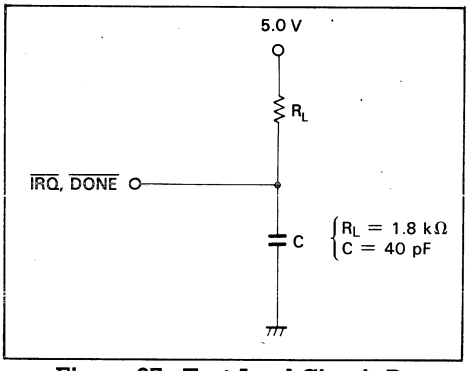


Figure 37. Test Load Circuit B

Refer to user's manual (No. ADE-602-010C) and application note (No. ADE-502-006A) for detail of this product.

HD63485

Graphic Memory Interface Controller (GMIC)

Description

The HD63485 LSI belongs to the ACRTC (advanced CRT controller) family. It provides memory access control to frame buffers for graphic display and drawing. Incorporating bus driver circuits and a DRAM (dynamic RAM) interface, the GMIC allows direct connection to DRAM with no external circuits. Its main function include address data latch, DRAM row and column address multiplexing, supplying $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{WE}$, and other signals, and generating the 2CLK signal for the ACRTC. Using the Hi-BiCMOS process, the HD63485 achieves high speed memory access with low power dissipation.

Type of Products

Part No.	Speed	Package
HD63485PS32	32MHz	64-pin Plastic Shrink DIP
HD63485PS48	48MHz	(DP-64S)
HD63485PS64	64MHz	
HD63485CP32	32MHz	68-pin PLCC
HD63485CP48	48MHz	(CP-68)
HD63485CP64	64MHz	

Features

- Dirves frame buffer memory directly (I_{OL} = 24 mA max)
- Generates DRAM signal : row and column addresses, $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{WE}$, etc
- High-speed dot rate input (64 MHz max)
- Direct ACRTC interface
- Generates horizontal scrolling control signals
- Generates load signals for horizontal smooth scrolling
- Programmable address incerment mode
- Generates 2CLK signal
- TTL-compatible input/output
- Single +5 V power supply
- Low power dissipation

Pin Description

Figure 1 shows the pin arrangement for the 64-pin shrink-type DIP and the 68-pin PLCC packages. Pins marked with * are bus drivers, which can handle a maximum output current I_{OL} of 24mA. Table 1 describes the pins.

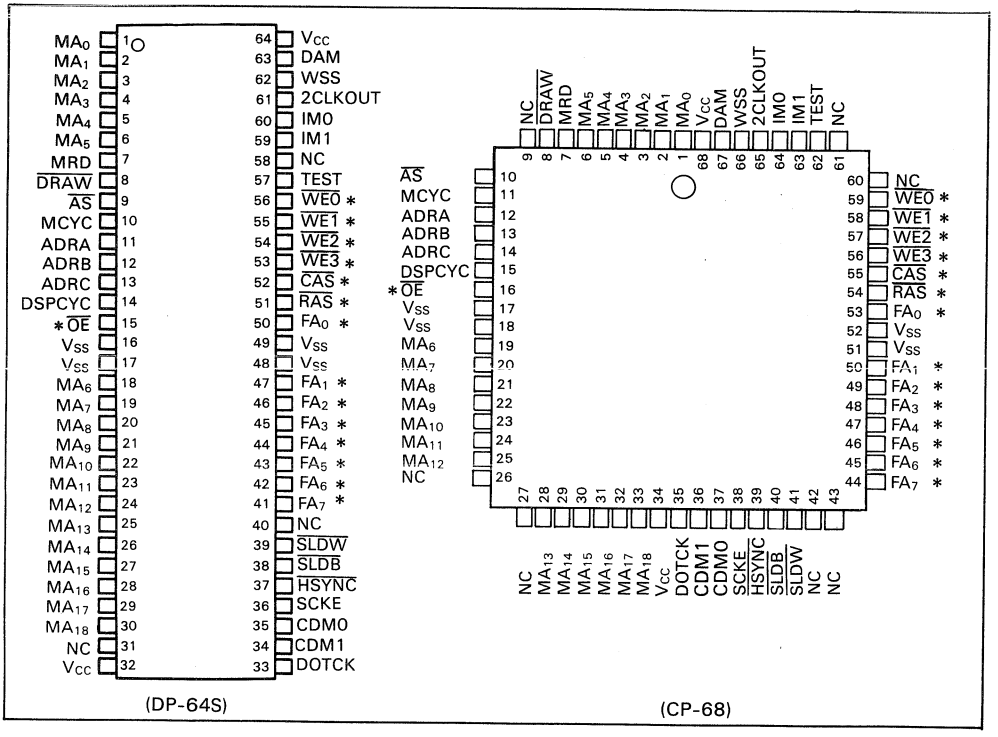


Figure 1. Pin arrangement

Power Supply (V_{SS}, V_{CC})

V_{SS} and V_{CC} are the GMIC power supply pins. V_{CC} pins are +5 V ±5 % supply pins. V_{SS} are the ground pins. Be sure to connect all four V_{SS} pins to ground and both V_{CC} pins to the power supply.

Table 1. Pin Description

Signal	Pin Number DIP-64	PLCC-68	I/O	Description
V_{CC}	32,64	34,68		+5 V power supply
V_{SS}	16,17, 48,49	17,18, 51,52		Ground
CDM1, CDM0	34,35	36,37	I	Clock division ratio
DAM	63	67	I	Dual access mode
IM1, IM0	59,60	63,64	I	Increment mode
WSS	62	66	I	Window smooth scroll
DOTCK	33	35	I	Dot clock
TEST	57	62	I	Test
2CLKOUT	61	65	O	Clock
MCYC	10	11	I	Memory cycle
$\overline{DRAW}$	8	8	I	Draw
MRD	7	7	I	Memory read
$\overline{AS}$	9	10	I	Address strobe
MA18-MA0	30-18, 6-1	33-28, 25-19, 6-1	I	Memory address bus
$\overline{HSYNC}$	37	39	I	Horizontal sync
$\overline{RAS}$	51	54	O	Row address strobe
$\overline{CAS}$	52	55	O	Column address strobe
$\overline{WE3}$-$\overline{WE0}$	53-56	56-59	O	Write enable
$\overline{OE}$	15	16	O	Output enable
FA7-FA0	41-47, 50	44-50, 53	O	Frame buffer address
ADRA-ADRC	11-13	12-14	O	Address
DSPCYC	14	15	O	Display cycle
SCKE	36	38	O	Shift clock enable
$\overline{SLDB}$, $\overline{SLDW}$	38, 39	40, 41	O	Shift load signals

Program Pins

Clock Division Ratio (CDM1, CDM0): The CDM1 and CDM0 inputs determine the division ratio used to generate 2CLKOUT for the ACRTC from the DOTCK input. See table 2.

Dual Access Mode (DAM): The DAM input sets the access mode as shown in table 3.

Increment Mode (IM 1, IM 0): The IM 1 and IM 0 inputs determine the addresses sent from memory addresses (MA 18-MA 0) as the frame buffer output (FA 7-FA 0) to accommodate different DRAM types. Table 4 shows the memory address outputs corresponding to the IM 1 and IM 0 settings. Note that the frame buffer addresses (FA 7-FA 0) have multiplexed memory address outputs.

IM inputs are closely related to the graphic address increment (GAI) of the ACRTC (see ACRTC user's manual).

Window Smooth Scroll (WSS): When the WSS input is low (0), each base screen can be scrolled in single access mode, dual access mode 0, and dual access mode 1. The $\overline{SLDB}$ signal contains the scrolling data.

When the WSS input is high (1), the window screen can be smooth scrolled in dual access mode 1. The $\overline{SLDW}$ signal contains the scrolling data.

Operation Control Signals

Dot Clock (DOTCK): The DOTCK input must be the same clock that is supplied to the shift register for video signal generation. Dot clock frequency is determined by the horizontal display resolution (pixel count) and the display period of one horizontal scan.

Test (TEST): The TEST input is used for manufacturing operational testing. It must be fixed low when the GMIC is mounted in a system.

ACRTC Interface Signals

Clock (2CLK): The 2CLKOUT clock output is a basic clock for the ACRTC's internal operation. The GMIC generates 2CLKOUT by dividing the high-speed dot clock by the ratio determined by the CDM 1 and CDM 0 inputs.

Table 2. Clock Division Ratio

CDM 1	CDM 0	Division Ratio
0	0	Not allowed
0	1	Divide by 4
1	0	Divide by 8
1	1	Divide by 16

Table 3. Access Modes

DAM	Access Mode
0	Single access mode
1	Dual access mode

Table 4. Increment Mode

IM 1	IM 0	Increment Mode	Address Output to FA 7-FA 0	Address Output to ADRC-ADRA
0	0	+1	MA_{15}-MA_8, MA_7-MA_0	MA_{18}, MA_{17}, MA_{16}
0	1	+2	MA_{16}-MA_9, MA_8-MA_1	MA_0, MA_{17}, MA_{18}
1	0	+4	MA_{17}-MA_{10}, MA_9-MA_2	MA_0, MA_1, MA_{18}
1	1	+8	MA_{18}-MA_{11}, MA_{10}-MA_3	MA_0, MA_1, MA_2

Memory Cycle (MCYC): The MCYC input indicates the ACRTC's frame buffer access timing. MCYC is low when the ACRTC is in the address cycle, and high when the ACRTC is in the data cycle.

Draw ($\overline{\text{DRAW}}$): The $\overline{\text{DRAW}}$ input indicates whether the ACRTC memory cycle is a drawing cycle. $\overline{\text{DRAW}}$ is low during drawing cycle, and high otherwise. The GMIC uses $\overline{\text{DRAW}}$ to recognize display cycles, and also to generate DRAM control signals ($\overline{\text{WE}}$ 3-$\overline{\text{WE}}$ 0).

Memory Read (MRD): The MRD input controls data transfer between frame buffers and the ACRTC. The ACRTC pulls MRD high when it reads data from the frame buffer, and low when it writes data.

The only exception is when the ACRTC is in superimpose display mode (dual access mode 1). In superimpose display mode, the ACRTC inputs a low level and reads data from a frame buffer in order to indicate that the display cycle is for a superimposed screen (window screen).

Address Storbe ($\overline{\text{AS}}$): The $\overline{\text{AS}}$ input is a latch timing signal for the memory address sent from the ACRTC. Additionally, $\overline{\text{AS}}$ indicates whether memory is begin accessed. For example, for horizontal zooming, the $\overline{\text{SLDB}}$ signal is provided at a lower frequency, corresponding to the lower frequency of $\overline{\text{AS}}$.

Memory Address Bus (MA_{18}-MA_0): The MA_{18}-MA_0 inputs are address signals for frame buffer access, provided by the ACRTC.

Horizontal Sync ($\overline{\text{HSYNC}}$): The $\overline{\text{HSYNC}}$ input is a DRAM refresh cycle control signal to horizontally synchronize CRT displays. The GMIC performs $\overline{\text{RAS}}$ only refresh when $\overline{\text{HSYNC}}$ is low and $\overline{\text{DRAW}}$ is high when $\overline{\text{AS}}$ pulses are input.

Setting $\overline{\text{HSYNC}}$ low informs the GMIC of the end of a raster display. Usually, the ACRTC's $\overline{\text{HSYNC}}$ output supplies this input.

Frame Buffer Access Signals

Row Address Strobe ($\overline{\text{RAS}}$): The GMIC outputs the DRAMs' $\overline{\text{RAS}}$ timing signal on the $\overline{\text{RAS}}$ output.

Column Address Strobe ($\overline{\text{CAS}}$): The GMIC outputs the DRAMs' $\overline{\text{CAS}}$ timing signal on the $\overline{\text{CAS}}$ output.

Write Enable ($\overline{\text{WE}}$ 3-$\overline{\text{WE}}$ 0): The GMIC outputs the DRAM's $\overline{\text{WE}}$ timing signals on the $\overline{\text{WE}}$ outputs. Since $\overline{\text{WE}}$ 3-$\overline{\text{WE}}$ 0 are controlled by the incerment mode (IM 1, IM 0) and by the lower two bits of the address (MA 1, MA 0), the GMIC can directly control up to four memory banks. Up to eight memory banks can be controlled by externally decoding the address (ADRC) and $\overline{\text{WE}}$ 3-$\overline{\text{WE}}$ 0.

$\overline{\text{WE}}$ 3-$\overline{\text{WE}}$ 0 are bus driver that can handle a maximum output current I_{OL} of 24 mA.

Output Enable ($\overline{\text{OE}}$): The GMIC outputs the DRAMs' output timing signal on the $\overline{\text{OE}}$ output. $\overline{\text{OE}}$ is a bus driver that can handle a maximum output current I_{OL} of 24 mA.

Frame Buffer Address (FA 7-FA 0): The GMIC outputs the multiplexed DRAM address on FA 7-FA 0. How the address is multiplexed depends on the incerment mode (table 4). FA 7-FA 0 are bus drivers that can handle a maximum output current I_{OL} of 24 mA.

Address (ADRA-ADRC): The GMIC latches three address bits other than those delivered on the FA 7-FA 0 bits and outputs them on ADRA-ADRC in one memory cycle.

GVAC Control Signals

Shift Clock Enable (SCKE): The SCKE output controls the GVACs' video signal generation shift register. It outputs a control signal for zooming according to the horizontal zoom signal (attribute control signal) from the ACRTC. The GVAC performs horizontal zoom by halting the clock when SCKE is low.

Shift Load Signals ($\overline{\text{SLDB}}$, $\overline{\text{SLDW}}$): The $\overline{\text{SLDB}}$ and $\overline{\text{SLDW}}$ outputs are load signals for the display data of the video signal generation shift register. The $\overline{\text{SLDB}}$ output is used for single access mode, dual access mode 0, and dual access mode 1. The $\overline{\text{SLDW}}$ output controls the window screen in dual access mode 1.

Display Cycle (DSPCYC): The DSPCYC output indicates whether a memory cycle is a display cycle.

DSPCYC is high during display cycle, and low otherwise.

$\overline{\text{AS}}$	$\overline{\text{DRAW}}$	MRD	cycle mode	memory cycle	DSPCYC
	L	L	Drawing Write	Memory Write	L
⌐	L	H	Drawing Read	Memory Read	L
Low pulse	H	L	Window Screen Display	Memory Read	H
	H	H	Backscreen Display	Memory Read	H
H	x	x	—	No Access	L

Functional Description

Figure 2 is a block diagram of the HD63485.

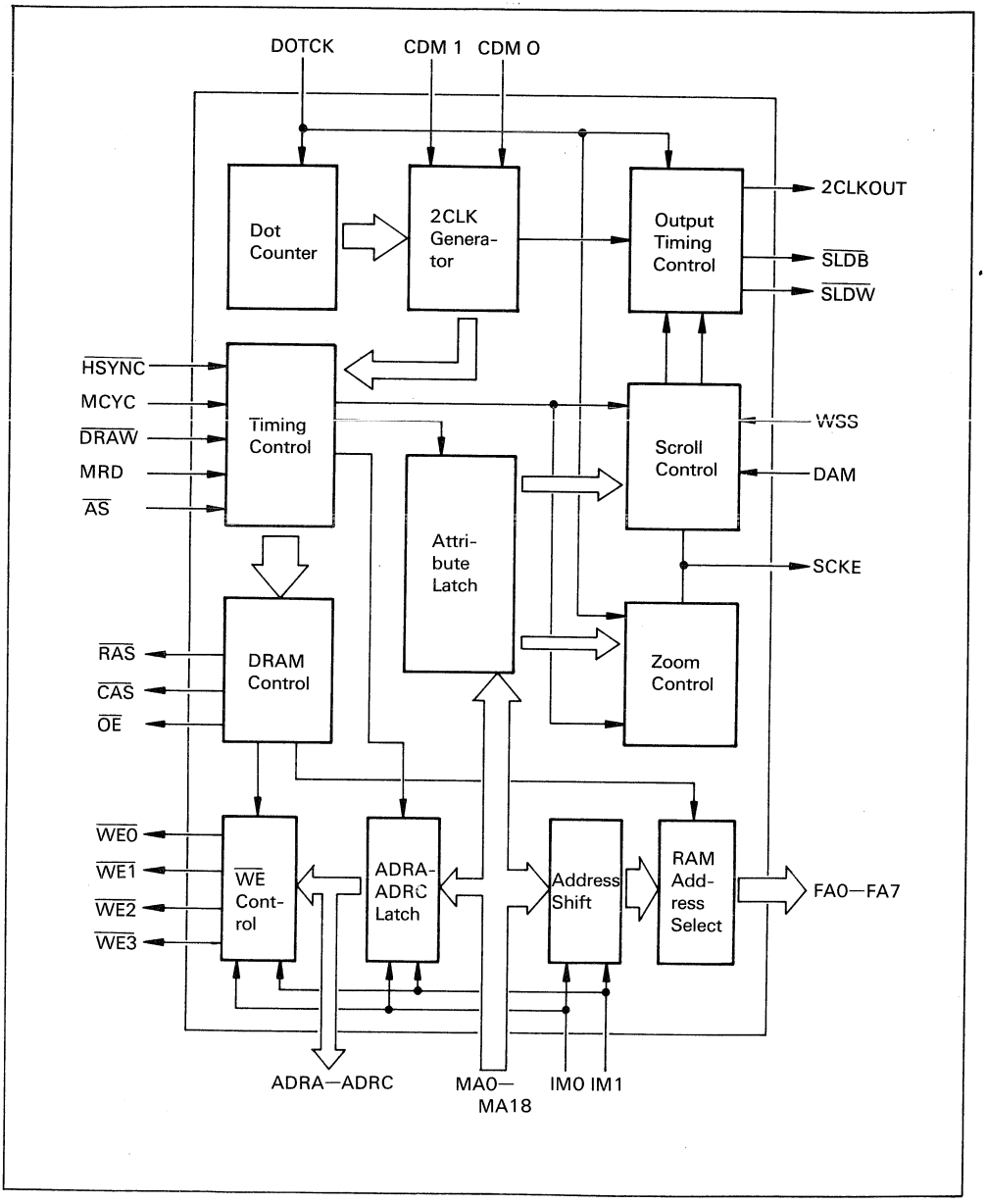


Figure 2. GMIC Block Diagram

2CLK Generator

The 2CLK generator generates 2CLKOUT for the ACRTC and itself by dividing the extemal DOTCK signal. The ratio of DOTCK to 2CLKOUT is set externally by the CDM 1 and CDM 0 inputs.

Attribute Latch

The attribute latch temporarily stores the attribute codes input from the ACRTC on MA 18-MA 0 used for horizontal zoom (HZ 3-HZ 0) and horizontal scroll dot (HSD 3-HSD 0).

Zoom Control

Zoom control generates the SCKE signal from DOTCK to control the GVAC clock for horizontal display zooming.

Scroll Control

Scroll control generates shift load signals ($\overline{\text{SLDB}}$, $\overline{\text{SLDW}}$) which control video signal generation for the GVAC.

Address Shifter

The address shifter stores memory addresses (MA 18-MA 0) sent from the ACRTC. It supplies them to the RAM address section according to the timesharing mode selcted by the graphic increment mode (IM 1, IM 0).

ADRA-ADRC Latches

The ADRA-ADRC latches store the lower or upper address bits which are not supplied to FA 7-FA 0 from the memory address sent from the ACRTC. It outputs them for the whole memory cycle.

RAM Address Selection

The RAM address selection circuits output the timeshared row and column addresses to the frame buffers according to the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ timing.

DRAM Control and $\overline{\text{WE}}$ Control

The DRAM and $\overline{\text{WE}}$ control circuits generate $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{OE}}$, and $\overline{\text{WE}}$ signals for frame buffer access from the ACRTC output signals.

System Description

Applications

The GMIC provides communications between the ACRTC and frame buffers. It contains control circuits for generating signals necessary for the ACRTC to access a frame buffer. In addition it generates basic signals for operating the ACRTC and control signals for the GVAC (graphic video attribute controller), which generates the video signals for a CRT display.

The GMIC's operation mode can be controlled by it program pins. This makes the GMIC suitable for a wide range of operations, from small, low-speed systems to large, high-speed systems, and it allows it to flexibly change to suit system specification changes.

Figure 3 shows a graphic system configuration using an ACRTC, GMIC, and GVACs. Using a GMIC for interface to the frame buffers and a GAVCs for CRT video signal generation creates a flexible, high-performance graphic system with a minimum component count.

System Configuration

The typical graphic system application for the GMIC and GVAC shown in figure 3 uses two GVACs, but the number of GVACs used can be changed to accommodate CRT resolution and colorigrey scale per pixels for various applications.

The GMIC receives memory addresses (MAD_{15}-MAD_0, MA_{18}-MA_{16}), address strobe ($\overline{AS}$), memory cycle (MCYC), draw ($\overline{DRAW}$), memory read ($\overline{MRD}$), and other ACRTC outputs, and generates control signals for the frame buffers. The frame buffers are generally constructed from DRAM, since graphic systems require large memory capacity frame buffers. The GMIC therefore uses a DRAM-compatible multiplexing system. Through this multiplexing, the GMIC delivers address outputs and control signals such as $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{OE}$, acting as a direct interface between the ACRTC and the frame buffers. Furthermore, the GMIC generates a basic clock signal for the ACRTC (2CLK) by dividing the high-speed dot clock. It also generates control signals for the GVAC.

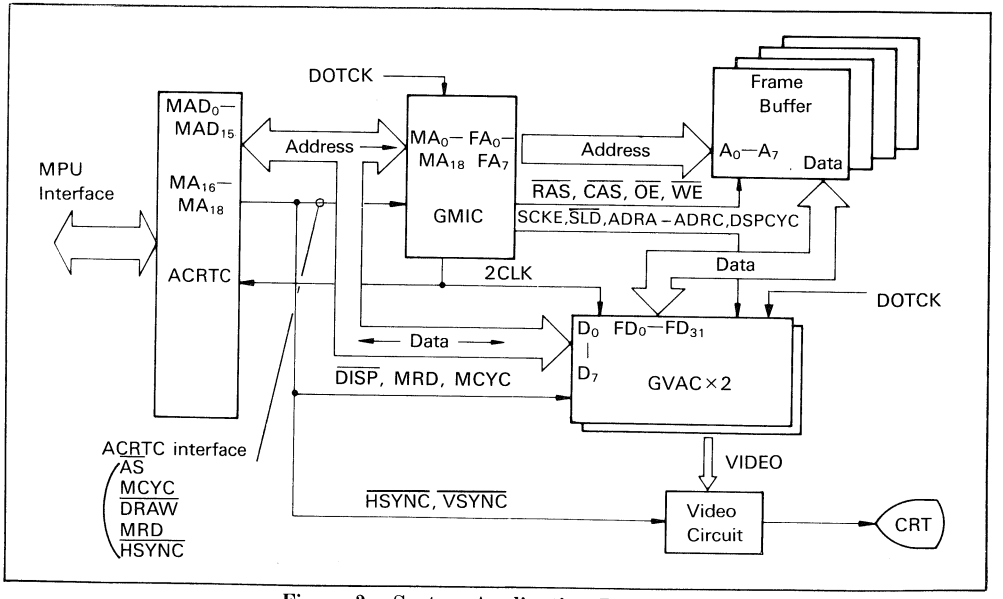


Figure 3. System Application Example

Operation

Basic Clock

Timing for signals to and from the GMIC is based on the dot clock (DOTCK) supplied to the GMIC and the clock output (2CLKOUT) generated by the GMIC. 2CLKOUT is generated by dividing the DOTCK input by the ratio selected by the CDM 1 and CDM 0 inputs. Figure 4 shows the relation between DOTCK and 2CLKOUT. The frequency of DOTCK depends on the speed and resolution of the CRT display. DOTCK (in MHz) equals the horizontal resolution (pixels/raster line) by the horizontal display raster scan period (μs per raster).

f_{DOTCK} = [Horizontal resolution (pixels/raster)] / [Horizontal display period (μs)] (MHz)

The dot clock dividing mode should be chosen considering the frame buffer cycle time and the speed of the ACRTC used. For high-speed drawing, a smaller division ratio should be used to supply a higher frequency chock to the ACRTC. For applications using low-speed frame buffers and extermal circuits, larger division rations should be selected to supply a lower frequency clock to the ACRTC.

Note: The maximum DOTCK frequency is sometimes limited by the DOTCK division ratio. If the division ratio is 8 or 16, the maximum frequency is allowed, but if a division ratio of 4 is used, the DOTCK frequency is limited to 32 MHz.

Frame Buffer Control

The GMIC is designed for use with DRAM frame buffer memories. Therefore, the GMIC generates DRAM access signals $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{OE}$. Also, it outputs row and column addresses to the RAM, timeshared according to $\overline{RAS}$ and $\overline{CAS}$.

Table 5 shows the GMIC frame buffer access modes. The memory cycles are roughly divided into six types. They are distinguished by the ACRTC's

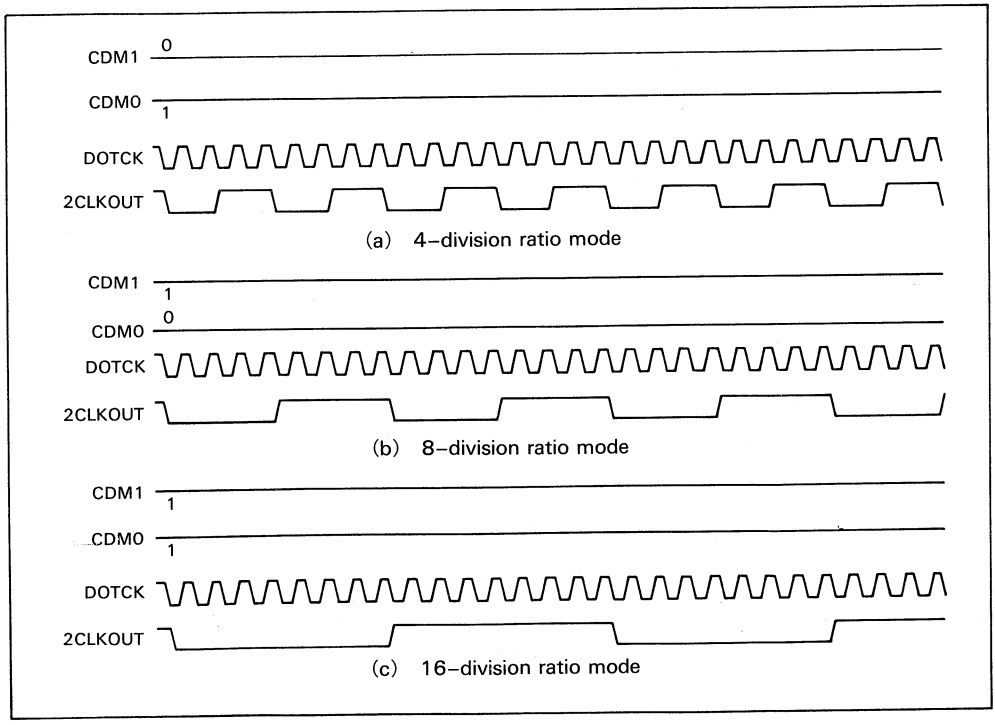


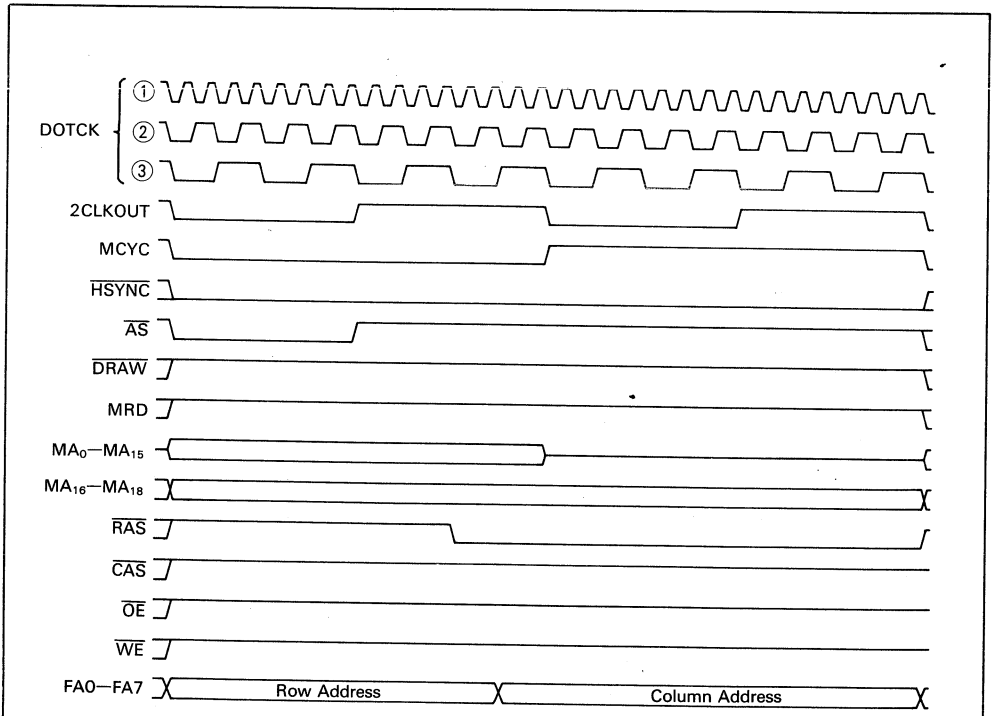
Figure 4. DOTCK Division

output signals ($\overline{AS}$, $\overline{HSYNC}$, $\overline{DRAW}$, MRD). Figure 5 shows $\overline{RAS}$ only refresh cycle timing. Figure 6 and 7 show read and write cycle timing, respectively.

Table 5. Memory Cycles

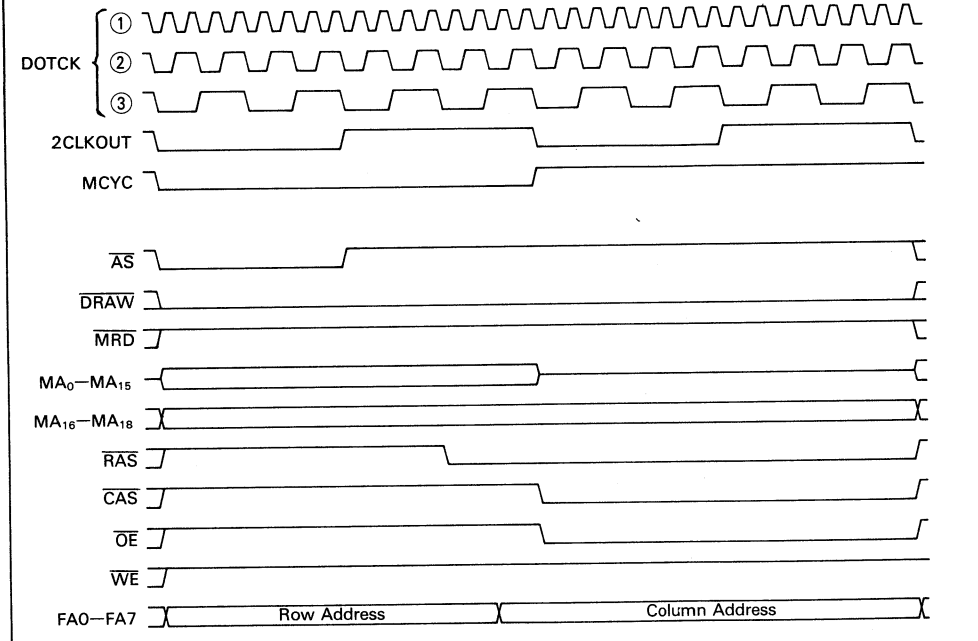
$\overline{AS}$	$\overline{HSYNC}$	$\overline{DRAW}$	MRD	Cycle Mode	Memory Cycle
Low	Low	High	High	Refresh cycle	RAS only refresh
pulse		Low	Low	Drawing write cycle	Memory write
		Low	High	Drawing read cycle	Memory read
	High	High	Low	Window screen cycle	Memory read
		High	High	Background screen display	Memory read
High		High	High		No access

Note: The GMIC performs a frame buffer refresh during a horizontal sync period ($\overline{HSYNC}$=low), with $\overline{DRAW}$ high and $\overline{AS}$ pulse applied. During a refresh cycle, only $\overline{RAS}$ is output. $\overline{CAS}$ and $\overline{OE}$ are not output.



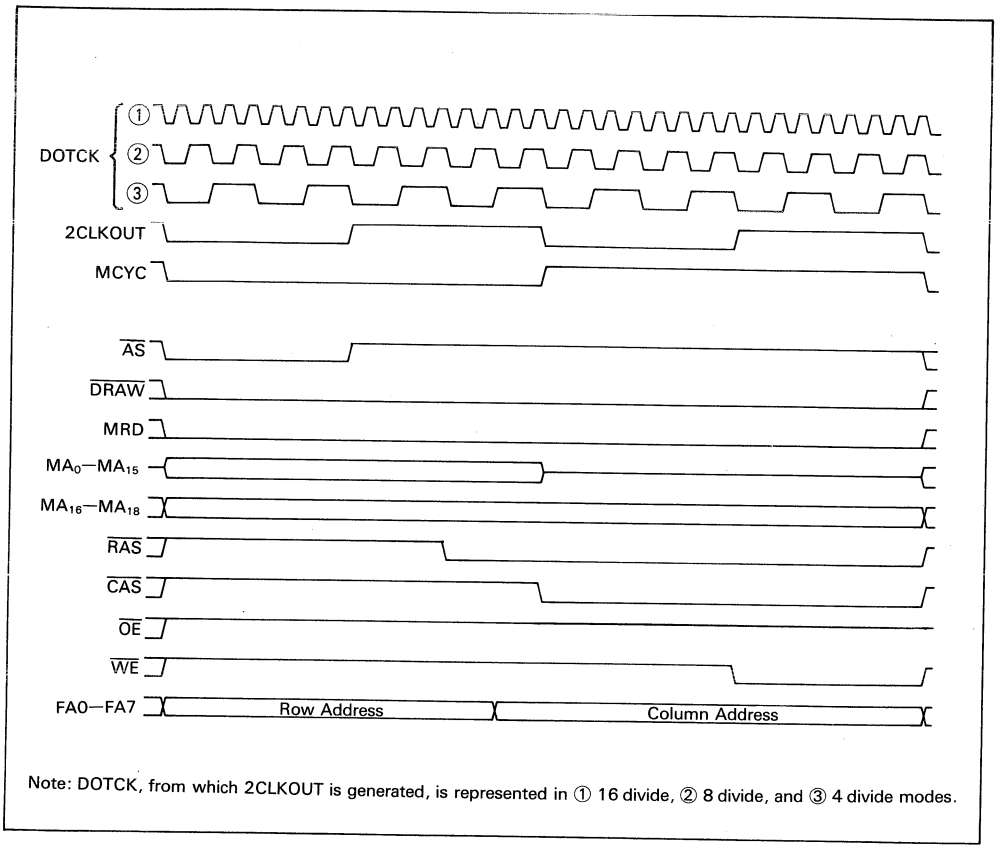
Note: DOTCK, from which 2CLKOUT is generated, is represented in ① 16 divide, ② 8 divide, and ③ 4 divide modes.

Figure 5. $\overline{RAS}$ Only Refresh Timing



Note: DOTCK, from which 2CLKOUT is generated, is represented in ① 16 divide, ② 8 divide, and ③ 4 divide modes.

Figure 6. Read Cycly Timing



Note: DOTCK, from which 2CLKOUT is generated, is represented in ① 16 divide, ② 8 divide, and ③ 4 divide modes.

Figure 7. Write Cycle Timing

Table 6 shows the relation between frame buffer addresses (FA7-FA0) and memory address (MA_{18}-MA_0), as determined by the increment mode (IM1, IM0). FA pins provide multiplexed addresses for DRAM, and the remaining address bits are output at ADRA-ADRC. The GMIC has four increment modes: +1, +2, +4, and +8. This mode should be set the same as the ACRTC's GAI (graphic address increment) mode. GAI mode is a bit set according to the frame buffer, which sets the increment mode for display address output for a graphic address.

Graphic drawing data is processed on a single word (16 bit) basis. The ACRTC sets the bit count per pixel by the graphic bit mode (GBM) in its command control register, which is more suitable for multicolor/grey scale systems. However, if one word is definitely read from a frame buffer during each display cycle, four pixels per word can be displayed when GBM is set to 4 bits per pixel. To implement a CRT display having a 1 bit per pixel resolution (16 pixels/word), an input clock four times faster must be supplied to the ACRTC. For more multicolor/grey scale systems, an ever faster clock is required.

On the other hand, if several words are read from a frame buffer during each display cycle, and the CRT can have a higher resolution without speeding up the ACRTC input clock. For example, in the +4 increment mode, when GBM is set to 4 bits/pixel, 4 words (64 bits) containing 16 pixels can be read in one display cycle.

For one word (16 bits) read during one display cycle, the GAI must be set to 000.

When 32/64/128 bits are required during one display cycle for a high-resolution or multicolor/grey scale system, GAI must be set to 001/010/011

Table 6. Frame Buffer and Memory Addresses

	+1 Mode		+2 Mode		+3 Mode		+4 Mode	
Frame Address	**Row**	**Col**	**Row**	**Col**	**Row**	**Col**	**Row**	**Col**
FA0	MA0	MA8	MA1	MA9	MA2	MA10	MA3	MA11
FA1	MA1	MA9	MA2	MA10	MA3	MA11	MA4	MA12
FA2	MA2	MA10	MA3	MA11	MA4	MA12	MA5	MA13
FA3	MA3	MA11	MA4	MA12	MA5	MA13	MA6	MA14
FA4	MA4	MA12	MA5	MA13	MA6	MA14	MA7	MA15
FA5	MA5	MA13	MA6	MA14	MA7	MA15	MA8	MA16
FA6	MA6	MA14	MA7	MA15	MA8	MA16	MA9	MA17
FA7	MA7	MA15	MA8	MA16	MA9	MA17	MA10	MA18
ADRA	MA16		MA0		MA0		MA0	
ADRB	MA17		MA17		MA1		MA1	
ADRC	MA18		MA18		MA18		MA2	

Table 7. $\overline{WE}$ Output Timing

Increment	Input						Output			
Mode	**DRAW**	**MRD**	**MA1**	**MA0**	**IM1**	**IM0**	**$\overline{WE3}$**	**$\overline{WE2}$**	**$\overline{WE1}$**	**$\overline{WE0}$**
	H	x	x	x	x	x	H	H	H	H
	L	H	x	x	x	x	H	H	H	H
+1	L	L	x	x	0	0	L	L	L	L
+2	L	L	x	0	0	1	H	L	H	L
	L	L	x	1	0	1	L	H	L	H
+4/+8	L	L	0	0	1	x	H	H	H	L
	L	L	0	1	1	x	H	H	L	H
	L	L	1	0	1	x	H	L	H	H
	L	L	1	1	1	x	L	H	H	H

respectively.

Table 7 shows the output condition of the write enable signals $\overline{WE3}$-$\overline{WE0}$. The four write enable signals can directly control up to four memory banks. The $\overline{WE}$ output is determined by $\overline{DRAW}$, MA0, IM1, and IM0.

Video Shifter Shift Load Signals ($\overline{SLDB}$, $\overline{SLDW}$)

$\overline{SLDB}$ and $\overline{SLDW}$ load timing signals control the timing of display data input from a frame buffer to the video signal generation shift register (parallel-to-serial conversion circuit). $\overline{SLDB}$ is used for base screen in single access mode, dual access mode 0, and dual access mode 1. $\overline{SLDW}$ is used for window screens in dual access mode 1.

Relation of Access Mode and WSS to $\overline{SLDB}$ and $\overline{SLDW}$: Table 8 shows the relationship between access modes, WSS, and $\overline{SLDB}$ and $\overline{SLDW}$. When WSS=0 in single access or dual access mode 0, $\overline{SLDB}$ output timing can be varied according to the amount of scrolling for one display cycle. $\overline{SLDW}$ is not output.

When WSS=0 in dual access mode 1 for the bese screen, $\overline{SLDB}$ output timing can be varied to accommodate smooth scrolling according to the horizontal scroll dot attribute control signals (HSD3-HSD0) supplied by the ACRTC. The $\overline{SLDW}$ signal is asserted for one period of the last dot clock during a display cycle. Its output cannot be varied for scrolling.

When WSS=1, for the window in dual access mode 1, $\overline{SLDB}$ signal is asserted and fixed for one period of the last dot clock of one display cycle, where as $\overline{SLDW}$ timing can be varied according to scrolling amount in one display cycle.

Amount of Scrolling and Output Timing: Figure 8 shows the output timing of the shift load signals ($\overline{SLDB}$, $\overline{SLDW}$) for different amounts of scrolling. With increased scrolling, the load signal is output earlier by one dot clock.

Figure 9, 10, and 11 show $\overline{SLDB}$ and $\overline{SLDW}$ timing for single access, dual access mode 0, and dual access mode 1, respectively. Figure 12, 13, and 14 show $\overline{SLDB}$ timing for double and triple zooming.

Table 9 shows the attribute codes set for the ACRTC and the corresponding scrolling amounts. Table 10 shows the relationship between the GMIC dot clock division ratios and GVAC shift register lengths in corresponding access modes. Display colors are determined by the shift register length and amount of display data simultaneously read set in the ACRTC's GAI. The single and dual access modes are described in the ACRTC User's Manual, 3. 2 CRT Interface.

Table 8. WSS, Access Mode, Shift Load Signals

WSS	Access Mode	$\overline{SLDB}$	$\overline{SLDW}$
0	Single access, Dual access 0	Scrolling amount is permitted	No output
	Dual access 1, Base screen	Scrolling amount is permitted	Scrolling impossible
1	Dual access 1, Base screen	Scrolling impossible	Scrolling amount is permitted

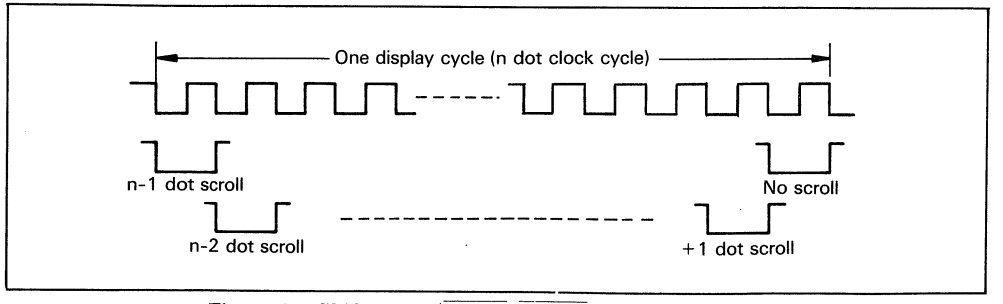


Figure 8. Shift Load ($\overline{SLDB}$, $\overline{SLDW}$) Output Timing

Table 9. ACRTC Attribute Codes and Scrolling Amounts

Shift Bit Length	HSD5	HSD4	HSD3	HSD2	HSD1	HSD0	Scroll Dot Count
16 bits	x	x	0	0	0	0	0
	x	x	0	0	0	1	1
	x	x	0	0	1	0	2
				⋮			
	x	x	1	1	1	0	14
	x	x	1	1	1	1	15
32 bits	x	0	0	0	0	0	0
	x	0	0	0	0	1	1
	x	0	0	0	1	0	2
				⋮			
	x	1	1	1	1	0	30
	x	1	1	1	1	1	31
64 bits	0	0	0	0	0	0	0
	0	0	0	0	0	1	1
	0	0	0	0	1	0	2
				⋮			
	1	1	1	1	1	0	62
	1	1	1	1	1	1	63

Note: The attribute code from the ACRTC supplies HSD3-HSD0, and memory address MA1 and MA0 supply HSD5 and HSD4. If these memory address bits are used (MA1 for 64-bit shifts, MA0 for 32-bit shifts), they must not be changed during one horizontal period.

Table 10. GMIC Division Ratio and GVAC Shift Lengths

Division Ratio	Single Access	Dual Access
Divide by 4	8 dot shift	16 dot shift
Divide by 8	16 dot shift	32 dot shift
Divide by 16	32 dot shift	64 dot shift (note)

Note: This mode cannot be used directly because the maximum shift register length is 32 dots.

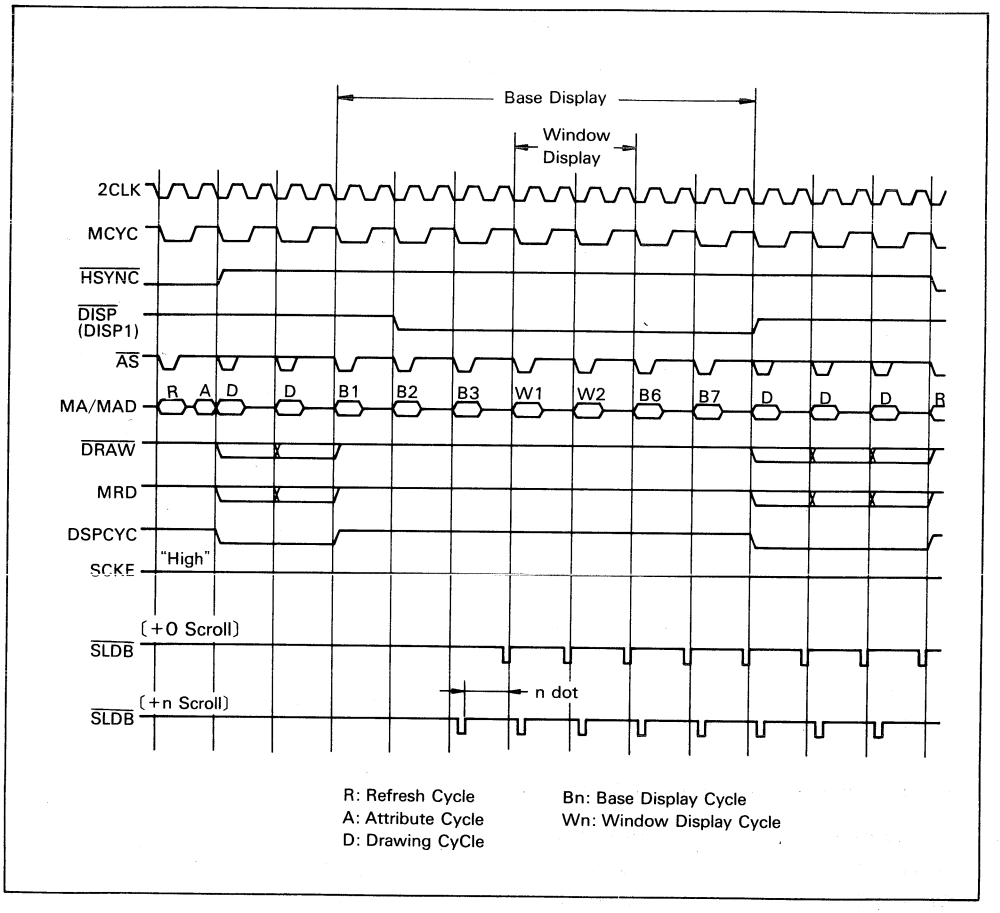


Figure 9. $\overline{\text{SLDB}}$ Timing (Single Access Mode)

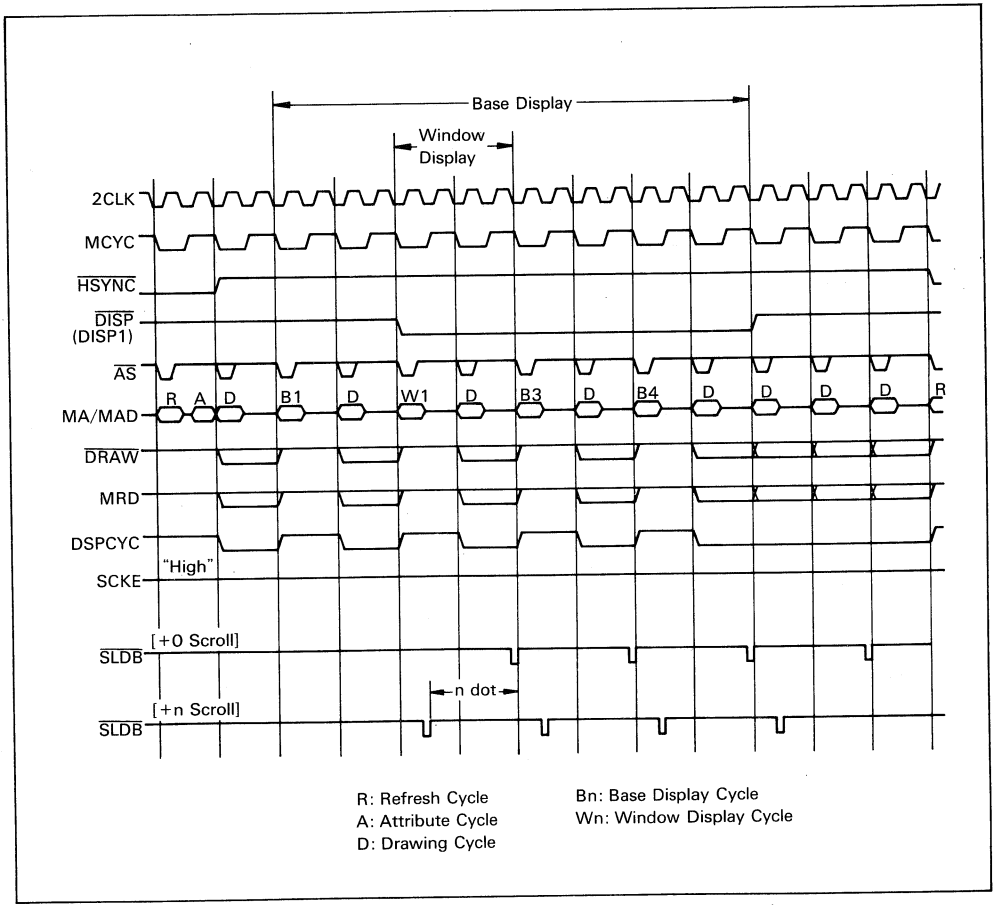


Figure 10. $\overline{\text{SLDB}}$ Timing (Dual Access Mode 0)

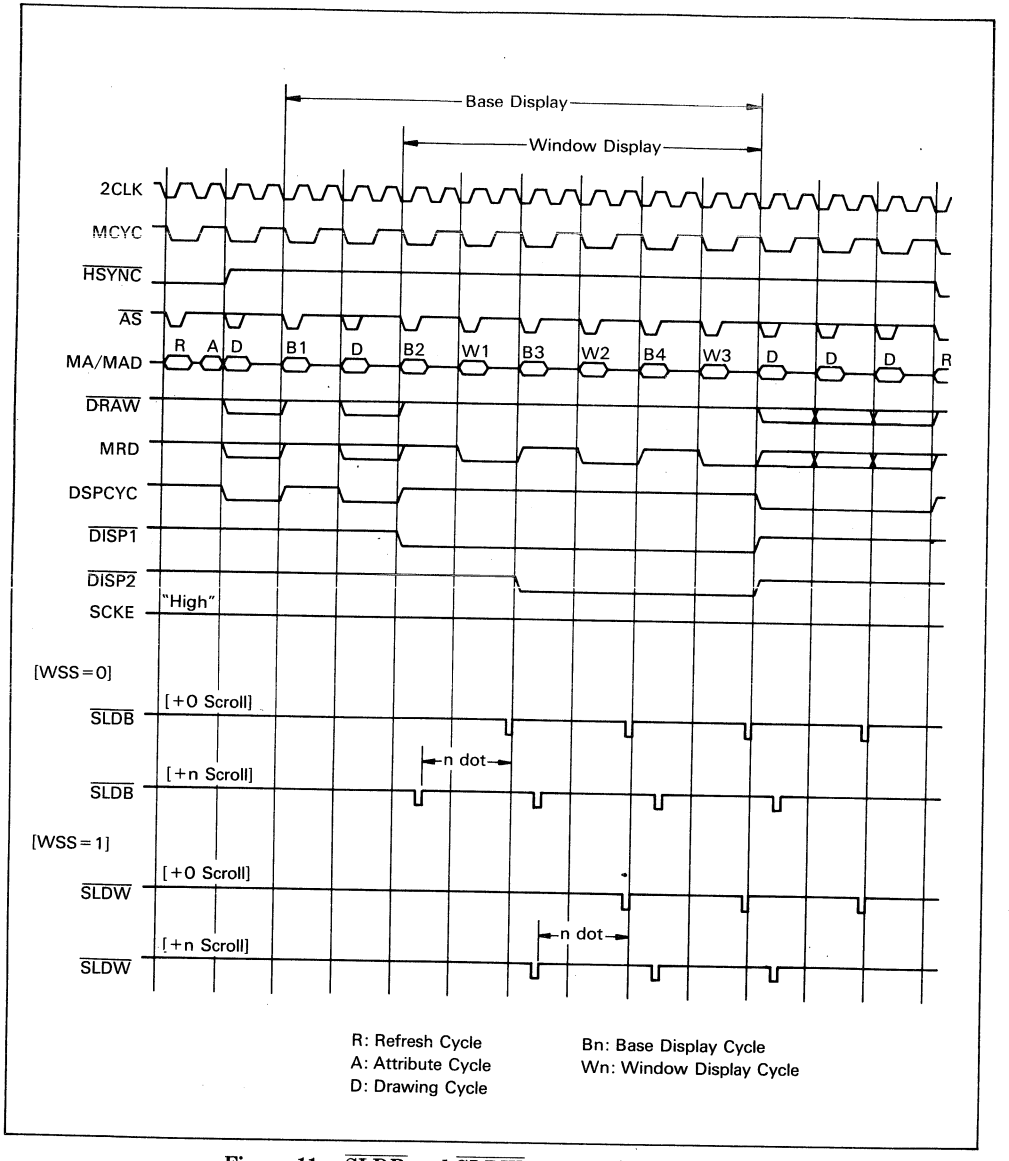


Figure 11. $\overline{\text{SLDB}}$ and $\overline{\text{SLDW}}$ Timing (Dual Access Mode 1)

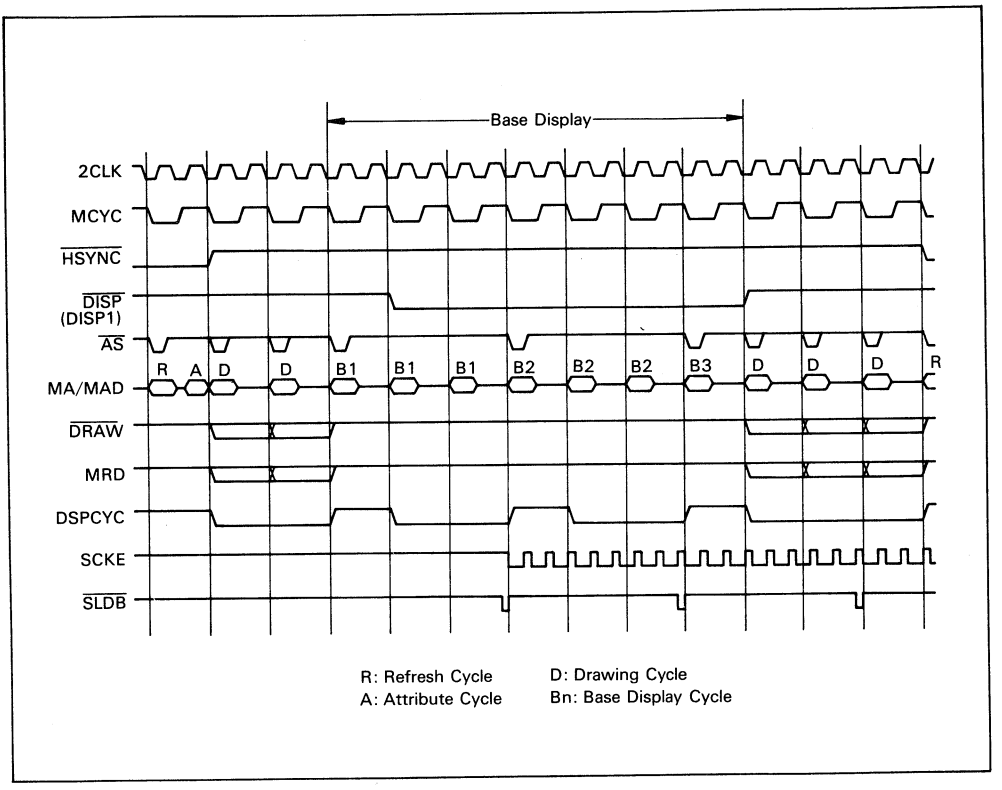


Figure 12. Zoom Display Timing (Single Access Mode, Triple Zoom)

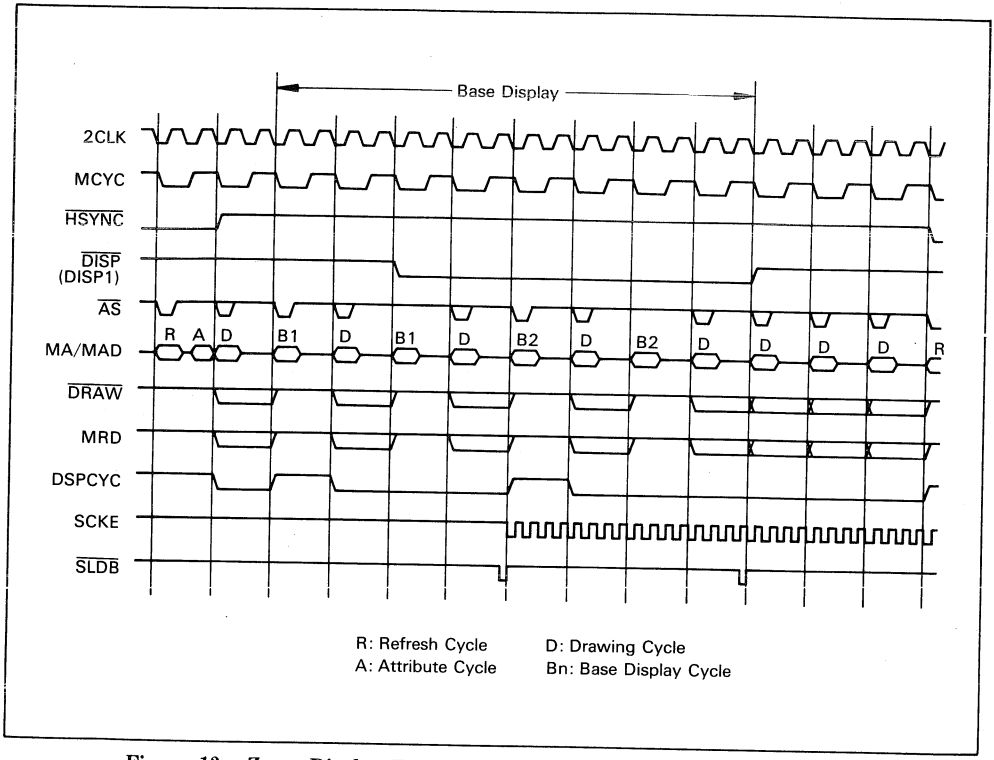


Figure 13. Zoom Display Timing (Dual Access Mode 0, Double Zoom)

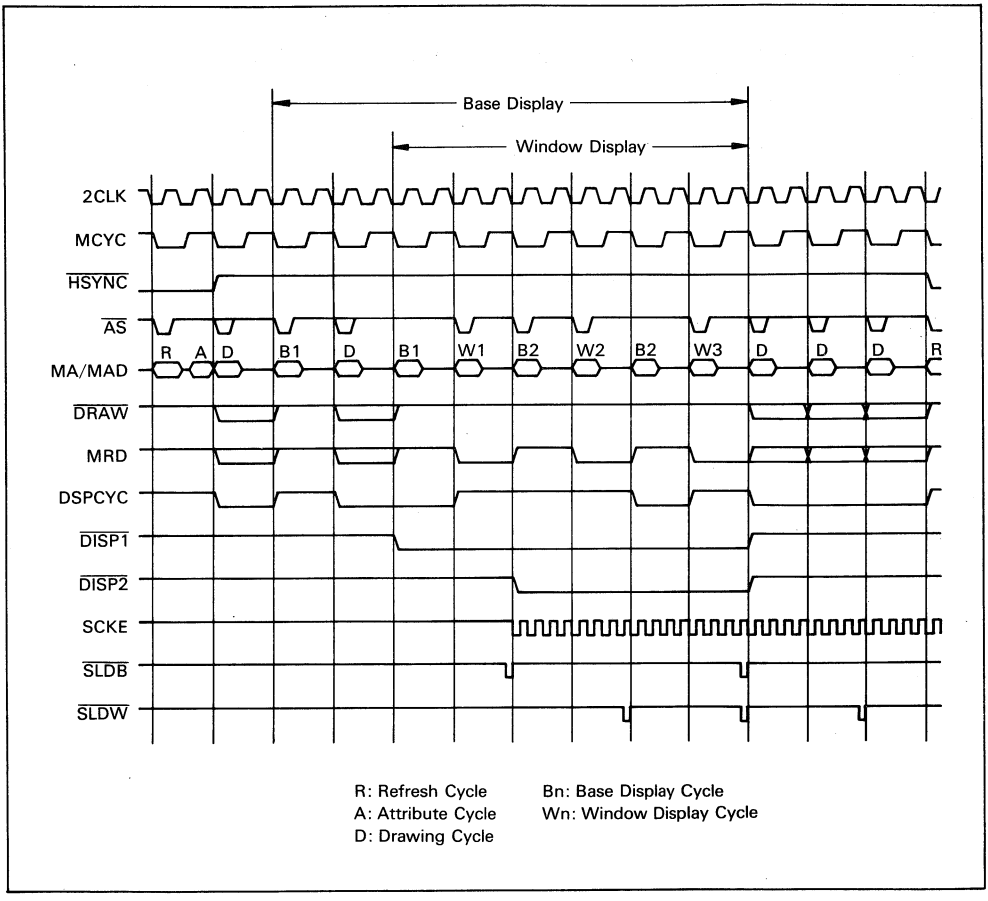


Figure 14. Zoom Display Timing (Dual Access Mode 1,Double Zoom)

Driving Priority Mode : In the ACRTC drawing priority mode, drawing memory access takes priority over display memory access. In this mode, when display data is provided in the same manner as in the 32-bit shift mode but the system does not enter a display cycle, and a total output of 32 bits is completed, low-level output are provided until the next display cycle.

Shift Clock Enable (SCKE)

Shift clock enable (SCKE) is a control signal for the GVAC video signal generation shift register. GVAC drives the shift register on the falling edge of the dot clock. The SCKE control signal decreases the dot clock frequency to set the zoom scale. Figure 15 shows triple zoom (HZ=0011) timing. Table 11 shows attribute codes and corresponding zoom scales.

Table 11. Attribute Codes and Zoom Scales

HZ3	HZ2	HZ1	HZ0	Zoom scale
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

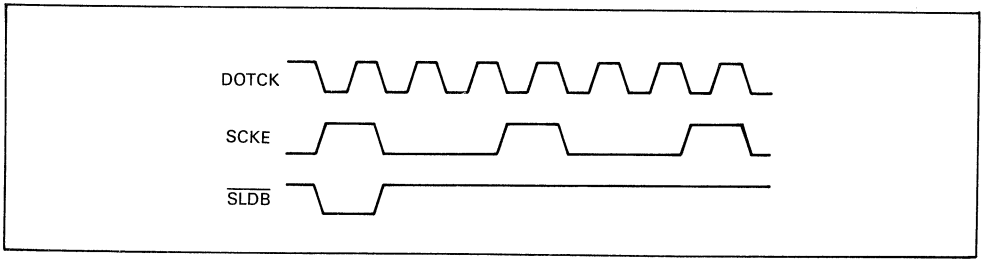


Figure 15. Triple Zoom Timing

Attribute Control Signals

The GMIC receives attribute code control signals for horizontal zooming and horizontal smooth scrolling from the ACRTC. Figure 16 shows attribute control output timing, and figure 17 shows the corresponding output pins.

The GMIC can control horizontal smooth scrolling of up to a 63-dot shift. However, the ACRTC outputs a 4-bit code (HSD3-HSD0), directly supporting up to a 15-dot shift. Therefore, the GMIC latches the lower 2 bits of the display adddress (MA0, MA1) output every display cycle into its internal register in order to control a 63-dot shift.

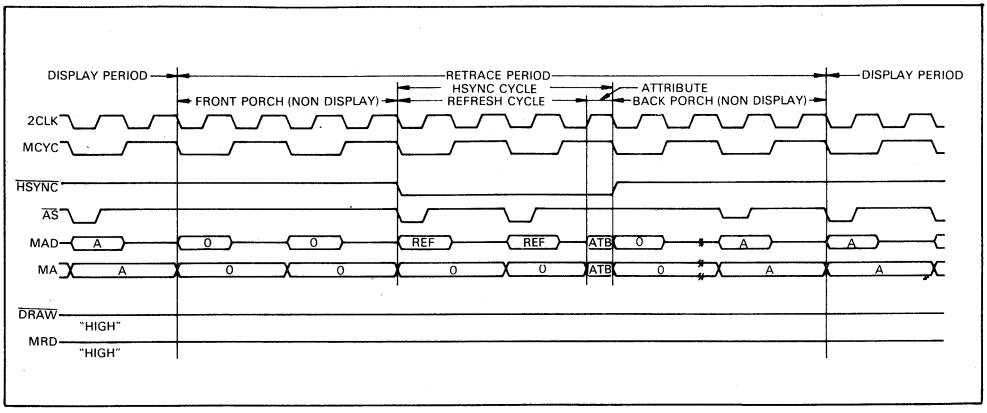


Figure 16. DRAM Refresh and Attribute Control Data Output (Single Access Mode)

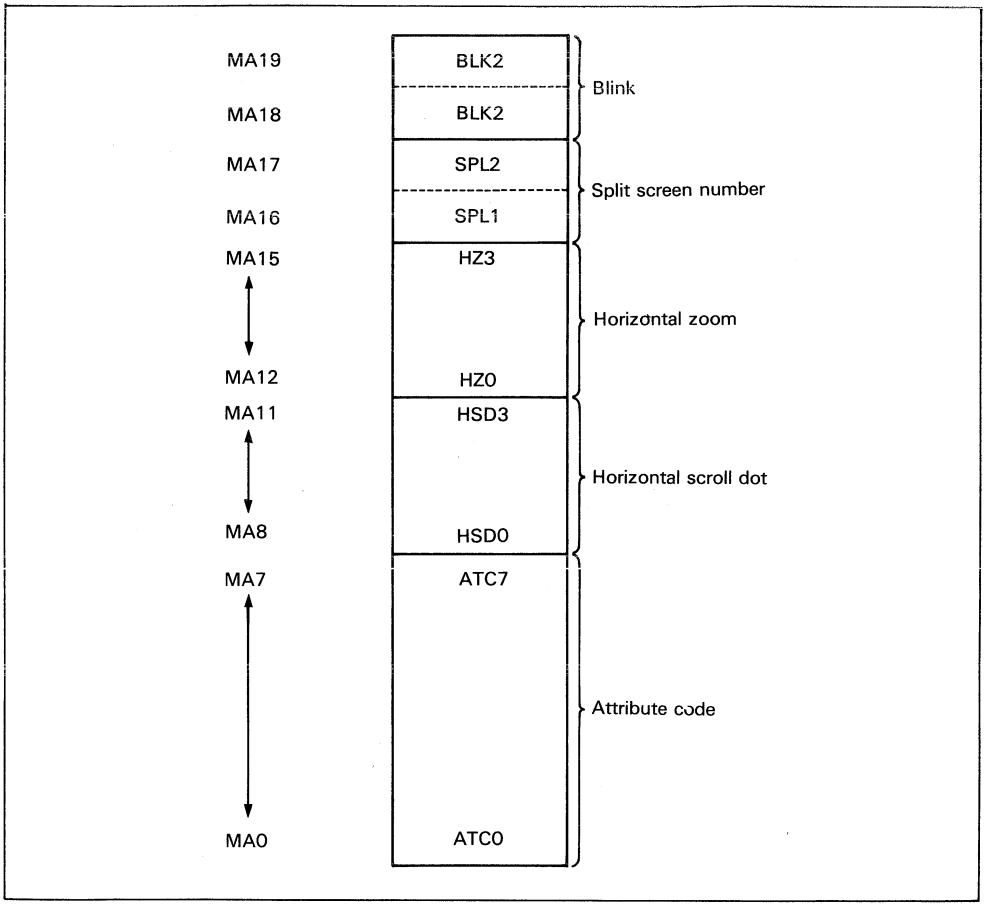


Figure 17. Attribute Control Signal Output Pins

Absolute Maximum Ratings (All voltages referenced to V_{SS} = 0 V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{in}	− 0.3 to V_{CC} + 0.3	V
Output voltage	V_{out}	5.5	V
Operating temperature	T_{opr}	0 to + 70	°C
Storage temperature	T_{str}	− 55 to + 150	°C

Notes: Using an LSI beyond in maximum ratings may result in its permanent destruction. LSIs should usually be operated under the recommended operating conditions. Exceeding any of these conditions may adversely affect its reliability.

Recommended Operating Conditions (All voltages referenced to V_{SS} = 0 V)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Input voltage low	V_{IL}	0	—	0.7	V
Input voltage high	V_{IH}	2.2	—	V_{CC}	V
Operating temperature	T_{opr}	0	25	70	°C

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, T_a = 0℃ to 70℃ unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Condition
Input voltage high		V_{IH}	2.2	V_{CC}	V	
Input voltage low		V_{IL}	−0.3	0.7	V	
Input clamp voltage		V_I		−1.5	V	V_{CC} = 4.75 V, I_{in} = −18 mA
Output voltage high	ADRA-ADRC, $\overline{SLDB}$, $\overline{SLDW}$, DSPCYC, SCKE, 2CLKOUT	V_{OH}	2.7		V	V_{CC} = 4.75V, I_{OH} = −400 mA
	$\overline{WE3}$-$\overline{WE0}$, FA7-FA0, $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$	V_{OH}	2.0		V	V_{CC} = 4.75 V, I_{OH} = −15 mA
Output voltage low	ADRA-ADRC, $\overline{SLDB}$, $\overline{SLDW}$, DSPCYC, SCKE 2CLKOUT	V_{OL}		0.5	V	V_{CC} = 4.75 V, I_{OL} = 8 mA
	$\overline{WE3}$-$\overline{WE0}$, FA7-FA0, $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$	V_{OL}		0.5	V	V_{CC} = 4.75 V, I_{OL} = 24 mA
Input current high		I_{IH}		20	μA	V_{CC} = 5.25 V, V_I = 2.7 V
Input current low		I_{IL}		−400	μA	V_{CC} = 5.25 V, V_I = 0.4 V
Output short circuit current		I_{OS}	−40	−120	mA	V_{CC} = 5.25 V
Current consumption		I_{CC}		160	mA	V_{CC} = 5.25 V
Input capacitance		C_{in}		10	pF	

AC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, T_a = 0℃ to + 70℃)

No	Item	Symbol	32 MHz Min	32 MHz Max	48 MHz Min	48 MHz Max	64 MHz Min	64 MHz Max	Unit	Figure
	DOTCK operation frequence	f		32		48		64	MHz	
①	DOTCK cycle time	t_C	31.3		20.8		15.6		ns	18
②	DOTCK high level pulse width	t_{HW}	12		9		6		ns	
③	DOTCK low level pulse width	t_{LW}	12		9		6		ns	
④	DOTCK rise time	t_R		5		5		5	ns	
⑤	DOTCK fall time	t_F		5		5		5	ns	
⑥	2CLKOUT delay	t_{2CLKD}		24		17		14	ns	19
⑦	MCYC setup time	t_{MCYCS}	t_C + 20		t_C + 20		t_C + 20		ns	20-23
⑧	MCYC hold time	t_{MCYCH}	0		0		0		ns	
⑨	$\overline{\text{HSYNC}}$ setup time	H_{HSS}	t_C + 20		t_C + 20		t_C + 20		ns	20-22
⑩	$\overline{\text{HSYNC}}$ hold time	t_{HSH}	0		0		0		ns	23
⑪	MRD setup time	t_{MRDS}	t_C + 20		t_C + 20		t_C + 20		ns	20-22
⑫	MRD hold time	t_{MRDH}	5		5		5		ns	20, 21, 23
⑬	$\overline{\text{DRAW}}$ setup time	t_{DRAWS}	t_C + 20		t_C + 20		t_C + 20		ns	20-22
⑭	$\overline{\text{DRAW}}$ hold time	t_{DRAWH}	5		5		5		ns	20, 21, 23
⑮	$\overline{\text{AS}}$ setup time (CDM = 01)	t_{ASS}	t_C + 25		t_C + 25		t_C + 25		ns	20-23
	$\overline{\text{AS}}$ setup time (CMD = 10)	t_{ASS}	$2t_C$ + 25		$2t_C$ + 25		$2t_C$ + 25		ns	
	$\overline{\text{AS}}$ setup time (CDM = 11)	t_{ASS}	$4t_C$ + 25		$4t_C$ + 25		$4t_C$ + 25		ns	
⑯	$\overline{\text{AS}}$ pulse width	t_{ASW}	25		25		25		ns	
⑰	Memory address setup time	t_{MAS}	10		10		10		ns	20-23
⑱	Memory address hold time	t_{MAH}	5		5		5		ns	
⑲	Attribute code setup time	t_{ACS}	20		20		20		ns	23
⑳	Attribute code hold time	t_{ACH}	5		5		5		ns	

AC Characteristics (cont)

No	Item	Symbol	32 MHz Min	32 MHz Max	48 MHz Min	48 MHz Max	64 MHz Min	64 MHz Max	Unit	Figure
㉑	$\overline{RAS}$ setup time (CDM = 01)	t_{RSS}	t_C − 20		t_C − 20		t_C − 20		ns	20-23
	$\overline{RAS}$ setup time (CDM = 10)	t_{RSS}	$2t_C$ − 20		$2t_C$ − 20		$2t_C$ − 20		ns	
	$\overline{RAS}$ setup time (CDM = 11)	t_{RSS}	$4t_C$ − 20		$4t_C$ − 20		$4t_C$ − 20		ns	
㉒	$\overline{RAS}$ hold time	t_{RSH}	3		3		3		ns	
㉓	$\overline{CAS}$ delay time (CDM = 01)	t_{CASD}	t_C − 7		t_C − 7		t_C − 7		ns	20, 21
	$\overline{CAS}$ delay time (CDM = 10)	t_{CASD}	$2t_C$ − 7		$2t_C$ − 7		$2t_C$ − 7		ns	
	$\overline{CAS}$ delay time (CDM = 11)	t_{CASD}	$4t_C$ − 7		$4t_C$ − 7		$4t_C$ − 7		ns	
㉓A	$\overline{CAS}$ delay time from 2CLK	t_{CASDH}		20		20		15	ns	
㉔	$\overline{CAS}$ hold time	t_{CASH}	3		3		3		ns	
㉕	Memory address setup time (CDM = 01)	t_{MASC}	t_C + 25		t_C + 25		t_C + 25		ns	20-23
	Memory address setup time (CDM = 10)	t_{MASC}	$2t_C$ + 25		$2t_C$ + 25		$2t_C$ + 25		ns	
	Memory address setup time (CDM = 11)	t_{MASC}	$4t_C$ + 25		$4t_C$ + 25		$4t_C$ + 25		ns	
㉖	Row address setup time	t_{RAS}	0		0		0		ns	
㉗	Row address hold time (CDM = 01)	t_{RAH}	$t_C/2$ − 2		$t_C/2$ − 2		$t_C/2$ − 2		ns	
	Row address hold time (CDM = 10)	t_{RAH}	t_C − 2		t_C − 2		t_C − 2		ns	
	Row address hold time (CDM = 11)	t_{RAH}	$2t_C$ − 2		$2t_C$ − 2		$2t_C$ − 2		ns	
㉘	Column address setup time	t_{CAS}	0		0		0		ns	20, 21
㉙	Column address hold time	t_{CAH}	0		0		0		ns	

AC Characteristics (cont)

No	Item	Symbol	32 MHz Min	32 MHz Max	48 MHz Min	48 MHz Max	64 MHz Min	64 MHz Max	Unit	Figure
㉚	$\overline{OE}$ delay time	t_{OED}		20		20		20	ns	20
㉛	$\overline{OE}$ hold time	t_{OEH}	3		3		3		ns	
㉜	$\overline{WE}$ delay time	t_{WED}	5	30	5	30	5	30	ns	21
㉝	$\overline{WE}$ hold time	t_{WEH}	3		3		3		ns	
㉞	Address delay time	t_{AD}		30		30		30	ns	
㉟	Address hold time	t_{AH}	0		0		0		ns	
㊱	SCKE delay time	t_{SCKD}	3	22	3	15	3	12	ns	18
㊲	$\overline{SLD}$ delay time	t_{SLDD}	5	24	5	17	5	17	ns	
㊳	DSPCYC delay time from $\overline{AS}$	t_{DSPDA}		40		40		40	ns	20
㊳A	DSPCYC delay time from $\overline{DRAW}$	t_{DSPDD}		20		20		20	ns	
㊴	DSPCYC hold time	t_{DSPH}	5		5		5		ns	

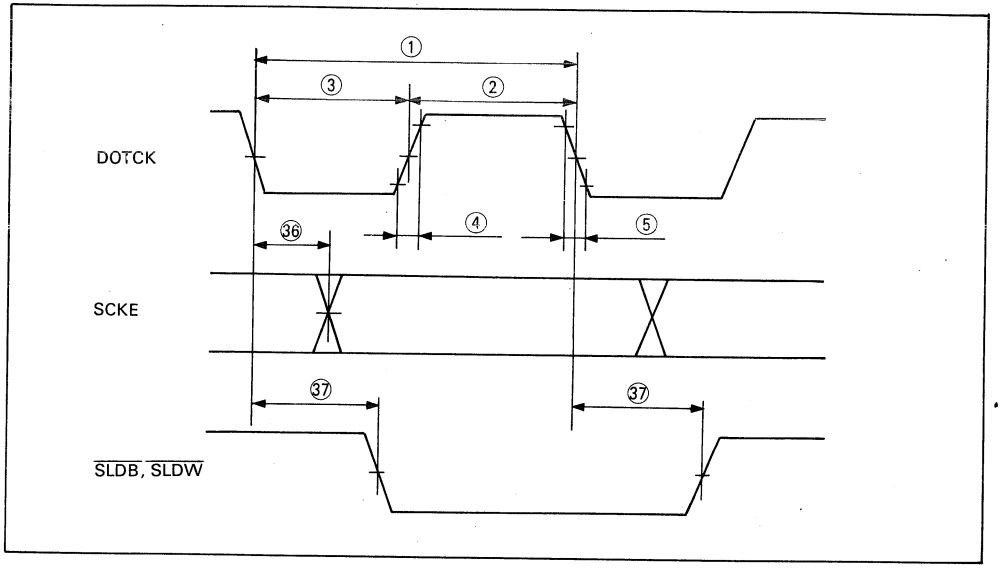


Figure 18. Clock

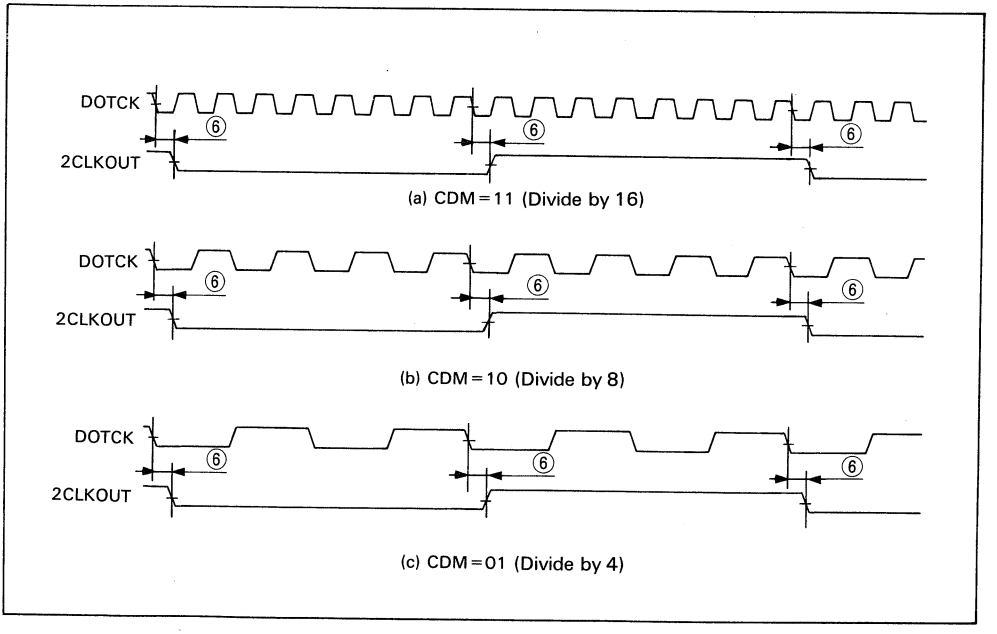


Figure 19. 2CLKOUT

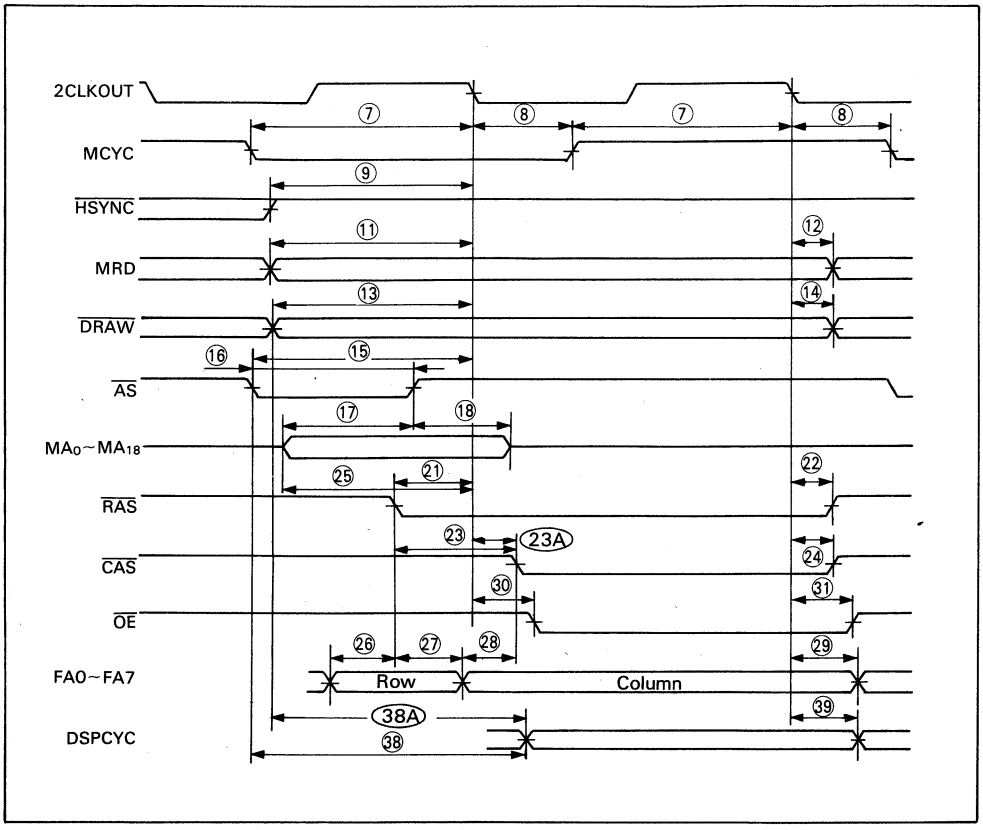


Figure 20. Memory Read Cycle (Drawing, Read and Display)

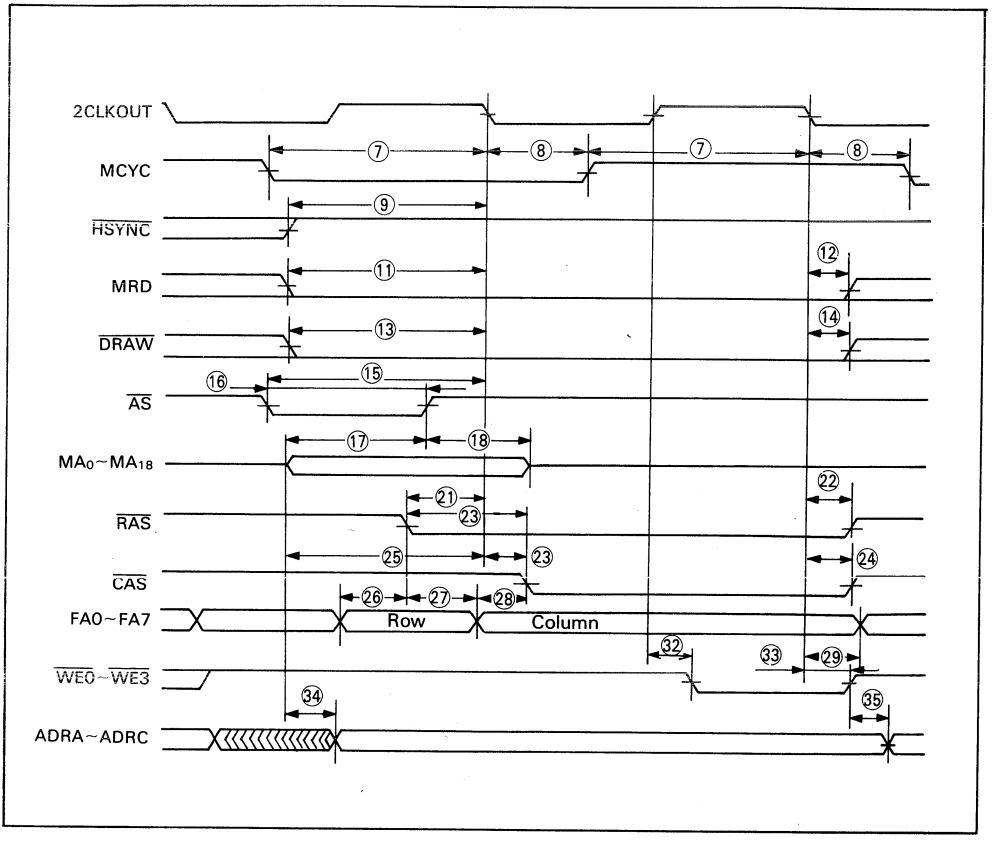


Figure 21. Memory Write Cycle

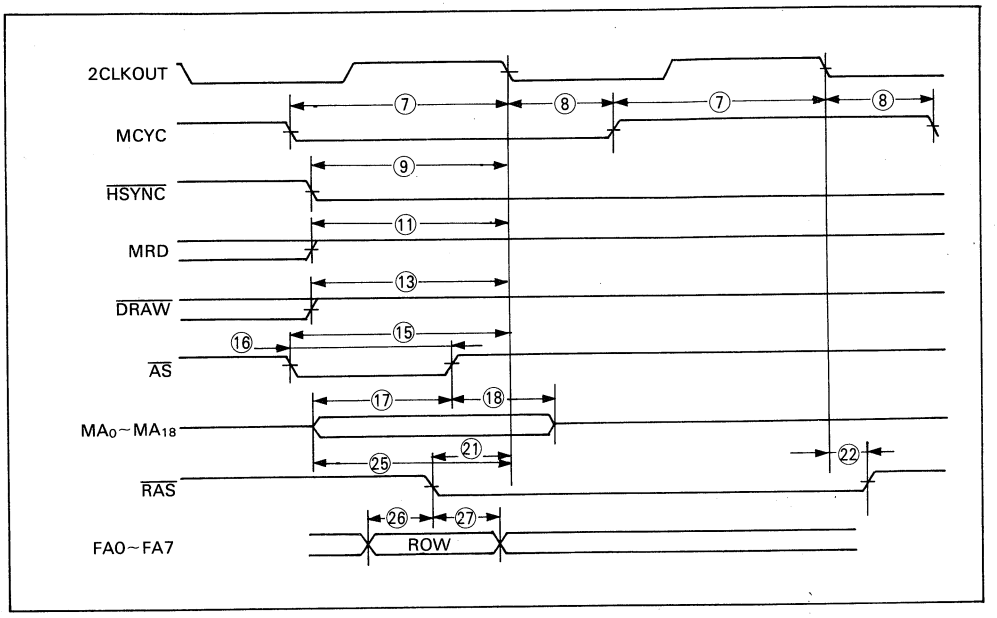


Figure 22. Refresh Cycle

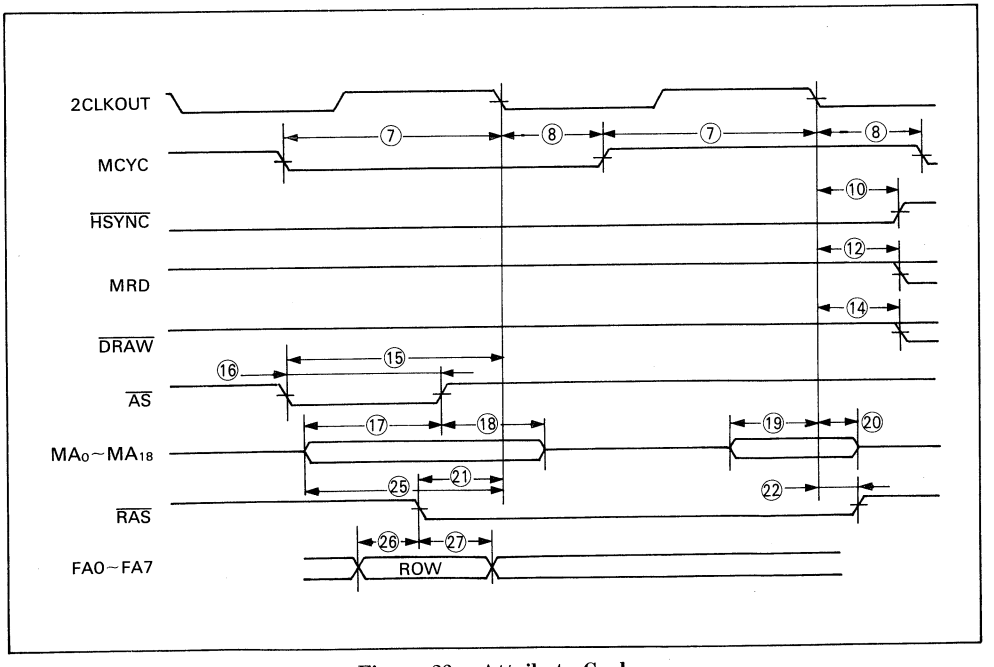
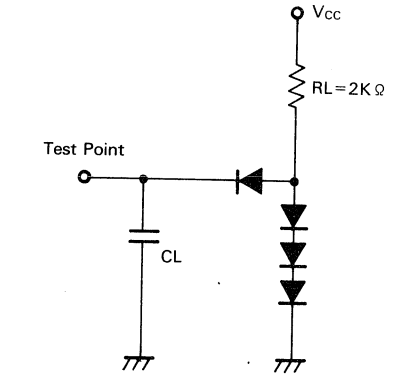


Figure 23. Attribute Cycle



Signal	CL(pF)
$\overline{SLDB}$, $\overline{SLDW}$	40
SCKE	40
2CLKOUT	40
$\overline{RAS}$	240
$\overline{CAS}$	240
$\overline{OE}$	240
$\overline{WE0}$~$\overline{WE3}$	120
FA0~FA7	160
ADRA~ADRC	120
DSPCYC	40

Note: All diodes are 1S2074Ⓗ's or the equivalent

Figure 24. Test Load Circuit

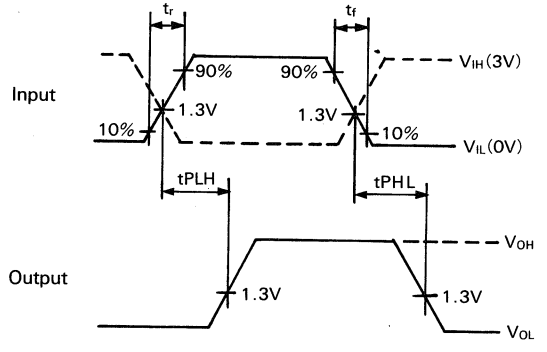


Figure 25. Input/Output waveforms

Reference Literature

Product	Data Sheet	User's Manual	Application Note	Others
HD63484 ACRTC	E-0045A	680-1-31A	Introduction to ACRTC Application 680-3-08 Circuits Software 680-3-07	Programming Reference AD-E0032A
HD63486 GVAC	AD-E0123	——		——

Refer to application note (No. 680-3-15) for detail of this product.

HD63486

Graphic Video Attribute Controller (GVAC)

Description

The HD63486 LSI belongs to the ACRTC (advanced CRT controller) family. It converts frame buffer data to serial video signals. It contains a shift register for parallel-to-serial conversion and the peripheral video control circuits necessary to generate high-speed video signals.

The programmable bit length of the shift register makes the GVAC suitable for multicolor graphics and monochrome grey scale applications. Additionally, multiple GVACs can be operated in parallel to further expand the field of applications. The GVAC's functions include horizontal smooth scrolling and horizontal zoom using control signals from the GMIC (graphic memory interface controller). Using the Hi-BiCMOS process, the HD63486 achieves high-speed video signal generation with low power dissipation.

Features

- Internal shift register for video signal control, programmable as:
  - —Four 8-bit shift registers
  - —Two 16-bit shift registers
  - —One 32-bit shift register
- High speed video signal generation (64 MHz dot rate)
- Multiple GVAC parallel operation
- Internal bidirectional data bus buffer for frame buffers
- Zooming and horizontal smooth scrolling (requires GMIC signals or equivalent)
- Direct ACRTC interface
- TTL-compatible input/output
- Single + 5 V power supply
- Low power dissipation

Type of Products

Part No.	Speed	Package
HD63486PS32	32 MHz	64-pin Plastic Shrink DIP
HD63486PS48	48 MHz	(DP-64S)
HD63486PS64	64 MHz	
HD63486CP32	32 MHz	68-pin PLCC
HD63486CP48	48 MHz	(CP-68)
HD63486CP64	64 MHz	

Pin Description

Figure 1 shows the pin arrangement for the 64-pin plastic shrink-type DIP and the 68-pin PLCC packages. Table 1 describes the pins.

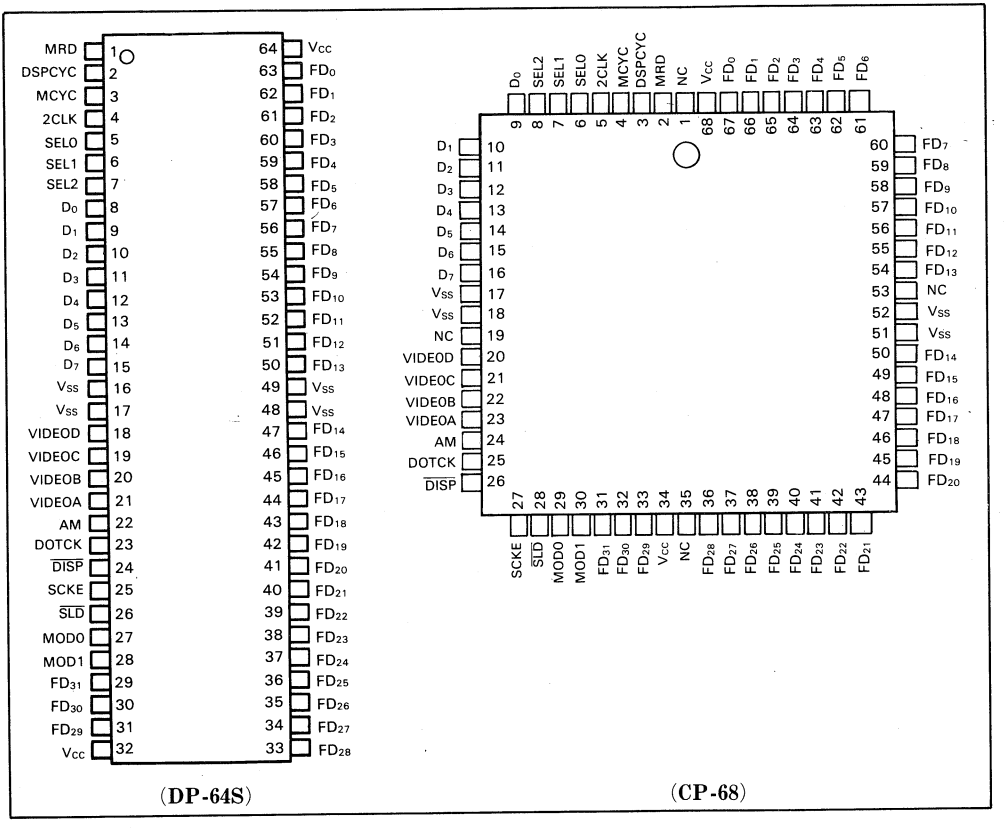


Figure 1. Pin Arrangement

Power Supply (V_{CC}, V_{SS})

V_{SS} and V_{CC} are the GVAC power supply pins. V_{CC} pins are $+5\,V \pm 5\%$ supply pins. V_{SS} are the ground pins. Be sure to connect all four V_{SS} pins to ground and both V_{CC} pins to the power supply.

ACRTC Signals

Clock (2CLK): The 2CLK input must be the same as the 2CLK input to the ACRTC. It is usually supplied by the GMIC 2CLKOUT output. 2CLK is used for data transfer between the ACRTC and frame buffers and as a timing signal for display data input.

Memory Cycle (MCYC): The MCYC input specifies frame buffer access by the ACRTC. It must be low when the ACRTC is in address cycle, and high when the ACRTC is in data cycle. MCYC controls the data buffers. It is usually supplied by the ACRTC's MCYC output.

Memory Read (MRD): The MRD input controls the direction of transfers between the ACRTC and frame buffers. When MRD is high, the GVACs transfer data from the frame buffers to the ACRTC. When MRD is low, the GVACs transfer data from the ACRTC to the frame buffers. MRD must be held high during a display read data cycle. Only during a display cycle for superimposed screen data (dual access mode 1) does the ACRTC input MRD low. This signal is usually supplied by the MRD output.

Display ($\overline{DISP}$): The $\overline{DISP}$ input is a composite signal indicating the screen's horizontal and vertical display period. Display timing output ($\overline{DISP1}$) is input when the ACRTC's DSP (display signal control) bit is set to 1. For superimposed display (dual access mode 1), $\overline{DISP1}$ must be input to a GVAC for background screens, while $\overline{DISP2}$ must be input the window screen from the ACRTC.

Data Bus (D_7-D_0): D_7-D_0 are the 8-bit data input/output for data transfer between the ACRTC and frame buffers. Usually, D_7-D_0 are connected to 8 bits of the memory address data bus (MAD_{18}-MAD_0) according to the operation mode selected by the MOD1, MOD0 inputs.

Table 1. Pin Description

Signal	Pin Number DIP-64	Pin Number PLCC-68	I/O	Description
V_{CC}	32, 64	34, 68		+5 V power supply
V_{SS}	16, 17, 48, 49	17, 18, 51, 52		Ground
2CLK	4	5	I	Clock
MCYC	3	4	I	Memory Cycle
MRD	1	2	I	Memory Read
$\overline{DISP}$	24	26	I	Display
D_7-D_0	15-8	16-9	I/O	Data Bus
MOD1, MOD0	28, 27	30, 29	I	Operation Mode
AM	22	24	I	Access Mode
DSPCYC	2	3	I	Display Cycle
SEL2-SEL0	7-5	8-6	I	Select
SCKE	25	27	I	Shift Clock Enable
$\overline{SLD}$	26	28	I	Shift Load
FD_{31}-FD_0	29-31, 33-47, 50-63	31-33, 36-50, 54-67	I/O	Frame Buffer Data
DOTCK	23	25	I	Dot Clock
VIDEOA-VIDEOD	21-18	23-20	O	Video Outputs

Operation Mode (MOD1, MOD0): The MOD1 and MOD0 inputs specify the length of the GVAC's internal video signal shift register and the operation mode for the control data bus data multiplexing between the ACRTC and the frame buffers. The operation mode setting is closely related to the ACRTC's graphic address increment mode (GAI), the graphic bit mode (GBM) which specifies the number of bits per pixel, and the frame buffer's access mode (ACM). These settings determine the shift length of one display cycle, and thus the settings for MOD1 and MOD0. The GMIC's clock division mode (CDM1, CDM0) is also related to MOD1 and MOD0. Table 2 shows how GVAC's operation mode is related to the ACRTC and GMIC settings. Other settings are allowed in a graphic syster with ACRTC, GMIC, GVAC, and additional circuits. For a description of GBM, GAI, and ACM, see the ACRTC User's Manual. For a description of CDM and DAM, see the GMIC Data Sheet.

Access Mode (AM): The AM input sets the GVACs to superimposed display mode. When the ACRTC's access mode (ACM) set to dual access mode 1 (11), AM switches between two GVACs for background and superimposed screens. In single access mode and dual access mode 0, AM must be set low. In dual access mode 1, AM should be set low for a background screen GVAC, and high for a superimposed screen GVAC.

GMIC Interface Signals

Display Cycle (DSPCYC): The DSPCYC input indicates whether a display cycle has been entered. DSPCYC set low signifies a nondisplay cycle, during which data is transferred between frame buffers and the ACRTC. DSPCYC set high indicates a display cycle, during which data from the frame buffers is transferred to the GVACs. The display cycle signal (DSPCYC) output from the GMIC is used for this input.

Select (SEL2-SEL0): The SEL2-SEL0 inputs are the lower three bits of the address specifying a particular word is the frame buffers to be transferred to the ACRTC. Since SEL2-SEL0 control the address bus connection between frame buffers and the ACRTC, it must be valid during a data cycle when MCYC is set high. The address outputs (ADRA-ADRC) from the GMIC usually supply these signals.

Shift Clock Enable (SCKE): The SCKE input specifies the timing for driving the GVAC's parallel-to-serial converter (shift register) for generating video signals (VIDEOA-VIDEOD). The GVAC's perform serial-to-parallel conversion by shifting one bit of display data every shift clock cycle. Using SCKE, the GVACs generate a lower frequency shift clock. Extending one shift clock cycle this way allows zooming. The SCKE output from the GMIC supplies this input.

Table 2. Operation Mode and GVAC, ACRTC, and GMIC Settings

GVAC	ACRTC			GMIC			
MOD 0 1	GBM 10 9 8	GAI 6 5 4	ACM 3 2	CDM 1 0	DAM	Bits/ Pixel	Shift Length	Max Dot Rate (MHz)
0 0	0 1 0	0 1 0	0 0	1 0	0	4	16	64
			0 1					
			1 0	0 1	1			32
			1 1					
0 1		0 1 1	0 0	1 1	0	4	32	64
			0 1					
			1 0	1 0	1			64
			1 1					
1 0	0 1 1	0 1 0	0 0	0 1	0	8	8	64
			0 1					
1 1		0 1 1	0 0	1 0	0	8	16	32
			0 1					
			1 0	0 1	1			
			1 1					

For systems with a superimpose function, SCKE must be held high for the superimposed window's GVAC (AM input high).

Shift Load ($\overline{SLD}$): The $\overline{SLD}$ input specifies the timing in which display data temporarily stored in the GVACs is supplied to the shift register. $\overline{SLD}$ is asserted for one period of the dot clock. Horizontal scrolling is implemented by shifting $\overline{SLD}$ on a dot clock basis during a single display cycle. $\overline{SLD}$ must be asserted once during each display cycle (shift length). $\overline{SLD}$ is usually input from the GMIC $\overline{SLDB}$ output for background screen GVACs (AM input low), and $\overline{SLDW}$ for window screen GVACs (AM input high).

Frame Buffer Data (FD_{31}-FD_0)

The 32-bit FD_{31}-FD_0 frame buffer data I/O bus transfers data between the ACRTC and frame buffers and inputs display data from the frame buffers. The 32 bits arj read simultaneounly from the frame buffer, and FD_{31}-FD_0 can be directly connected to the frame buffer data I/O pins.

CRT Display Interface

Dot Clock (DOTCK): The DOTCK input is the basic video signal generating clock. The DOTCK frequency is determined by the CRT horizontal resolution (pixel count) and the horizontal scan display period. This clock is usually the same signal applied to the GMIC DOTCK input.

Video Outputs (VIDEOA-VIDEOD): VIDEOA -VIDEOD are the four bits output from the GVAC's parallel-to-serial conversion shift register. They are supplied during a display period specified by the display signal ($\overline{DISP}$). Which outputs are usable depends on the operation mode (MOD1, MOD0) input. Table 3 shows the usable video signals and corresponding MOD1 and MOD0 signals.

Table 3. Operation Mode and Video Outputs

Mode		Video Output				Bits/	
MOD1	MOD0	VIDEOA	VIDEOB	VIDEOC	VIDEOD	Pixel	Shift Length
0	0	Avail	Not avail	Avail	Not avail	4	16
0	1	Avail	Not avail	Not avail	Not avail	4	32
1	0	Avail	Avail	Avail	Avail	8	8
1	1	Avail	Not avail	Avail	Not avail	8	16

Functional Description

Figure 2 is a block diagram of the GVAC.

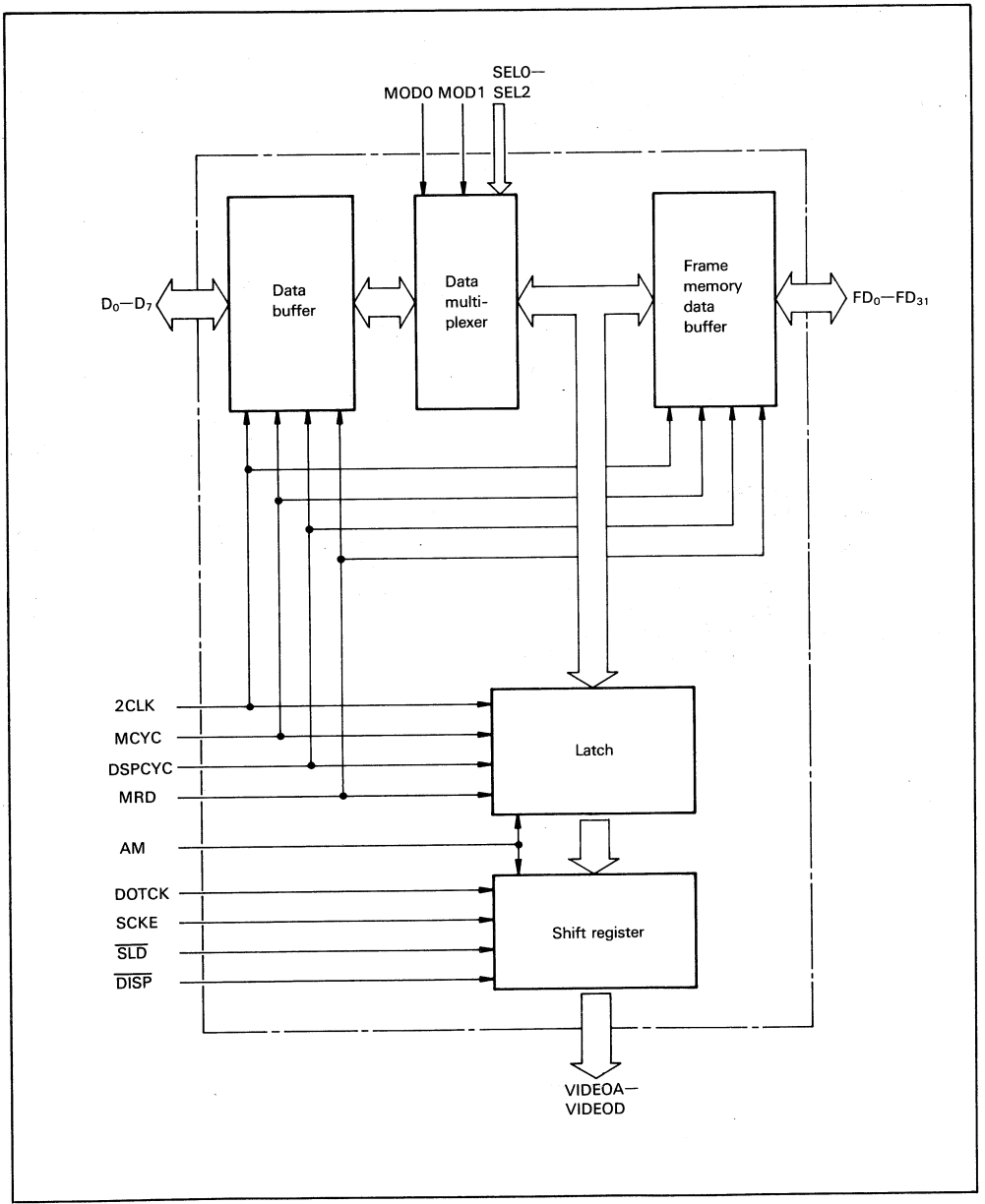


Figure 2. GVAC Block Diagram

Frame Memory Data Buffer

The 32-bit bidirectional frame memory data buffer consists of input and output buffers to transfer data to and from the frame buffers in response to data transfer requests from the ACRTC.

The three-state output buffer is enabled only during a memory write cycle by memory cycle (MCYC) and memory read (MRD) signals from the ACRTC, and display cycle (DSPCYC) from the GMIC. A 32-bit output buffer to be enabled is selected by select signals (SEL2-SEL0) from the GMIC and the operation mode (MOD1, MOD0) set externally.

The input buffer reads data from the frame buffers.

Data Buffers

The 8-bit input/output buffer transfers data between the ACRTC and frame buffers.

The output buffer is a three-state buffer which is enabled during a frame buffer read cycle by memory cycle (MCYC) and memory read (MRD) signals from the ACRTC, and display cycle (DSPCYC) from the GMIC.

The input buffer supplies drawing data from the ACRTC to the frame buffers.

Data Multiplexer

The data multiplexer is a direct connection between the frame buffers and the data buffer's data bus which leads to the ACRTC's and frame buffer's data bus. The bus connection in controlled by select signals (SEL2-SEL0) and the operation mode (MOD1, MOD0) set externally to enable transfer between the ACRTC and frame buffers.

Latch

The latch recognizes a display data read cycle by memory cycle (MCYC) and memory read (MRD) signals from the ACRTC, and clock (2CLK) and display cycle (DSPCYC) from the GMIC, and the access mode (AM) input. During a display data read cycle, the latch temporarily stores 32-bit display data input from a frame memory data buffer. It sends the stored data to the shift register for parallel-to-serial conversion.

Shift Register

The 32-bit shift register performs parallel-to-serial conversion on display data stored in the latch to provide video signal output. When the latch receives the shift load ($\overline{\text{SLDB}}$, $\overline{\text{SLDW}}$) and shift clock enable (SCKE) signals from the GMIC, it feeds the display data it has stored to the shift register. The shift register supplies one bit of display data every dot clock cycle while SCKE is asserted. When the ACRTC's display cycle signal (DISP) is negated, the shift register does not output a video signal.

When the GMIC shifts the timing of the shift load ($\overline{\text{SLDB}}$, $\overline{\text{SLDW}}$) output on a dot clock basis, the GVAC performs horizontal smooth scrolling. When the GMIC extends the shift clock enable signal (SCKE) based on the dot clock, it performs horizontal zoom.

System Description

Applications

The GVAC internal circuits perform three major functions:

- Converting parallel display data read from the frame buffers by the ACRTC to serial from and delivering them to the CRT as video signals
- Transferring data between the ACRTC and frame buffers
- Zooming and horizontal smooth scrolling according to signals from the GMIC

Furthermore, the GVACs' operation mode can be set according to the ACRTC's operation mode by the program input signals. This programmability makes the GVAC suitable for a wide range of applications, from slow, small systems to fast, large systems. It also permits the GVACs to accommodate system specification changes.

Figure 3 shows a graphic system configuration using an ACRTC, GMIC and GVACs. With the GMIC used for interfacing with frame buffers and the GVACs generating the video signals, a flexible, high-performance graphic system is constructed with a minimum number of parts.

System Configuration

The system example in figure 3 uses two GVACs, but the number of GVACs can be varied to meet different CRT resolution and color per pixel (or grey scale) applications.

The GVACs recognize a display data read cycle by decoding ACRTC output signals such as memory cycle (MCYC) and memory read (MRD) and GMIC output signals such as display cycle (DSPCYC). In the display data read cycle, the GVACs latch display data from the frame buffers. They pass the display data to the internal shift register for parallel-to-serial conversion when they receive the shift load signal ($\overline{SLDB}$ or $\overline{SLDW}$) from the GMIC. The GVACs perform successive parallel-to-serial conversion synchronously with the dot clock when they receive the shift clock enable (SCKE) output from the GMIC. This generates the video signals.

A GVAC can receive 32-bit display data (FD_{31}-FD_0) from one frame buffer. Furthermore, it provides a connection from the ACRTC's data bus (D_7-D_0) to the frame buffers data bus (FD_{31}-FD_0), enabling direct data transfer between the two. The GVACs also implement horizontal smooth scrolling and zooming, controlled by the shift load ($\overline{SLDB}$, $\overline{SLDW}$) and shift clock enable (SCKE) signals from the GMIC.

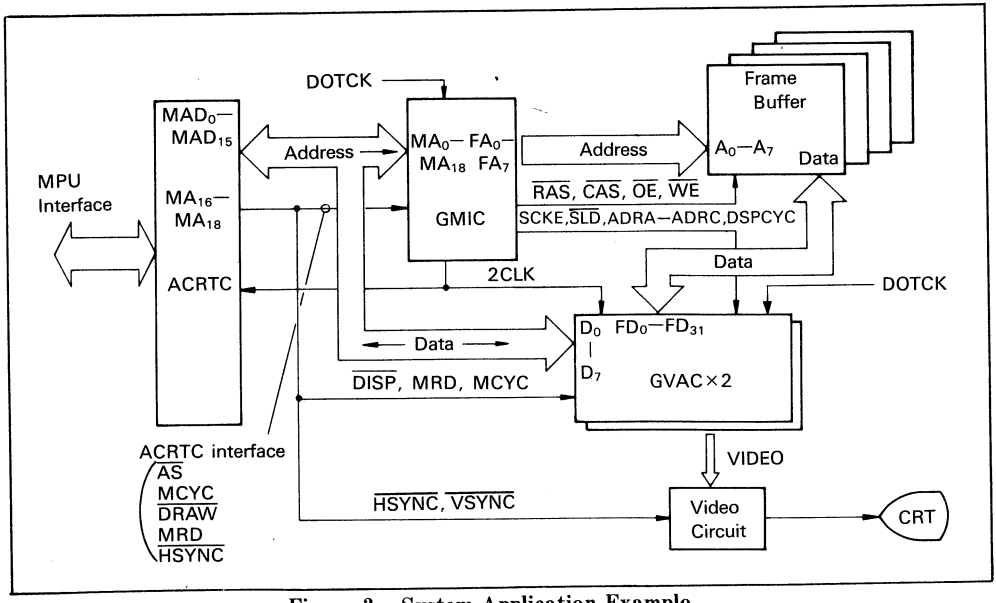


Figure 3. System Application Example

Operation

Data Transfer

The GVACs contain control circuits for bidirectional transfer between the ACRTC and frame buffers. To transfer data, the GVACs receive the ACRTC's memory cycle (MCYC) and memory read (MRD) signals, and the GMIC's display cycle (DSPCYC). From these signals, the GVACs recognize a drawing data transfer cycle. Connection between the ACRTC's data bus and the frame buffer's data bus is controlled by the select signals (SEL2-SEL0) from the GMIC and the operation mode (MOD1, MOD0) inputs.

The GVACs recognize a nondisplay cycle when DSPCYC is low. In nondisplay cycles, the data transfer direction is determined by the memory read signal (MRD). MRD high signifies a read cycle to transfer data from frame buffers to the ACRTC. MRD low signifies a write cycle to transfer data from the ACRTC to the frame buffers. Timing for the data transfer is determined by the MCYC input. When MCYC is high, frame buffers or the ACRTC three-state output buffers are enabled for transfer.

Drawing Write Cycle : The GVACs recognize a drawing write cycle when both DSPCYC and MRD are low. Figure 4 shows the timing for a drawing write cycle.

When MCYC is high during this cycle, the GVACs enable the frame memory data buffer, and output data from the ACRTC one word at a time to the frame buffers, based on the operation mode (MOD1, MOD0) inputs and the select signals (SEL2 -SEL0) from the GMIC. Table 4 shows the connections between FD and D pins when MOD1 and MOD0 are set to 00. When SEL2-SEL0 are set to 000 D_0-D_3 from the ACRTC are output to FD_0-FD_3, D_4-D_7 are output to FD_{16}-FD_{19}, and the other FD pins are high-impedance. Table 5-7 show the relation of D to FD in other modes.

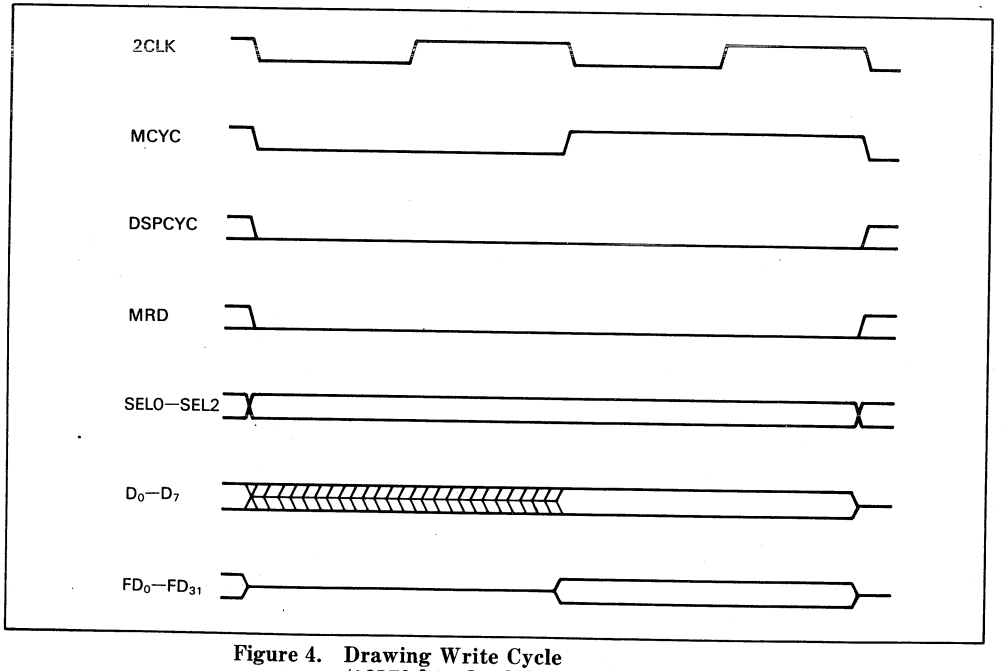


Figure 4. Drawing Write Cycle
(ACRTC [MAD] → [D] GVAC [FD] → Frame buffers)

Table 4. Connection Between D and FD Pins, Drawing Cycle, MOD1, MOD0 = 00 (4 Bits/Pixel, 16-Bit Shift Mode)

SEL2-SEL0	D0	D1	D2	D3	D4	D5	D6	D7
000	FD_0	FD_1	FD_2	FD_3	FD_{16}	FD_{17}	FD_{18}	FD_{19}
001	FD_4	FD_5	FD_6	FD_7	FD_{20}	FD_{21}	FD_{22}	FD_{23}
010	FD_8	FD_9	FD_{10}	FD_{11}	FD_{24}	FD_{25}	FD_{26}	FD_{27}
011	FD_{12}	FD_{13}	FD_{14}	FD_{15}	FD_{28}	FD_{29}	FD_{30}	FD_{31}
100-111	Not used							

Note: All other FD pins high impedance.

Table 5. Connection Between D and FD Pins, Drawing Cycle, MOD1, MOD0 = 01 (4 Bits/Pixel, 32-Bit Shift Mode)

SEL2-SEL0	D0	D1	D2	D3	D4	D5	D6	D7
000	FD_0	FD_1	FD_2	FD_3	NC	NC	NC	NC
001	FD_4	FD_5	FD_6	FD_7	NC	NC	NC	NC
010	FD_8	FD_9	FD_{10}	FD_{11}	NC	NC	NC	NC
011	FD_{12}	FD_{13}	FD_{14}	FD_{15}	NC	NC	NC	NC
100	FD_{16}	FD_{17}	FD_{18}	FD_{19}	NC	NC	NC	NC
101	FD_{20}	FD_{21}	FD_{22}	FD_{23}	NC	NC	NC	NC
110	FD_{24}	FD_{25}	FD_{26}	FD_{27}	NC	NC	NC	NC
111	FD_{28}	FD_{29}	FD_{30}	FD_{31}	NC	NC	NC	NC

Note: All other FD pins high inpedance
NC = No connection

Table 6. Connection Between D and FD Pins, Drawing Cycle, MOD1, MOD0 = 10 (8 Bits/Pixel, 8-Bit Shift Mode)

SEL2-SEL0	D0	D1	D2	D3	D4	D5	D6	D7
000	FD_0	FD_1	FD_8	FD_9	FD_{16}	FD_{17}	FD_{24}	FD_{25}
001	FD_2	FD_3	FD_{10}	FD_{11}	FD_{18}	FD_{19}	FD_{26}	FD_{27}
010	FD_4	FD_5	FD_{12}	FD_{13}	FD_{20}	FD_{21}	FD_{28}	FD_{29}
011	FD_6	FD_7	FD_{14}	FD_{15}	FD_{22}	FD_{23}	FD_{30}	FD_{31}
100-111	Not used							

Note: All other FD pins high impedance.

Table 7. Connection Between D and FD Pins, Drawing Cycle, MOD, MOD = 11 (8 Bits/Pixel, 16-Bit Shift Mode)

SEL2-SEL0	D0	D1	D2	D3	D4	D5	D6	D7
000	FD_0	FD_1	NC	NC	FD_{16}	FD_{17}	NC	NC
001	FD_2	FD_3	NC	NC	FD_{18}	FD_{19}	NC	NC
010	FD_4	FD_5	NC	NC	FD_{20}	FD_{21}	NC	NC
011	FD_6	FD_7	NC	NC	FD_{22}	FD_{23}	NC	NC
100	FD_8	FD_9	NC	NC	FD_{24}	FD_{25}	NC	NC
101	FD_{10}	FD_{11}	NC	NC	FD_{26}	FD_{27}	NC	NC
110	FD_{12}	FD_{13}	NC	NC	FD_{28}	FD_{29}	NC	NC
111	FD_{14}	FD_{15}	NC	NC	FD_{30}	FD_{31}	NC	NC

Note: All other FD pins high impedance.
NC = No connection

Drawing Read Cycle : The GVACs recognize a drawing read cycle when DSPCYC is low and MRD is high. Figure 5 shows the timing for a drawing read cycle.

When MCYC is high during this cycle, the GVACs enable the data buffer (D_7-D_0) for the ACRTC and output a word from the frame buffers selected by the operation mode (MOD1, MOD0) inputs and the select signals (SEL2-SEL0) from the GMIC. Table 4 shows the connections between FD and D pins when MOD1 and MOD0 are set to 00. When SEL2-SEL0 are set to 000, data from FD_0-FD_3 from the ACRTC are output to D_0-D_3, data from FD_{16}-FD_{19} are output to D_4-D_7, and the other FD pins cannot be used. Table 5-7 show the relation of D to FD in other modes. D pins which are not connected (NC) must be held high by pull-up resistors.

GVAC Connections

The GVACs allow three shift modes to be selected externally through the operation mode pins (MOD1, MOD0). The number of GVACs used is determined by the selected shift mode, graphic bit mode (GBM) which sets ACRTC bits per pixel, and graphic address increment mode (GAI) which sets the number of display data bits read from the frame buffers simultaneously (table 8).

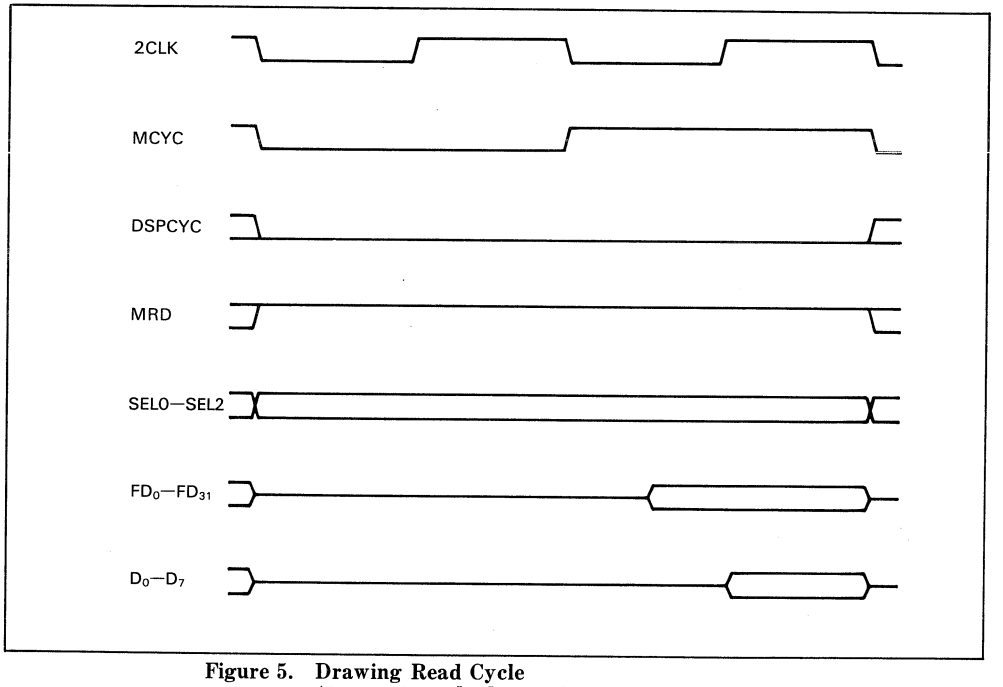


Figure 5. Drawing Read Cycle
(Frame buffer → [FD] GVAC [D] → ACRTC [MAD])

Table 8. Number of GVACs

ACRTC		GVAC						
GBM	GAI	MOD		Bits/	Words	Bits	Shift	Number of
1098	654	1	0	Pixel	Read	Read	Length	GVACs
000	000	0	0	1	1	16	16	1 (2)*
	001	0	1	1	2	32	32	1 (2)*
001	000	1	0	2	1	16	8	1 (2)*
	001	0	0	2	2	32	16	1 (2)*
	010	0	1	2	4	64	32	2 (4)*
010	001	1	0	4	2	32	8	1 (2)*
	010	0	0	4	4	64	16	2 (4)
	011	0	1	4	8	128	32	4 (8)
011	010	1	0	8	4	64	8	2 (4)
	011	1	1	8	8	128	16	4 (8)
100	011	1	0	16	8	128	8	4 (8)*

Notes: 1. *Indicates that data transfers between frame buffers and the ACRTC requires external circuits since the GVACs to ACRTC data transfer function cannot be used directly.
2. Parenthesized values are the number of GVACs required for superimpose mode (dual access mode 1) applications.

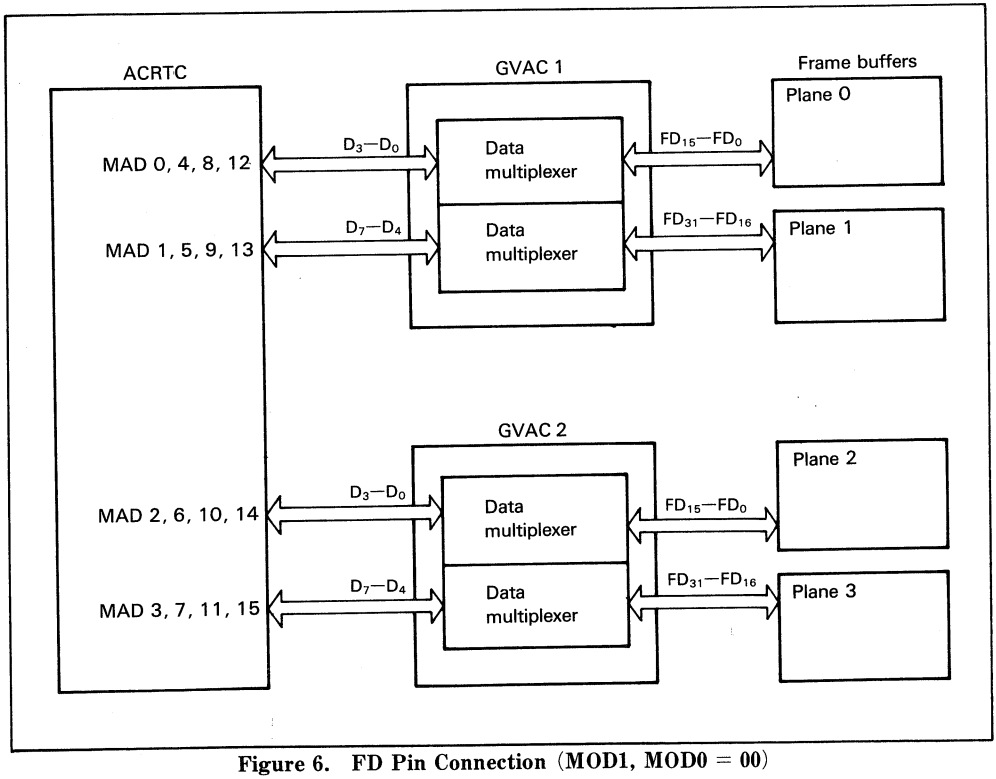


Figure 6. FD Pin Connection (MOD1, MOD0 = 00)

Data Connections

Figure 6 illustrates the data pin connection with MOD1, MOD0 set to 00. In this mode, one pixel consists of 4 bits, and four words (64 bits) are read from the frame buffers at one time.

ACRTC and GVAC Connection

ACRTC Display Data Bit Configuration : The ACRTC handles display data on a pixel basis, the ACRTC's mimimum unit. The ACRTC transfers data on a word (16-bit) basis. One memory word can consist of one or more pixels. The ACRTC's graphic bit mode (GBM) selects one of five types of pixel count. The GVACs directly support data transfers of 4 bits or 8 bits per pixel. In 4 bit/pixel mode, 16 colors or shades of grey can be implemented at one time. In 8 bit/pixel mode, 256 colors or 256 shades of grey can be realized. Figure 7 shows pixel data processed by the ACRTC depending on operation mode pin 1 (MOD1). For details on the graphic bit mode, see the ACRTC User's Manual, 5.5.6 Graphic Bit Mode.

GVAC and Graphic Data : The GVACs must be connected to handle data on a one-pixel bit plane basis. Table 9 shows the relationship between operation mode 1 (MOD1), pixel number, bit plane number, and ACRTC data.

Connection Between GVACs and ACRTC: The connection to the ACRTC depends on the operation mode (MOD1, MOD0). Table 10 shows the connection with MOD1, MOD0 = 00. In this mode, each pixel is four bits. GVAC1 handles bit planes 0 and 1, and GVAC2 handles bit planes 2 and3. The connection between the ACRTC and GVACs is determined by bit plane number and pixel number for one word from the ACRTC. In table 9, for example, ACRTC pin MAD0 corresponds to bit plane 0 for pixel number 0. From table 10, therefore, bit plane number 0 for GVAC1 is connected to pin D_0 for pixel number 1. Connection to the ACRTC in other modes are shown in table 11-13.

Table 9. Pixel Number and Plane Number

		MAD															
MOD1	ACRTC	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pixel No.	3				2				1				0			
	Bit Plane No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
1	Pixel No.	1								0							
	Bit Plane No.	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

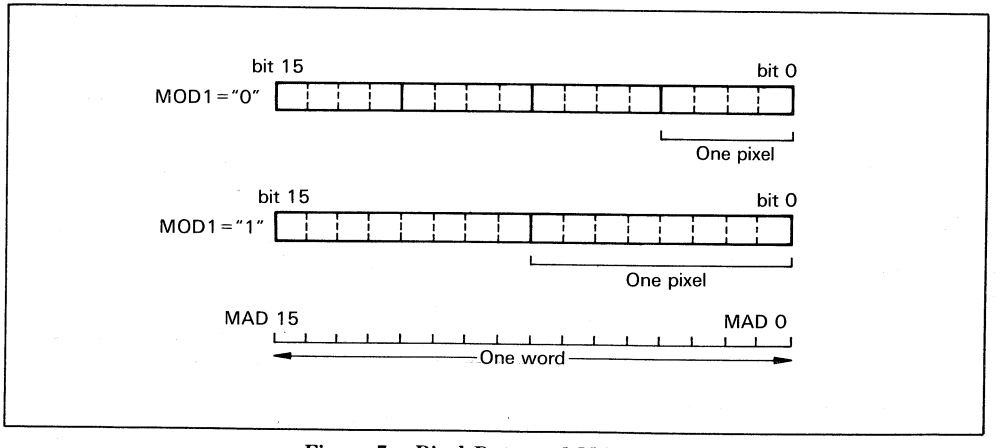


Figure 7. Pixel Data and MOD1

Table 10. ACRTC and GVAC Pin Connection, MOD1, MOD0 = 00 (4 Bits/Pixel, 16-Bit Shift Mode)

	MAD															
Connection	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pin Connection	D_7	D_3	D_7	D_3	D_6	D_6	D_6	D_2	D_5	D_1	D_5	D_1	D_4	D_0	D_4	D_0
GVAC	2	2	1	1	2	2	1	1	2	2	1	1	2	2	1	1
Pixel Number	3	3	3	3	2	2	2	2	1	1	1	1	0	0	0	0
Bit Plane	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
Frame Buffer Pixel Number	3	3	3	3	2	2	2	2	1	1	1	1	0	0	0	0

Table 11. ACRTC and GVAC Pin Connection, MOD1, MOD0 = 01 (4 Bits/Pixel, 32-Bit Shift Mode)

	MAD															
Connection	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pin Connection	D_3	D_3	D_3	D_3	D_2	D_2	D_2	D_2	D_1	D_1	D_1	D_1	D_0	D_0	D_0	D_0
GVAC	4	3	2	1	4	3	2	1	4	3	2	1	4	3	2	1
Pixel Number	3	3	3	3	2	2	2	2	1	1	1	1	0	0	0	0
Bit Plane	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
Frame Buffer Pixel Number	3	3	3	3	2	2	2	2	1	1	1	1	0	0	0	0

Note: D_7-D_4 cannot used in this mode

Table 12. ACRTC and GVAC Pin Connection, MOD1, MOD0 = 10 (8 Bits/Pixel, 8-Bit Shift Mode)

	MAD															
Connection	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pin Connection	D_7	D_5	D_3	D_1	D_7	D_5	D_3	D_1	D_6	D_4	D_2	D_0	D_6	D_4	D_2	D_0
GVAC	2	2	2	2	1	1	1	1	2	2	2	2	1	1	1	1
Pixel Number	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit Plane	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Frame Buffer Pixel Number	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Table 13. ACRTC and GVAC Pin Connection, MOD1, MOD0 = 11 (8-Bits/Pixel, 16-Bit Shift Mode)

	MAD															
Connection	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pin Connection	D_5	D_1	D_5	D_1	D_5	D_1	D_5	D_1	D_4	D_0	D_4	D_0	D_4	D_0	D_4	D_0
GVAC	4	4	3	3	2	2	1	1	4	4	3	3	2	2	1	1
Pixel Number	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit Plane	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Frame Buffer Pixel Number	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Note: D_7, D_6, D_3, D_2 cannot be used in this mode

Connection Between Frame Buffers and GVACs: Like the connection to the ACRTC, the data connection to the frame buffers is made on the basis of a bit plane consisting of one word, sequentially from the lower pixel address. Table 14 shows pixel number for the frame buffer's word (16 bits) vs bit plane number for one pixel in relation to operation mode 1 (MOD1).

Table 15 shows the connection between the GVACs and frame buffers with MOD1, MOD0 = 00. In this mode, the ACRTC's graphic address increment (GAI) is set to +4 mode, and 4-word data is simultaneously read from the frame buffers. GVAC1 handles bit planes 0 and 1, and GVAC2 handles bit planes 2 and 3. For example, pin FD_0 of GVAC1 is connected to a data pin of pixel number 0 of the n + 0 address of bit plane number 0. Connections in other modes are shown in tables 16-18.

Table 14. One-Word Frame Buffer Pixel Number and Corresponding Bit Plame Number

		One word of frame buffer															
		Pixel Number															
MOD1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Bit Plane No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Pixel No.	3				2				1				0			
1	Bit Plane No.	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Pixel No.	1								0							

Table 15. GVAC and Frame Buffer Pin Connection, MOD1, MOD0 = 00 (4 Bits/Pixel, 16-Bit Shift Mode)

GVAC		FD31	FD30	FD29	FD28	FD27	FD26	FD25	FD24	FD23	FD22	FD21	FD20	FD19	FD18	FD17	FD16	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
1	Bit Plane No.	1																0															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+3				n+2				n+1				n+0				n+3				n+2				n+1				n+0			
2	Bit Plane No.	3																2															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+3				n+2				n+1				n+0				n+3				n+2				n+1				n+0			

Table 16. GVAC and Frame Buffer Pin Connection, MOD1, MOD0 = 01 (4 Bits/Pixel, 32-Bit Shift Mode)

GVAC		FD31	FD30	FD29	FD28	FD27	FD26	FD25	FD24	FD23	FD22	FD21	FD20	FD19	FD18	FD17	FD16	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
1	Bit Plane No.	0																															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+7				n+6				n+5				n+4				n+3				n+2				n+1				n+0			
2	Bit Plane No.	1																															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+7				n+6				n+5				n+4				n+3				n+2				n+1				n+0			
3	Bit Plane No.	2																															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+7				n+6				n+5				n+4				n+3				n+2				n+1				n+0			
4	Bit Plane No.	3																															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+7				n+6				n+5				n+4				n+3				n+2				n+1				n+0			

Video Signal Generation

A GVAC performs parallel-to-serial conversion on 32-bit data read from frame buffers using the shift register, and produces 4-bit video signals (VIDEOA -VIDEOD).

The GVAC recognizes the cycle in which display data is read from frame buffers by memory cycle (MCYC) and memory read (MRD) signals from the ACRTC, display cycle (DSPCYC) from GMIC, and access mode (AM) signal externally set. The GVAC then latches 32-bit data supplied from FD_0-FD_{31} pins.

The latched display data is fed to the shift register on the falling edge of the dot clock (DOTCK) when the shift load ($\overline{SLD}$) input is asserted. This data is then shifted on the falling edge of the dot clock (DOTCK) when shift clock enable (SCKE) is asserted.

As seen in figure 8, 32-bit display data is output sequentially to four video signal pins one bit by one bit per dot clock (DOTCK).

- VIDEOA : 32 bits of FD_0-FD_{31}
- VIDEOB : 24 bits of FD_8-FD_{31}
- VIDEOC : 16 bits of FD_{16}-FD_{31}
- VIDEOD : 8 bits of FD_{24}-FD_{31}

Using the display timing signal ($\overline{DISP}$) from the ACRTC, 4-bit shift register output data can be masked. That is, while $\overline{DISP}$ is asserted, shift register output is provided as video signals, and while it is negated, shift register output is held low, and video signals are not output. The required number of dot cycles per display cycle is the same as the shift length value set by the operation mode (MOD1, MOD0).

Table 19 shows the dot clock cycle count per display cycle vs operation mode (MOD1, MOD0).

Table 17. GVAC and Frame Buffer Pin Connection, MOD1, MOD0 = 10 (8 Bits/Pixel, 8-Bit Shift Mode)

GVAC		FD31	FD30	FD29	FD28	FD27	FD26	FD25	FD24	FD23	FD22	FD21	FD20	FD19	FD18	FD17	FD16	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
	Bit Plane No.	3								2								1								0							
1	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0	
	Bit Plane No.	7								6								5								4							
2	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0	

Table 18. GVAC and Frame Buffer Pin Connection, MOD1, MOD0 = 11 (8 Bits/Pixel, 16-Bit Shift Mode)

GVAC		FD31	FD30	FD29	FD28	FD27	FD26	FD25	FD24	FD23	FD22	FD21	FD20	FD19	FD18	FD17	FD16	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
	Bit Plane No.	1																0															
1	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0		n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0	
	Bit Plane No.	3																2															
2	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0		n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0	
	Bit Plane No.	5																4															
3	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0		n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0	
	Bit Plane No.	7																6															
4	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0		n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0	

Figure 9, 10 and 11 show ACRTC frame buffer access vs video outputs in single access mode, dual access mode 0, and dual access mode 1. Superimposed display in dual access mode 1 requires that the window smooth scroll input (WSS) be high.

The GVAC provides display data output sequentially from four video outputs VIDEOA-VIDEOD synchronously with the dot clock while the shift clock enable input (SCKE) is asserted. Figure 12 shows the video signals output in GMIC divide-by-16 mode, GVAC's MOD1, MOD0 = 01, 32-bit shift mode. When shift load ($\overline{SLD}$) is asserted, display data (FD_{31}-FD_0) is sent to the shift register at the rising edge of the dot clock (DOTCK) to provide the sequential outputs. That is, video output A (VIDEOA) receives sequential outputs starting with FD_0, and the other video pins receive display data likewise. Figure 13 shows the video signals output in GMIC divide-by-4 mode, GVAC in 16-bit shift mode, and the ACRTC set in dual access mode 0. Figure 14 shows video outputs in the 8-bit shift mode, with the other conditions the same as in figure 13.

Table 19. Shift Length and Shift Clock

MOD1	MOD0	Shift Length	Dot Clocks/ Display Cycle
0	0	16	16
0	1	32	32
1	0	8	8
1	1	16	16

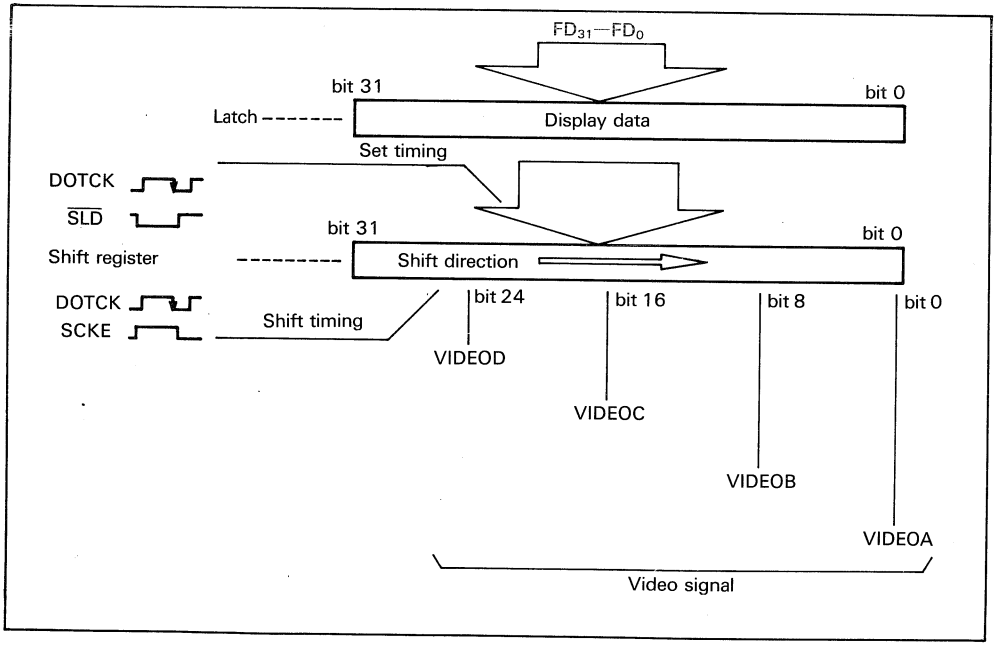


Figure 8. Video Signal Generation

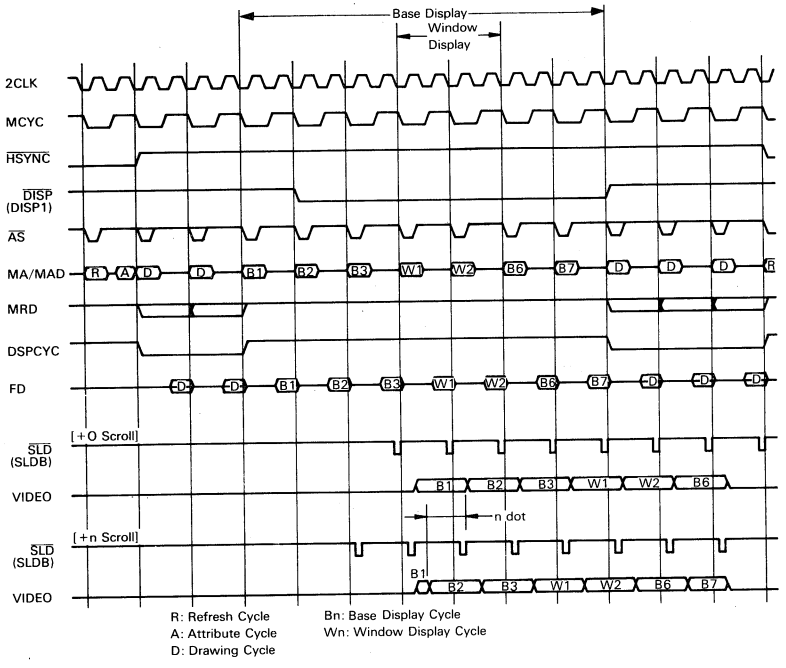


Figure 9. Video Output Timing (Single Access Mode)

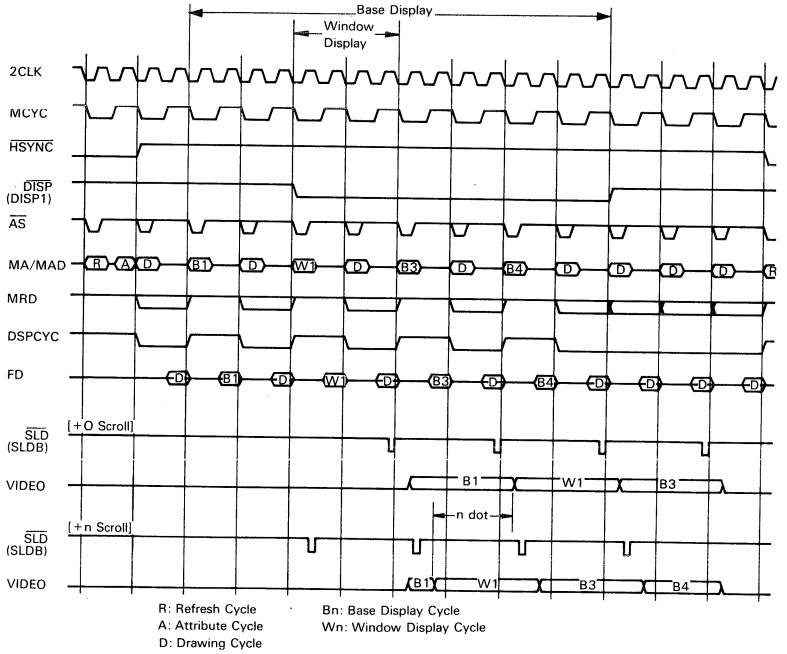


Figure 10. Video Output Timing (Dual Access Mode 0)

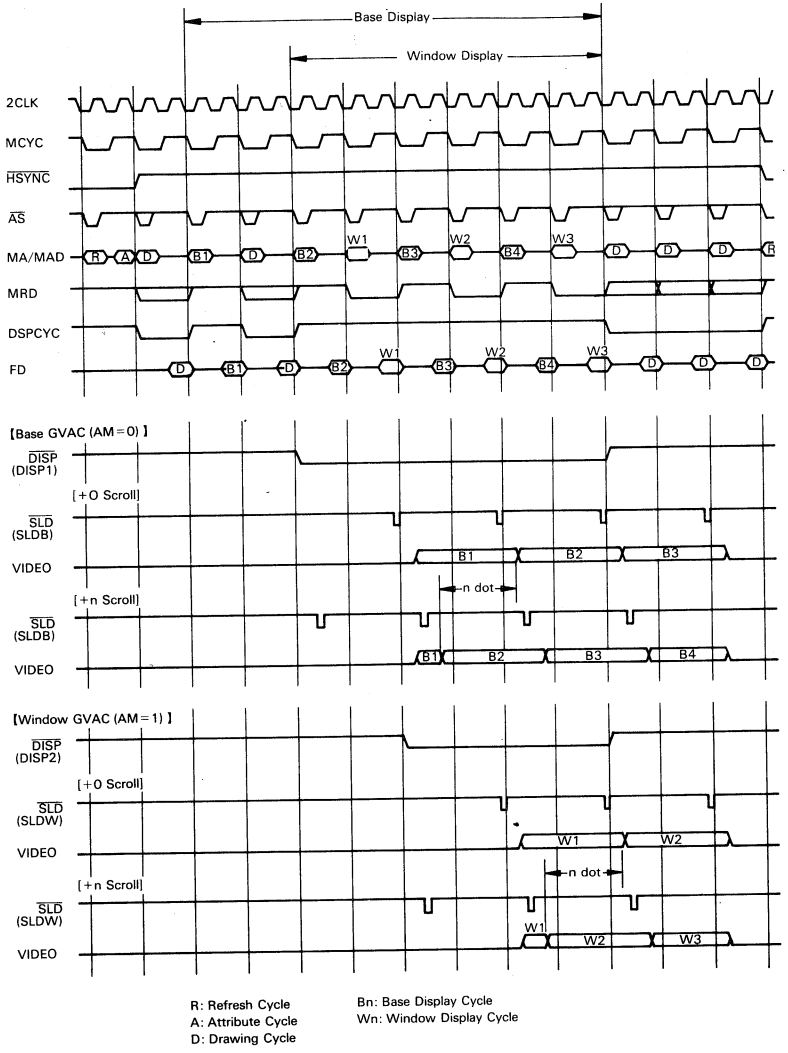


Figure 11. Video Output Timing (Dual Access Mode 1)

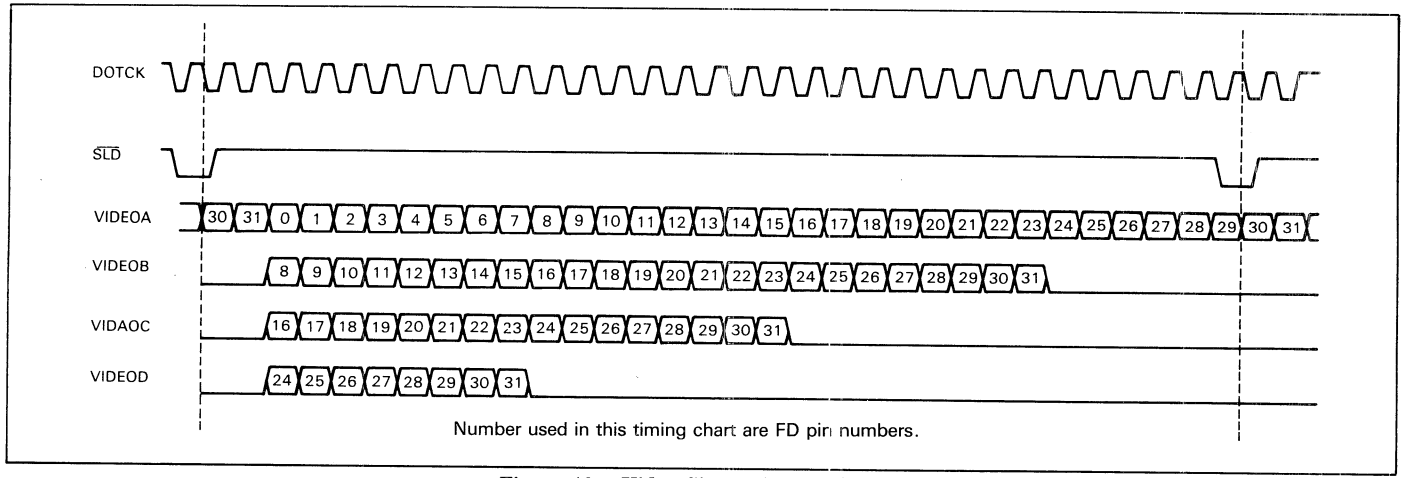


Figure 12. Video Signal Output (32-Dot Shift)

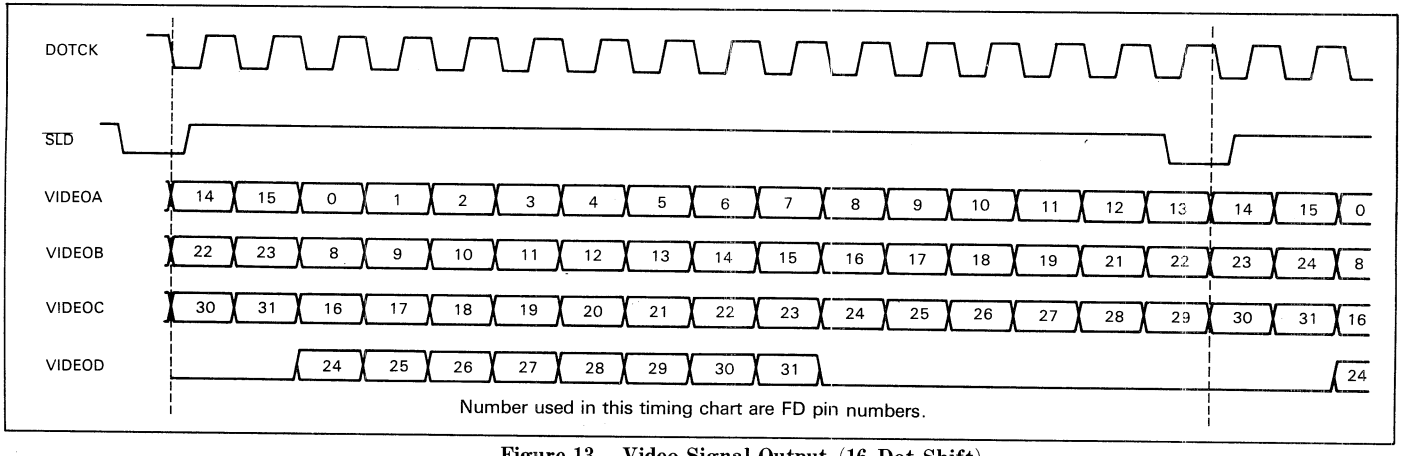


Figure 13. Video Signal Output (16-Dot Shift)

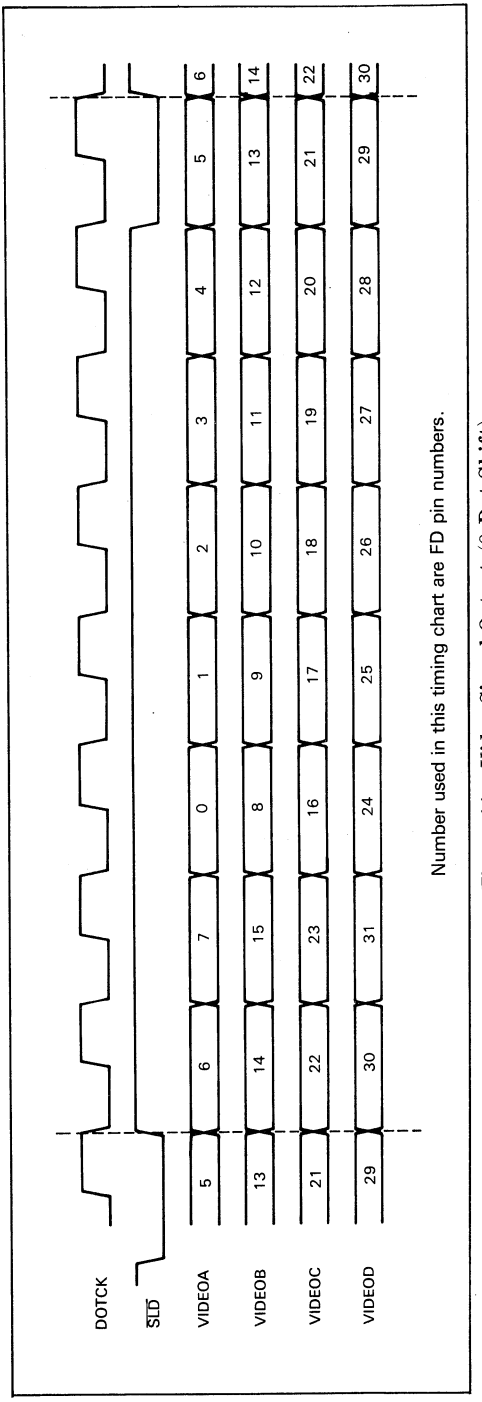


Figure 14. Video Signal Output (8-Dot Shift)

Horizontal Smooth Scrolling

The GVAC performs horizontal smooth scrolling when the assertion period of the shift load signal ($\overline{SLD}$) is shifted on a dot clock basis. Table 20 shows horizontal smooth scroll dot count vs shift amount for the shift load signal ($\overline{SLD}$) in units of one dot clock cycle. Smooth scrolling is easily implemented by specifying the ACRTC's horizontal smooth scrolling dot (HSD) and sending the GMIC's $\overline{SLDB}/\overline{SLDW}$ signal to the GVAC. HSD and $\overline{SLDB}/\overline{SLDW}$ are discussed in the ACRTC User's Manual, and GMIC Data Sheet respectively.

Figure 15-18 illustrate video signal outputs for smooth scrolling vs frame buffer access in each mode. Video output start timing for display data is shifted corresponding to the shifted assertion of the HSD input. This video signal output is ANDed with the display timing signal ($\overline{DISP}$) and two-memory-cycle delayed (a signal indicating the output enable period for the video pins). Therefore, the video output signal of display data read from frame buffers by the first display amount. In the last display cycle of a raster, accessed display data output bits corresponding to the scrolling amount are displayed, and the remaining bits are removed.

Horizontal Zoom

Video signals for zooming are obtained when the period of the shift clock corresponding to the dot clock is extended by the shift clock enable (SCKE) input. The ACRTC specifies the zoom scale (HZ3-HZ0), and the GMIC outputs the SCKE control signal according to the specified zoom scale. SCKE is sent to the GVACs to implement zooming. Figures 15-17 show zoom display timing for each mode. In figure 15, quadruple zoom is performed by applying the shift clock enable (SCKE) once during the four-cycle dot clock (DOTCK).

Table 20. Horizontal Smooth Scroll Amount and $\overline{SLD}$ Cycle Count

MOD		Dot count for horizontal smooth scroll																Shift
1	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	length
0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	32
1	0	0	1	2	3	4	5	6	7	Cannot be used								8
1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

MOD		Dot count for horizontal smooth schrool																Shift
1	0	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	length
0	0	Cannot be used																6
0	1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	0	Cannot be used																8
1	1	Cannot be used																16

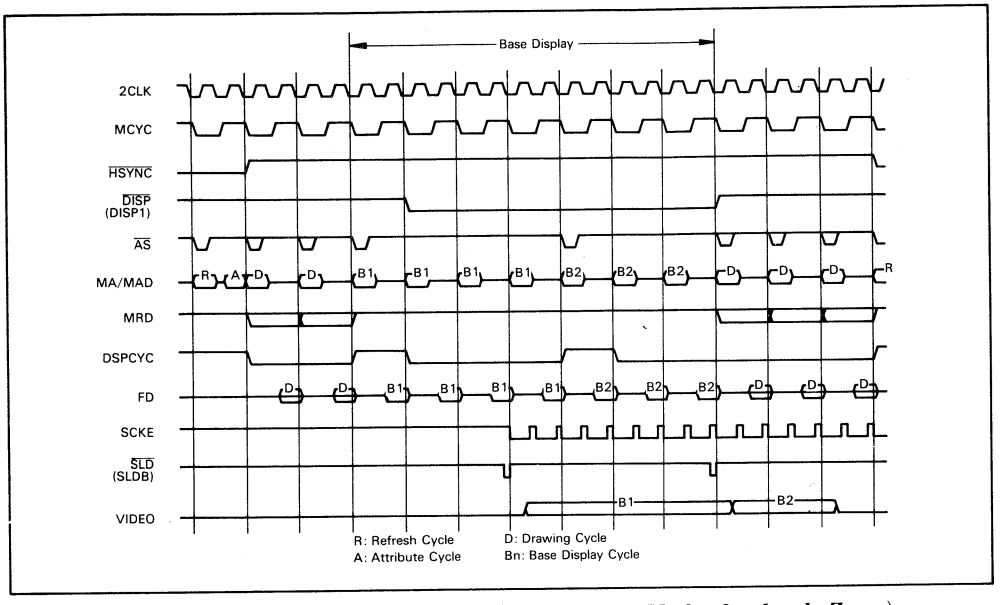


Figure 15. Zoom Display Timing (Single Access Mode, Quadruple Zoom)

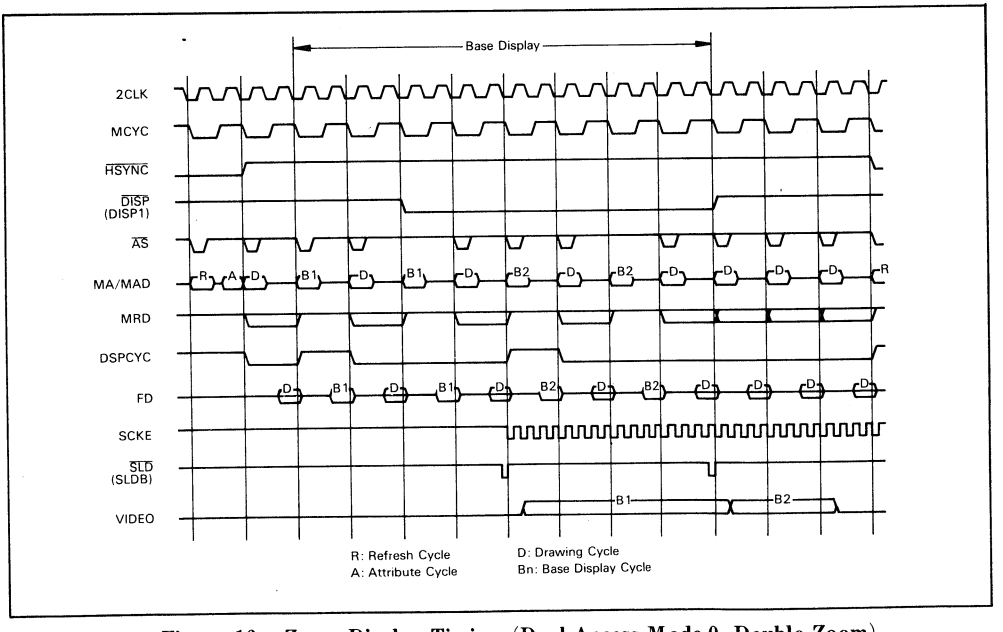


Figure 16. Zoom Display Timing (Dual Access Mode 0, Double Zoom)

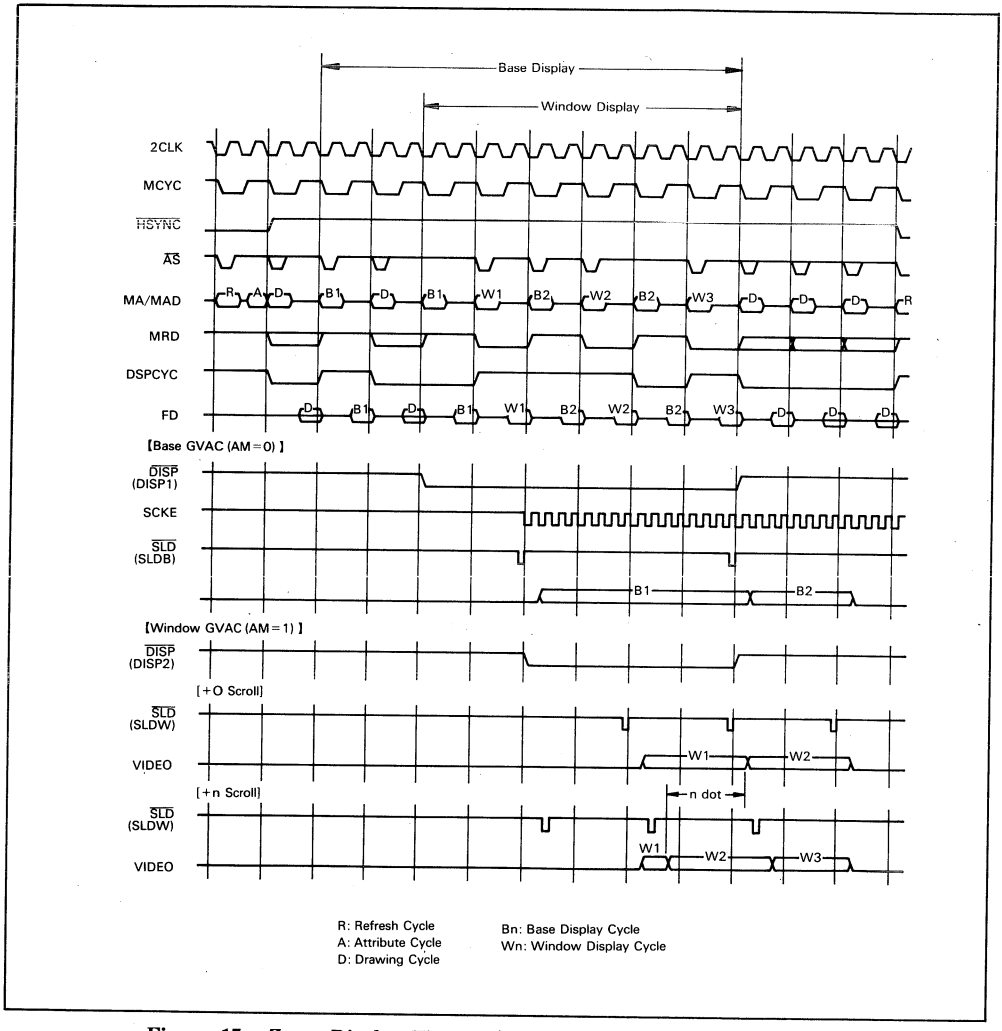


Figure 17. Zoom Display Timing (Dual Access Mode 1, Double Zoom)

Absolute Maximum Ratings (All voltages referenced to $V_{SS} = 0$ V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{in}	−0.3 to V_{CC} +0.3	V
Output voltage	V_{out}	5.5	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{str}	−55 to +150	°C

Notes: Using an LSI beyond its maximum ratings may result in its permanent destruction. LSI's should usually be operated under the recommended operating conditions. Exceeding any of these conditions may adversely affect its reliabity.

Recommended Operating Conditions (All voltages referenced to $V_{SS} = 0$ V)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Input voltage low	V_{IL}	0	—	0.7	V
Input voltage high	V_{IH}	2.2	—	V_{CC}	V
Operating temperature	T_{opr}	0	25	70	°C

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, T_a = 0℃ to +70℃, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Condition
Input voltage high		V_{IH}	2.2	V_{CC}	V	
Input voltage low		V_{IL}	−0.3	0.7	V	
Input clamp voltage		V_I		−1.5	V	V_{CC} = 4.75 V, I_{in} = −18 mA
Output voltage high		V_{OH}	2.7		V	V_{CC} = 4.75 V, I_{OH} = −400 mA
Output voltage low		V_{OL}		0.5	V	V_{CC} = 4.75 V, I_{OL} = 8 mA
Input current high		I_{IH}		20	μA	V_{CC} = 5.25 V, V_I = 2.7 V
Input current low		I_{IL}		−400	μA	V_{CC} = 5.25 V, V_I = 0.4 V
Output short circuit current		I_{OS}	−40	−120	mA	V_{CC} = 5.25 V
Current consumption		I_{CC}		160	mA	V_{CC} = 5.25 V
Input capacitance		C_{in}		10	pF	
Off-state output current	D_7-D_0,	I_{OZH}		20	μA	V_{CC} = 5.25 V, V_O = 2.7 V
	FD_{31}-FD_0	I_{OZL}		−20	μA	V_{CC} = 5.25 V, V_O = 0.4 V

AC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, T_a = 0℃ to +70℃)

			32 MHz		48 MHz		64 MHz			
No	Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Figure
	DOTCK operation frequency	f		32		48		64	MHz	
①	DOTCK cycle time	t_C	31.3		20.8		15.6		ns	18
②	DOTCK high level pulse width	t_{HW}	12		9		6		ns	
③	DOTCK low level pulse width	t_{LW}	12		9		6		ns	
④	DOTCK rise time	t_R		5		5		5	ns	
⑤	DOTCK fall time	t_F		5		5		5	ns	
⑥	SCKE setup time	t_{SCKS}	6		2		0		ns	
⑦	SCKE hold time	t_{SCKH}	5		5		5		ns	
⑧	$\overline{SLD}$ setup time	t_{SLDS}	6		2		0		ns	
⑨	$\overline{SLD}$ hold time	t_{SLDH}	3		3		3		ns	
⑩	VIDEO delay time	t_{VD}	3	24	3	17	3	14	ns	
⑪	2CLK setup time	t_{2CKS}	6		2		0		ns	19-21
⑫	MCYC setup time	t_{MCYCS}	30		30		30		ns	
⑬	MCYC hold time	t_{MCYCH}	0		0		0		ns	
⑭	FD threestate recovery time	t_{FDR}	5		5		5		ns	20
⑮	FD setup time	t_{FDS}	30		30		30		ns	21
⑯	FD hold time	t_{FDH}	5		5		5		ns	

AC Characteristics (cont)

No	Item	Symbol	32 MHz Min	32 MHz Max	48 MHz Min	48 MHz Max	64 MHz Min	64 MHz Max	Unit	Figure
⑰	D three state recovery time	t_{DR}	5		5		5		ns	19
⑱	D hold time	t_{DH}	5		5		5		ns	
⑲	FD delay time from D	t_{FDDLY}		30		30		18	ns	20
⑳	D delay time from FD	t_{DDLY}		30		30		18	ns	19
㉑	SEL setup time	t_{SELS}	10		10		10		ns	19, 20
㉒	SEL hold time	t_{SELH}	5		5		5		ns	
㉓	DSPCYC setup time	t_{DSPS}	20		20		20		ns	19-21
㉔	DSPCYC hold time	t_{DSPH}	5		5		5		ns	
㉕	MRD setup	t_{MRDS}	20		20		20		ns	
㉖	MRD hold time	t_{MRDH}	10		10		10		ns	
㉗	$\overline{DISP}$ setup time	t_{DISPS}	20		20		20		ns	21

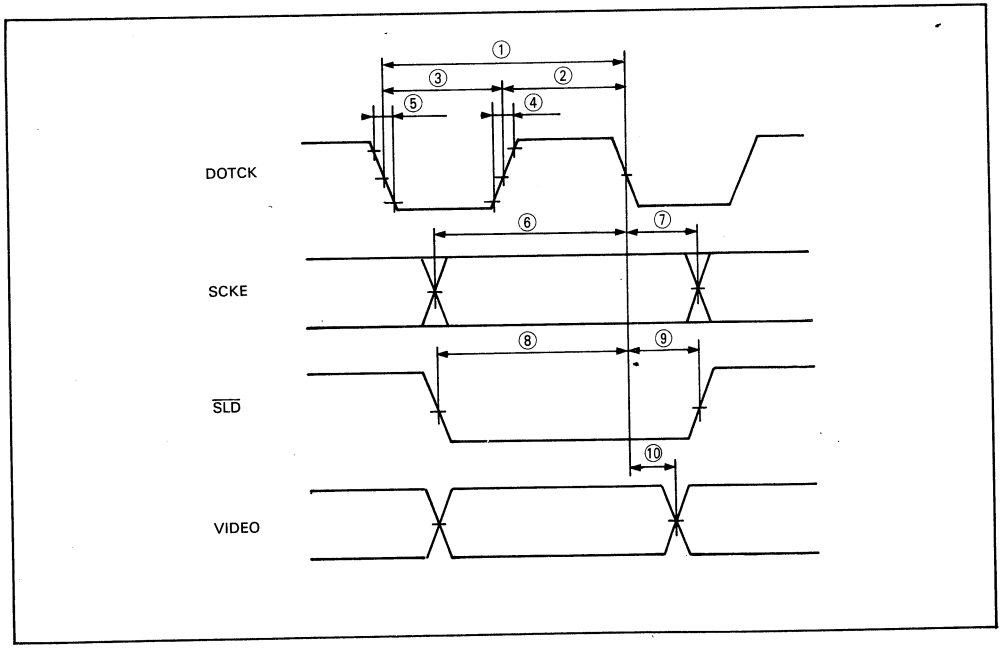


Figure 18. Dot Clock

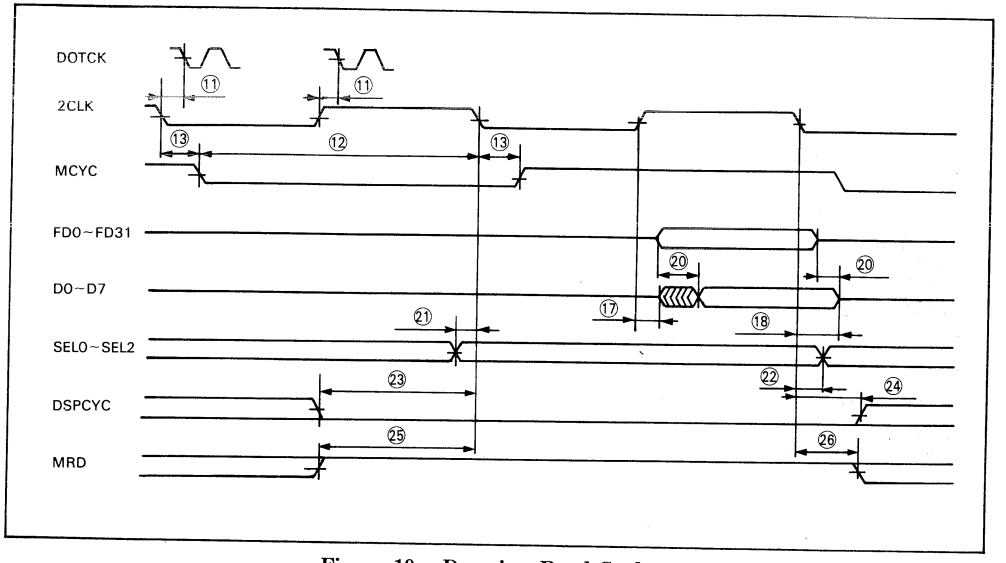


Figure 19. Drawing Read Cycle

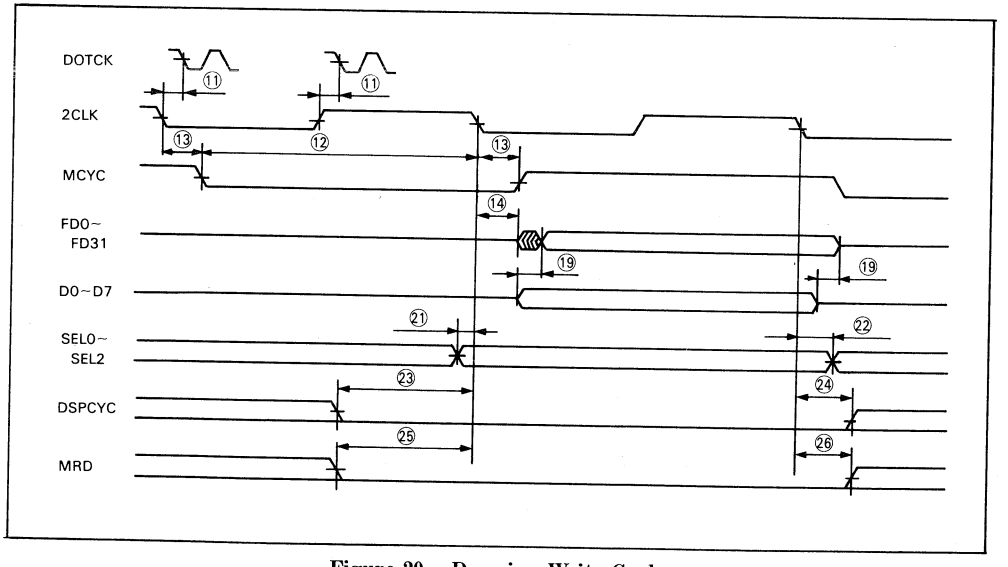


Figure 20. Drawing Write Cycle

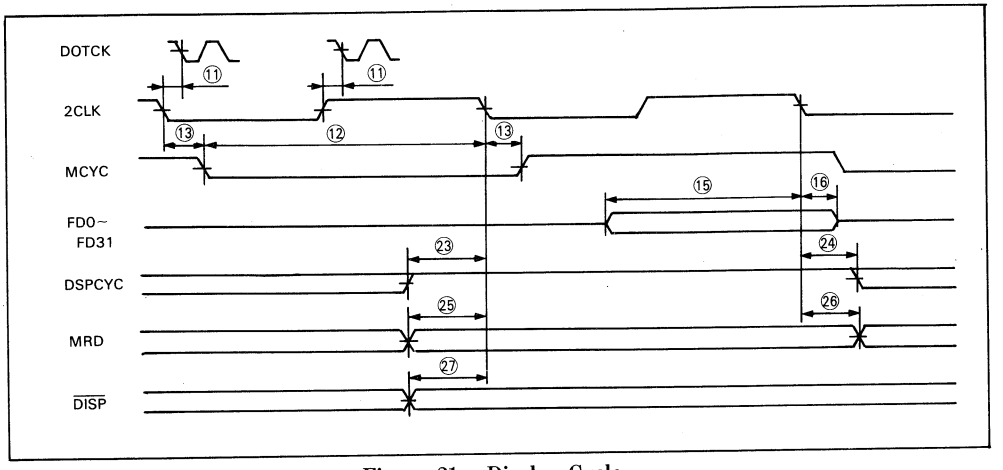
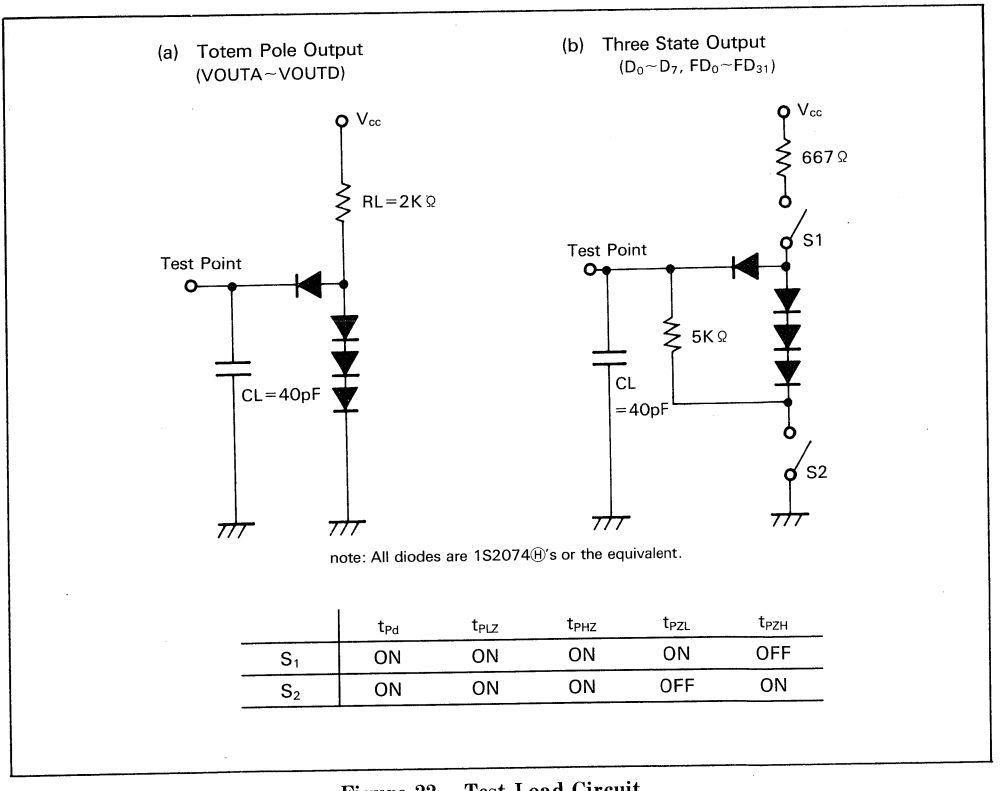


Figure 21. Display Cycle



note: All diodes are 1S2074Ⓗ's or the equivalent.

	t_{Pd}	t_{PLZ}	t_{PHZ}	t_{PZL}	t_{PZH}
S_1	ON	ON	ON	ON	OFF
S_2	ON	ON	ON	OFF	ON

Figure 22. Test Load Circuit

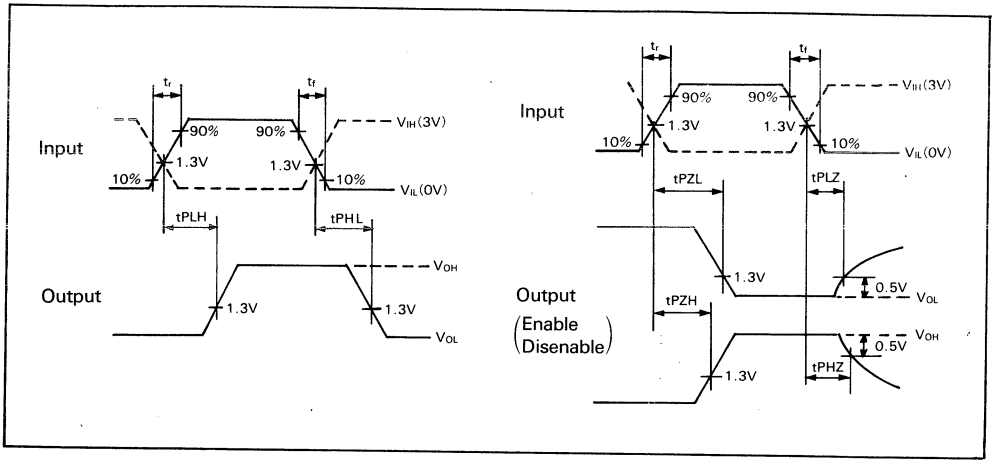


Figure 23. Input/Output waveforms

Reference Literature

Product	Data Sheet	User's Manual	Application Note	Others
HD63484 ACRTC	E-0045A	680-1-31A	Introduction to ACRTC Application 680-3-08 Circuits Software 680-3-07	Programming Reference AD-E0032A
HD63485 GMIC	AD-E0122	——		——

Refer to application note (No. 680-3-15) for detail of this product.

HD63487

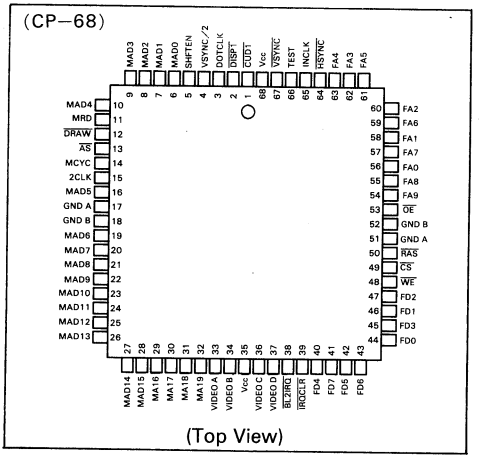
Memory Interface and Video Attribute Controller (MIVAC)

The MIVAC belongs to the HD63484 ACRTC (Advanced CRT Controller) family. It includes peripheral control circuits for graphic display on a chip. Incorporating bus driver circuits and a DRAM interface, the MIVAC allows direct connection to DRAMs with no external circuits. On-chip Parallel/Serial converting shift register generates high speed video signals. Adopting static column mode, fast memory access achieves high throughput in spite of narrow memory data bus. The MIVAC provides most functions required at peripherals of a frame buffer for graphic display constructed with 1 to 4 memory chips, and enables small size graphic system easily. Using the Hi-BiCMOS process, the MIVAC achieves high speed memory access with low power dissipation.

Features

- Directly connected with 1 to 4 memory devices (x 4 bit organization, static column mode)
- Generates DRAM interface signals: row and column address, $\overline{RAS}$, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$ and memory data
- Generates high speed video signal: dot rate of 33MHz (max)
- 16 kinds of operation modes by the combination of;
  —2, 4 and 16 colors (1, 2 and 4 bit/pixel)
  —8, 16 and 32 dot shift
  —Single/Dual access
  —1, 2 and 4 chips memory
- Blinking block cursor display
- Memory variation: 256kx4 static column mode DRAM
- Generates special clock to drive the ACRTC (asymmetrical 2CLK)
- Input clock divider to generate dot clocks (divided by 1, 2 and 4)
- Supports frame sequential application
  —$\overline{VSYNC}$ divider and VSYNC/2 output
  —4 → 2 bit video output multiplexer
- BLINK2 interrupting control ($\overline{BL2IRQ}$ output)
- $\overline{CS}$ before $\overline{RAS}$ refresh
- Direct interface with the ACRTC
- Supports hardware window of ACRTC
- TTL compatible input/output
- Single +5V power supply
- Low power dissipation

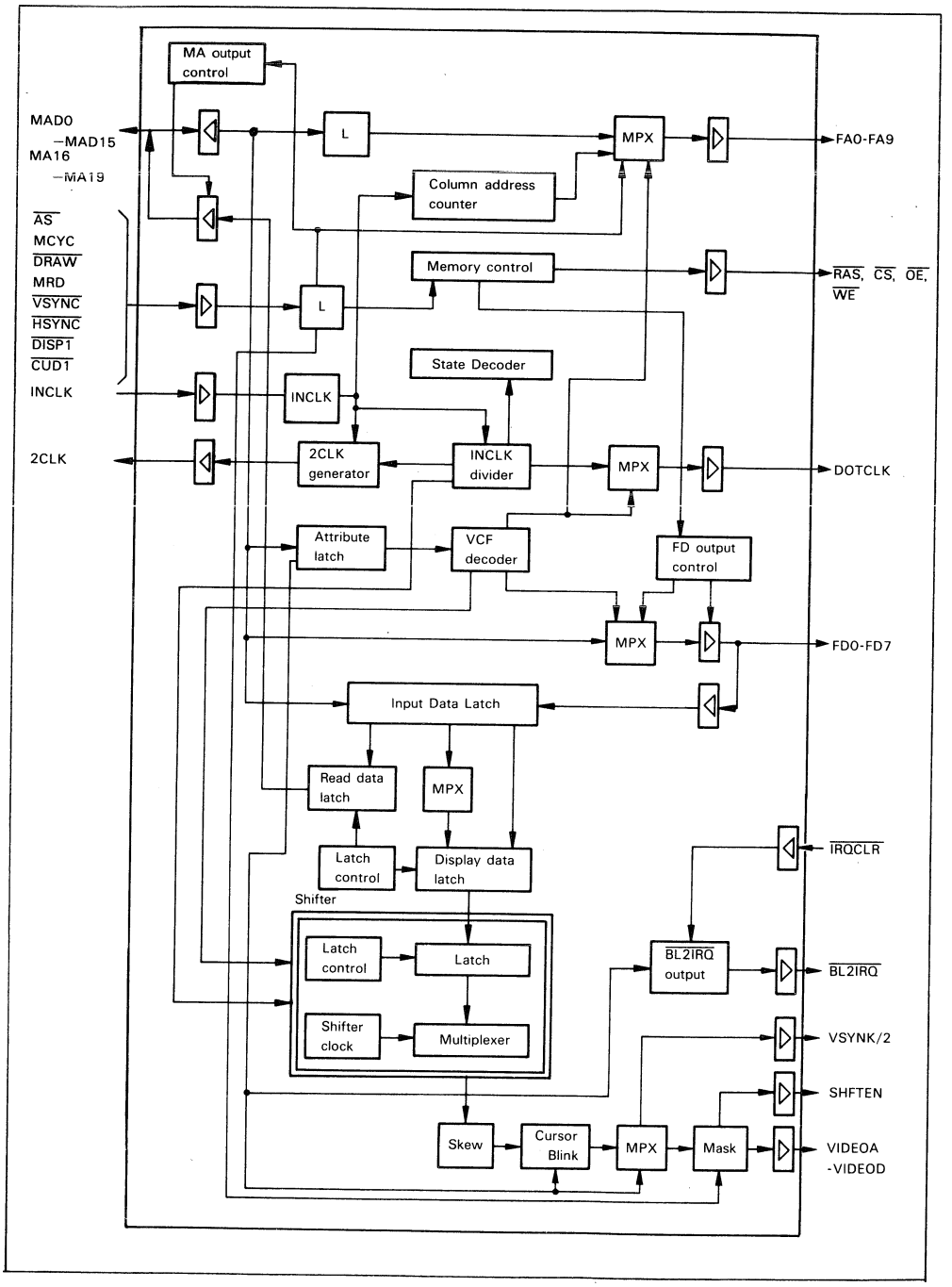
Pin Assignment



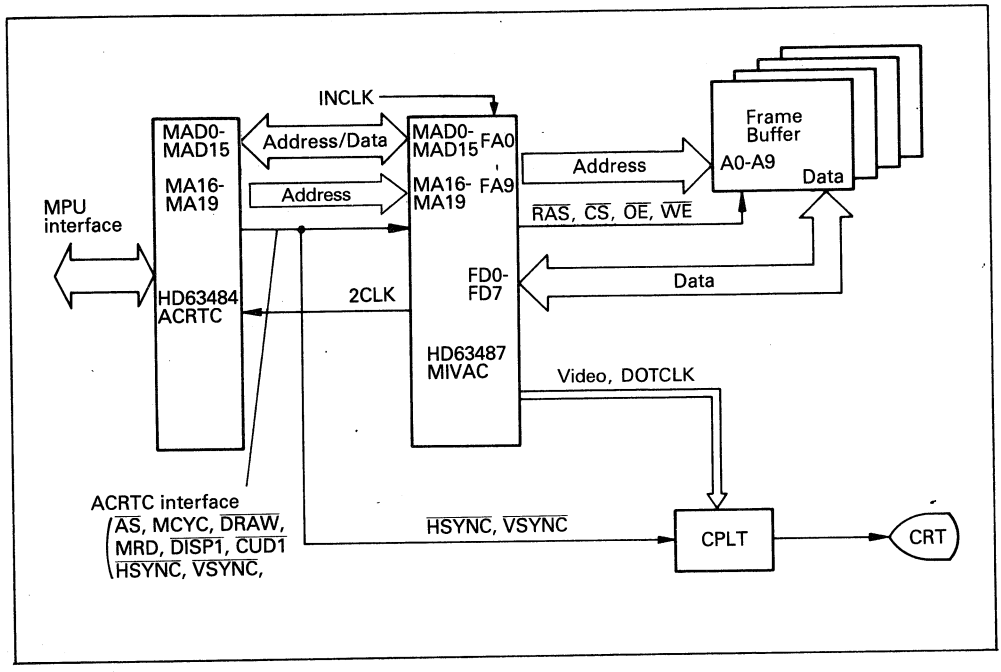
Function Table

Mode	Attribute code (ACRTC) MAD3	MAD2	MAD1	MAD0	MCYC Fetch	Access Mode	Memory Chip	Bit/ Pixel	Shifted Dot	DOTCK Division
0	0	0	0	0	1	Single	1	1	16	1
1	0	0	0	1	1	Single	1	2	8	2
2	0	0	1	0	1	Single	1	4	4	4
3	0	0	1	1	1	Single	2	2	16	1
4	0	1	0	0	1	Single	2	4	8	2
5	0	1	0	1	1	Single	4	4	16	1
6	0	1	1	0	1	Dual	1	1	16	2
7	0	1	1	1	1	Dual	1	2	8	4
8	1	0	0	0	1	Dual	2	1	32	1
9	1	0	0	1	1	Dual	2	2	16	2
A	1	0	1	0	1	Dual	2	4	8	4
B	1	0	1	1	1	Dual	4	2	32	1
C	1	1	0	0	1	Dual	4	4	16	2
D	1	1	0	1	2	Single	1	2	32	1
E	1	1	1	0	2	Single	1	4	16	2
F	1	1	1	1	2	Single	2	4	32	1

Block Diagram



System Application Example



Power Supply (V_{CC}, V_{SS})

V_{SS} and V_{CC} are the MIVAC power supply pins. V_{CC} pins are +5V ±5% supply pins. V_{SS} are the ground pins. Be sure to connect all four V_{SS} pins to ground and both V_{CC} pins to the power supply.

Operation Control Signals

In Clock (INCLK): This is basic operating clock for the MIVAC.

Test (TEST): The TEST input is used for manufacturing operational testing. It must be fixed low when the MIVAC is mounted in a system.

ACRTC Interface Signals

Clock (2CLK): The 2CLK clock output is a basic clock for the ACRTC's internal operation. The MIVAC generates 2CLK by dividing the INCLK.

Memory Cycle (MCYC): The ACRTC's MCYC output supplies this input. The MCYC input indicates the ACRTC's frame buffer access timing. MCYC is low when the ACRTC is in the address cycle, and high when the ACRTC is in the data cycle.

Draw ($\overline{DRAW}$): The ACRTC's $\overline{DRAW}$ output supplies this input. The $\overline{DRAW}$ input indicates whether the ACRTC memory cycle is a drawing cycle. $\overline{DRAW}$ is low during drawing cycle, and high otherwise. The MIVAC uses $\overline{DRAW}$ to recognize display cycles, and also to generate DRAM control signals.

Memory Read (MRD): The ACRTC's MRD output supplies this input. The MRD input controls data transfer between frame buffers and the ACRTC. The ACRTC pulls MRD high when it reads data from the frame buffer, and low when it writes data.

Address Strobe ($\overline{AS}$): The ACRTC's $\overline{AS}$ output supplies this input. The $\overline{AS}$ input is a latch timing signal for the memory address sent from the ACRTC. Additionally, $\overline{AS}$ indicates whether memory is begun accessed.

Horizontal Sync ($\overline{HSYNC}$): The ACRTC's $\overline{HSYNC}$ output supplies this input. The $\overline{HSYNC}$ input is a DRAM refresh cycle control signal to horizontally synchronize CRT displays. The MIVAC performs $\overline{CS}$ before RAS refresh when $\overline{HSYNC}$ is low and $\overline{DRAW}$ is high when $\overline{AS}$ pulses are input.

Vertical Sync ($\overline{VSYNC}$): The ACRTC's output supplies this input. The MIVAC internally divides $\overline{VSYNC}$ by 2 to generate the VSYNC/2 output.

Display 1 ($\overline{DISP1}$): The ACRTC's $\overline{DISP1}$ output supplies this input. It indicates the screen's display period. Usually, the ACRTC's DSP (display signal control) bit is set to 1.

Cursor Display 1 ($\overline{CUD1}$): The ACRTC's $\overline{CUD1}$ output supplies this input. It is low when the graphic cursor is display period.

Memory Address/Data 0-15 (MAD0-MAD15): The ACRTC's MAD0-MAD15 output supplies this input. When MCYC is low, MAD0-MAD15 indicate the frame buffer address. When MCYC is high, they transfer the drawing data to and from the frame buffer.

Memory Address 16-19 (MA16-MA19): The ACRTC's address MA16-MA19 for frame buffer access supplies this input.

Frame Buffer Access Signals

Row Address Strobe ($\overline{RAS}$): The MIVAC outputs the DRAMs' $\overline{RAS}$ timing signal on the $\overline{RAS}$ output.

Chip Select ($\overline{CS}$): The MIVAC outputs the DRAMs' $\overline{CS}$ timing signal on the $\overline{CS}$ output.

Write Enable ($\overline{WE}$): The MIVAC outputs the DRAM's $\overline{WE}$ timing signals on the $\overline{WE}$ outputs.

Output Enable ($\overline{OE}$): The MIVAC outputs the DRAMs' output timing signal on the $\overline{OE}$ output.

Frame Buffer Address (FA0-FA7): The MIVAC outputs the multiplexed DRAM address on FA0-FA7.

Frame Buffer Data (FD0-FD7)

The 8 bit FD0-FD7 frame buffer data I/O bus transfers data between the ACRTC and frame buffers and inputs display data from the frame buffers. In 1 chip memory mode, FD0-FD3 is used. In 2 or 4 chips memory mode, FD0-FD7 is used.

CRT Display Interface

Dot Clock (DOTCLK): The MIVAC internally divides INCLK by 1, 2 or 4 to generate the DOTCLK output. DOTCLK division ratio depends on VCF0-VCF3 of attribute code.

Video Outputs (VIDEOA-VIDEOD): VIDEOA-VIDEOD are the four bits output from the MIVAC's parallel-to-serial conversion shift register. They are supplied during a display period specified by the display signal ($\overline{DISP}$). Which outputs are usable depends on the attribute code (VCF0-VCF3).

Shift Enable (SHFTEN): SHFTEN is active high output. This output indicates the active display period of the screen.

Vertical Sync Divide-by-2 (VSYNC/2): VSYNC/2 output is $\overline{VSYNC}$ signal from the ACRTC divided by two.

Others

BLINK2 Interrupt ($\overline{BL2IRQ}$): This output is sat by BLINK2 (MA19) of the attribute code. $\overline{BL2IRQ}$ is low when BLINK2 is high.

BLINK2 Interrupt Clear ($\overline{IRQCLR}$): This input clears the $\overline{BL2IRQ}$ signal. When $\overline{IRQCLR}$ is low, $\overline{BL2IRQ}$ is clear and high.

Pin Description

Signal	Description	Pin No.
V_{CC}	Power	68
V_{CC}	Power	35
V_{SS}	Logic ground	52
V_{SS}	Logic ground	51
V_{SS}	Logic ground	18
V_{SS}	Logic ground	17
2CLK	Output clock to the ACRTC	15
MCYC	Memory cycle input from the ACRTC	14
$\overline{DRAW}$	Draw input from the ACRTC	12
$\overline{MRD}$	Memory read input from the ACRTC	11
$\overline{AS}$	Address strobe input from the ACRTC	13
MAD0	Multiplex frame buffer address/data to/from ACRTC	6
MAD1	Multiplex frame buffer address/data to/from ACRTC	7
MAD2	Multiplex frame buffer address/data to/from ACRTC	8
MAD3	Multiplex frame buffer address/data to/from ACRTC	9
MAD4	Multiplex frame buffer address/data to/from ACRTC	10
MAD5	Multiplex frame buffer address/data to/from ACRTC	16
MAD6	Multiplex frame buffer address/data to/from ACRTC	19
MAD7	Multiplex frame buffer address/data to/from ACRTC	20
MAD8	Multiplex frame buffer address/data to/from ACRTC	21
MAD9	Multiplex frame buffer address/data to/from ACRTC	22
MAD10	Multiplex frame buffer address/data to/from ACRTC	23
MAD11	Multiplex frame buffer address/data to/from ACRTC	24
MAD12	Multiplex frame buffer address/data to/from ACRTC	25
MAD13	Multiplex frame buffer address/data to/from ACRTC	26
MAD14	Multiplex frame buffer address/data to/from ACRTC	27
MAD15	Multiplex frame buffer address/data to/from ACRTC	28
MA16	Memory address line 16 from the ACRTC	29
MA17	Memory address line 17 from the ACRTC	30
MA18	Memory address line 18 from the ACRTC	31
MA19	Memory address line 19 from the ACRTC	32

Pin Description (cont)

Signal	Description	Pin No.
$\overline{\text{HSYNC}}$	Holizontal sync input from the ACRTC	64
$\overline{\text{VSYNC}}$	Vertical sync input from the ACRTC	67
VSYNC/2	Vertical sync divide-by-2 output	4
$\overline{\text{CUD1}}$	Cursor control input from the ACRTC	1
$\overline{\text{DISP1}}$	Display input from the ACRTC	2
$\overline{\text{RAS}}$	Row address strobe output to DRAM	50
$\overline{\text{CS}}$	Chip select output to DRAM	49
$\overline{\text{WE}}$	Write enable output to DRAM	48
$\overline{\text{OE}}$	Output enable output to DRAM	53
FA0	Frame buffer (memory) address output 0	56
FA1	Frame buffer (memory) address output 1	58
FA2	Frame buffer (memory) address output 2	60
FA3	Frame buffer (memory) address output 3	62
FA4	Frame buffer (memory) address output 4	63
FA5	Frame buffer (memory) address output 5	61
FA6	Frame buffer (memory) address output 6	59
FA7	Frame buffer (memory) address output 7	57
FA8	Frame buffer (memory) address output 8	55
FA9	Frame buffer (memory) address output 9	54
FD0	Frame buffer data input/output line 0	44
FD1	Frame buffer data input/output line 1	46
FD2	Frame buffer data input/output line 2	47
FD3	Frame buffer data input/output line 3	45
FD4	Frame buffer data input/output line 4	40
FD5	Frame buffer data input/output line 5	42
FD6	Frame buffer data input/output line 6	43
FD7	Frame buffer data input/output line 7	41
INCLK	Main timing clock input	65
DOTCLK	DOT clock output to video circuit	3
VIDEOA	Video A output	33
VIDEOB	Video B output	34
VIDEOC	Video C output	36
VIDEOD	Video D output	37
TEST	Test pin input	66
SHFTEN	Shift enable output	5
$\overline{\text{BL2IRQ}}$	BLINK2 interrupt output	38
$\overline{\text{IRQCLR}}$	BLINK2 interrupt clear input	39

Operation

Basic operating clock

Output signals from MIVAC define INCLK which inputs to MIVAC as a basic operating clock, and input signals to MIVAC define 2CLK which is output from MIVAC as well. 2CLK, the basic operating clock of ACRTC which is output from MIVAC, is generated from INCLK. In order to save the memory access time, 2CLK is configurated unsymmetrically between the first half and the latter half of cycle times as shown below.

Frame buffer control

MIVAC uses the DRAM of the static column mode as a memory for the frame buffer, and reduces the number of memory used for the frame buffer by accessing the memory several times per memory cycles. Using one, two, and four DRAMs respectively, MIVAC can deal with various kinds of applications. Figure 2 shows the connection of MIVAC to the DRAM.

To control these DRAMs, MIVAC generates $\overline{RAS}$, $\overline{CS}$, $\overline{OE}$ and $\overline{WE}$. And it outputs the row and the column address as the ones for DRAM, adapting to the timing of $\overline{RAS}$ and $\overline{CS}$.

The Drawing Read cycle is shown in figure 3, the Drawing Write cycle in figure 4, the Display Read cycle in figure 5 and 6, and $\overline{CS}$ before $\overline{RAS}$ Refresh cycle in figure 7 respectively.

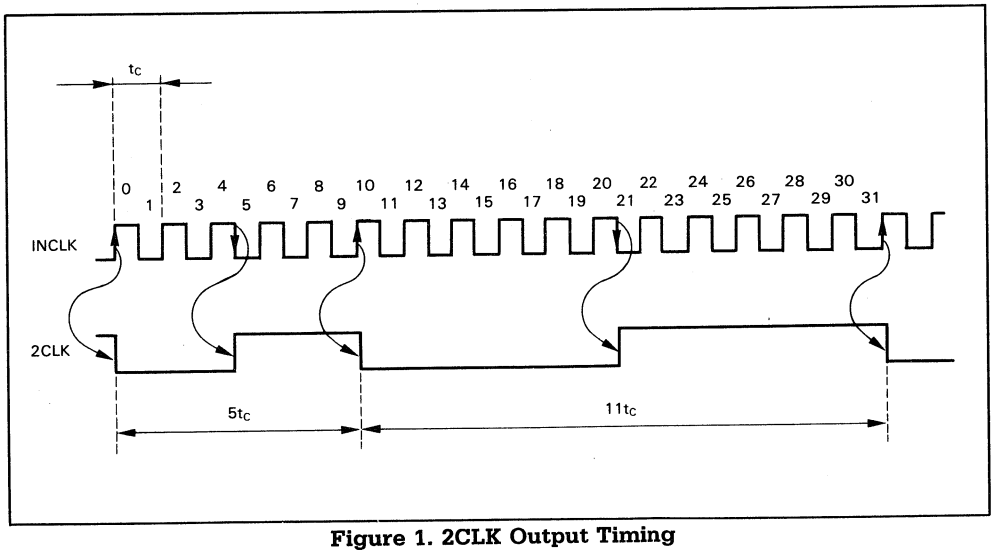


Figure 1. 2CLK Output Timing

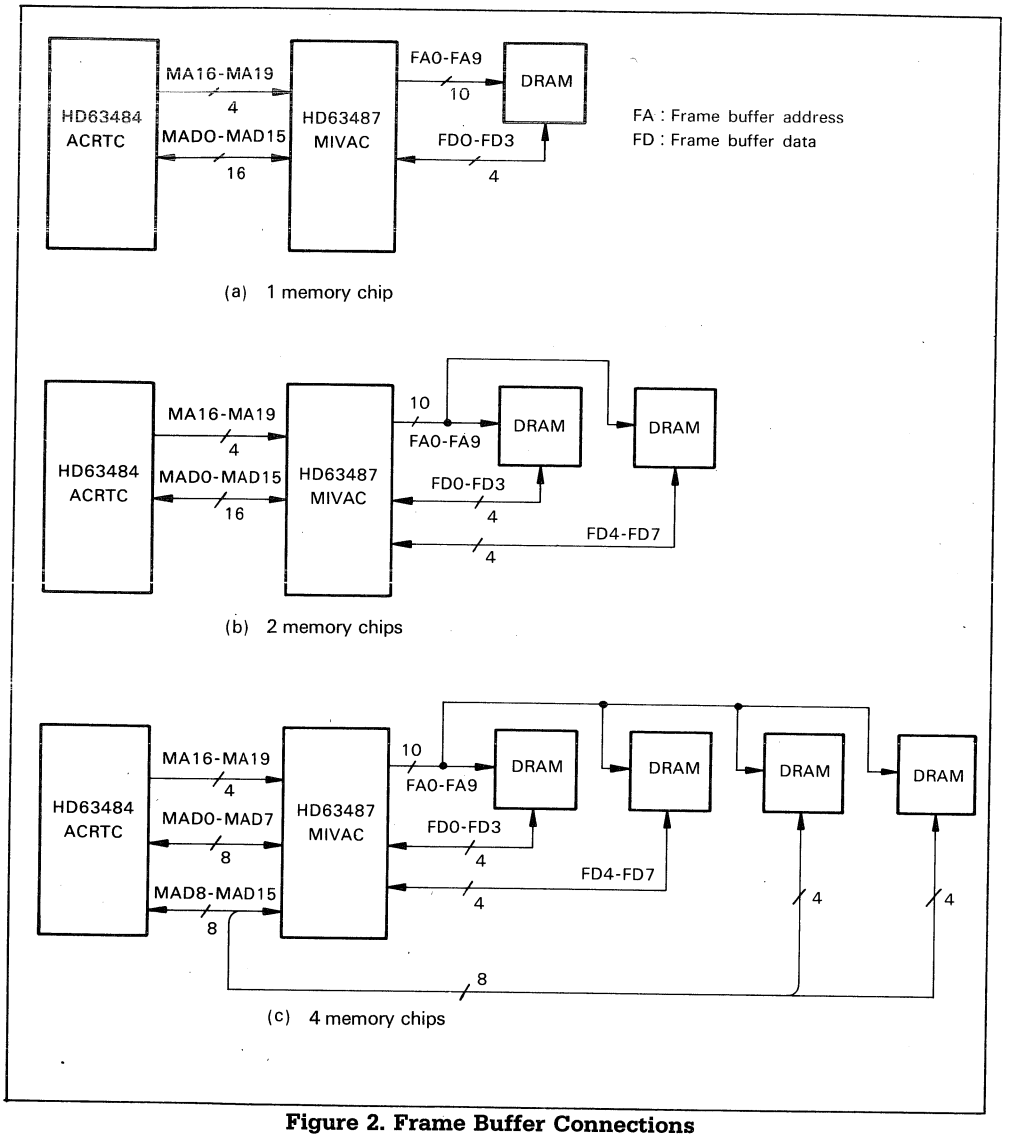


Figure 2. Frame Buffer Connections

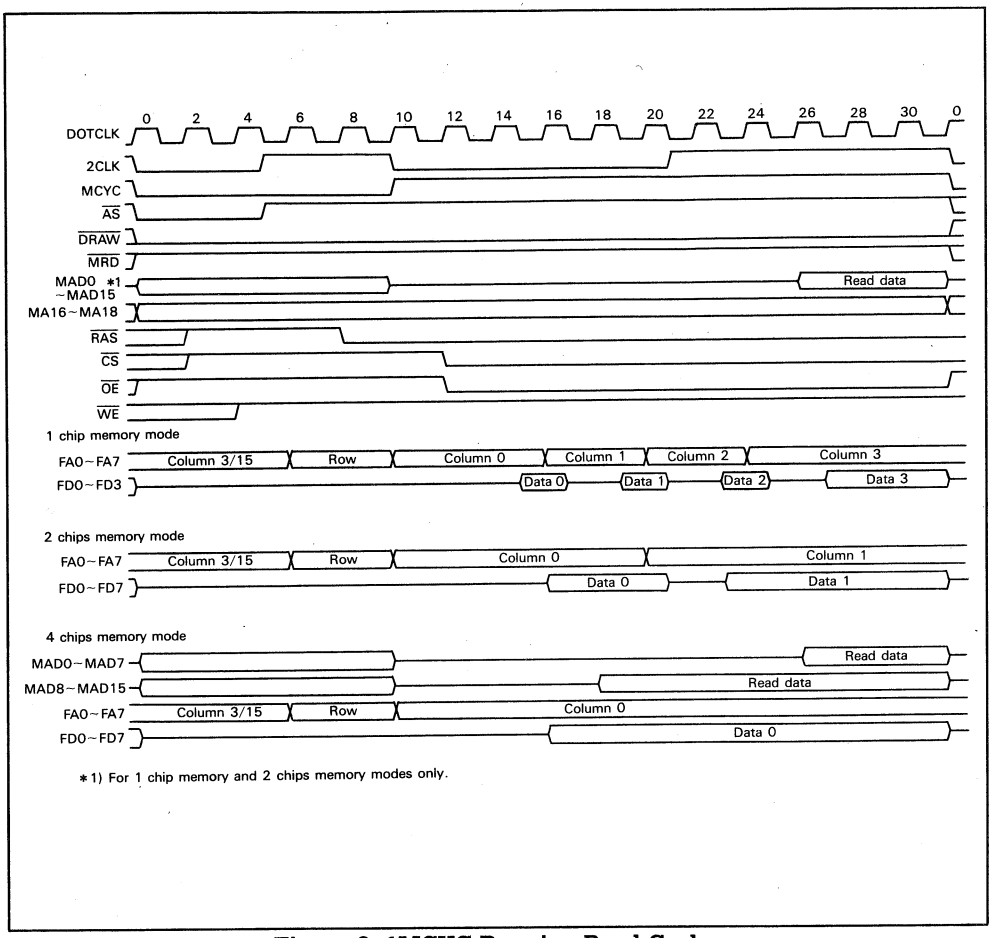


Figure 3. 1MCYC Drawing Read Cycle

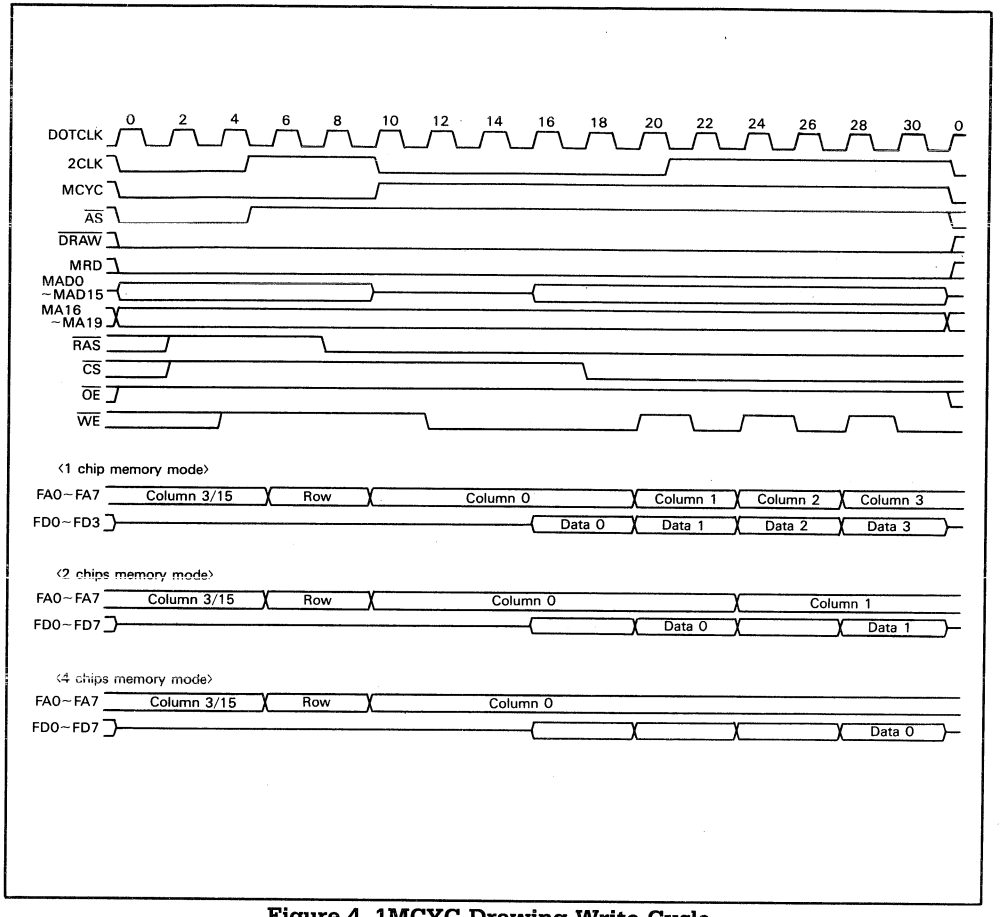


Figure 4. 1MCYC Drawing Write Cycle

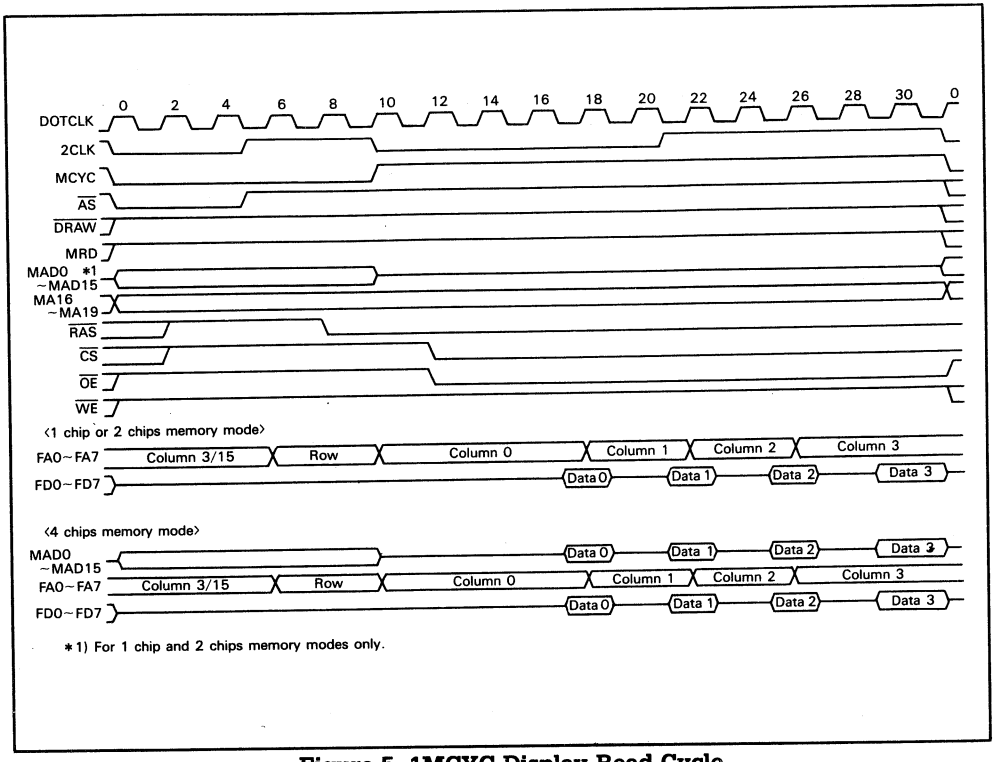


Figure 5. 1MCYC Display Read Cycle

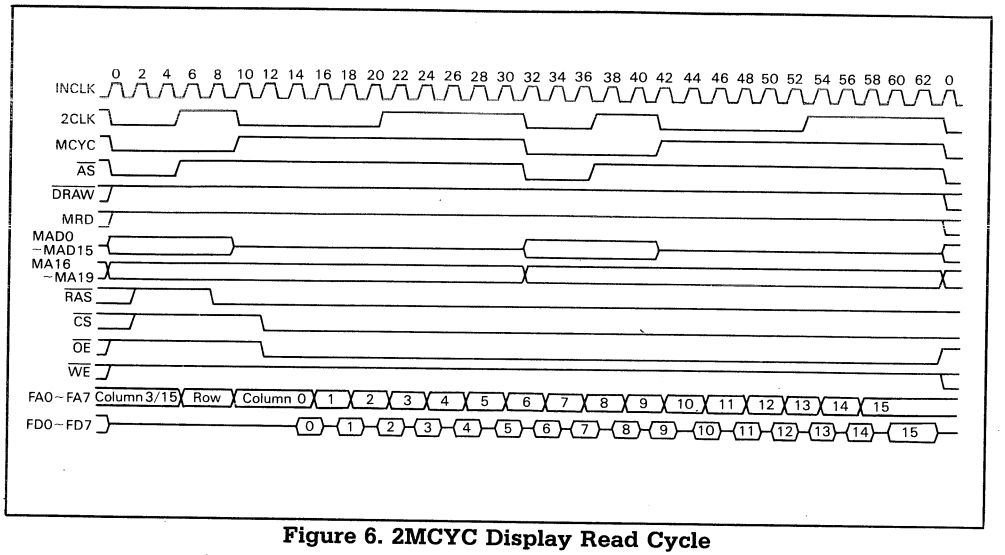


Figure 6. 2MCYC Display Read Cycle

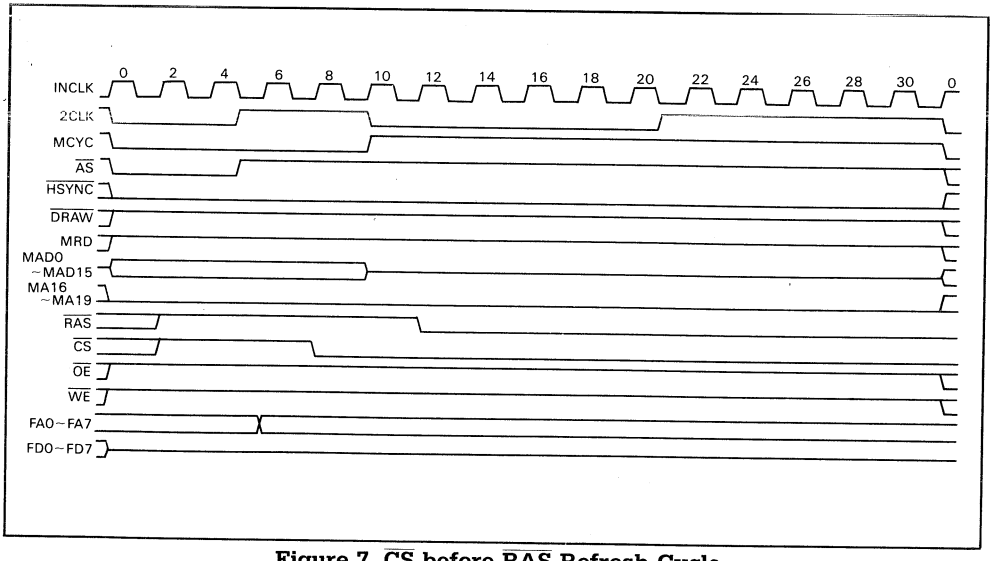


Figure 7. $\overline{CS}$ before $\overline{RAS}$ Refresh Cycle

Data Transfer

The MIVAC contain control circuits for bidirectional transfer between the ACRTC and frame buffers. To transfer data, the MIVAC receive the ACRTC's memory cycle (MCYC), memory read (MRD), draw ($\overline{DRAW}$) and address strobe ($\overline{AS}$) signals.

The MIVAC recognize a nondisplay cycle when $\overline{DRAW}$ is low. In nondisplay cycles the data transfer direction is determined by the memory read signal (MRD). MRD high signifies a read cycle to transfer data from frame buffers to the ACRTC. MRD low signifies a write cycle to transfer data from the ACRTC to the frame buffers. Timing for the data transfer is determined by the MCYC input. When MCYC is high, frame buffers or the ACRTC three-state output buffers are enabled for transfer.

Drawing Write Cycle: The MIVAC recognize a drawing write cycle when both $\overline{DRAW}$ and MRD are low.

Drawing Read Cycle: The MIVAC recognize a drawing read cycle when $\overline{DRAW}$ is low and MRD is high.

When MCYC is high during this cycle, the MIVAC enable the data buffer (MAD0-MAD15) for the ACRTC and output a word from the frame buffers.

Video signal generation

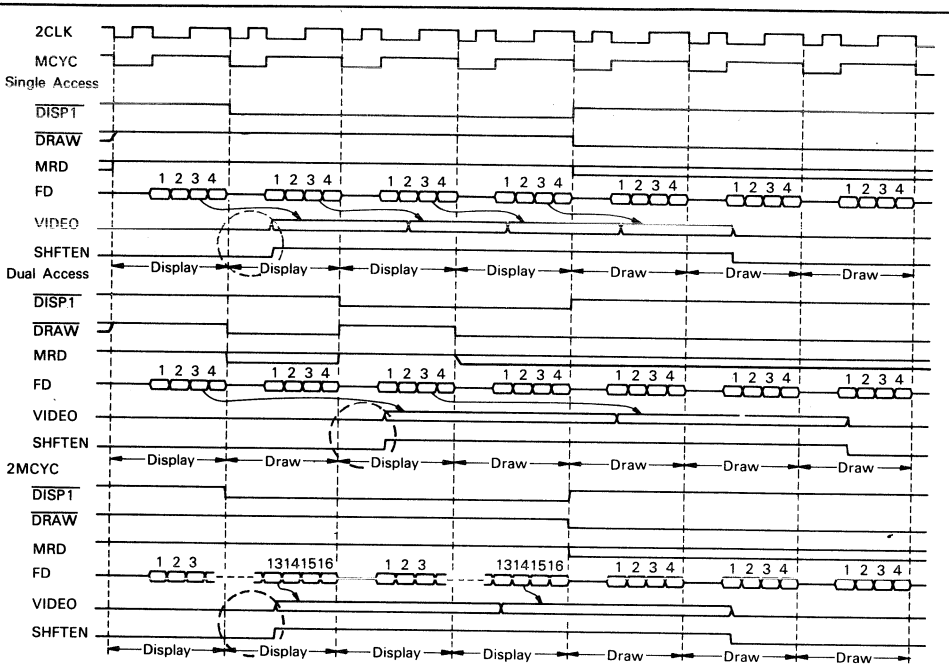
MIVAC converts the parallel display data, which is output from the frame buffer, to serial in the internal shift register, and outputs the display data from VIDEOA-VIDEOD pins after making it simultaneous with DOTCLK. As the pins for VIDEOA-VIDEOD are determined by the graphic bit mode, they must be connected to CRT carefully. Table 1 shows the relation between the mode and the used pins.

Figure 8 shows the relation between the memory access and the video output.

Table 1. Operation Mode and Video Outputs

Mode	Graphic bit mode (bit/pixel)	Display colors (or Gray scale)	VIDEOA	VIDEOB	VIDEOC	VIDEOD
0	1	Monochrome (2)	○	×	×	×
1	2	4 (4)	○	○	×	×
2	4	16 (16)	○	○	○	○
3	2	4 (4)	○	○	×	×
4	4	16 (16)	○	○	○	○
5	4	16 (16)	○	○	○	○
6	1	Monochrome (2)	○	×	×	×
7	2	4(4)	○	○	×	×
8	1	Monochrome (2)	○	×	×	×
9	2	4 (4)	○	○	×	×
A	4	16 (16)	○	○	○	○
B	2	4 (4)	○	○	×	×
C	4	16 (16)	○	○	○	○
D	2	4 (4)	○	○	×	×
E	4	16 (16)	○	○	○	○
F	4	16 (16)	○	○	○	○

○ : Available
× : Not available



Following figure shows the detailed timing of SHFTEN and VIDEO output at sign of ○.

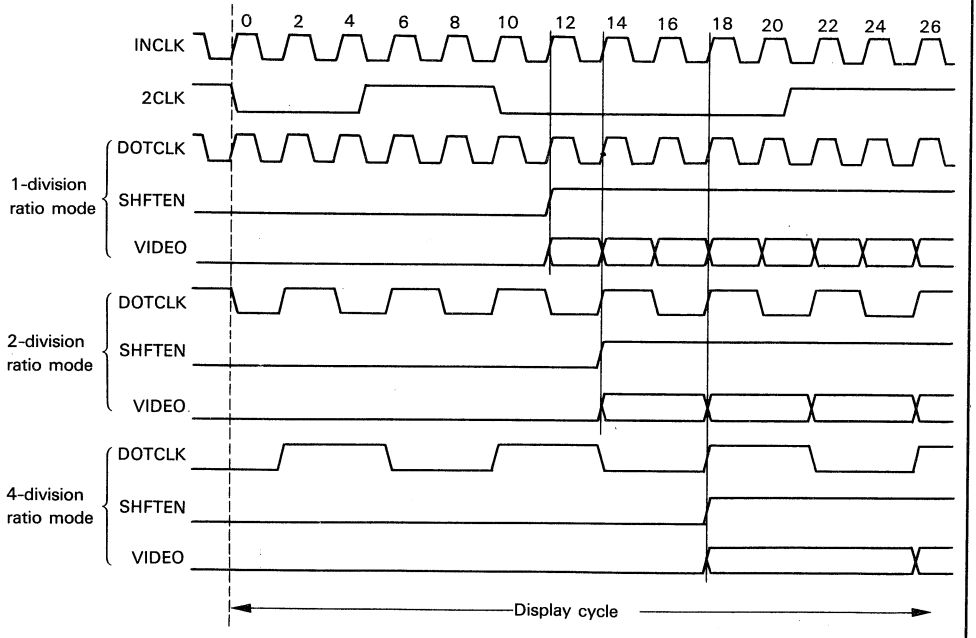


Figure 8. Display Timing (Single Access, Dual Access, 2MCYC)

Attribute Control Codes

The MIVAC sets colors, the number of shift bits, and access mode when it receives attribute codes and blink information from the ACRTC. The ACRTC outputs 20 bits of attribute control codes (MAD0 to MAD15, MA16 and MA19) during the attribute control code output cycle (figure 9). This information includes user-definable codes and blink control codes (figure 10).

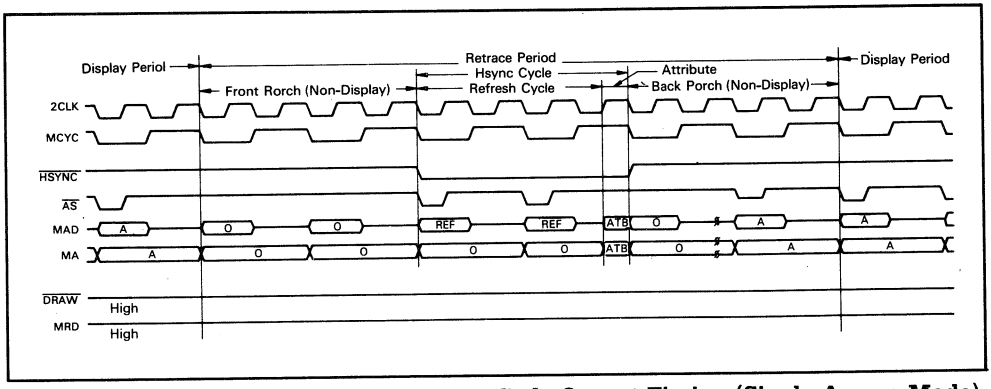


Figure 9. DRAM Refresh and Attribute Code Output Timing (Single Access Mode)

Signal	Attribute Control Codes	
MA19	BLINK2	BL2IRQ output
MA18	BLINK1	Graphic cursor cursor blinking
MA17	SPL2	
MA16	SPL1	
MAD15	HZ3	
⟆	⟆	
MAD12	HZ0	MIVAC does not use
MAD11	HSD3	
⟆	⟆	
MAD8	HSD0	
MAD7	MUXEN	Video multiplex output enable
MAD6	VMD	Frame buffer depth
MAD5	CUR1	Color of graphic cursor
MAD4	CUR0	
MAD3	VCF3	MIVAC operating modes
MAD2	VCF2	Attribute Control Codes
MAD1	VCF1	
MAD0	VCF0	

Figure 10. Attribute Control Codes

VCF0—VCF3 (MAD0—MAD3)

VCF0 to VCF3 (MAD0 to MAD3) define sixteen basic operating modes as shown in the tables 2 and 3.

Table 2. Operating Modes

Mode	ACRTC Attribute Code Setting VCF3	VCF2	VCF1	VCF0	Screen Configuration (Dots × Rasters)	Frame Buffer (Bytes)	ACRTC Operating Frequency (MHz)	Memory Access	Access Mode	Memory Chips	Color Gradation	Shift (Bits)	DOTCLK Division Ratio	DOTCLK Maximum Frequency (MHz)
0	0	0	0	0	640×200, 350, 400, 480	512k/128k	4.13	480 ns/ 4 times	Single access mode	1	B&W	16	1	33
1	0	0	0	1	640×200, 480×240, 320×200, 240						4	8	2	16.5
2	0	0	1	0	320×200, 240 256×192						16	4	4	8.25
3	0	0	1	1	640×200, 350, 400, 480	1M/256k				2	4	16	1	33
4	0	1	0	0	640×200, 480×240, 320×200, 240						16	8	2	16.5
5	0	1	0	1	640×200, 350, 400, 480	2M/512k				4		16	1	33
6	0	1	1	0	640×200, 480×240, 320×200, 240	512k/128k			Dual access mode 0	1	B&W		2	16.5
7	0	1	1	1	320×200, 240 256×192						4	8	4	8.25
8	1	0	0	0	640×200, 350, 400, 480	1M/256k				2	B&W	32	1	33
9	1	0	0	1	640×200, 480×240, 320×200, 240						4	16	2	16.5
A	1	0	1	0	320×200, 240 256×192						16	8	4	8.25
B	1	0	1	1	640×200, 350, 400, 480	2M/512k				4	4	32	1	33
C	1	1	0	0	640×200, 480×240, 320×200, 240						16	16	2	16.5
D	1	1	0	1	640×200, 350, 400, 480	512k/128k		960 ns/ 16 times	Single access mode	1	4	32	1	33
E	1	1	1	0	640×200, 480×240, 320×200, 240						16	16	2	16.5
F	1	1	1	1	640×200, 350, 400, 480	1M/256k				2		32	1	33

Table 3. Dot Clock Frequency Range

Mode	Frequency
0, 3, 5, 8, B, D, F	33—11 MHz
1, 4, 6, 9, C, E	16.5—5.5 MHz
2, 7, A	8.25—2.75 MHz

MCYC Fetch: The MCYC fetch defines the number of cycles.

1: One, two, or four memories
2: One or two memories

Access Mode: The MIVAC supports single- and dual-access 0 modes.

1: Single access/dual access 0
2: Single access

Memory Chips: The MIVAC can connect one, two, or four memory chips.

1 chip : connect FD0 to FD3 to data bus
2 chips: connect FD0 to FD8 to data bus
3 chips: connect FD0 to FD7 to low-order 8 bits, and MAD8 to MAD15 to high-order 8 bits of data bus.

Bit/Pixel: The MIVAC can display:

- 1 bit/pixel (B&W)
- 2 bits/pixel (4 colors)
- 4 bits/pixel (16 colors)

Dot Shift: The MIVAC can shift by 4, 8, 16, or 32 dots.

DOTCLK Division: The MIVAC can divide the INCLK frequency by 1, 2, or 4 depending on the number of shifted dots and access modes.

CUR0 and CUR1 (MAD4 and MAD5)

CUR0 and CUR1 set the cursor color (table 4).

VMD0 (MAD6)

VMD0 selects memory chips (table 5).

MUXEN (MAD7)

MUXEN selects the multiplex video output. Multiplexing is defined by MUXEN and VSYNC/2 (table 6). VSYNC/2 is obtained by dividing $\overline{\text{VSYNC}}$ from the ACRTC by 2.

Note: VIDEOD is not multiplexed.

BLINK1 (MA18)

BLINK1 defines the blinking of cursor (table 7).

BLINK2 (MA19)

BLINK2 controls $\overline{\text{BL2IRQ}}$ output. When BLINK2 is 1, $\overline{\text{BL2IRQ}}$ is asserted (low).

Table 4. Cursor Color

CUR1	CUR0	Cursor Color
0	0	Black (VIDEOA to VIDEOD = 0)
0	1	White (VIDEOA to VIDEOD = 1)
1	0	Color specified by each bit (VIDEOA to VIDEOD) is inverted
1	1	Color specified by each bit (VIDEOA to VIDEOC) is inverted. (VIDEOD is not changed.)

Table 5. Memory Chips

VMD	Memory chips
0	256k words × 4 bit DRAM
1	1M words × 4 bit DRAMs

Table 6. Video Multiplex

MUXEN	VSYNC/2	VIDEOA	VIDEOB
0	0	A	B
	1	A	B
1	0	A	B
	1	C	D

Table 7. Cursor Blink

BLINK1	Cursor
0	No blinking
1	Blinking

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC} (Note)	−0.3 to +7.0	V
Input Voltage	V_{in} (Note)	−0.3 to V_{CC}+0.3	V
Output Voltage	V_{out} (Note)	5.5	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Note: This value is in reference to V_{SS} = 0 V.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} (Note)	4.75	5.00	5.25	V
Input "Low" Level Voltage	V_{IL} (Note)	0	—	0.7	V
Input "High" Level Voltage	V_{IH} (Note)	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

Note: This value is in reference to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics

(V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C unless otherwise noted.)

Item		Symbol	Min	Max	Unit	Test Condition
Input "High" Level Voltage	All Inputs	V_{IH}	2.2	V_{CC}	V	
Input "Low" Level Voltage	All Inputs	V_{IL}	−0.3	0.7	V	
Input Clamp Voltage	All Inputs	V_I	—	−1.5	V	V_{CC} = 4.75 V I_{IN} = 18 mA
Output "High" Level Voltage	All Outputs	V_{OH}	2.7	—	V	V_{CC} = 4.75 V I_{OH} = −400 μA
Output "Low" Level Voltage	All Outputs	V_{OL}	—	0.5	V	V_{CC} = 4.75 V I_{OL} = 8 mA
"High" Level Input Current	All Inputs	I_{IH}	—	20	μA	V_{CC} = 5.25 V V_I = 2.7 V
"Low" Level Input Current	All Inputs	I_{IL}	—	−400	μA	V_{CC} = 5.25 V V_I = 0.4 V
Short Circuit Output Current	All Outputs	I_{OS}	−40	−120	mA	V_{CC} = 5.25 V
Supply Current		I_{CC}	—	120	mA	V_{CC} = 5.25 V

AC Characteristics

(V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C unless otherwise noted.)

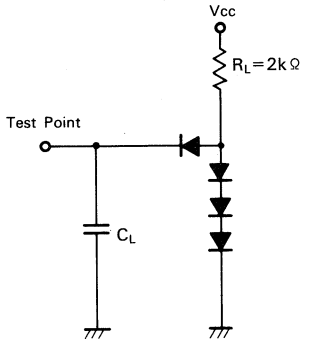
No.	Item	Symbol	Reference Figure#	Min	Max	Unit
1	INCLK Cycle Time	t_C	11	30	—	ns
2	INCLK High Level Pulse Width	t_{WH}	11	12	—	ns
3	INCLK Low Level Pulse Width	t_{LW}	11	12	—	ns
4	INCLK Rise Time	t_R	11	—	5	ns
5	INCLK Fall Time	t_F	11	—	5	ns
6	2CLK Delay Time	t_{2CLKD}	11	—	15	ns
7	MCYC Setup Time	t_{MCYCS}	11	10	—	ns
8	MCYC Hold Time	t_{MCYCH}	11	0	—	ns
9	$\overline{\text{HSYNC}}$ Setup Time	t_{HSS}	11	15	—	ns
10	$\overline{\text{HSYNC}}$ Hold Time	t_{HSH}	11	0	—	ns
11	$\overline{\text{DISP1}}$ Setup Time	t_{DISPS}	11	20	—	ns
12	MRD Setup Time	t_{MRDS}	11	15	—	ns
13	MRD hold Time	t_{MRDH}	11	5	—	ns
14	$\overline{\text{DRAW}}$ Setup Time	t_{DRAWS}	11	15	—	ns
15	$\overline{\text{DRAW}}$ Hold Time	t_{DRAWH}	11	5	—	ns
16	$\overline{\text{AS}}$ Setup Time	t_{ASS}	11	20	—	ns
17	$\overline{\text{AS}}$ Pulse Width	t_{ASW}	11	25	—	ns
18	Memory Address Setup Time	t_{AS}	11	25	—	ns
19	Memory Address Hold Time	t_{AH}	11	0	—	ns
20	$\overline{\text{CUD1}}$ Setup Time	t_{CUDS}	11	5	—	ns
21	$\overline{\text{VSYNC}}$ Setup Time	t_{VSS1}	17	5	—	ns
22	Attribute Code Delay Time	t_{ACS}	20	—	100	ns
23	Attribute Code Hold Time	t_{ASH}	20	5	—	ns
24	$\overline{\text{RAS}}$ Delay Time	t_{RSD}	11	—	15	ns
25	$\overline{\text{RAS}}$ Precharge Time	t_{RSP}	11	3tc-10	—	ns
26	$\overline{\text{CS}}$ Delay Time 1	t_{CSDL}	11	—	15	ns
27	$\overline{\text{OE}}$ Delay Time 1	t_{OED1}	11	—	15	ns
28	2CLK Delay Time from $\overline{\text{OE}}$	t_{2CKD}	11	0	10	ns
29	Valid MAD0-MA19 to Valid Low Address Delay Time	t_{RAD}	11	—	25	ns
30	Column Address Delay Time	t_{CAD}	11	5	25	ns
31	FD Setup Time	t_{FDS}	11	8	—	ns
32	FD Hold Time 1	t_{FDH1}	11	5	—	ns
33	FD Hold Time 2	t_{FDH2}	11	2	—	ns
34	Valid FD to Valid MAD Delay	t_{MADV}	11	—	10	ns
35	Read Data Turn on Time	t_{RDTV}	11	0	—	ns
36	Read Data Hold Time	t_{RDH}	11	3	—	ns

AC Characteristics (cont)

(V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C unless otherwise noted.)

No.	Item	Symbol	Reference Figure#	Min	Max	Unit
37	$\overline{WE}$ Delay Time	t_{WED}	14	—	25	ns
38	$\overline{WE}$ Low Pulse Width	t_{WLW}	14	tc-15	—	ns
39	$\overline{WE}$ High Pulse Width	t_{WHW}	14	tc-15	—	ns
40	$\overline{CE}$ low to $\overline{WE}$ Pulse Width	t_{CWEW}	14	tc-15	—	ns
41	Draw Write Data Setup Time	t_{WDS}	14	15	—	ns
42	FD Delay Time 1	t_{FDD1}	14	—	20	ns
43	FD Delay Time 2	t_{FDD2}	14	—	20	ns
44	$\overline{WE}$/$\overline{CS}$ Low to FD Hold Time	t_{WFDHW}	14	tc-10	—	ns
45	$\overline{WE}$/$\overline{CS}$ Low to Address Hold	t_{WAHW}	14	tc-5	—	ns
46	FD Hold Time	t_{FDHW}	14	0	—	ns
47	FD Turn Off Time	t_{FDTI}	14	—	50	ns
48	VSYNC/2 Delay Time	t_{VS2D}	11	—	25	ns
49	DOTCLK Delay Time	t_{DCD}	11	—	15	ns
50	VIDEO Delay Time	t_{VD}	11	−5	5	ns
51	$\overline{BL2IRQ}$ Delay Time	t_{IRQD}	20	—	10	ns
52	IRQCLR to$\overline{BL2IRQ}$ Clear Delay Time	t_{IRQCD}	20	—	20	ns
53	SHFTEN Delay Time	t_{SFTEND}	11	−5	5	ns

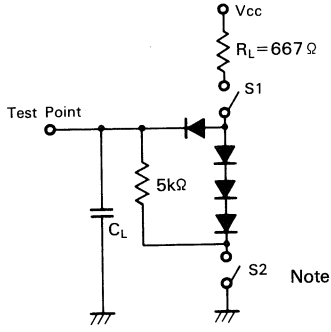
Test Circuit



Note: All diodes are 1S2074Ⓗ's or the equivalent.

Signal	C_L (pF)
2CLK	40
DOTCK	
VSYNC/2	
$\overline{RAS}$	
$\overline{CS}$	
$\overline{WE}$	
$\overline{OE}$	
FA0-FA9	
VIDEOA-VIDEOD	
SHFTEN	
$\overline{BL2IRQ}$	

(a) Totem Pole Output



Note: All diodes are 1S2074Ⓗ's or the equivalent.

Signal	C_L (pF)
MAD0-MAD15	40
FD0-FD7	

(b) Three State Output

Reference

Display Data Fetch	Memory Chip	Cycle Mode	Figure No.
4 Fetch/1 MCYC	1 Chip	Drawing Read Cycle	11
		Drawing Write Cycle	14
		Display Cycle	17
		Refresh & Attribute Cycle	20
	2 Chips	Drawing Read Cycle	12
		Drawing Write Cycle	15
		Display Cycle	17
		Refresh & Attribute Cycle	20
	4 Chips	Drawing Read Cycle	13
		Drawing Write Cycle	16
		Display Cycle	18
		Refresh & Attribute Cycle	20
16 Fetch/2 MCYC	1 Chips	Drawing Read Cycle	11
		Drawing Write Cycle	14
		Display Cycle	19
		Refresh & Attribute Cycle	20
	2 Chips	Drawing Read Cycle	12
		Drawing Write Cycle	15
		Display Cycle	19
		Refresh & Attribute Cycle	20

Timing Chart

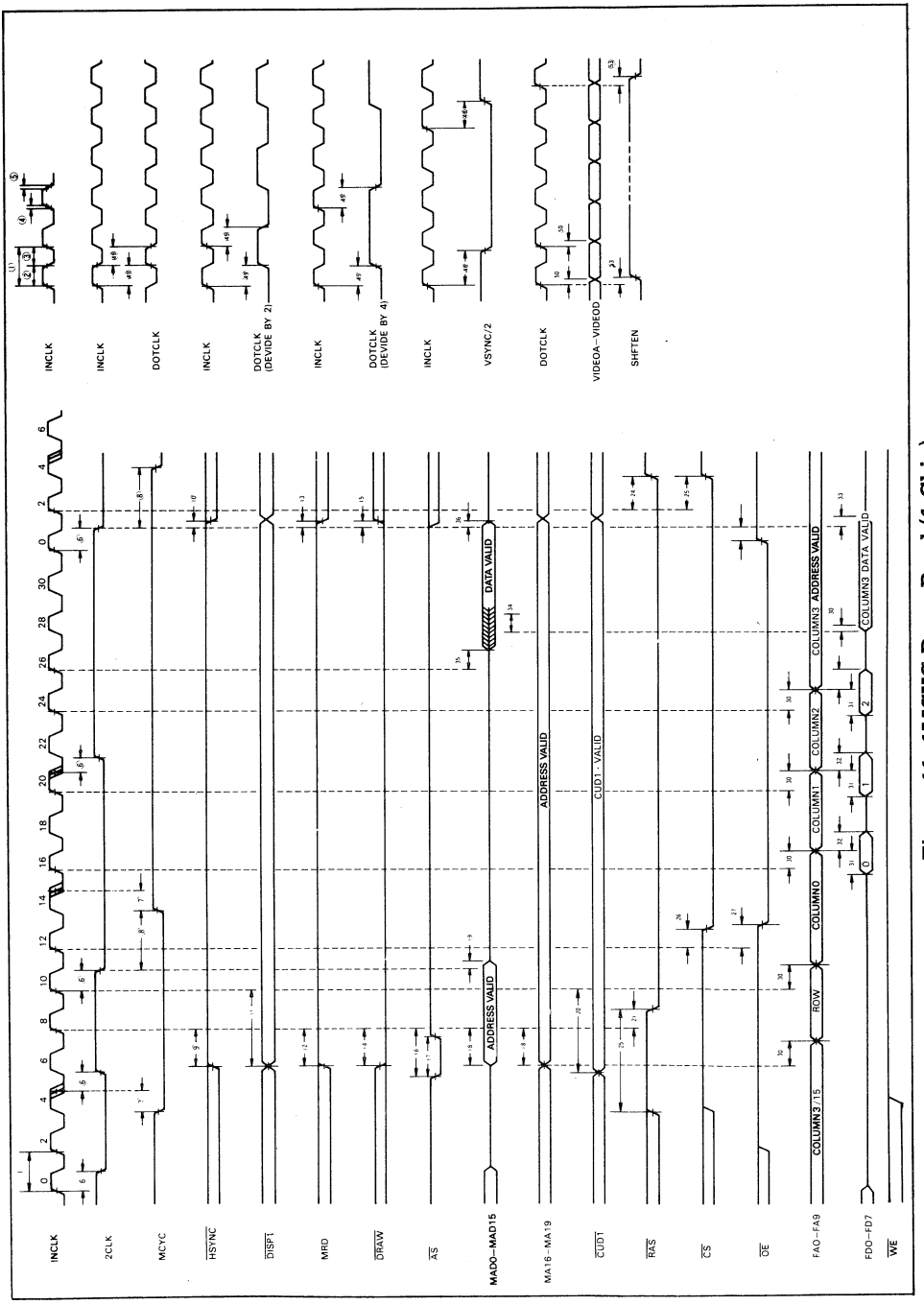


Figure 11. 1MCYC Draw Read (1 Chip)

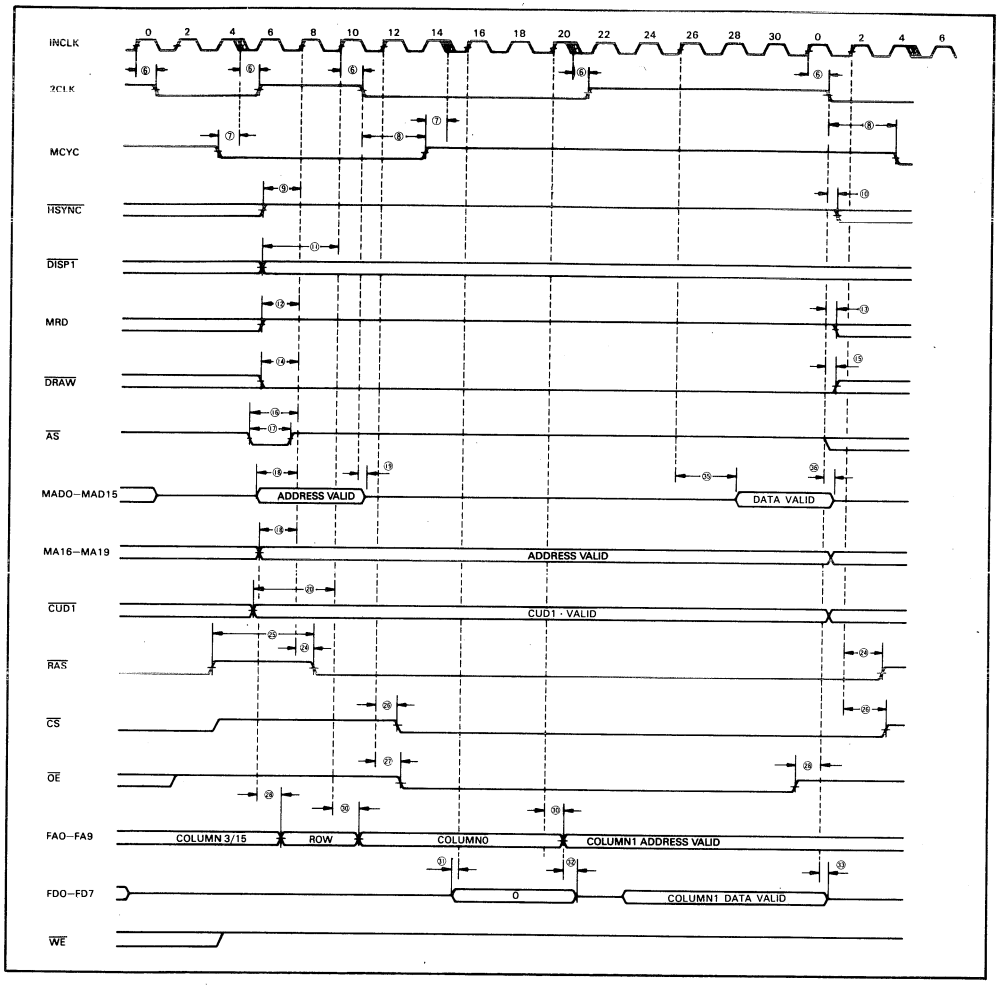


Figure 12. 1MCYC Draw Read (2 Chip)

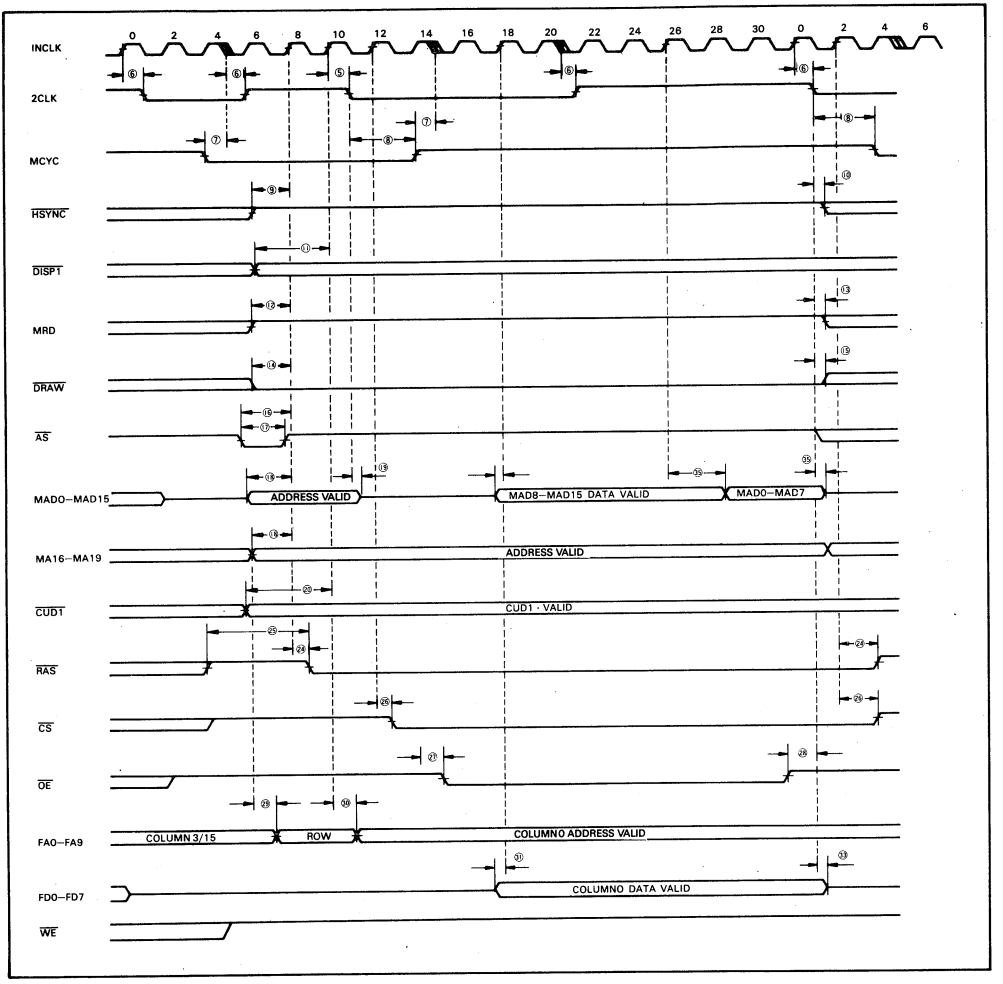


Figure 13. 1MCYC Draw Read (4 Chip)

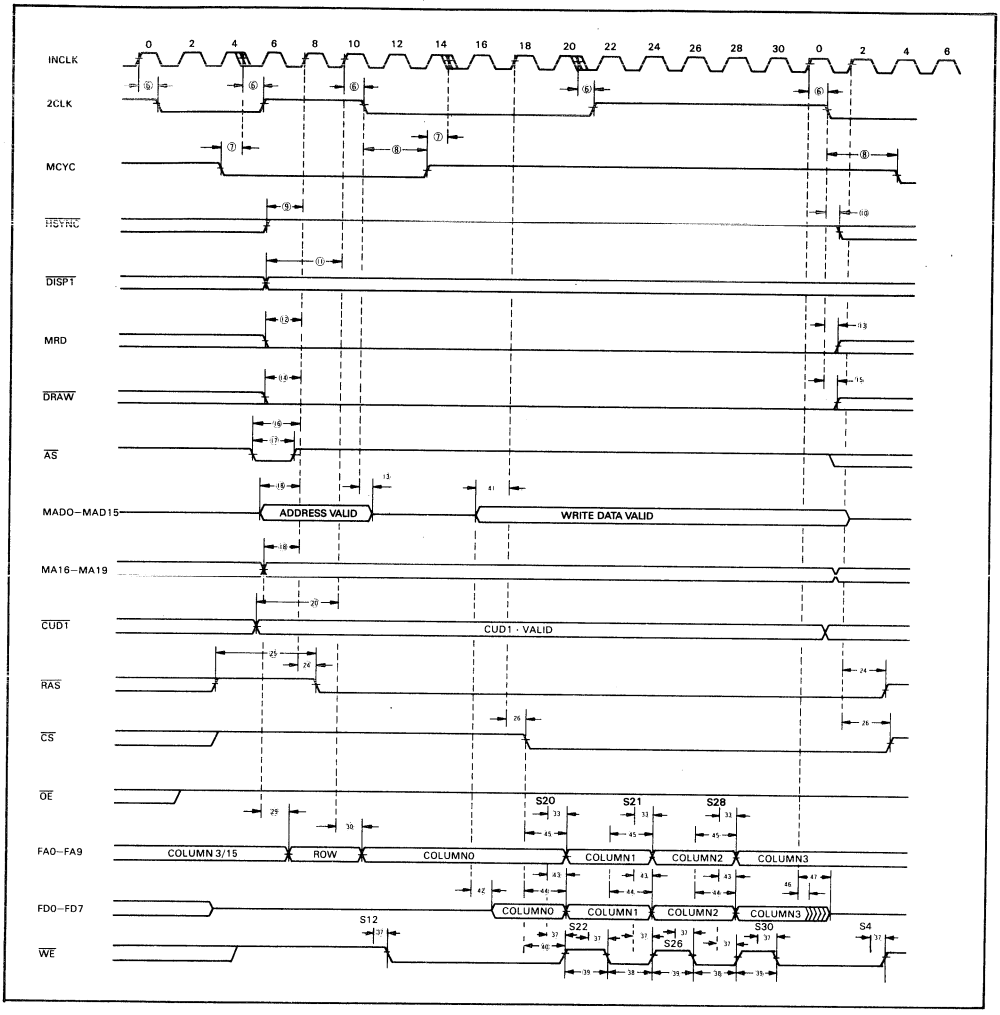


Figure 14. 1MCYC Draw Write (1 Chip)

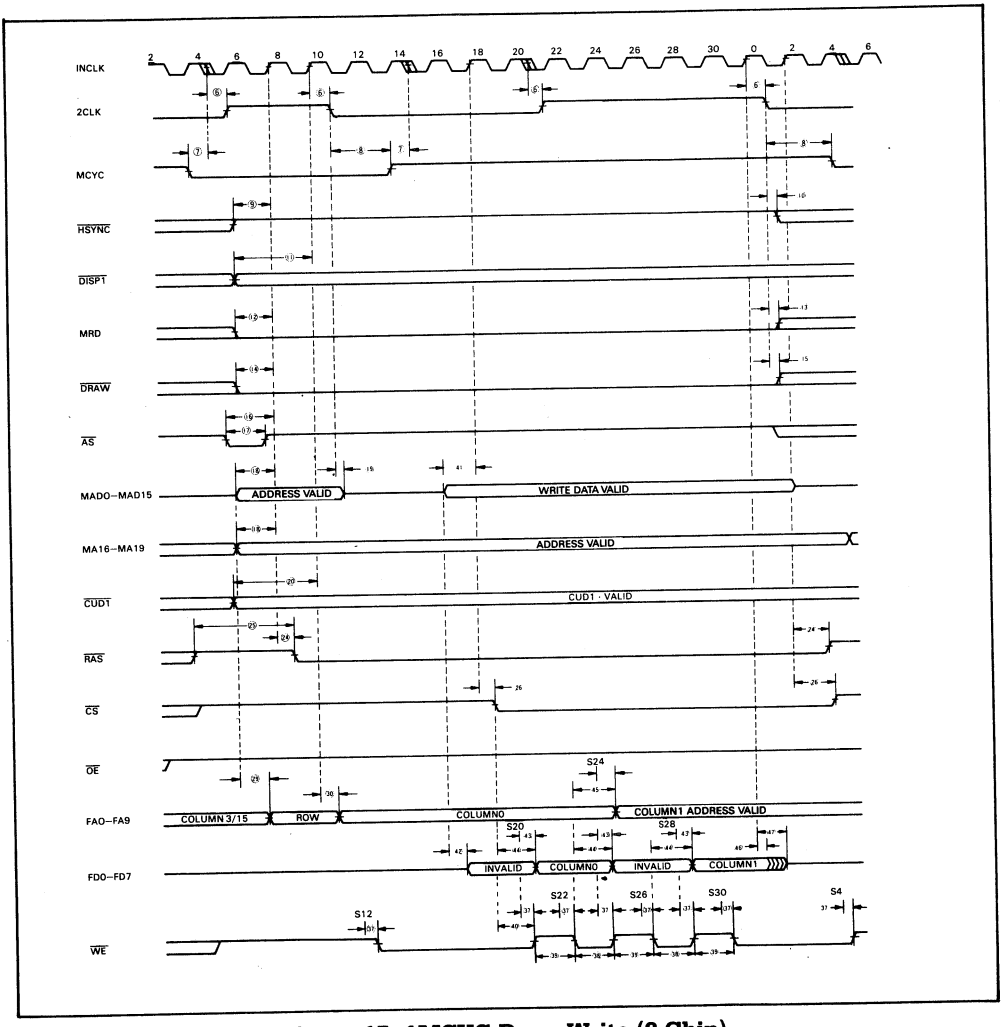


Figure 15. 1MCYC Draw Write (2 Chip)

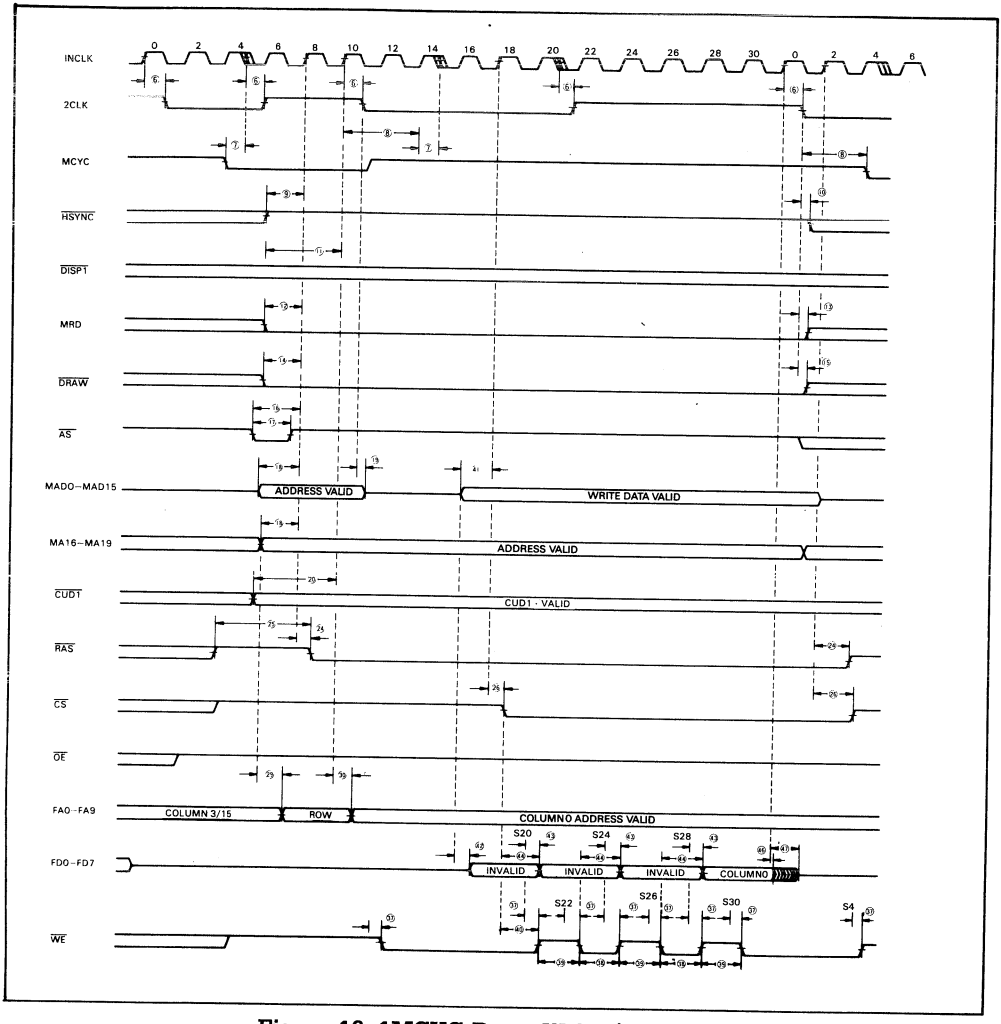


Figure 16. 1MCYC Draw Write (4 Chip)

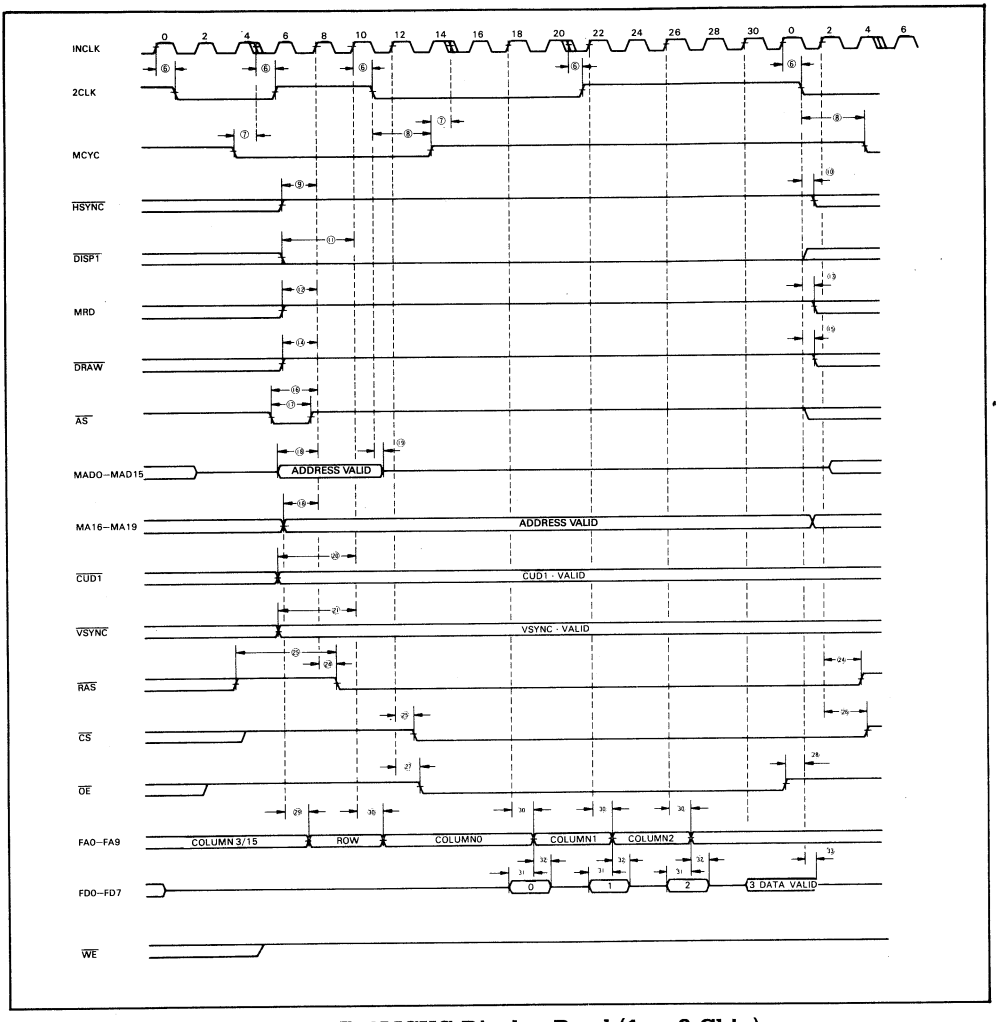


Figure 17. 1MCYC Display Read (1 or 2 Chip)

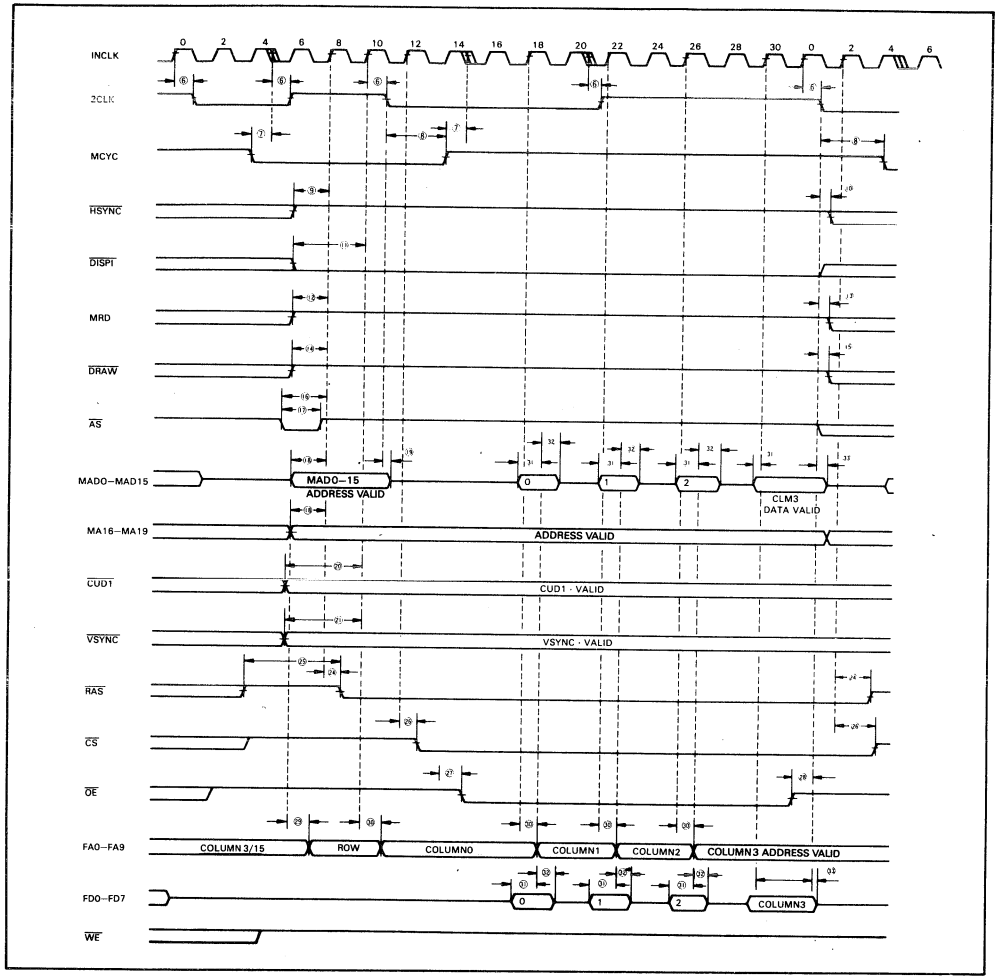


Figure 18. 1MCYC Display Read (4 Chip)

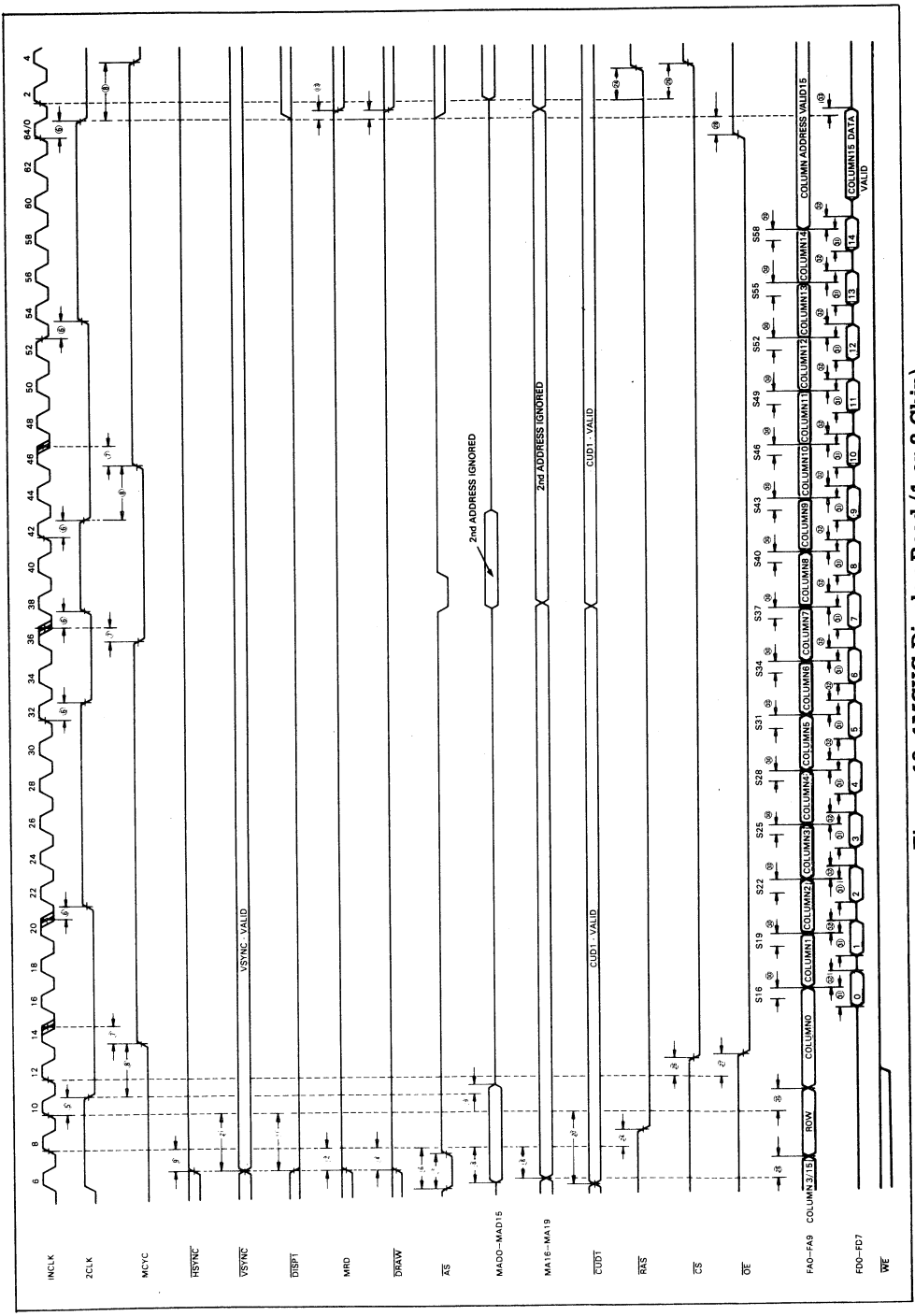


Figure 19. 1MCYC Display Read (1 or 2 Chip)

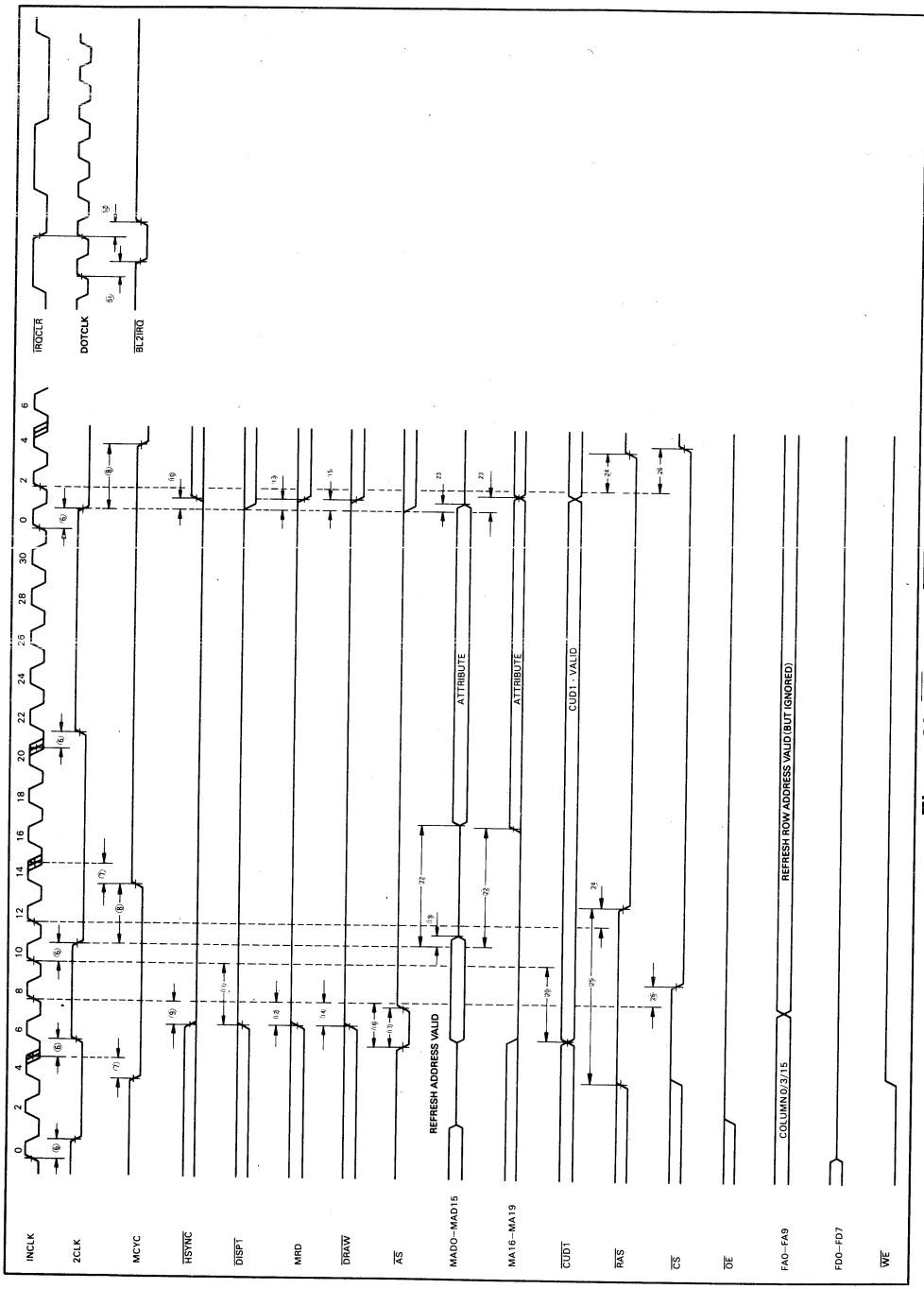


Figure 20. CS before RAS Refresh

Refer to application note (No. ADE-507-001) for detail of this product.

HD63645/HD64645

LCD Timing Controller (LCTC)

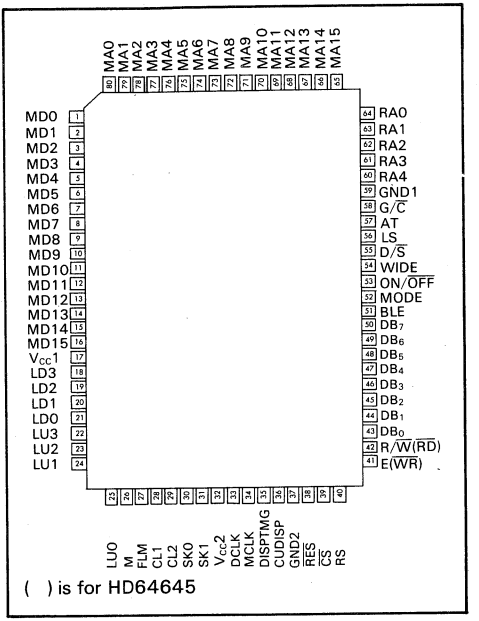
Description

The HD63645/HD64645 LCTC is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Pin Arrangement



Features

- Software compatible with the HD6845 CRTC
- Programmable screen size:
  —Up to 1024 dots (height)
  —Up to 4096 dots (width)
- High-speed data transfer:
  —Up to 20 Mbits/sec in character mode
  —Up to 40 Mbits/sec in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font:
  —1-32 dots (height)
  —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical smooth scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver: HD61104 (column) and HD61105 (common), HD66106 and HD66107T (column/common)
- CPU interface: 68 family (HD63645), 80 family (HD64645, HD64646)
- CMOS process
- Single +5 V ±10%
- 80-pin plastic QFP (FP-80)

Ordering Information

Type No.	Bus Timing	Bus Interface	Package
HD63645	2 MHz	68 System	80-pin Plastic QFP (FP-80)
HD64645	4 MHz	80 System	80-pin Plastic QFP (FP-80)
HD64646	4 MHz	80 System	80-pin Plastic QFP (FP-80B)

Note: See HD64646 data sheet in this data book.

Pin Description

Symbol	Pin Number	Name	I/O
$V_{CC}1$, $V_{CC}2$	17, 32	V_{CC}	—
GND1, GND2	37, 59	Ground	—
LU0-LU3	22-25	LCD Up Panel Data 0-3	O
LD0-LD3	18-21	LCD Down Panel Data 0-3	O
CL1	28	Clock One	O
CL2	29	Clock Two	O
FLM	27	First Line Marker	O
M	26	M	O
MA0-MA15	65-80	Memory Address 0-15	O
RA0-RA4	60-64	Raster Address 0-4	O
MD0-MD7	1-8	Memory Data 0-7	I
MD8-MD15	9-16	Memory Data 8-15	I
DB_0-DB_7	43-50	Data Bus 0-7	I/O
$\overline{CS}$	39	Chip Select	I
E	41	Enable (HD63645 Only)	I
R/$\overline{W}$	42	Read/Write (HD63645 Only)	I
$\overline{WR}$	41	Write (HD64645 Only)	I
$\overline{RD}$	42	Read (HD64645 Only)	I
RS	40	Register Select	I
$\overline{RES}$	38	Reset	I
DCLK	33	D Clock	I
MCLK	34	M Clock	O
DISPTMG	35	Display Timing	O
CUDISP	36	Cursor Display	O
SK0	30	Skew 0	I
SK1	31	Skew 1	I
ON/$\overline{OFF}$	53	On/Off	I
BLE	51	Blink Enable	I
AT	57	Attribute	I
G/$\overline{C}$	58	Graphic/Character	I
WIDE	54	Wide	I
LS	56	Large Screen	I
D/$\overline{S}$	55	Dual/Single	I
MODE	52	Mode	I

Pin Functions

Power Supply ($V_{CC}1$, 2, GND)

Power Supply Pin (+5 V): Connect $V_{CC}1$ and $V_{CC}2$ with +5 V power supply circuit.

Ground Pin (0 V): Connect GND1 and GND2 with 0 V.

LCD Interface

LCD Up Panel Data (LU0-LU3), LCD Down Panel Data (LD0-LD3): LU0-LU3 and LD0-LD3 output LCD data as shown in table 1.

Clock One (CL1): CL1 supplies timing clocks for display data latch.

Clock Two (CL2): CL2 supplies timing clock for display data shift.

First Line Marker (FLM): FLM supplies first line marker.

M (M): M converts liquid crystal drive output to AC.

Memory Interface

Memory Address (MA0-MA15): MA0-MA15 supply the display memory address.

Raster Address (RA0-RA4): RA0-RA4 supply the raster address.

Memory Data (MD0-MD7): MD0-MD7 receive the character dot data and bit-mapped data.

Memory Data (MD8-MD15): MD8-MD15 receive attribute code data and bit-mapped data.

MPU Interface

Data Bus (DB0-DB7): DB0-DB7 send/receive data as a three-state I/O common bus.

Chip Select ($\overline{CS}$): $\overline{CS}$ selects a chip. Low level enables MPU read/write of the LCTC internal registers.

Enable (E): E receives an enable clock. (HD63645F only).

Read/Write (R/$\overline{W}$): R/$\overline{W}$ enables MPU read of the LCTC internal registers when R/$\overline{W}$ is high, and MPU write when low. (HD63634F only).

Write ($\overline{WR}$): $\overline{WR}$ receives MPU write signal. (HD64645F Only)

Read ($\overline{RD}$): $\overline{RD}$ receives MPU read signal. (HD64645F Only)

Register Select (RS): RS selects registers. (Refer to table 5.)

Reset ($\overline{RES}$): $\overline{RES}$ performs external reset of the LCTC. Low level of $\overline{RES}$ stops and zero-clears the LCTC internal counter. No register contents are affected.

Timing Signal

D Clock (DCLK): DCLK inputs the system clock.

M Clock (MCLK): MCLK indicates memory cycle; DCLK is divided by four.

Display Timing (DISPTMG): DISPTMG high indicates that the LCTC is reading display data.

Cursor Display (CUDISP): CUDISP supplies cursor display timing; connect with MD12 in character mode.

Skew 0 (SK0)/Skew 1 (SK1): SK0 and SK1 control skew timing. Refer to table 2.

Mode Select

The mode select pins ON/$\overline{OFF}$, BLE, AT, G/$\overline{C}$,

Table 1. LCD Up Panel Data and LCD Down Panel Data

	Single Screen		
Pin name	**4-Bit Data**	**8-Bit Data**	**Dual Screen**
LU0-LU3	Data output	Data output	Data output for upper screen
LD0-LD3	Disconnected	Data output	Data output for lower screen

and WIDE are ORed with the mode register (R22) to determine the mode.

On/Off (ON/$\overline{OFF}$): ON/$\overline{OFF}$ switches display on and off. (High = display on).

Blink Enable (BLE): BLE high level enables attribute code "blinking" (MD13) and provides normal/blank blinking of specified characters for 32 frames each.

Attribute (AT): AT controls character attribute functions.

Graphic/Character (G/$\overline{C}$): G/$\overline{C}$ switches between graphic and character display mode (graphic display when high).

Wide (WIDE): WIDE switches between normal and wide display mode (high = wide display, low = normal display).

Large Screen (LS): LS controls a large screen. LS high provides a data transfer rate of 40 Mbits/s for a graphic display. Also used to specify 8-bit LCD interface mode. For more details, refer to page 26.

Dual/Single (D/$\overline{S}$): D/$\overline{S}$ switches between single and dual screen display (dual screen display when high).

Mode (MODE): MODE controls easy mode. MODE high sets duty ratio, maximum number of rasters, cursor start/end rasters, etc. (Refer to table 9.)

Table 2. Skew Signals

SK0	SK1	Skew Function
0	0	No skew
1	0	1-character time skew
0	1	2-character time skew
1	1	Inhibited combination

Function Overview

LCD and CRT Display Systems

Figure 1 shows a system using both LCD and CRT displays.

Main Features of HD63645F/HD64645F

Main features of the LCTC are :

- High-resolution liquid crystal display screen control (up to 720 × 512 dots)
- Software compatible with HD6845 (CRTC)
- Built-in character attribute control circuit

Table 3 shows how the LCTC can be used.

Table 3. Functions, Application, and Configuration

Classification	Item	Description
Functions	Screen Format	Programmable horizontal scanning cycle by the character clock period Programmable multiplexing duty ratio from static up to 1/512 Programmable number of displayed characters per character row Programmable number of rasters per character row (number of vertical dots within a character row + space between character rows)
	Cursor Control	Programmable cursor display position, corresponding to RAM address Programmable cursor height by setting display start/end rasters Programmable blink rate, 1/32 or 1/64 frame rate
	Memory Rewriting	Time for rewriting memory set either by specifying number of horizontal total characters or by cycle steal utilizing MCLK
	Memory Addressing	16-bit memory address output, up to 64 kbytes x 2 memory accessible DRAM refresh address output
	Paging and Scrolling	Paging by updating start address Horizontal scrolling by the character, by setting horizontal virtual screen width Vertical smooth scrolling by updating display start raster
	Character Attributes	Reverse video, blinking, nondisplay (white or black) character attributes
Application	CRTC Compatible	Facilitates system replacement of CRT display with LCD.
	OR Function	Enables superimposing display of character screen and graphic screen
Configuration	LCTC Configuration	Single 5 V power supply I/O TTL compatible except $\overline{RES}$, MODE, SK0, SK1 Bus connectable with HMCS 6800 family (HD63645) Bus connectable with 80 family (HD64645) CMOS process Internal logic fully static 80-pin flat plastic package

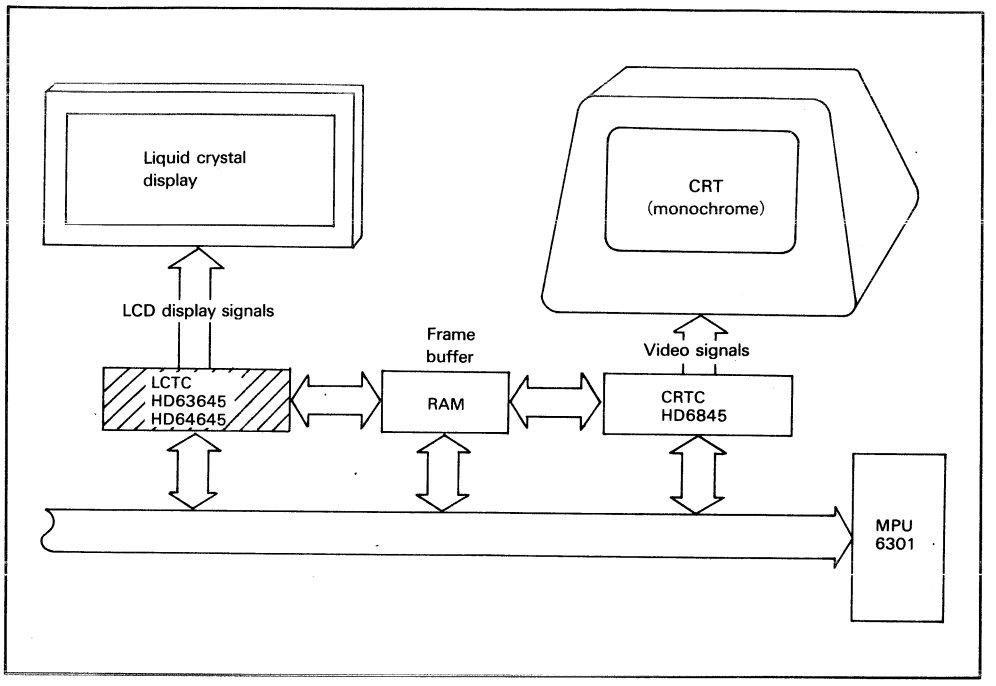


Figure 1. LCD and CRT Displays

Internal Block Diagram

Figure 2 is a block diagram of the LCTC.

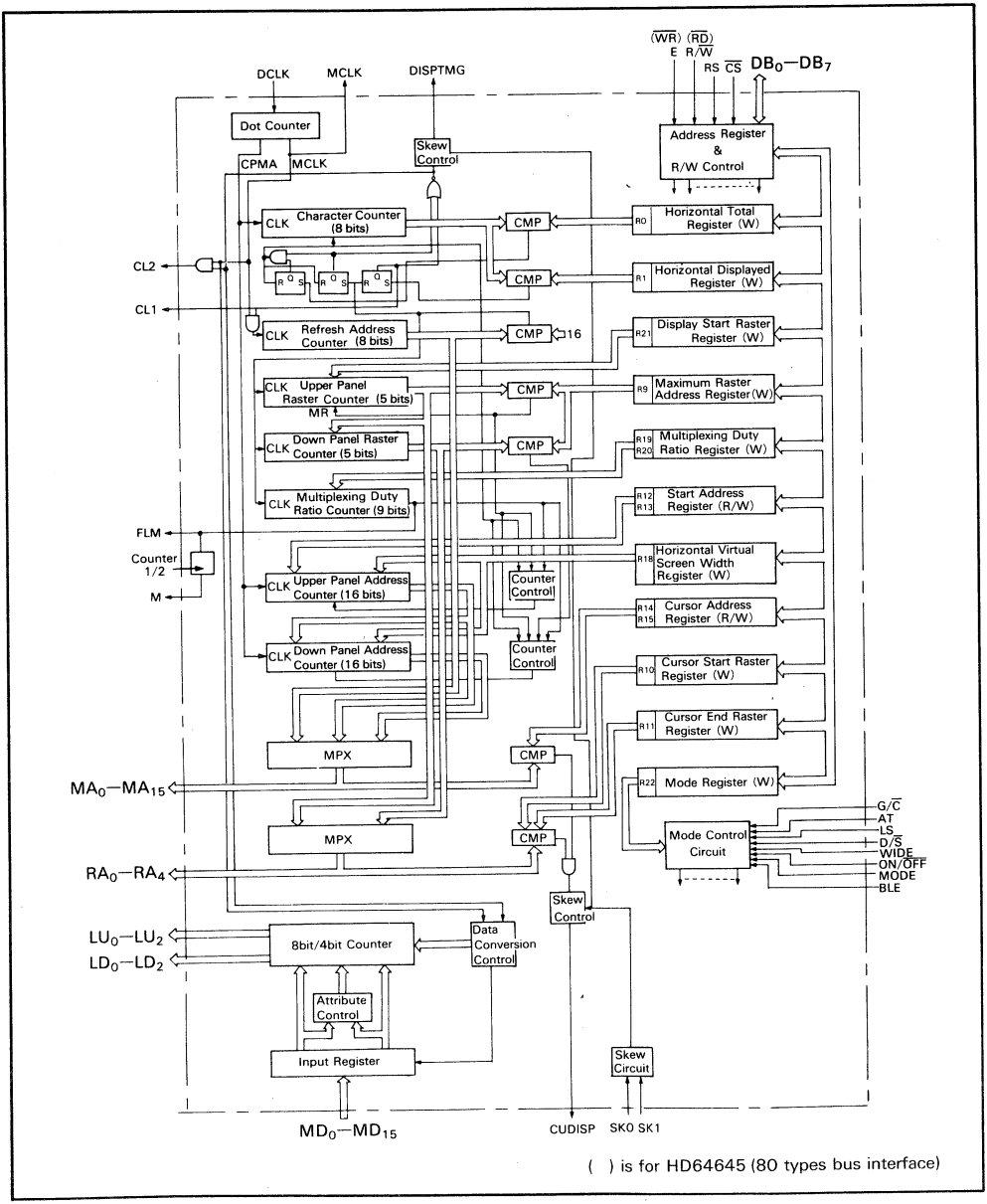


Figure 2. LCTC Block Diagram

System Block Configuration Examples

Figure 3 is a block diagram of a character/graphic display system. Figure 5 shows two examples using LCD drivers.

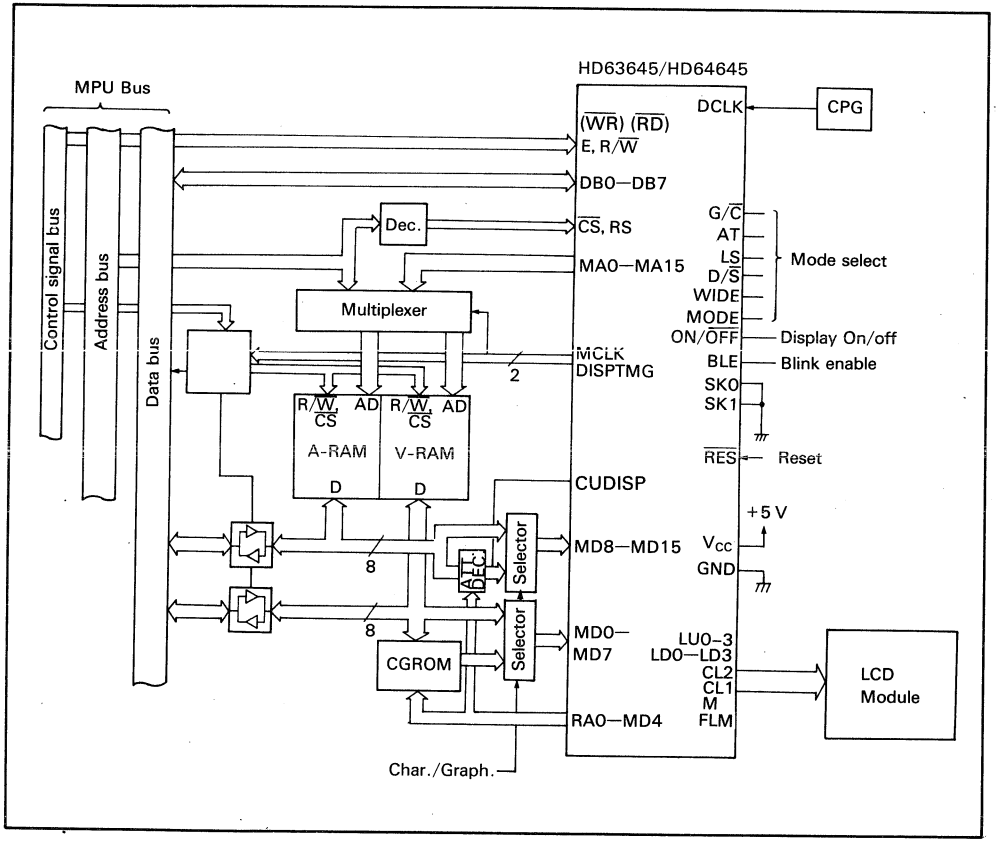
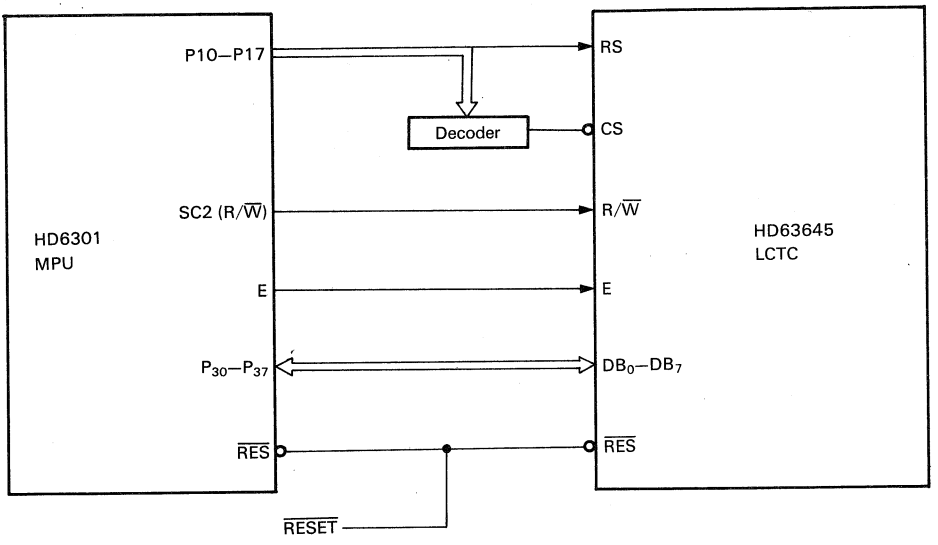


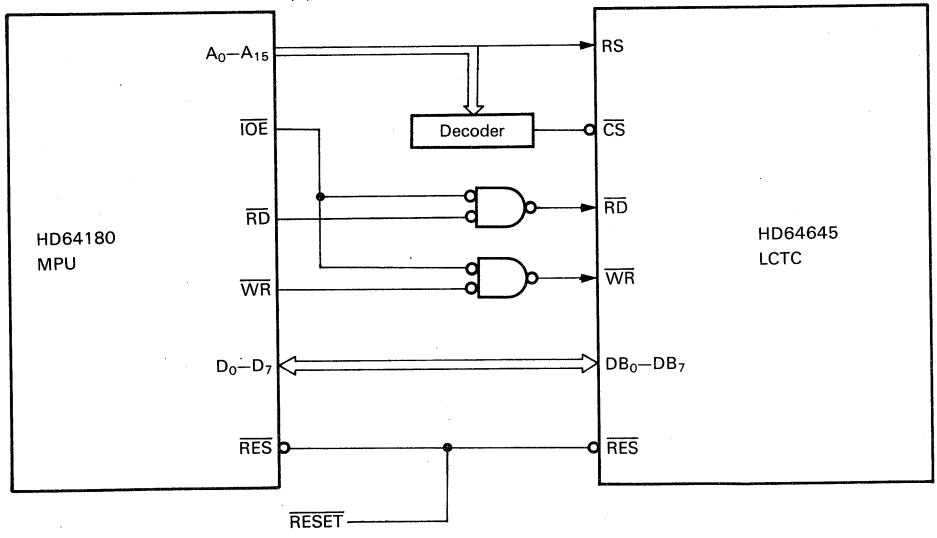
Figure 3. Character/Graphic Display System Example

Interface to MPU



Note: HD6301 is set in mode 5. P10—P17 are used as output ports, and P30—P37 as data buses. SC2 outputs R/W here.

(1) Interface between HD6301 and HD63645



Note: Concerning 80 family MPU's, I/O space is separate from memory space in software. Thus the LCTC, a part of I/O, needs the ANDed signals of the interface signals and IOE. So IOE and RD, and IOE and WR should be ORed to satisfy t_{AS}, the timing of CS, RD, and WR.

(2) Interface between HD64180 and HD64645

Figure 4. Interface to MPU

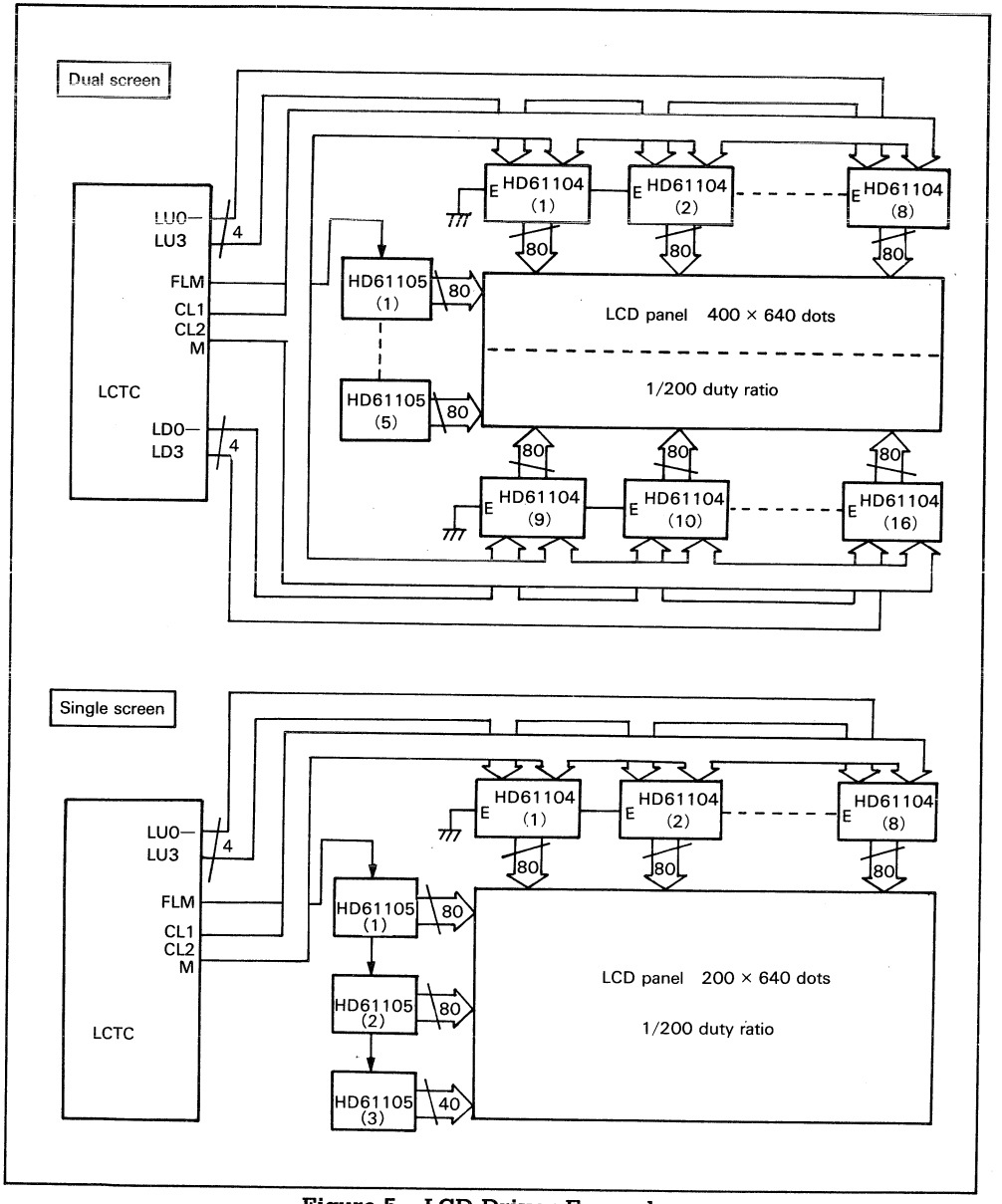


Figure 5. LCD Driver Examples

Registers

Table 5 shows the register mapping. Table 5 describes the in function. Table 6 shows the differences between CRTC and LCTC registers.

Table 4. Registers Mapping

		Address Register	Reg.					Data Bit							
CS	RS	43210	No.	Register Name	Program Unit	Symbol	R/W	7	6	5	4	3	2	1	0
1	–	------		Invalid	–	–	–								
0	0	------	AR	Address Register	–	–	W								
0	1	00000	R0	Horizontal Total Characters	Character[3]	Nht	W								
0	1	00001	R1	Horizontal Displayed Characters	Character	Nhd	W								
0	1	01001	R9	Maximum Raster Address	Raster	Nr	W								
0	1	01010	R10	Cursor Start Raster	Raster[4]	Ncs	W		B	P					
0	1	01011	R11	Cursor End Raster	Raster	Nce	W								
0	1	01100	R12	Start Address (H)	Memory Address	–	R/W								
0	1	01101	R13	Start Address (L)	Memory Address	–	R/W								
0	1	01110	R14	Cursor Address (H)	Memory Address	–	R/W								
0	1	01111	R15	Cursor Address (L)	Memory Address	–	R/W								
0	1	10010	R18	Horizontal Virtual Screen Width	Character	Nir	W								
0	1	10011	R19	Multiplexing Duty Ratio (H)	Raster[3]	Ndh	W								
0	1	10100	R20	Multiplexing Duty Ratio (L)	Raster[3]	Ndl	W								
0	1	10101	R21	Display Start Raster	Raster	Nsr	W								
0	1	10110	R22	Mode Register	—Note[5]	–	W				ON/ OFF	G/C	WIDE	BLE	AT

Notes : 1. ▨ : Invalid data bits

2. R/W indicates whether write access or read access is enabled to/from each register.
   W : Only write accessible
   R/W : Both read and write accessible
3. The "value to be specified less 1" should be programmed in these registers (R0, R1) and R20).
4. Data bits 5 and 6 of cursor start register control the cursor status as shown below. (For more details, refer to page 27).

B	P	Cursor Blink Mode
0	0	Cursor on ; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

5. The OR of mode pin status and mode register data determines the mode.
6. Registers R2-R8, R16, and R17 are not assigned for the LCTC. Programming to these registers, will be ignored.

Table 5. Internal Register Description

Reg. No.	Register Name	Size (Bits)	Description
AR	Address Register	5	Specifies the internal control registers (R0, R1, R9-R15, R18-R22) address to be accessed
R0	Horizontal Total Characters	8	Specifies the horizontal scanning period
R1	Horizontal Displayed Characters	8	Specifies the number of displayed characters per character row
R9	Maximum Raster Address	5	Specifies the number of rasters per character row, including the space between character rows
R10	Cursor Start Raster	5+2	Specifies the cursor start raster address and its blink mode
R11	Cursor End Raster	5	Specifies the cursor end raster address
R12	Start Address (H)	16	Specify the display start address
R13	Start Address (L)		
R14	Cursor Address (H)	16	Specify the cursor display address
R15	Cursor Address (L)		
R18	Horizontal Virtual Screen Width	8	Specifies the length of one row in memory space for horizontal scrolling
R19	Multiplexing Duty Ratio (H)	9	Specify the number of rasters for one screen
R20	Multiplexing Duty Ratio (L)		
R21	Display Start Raster	5	Specifies the display start raster within a character row for smooth scrolling
R22	Mode Register	5	Controls the display mode

*For more details of registers, refer to "Internal Registers".

Table 6. Internal Register Comparison between LCTC and CRTC

Reg. No.	LCTC HD63645/HD64645	Comparison	CRTC HD6845
AR	Address Register	Equivalent to CRTC	Address Register
R0	Horizontal Total Characters		Horizontal Total Characters
R1	Horizontal Displayed Characters		Horizontal Displayed Characters
R2		Particular to CRTC ; unnecessary for LCTC	Horizontal Sync Position
R3			Sync Width
R4			Vertical Total Characters
R5			Vertical Total Adjust
R6			Vertical Displayed Characters
R7			Vertical Sync Position
R8			Interlace and Skew
R9	Maximum Raster Address	Equivalent to CRTC	Maximum Raster Address
R10	Cursor Start Raster		Cursor Start Raster
R11	Cursor End Raster		Cursor End Raster
R12	Start Address (H)		Start Address (H)
R13	Start Address (L)		Start Address (L)
R14	Cursor Address (H)		Cursor (H)
R15	Cursor Address (L)		Cursor (L)
R16		Particular to CRTC ; unnecessary for LCTC	Light Pen (H)
R17			Light Pen (L)
R18	Horizontal Virtual Screen Width	Additional registers for LCTC	
R19	Multiplexing Duty Ratio (H)		
R20	Multiplexing Duty Ratio (L)		
R21	Display Start Raster		
R22	Mode Register		

Functional Description

Programmable Screen Format

Figure 6 illustrates the relation between LCD display screen and registers. Figure 7 shows a timing chart of signals output from the LCTC in mode 5 as an example.

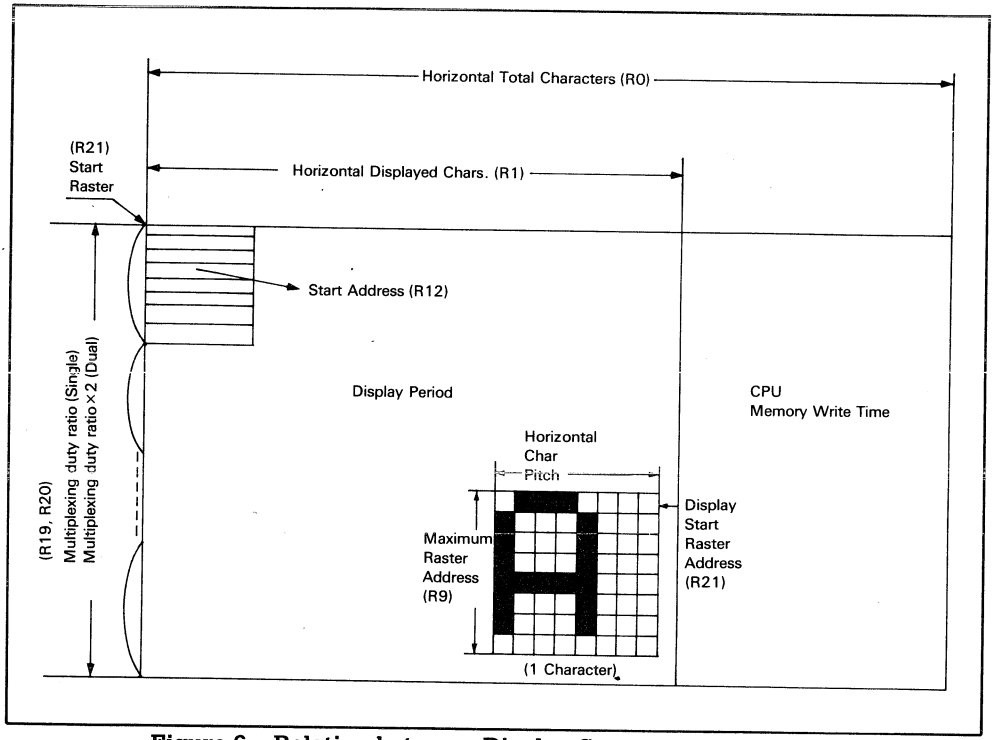


Figure 6. Relation between Display Screen and Registers

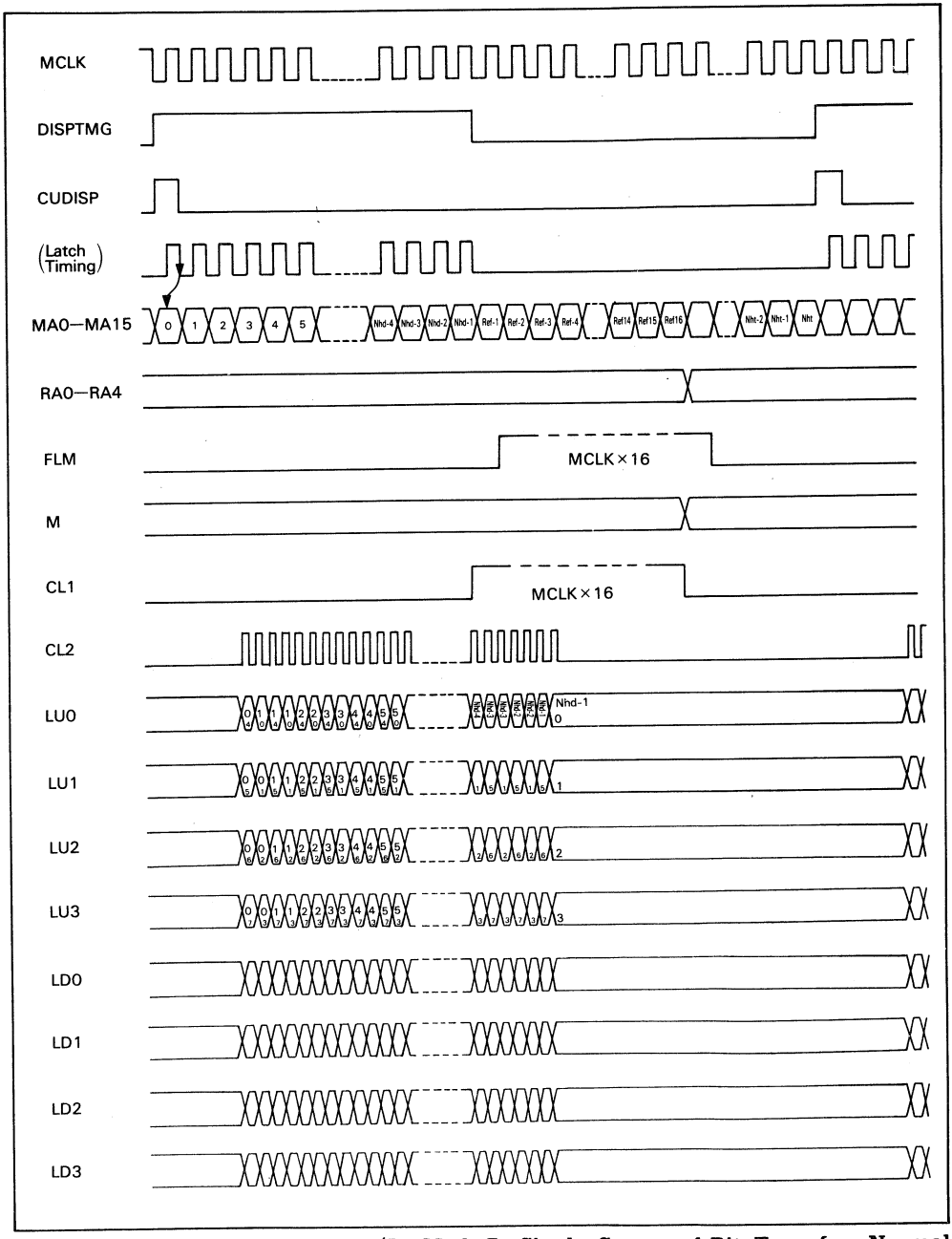


Figure 7. LCTC Timing Chart (In Mode 5: Single Screen, 4-Bit Transfer, Normal Character Display)

Cursor Control

The following cursor functions (figure 8) can be controlled by programming specific registers.

- Cursor display position
- Cursor height
- Cursor blink mode

A cursor can be displayed only in character mode. Also, CUDISP pin must be connected to MD12 pin to display a cursor.

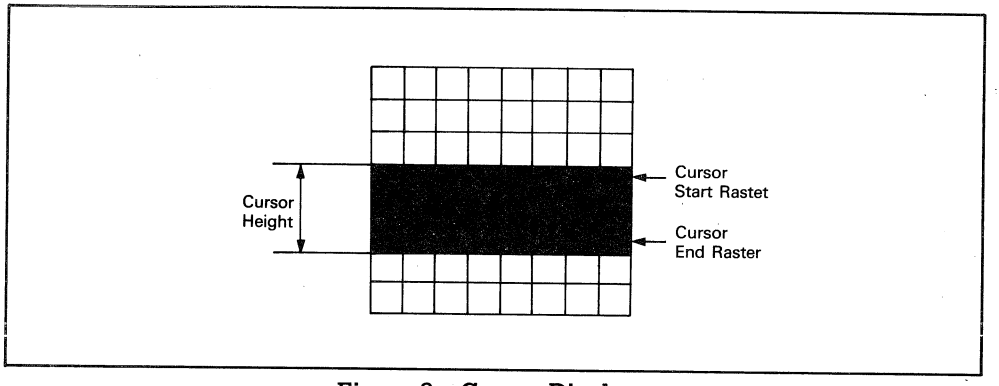


Figure 8. Cursor Display

Character Mode and Graphic Mode

The LCTC supports two types of display modes; character mode and graphic mode. Graphic mode 2 is provided to utilize software for system using the CRTC (HD6845).

The display mode is controlled by an OR between the mode select pins (D/$\overline{S}$, G/$\overline{C}$, LS, WIDE, AT) and mode register (R22).

Character Mode : Character mode displays characters by using CG-ROM. The display data supplied from memory is accessed in 8-bit units. A variety of character attribute functions are provided, such as reverse video, blinking, nondisplay (white or black), etc., by storing the attribute data in attribute RAM (A-RAM).

Figure 9 illustrates the relation between character display screen and memory contents.

Graphic Mode 1 : Graphic Mode 1 directly displays data stored in a graphic memory buffer. The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. Figure 10 illustrates the relation between graphic display screen and memory contents.

Graphic Mode 2 : Graphic mode 2 utilizes software for the system using the CRTC (HD6845). The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. The same memory addresses are output repeatedly a number of times specified by maximum raster register (R9). The raster address is output in the same way as character mode.

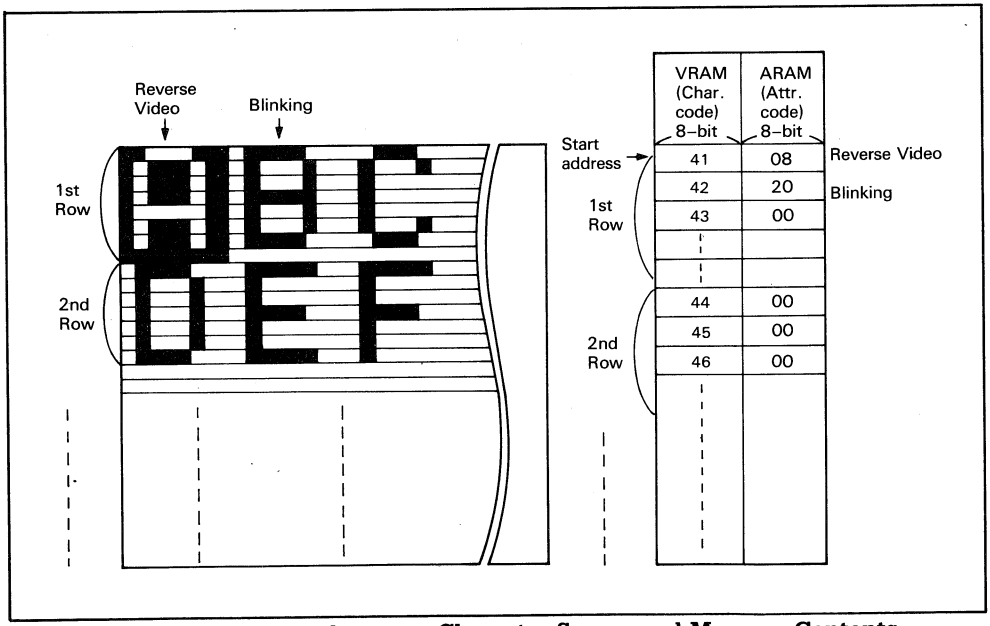


Figure 9. Relation between Character Screen and Memory Contents

Horizontal Virtual Screen Width

Horizontal virtual screen width can be specified by the character in addition to the number of horizontal displayed characters (figure 11).

The display screen can be scrolled in any direction by the character, by setting the horizontal virtual screen width and updating the start address. This function is enabled by programming the horizontal virtual screen width register (R18).

Figure 12 shows an example.

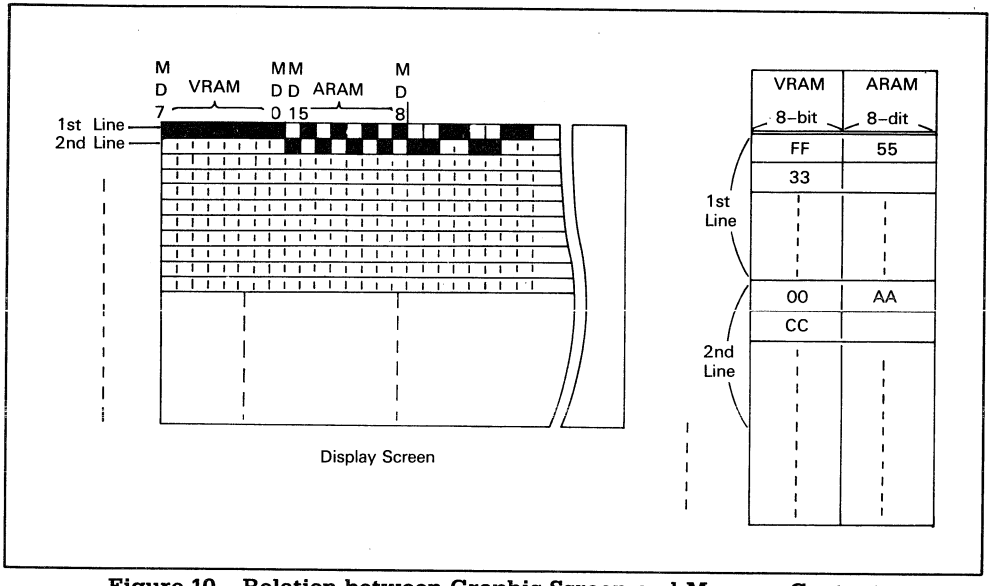


Figure 10. Relation between Graphic Screen and Memory Contents

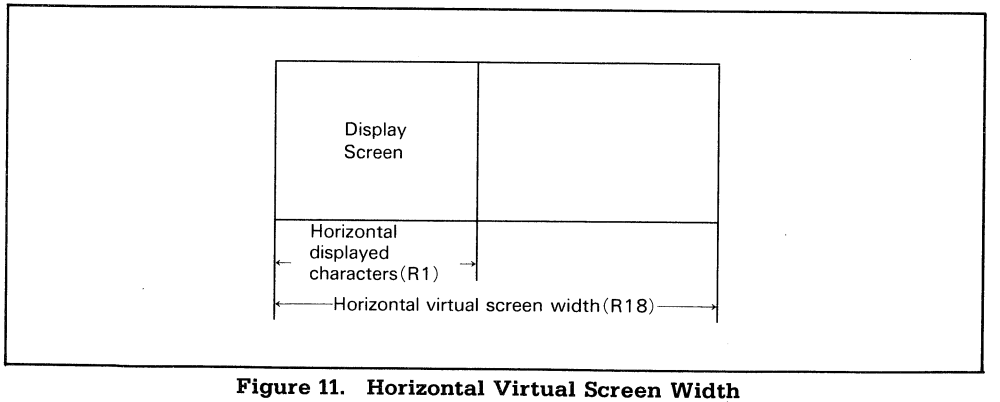


Figure 11. Horizontal Virtual Screen Width

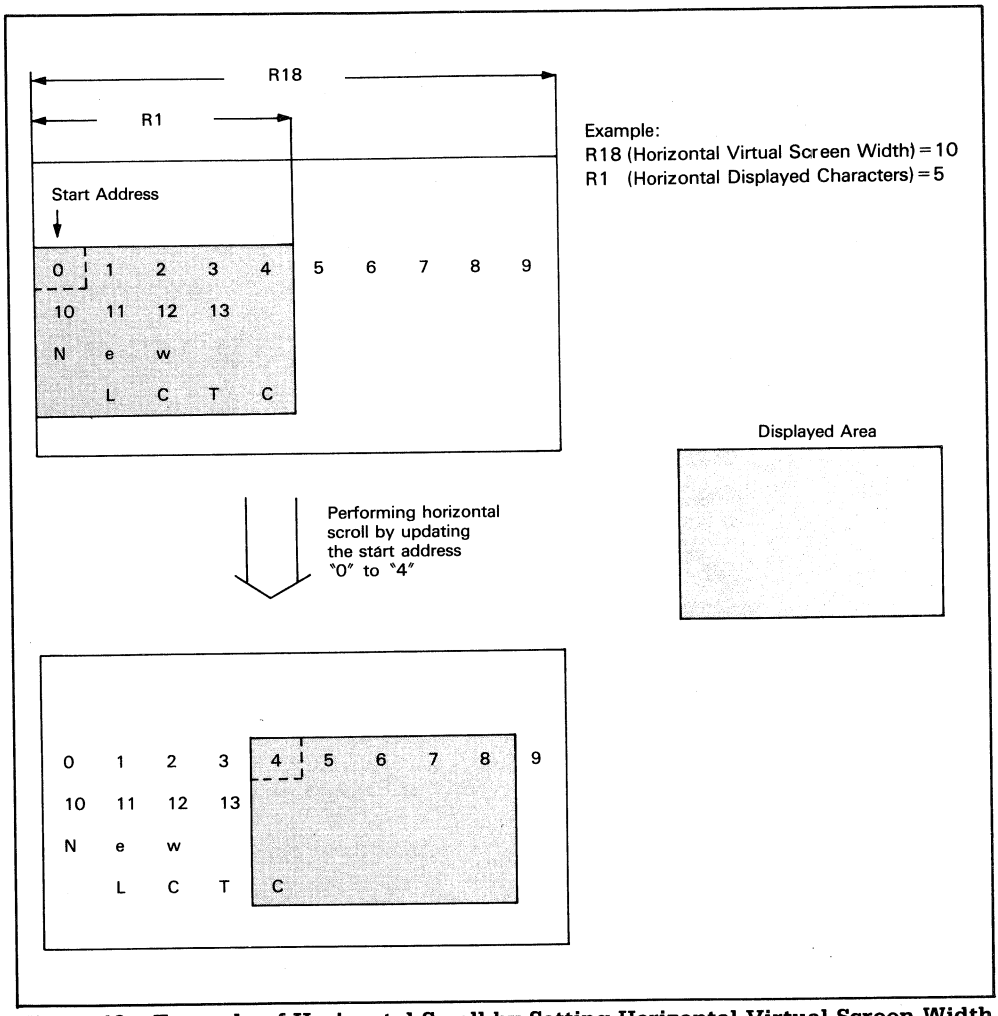


Figure 12. Example of Horizontal Scroll by Setting Horizontal Virtual Screen Width

Smooth Scroll

Vertical smooth scrolling (figure 13) is performed by updating the display start raster, as specified by the start raster register (R21). This function is offered only in character mode.

Wide Display

The character to be displayed can be doubled in width, by supplying the same data twice (figure 14). This function is offered only in character mode, and controlled either by bit 2 of the mode register (R22) or by the WIDE pin.

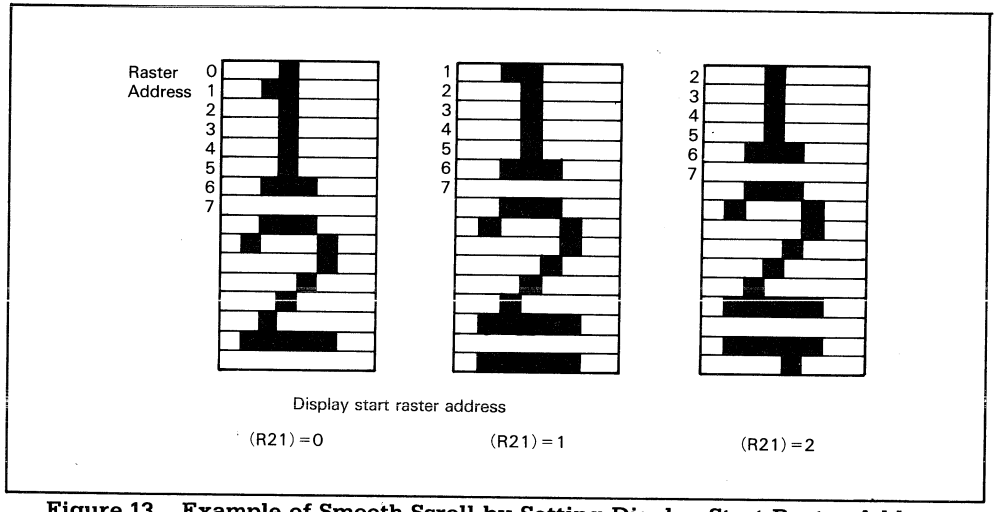


Figure 13. Example of Smooth Scroll by Setting Display Start Raster Address

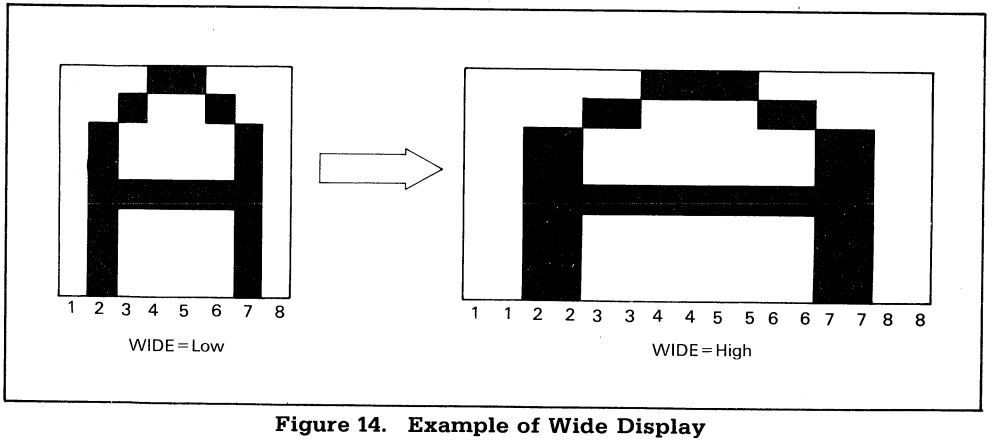


Figure 14. Example of Wide Display

Attribute Functions

A variety of character attribute functions such as reverse video, blinking, nondisplay (white) or nondisplay (black) can be implemented by storing the attribute data in A-RAM (attribute RAM). Figure 15 shows a display example using each attribute function.

The attribute functions are offered only in character mode, and controlled either by bit 0 of the mode register (R22) or the AT pin. As shown in figure 15, a character attribute can be specified by placing the character code on MD0-MD7, and the attribute code on MD11-MD15. MD8-MD10 are invalid.

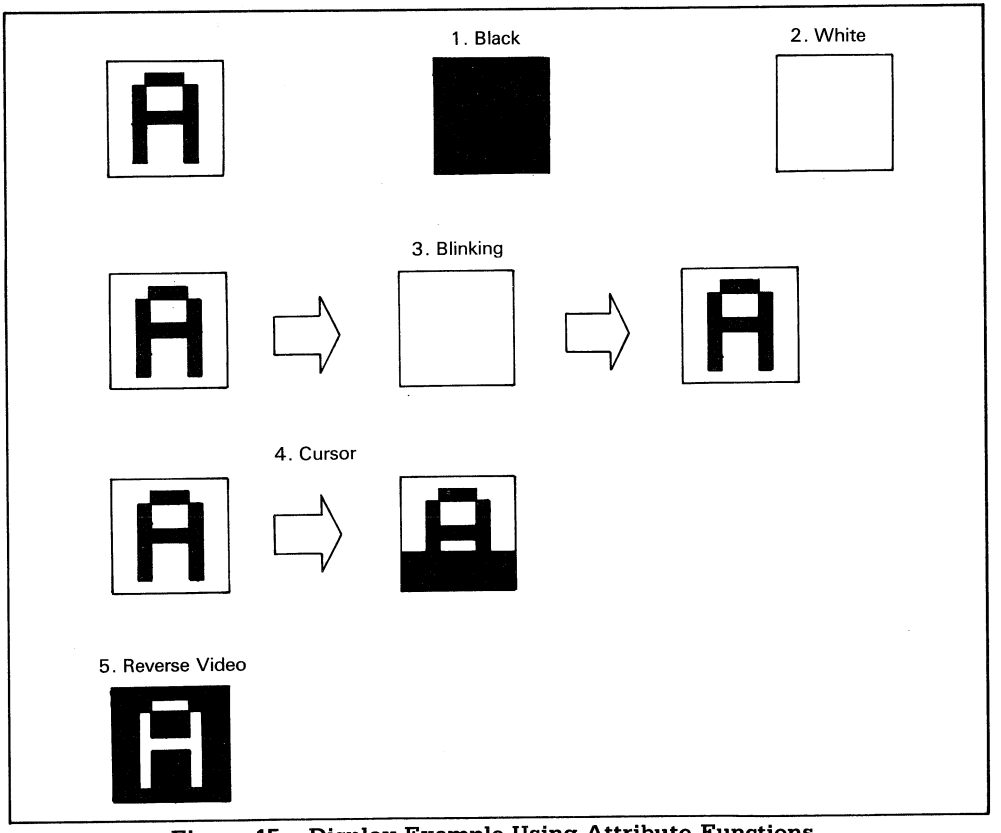


Figure 15. Display Example Using Attribute Functions

MD Input	15	14	13	12	11	10-8	7-0
Function	Non-display (black)	Non-display (white)	Blinking	Cursor	Reverse video	* * *	Character Code

* : Invalid

Figure 16. Attribute Code

OR Function —Superimposing Characters and Graphics

The OR function (figure 17) generates the OR of the data entered into MD0-MD7 (e.g. character data) and the data into MD8-MD15 (e.g. graphic data) in the LCTC and transfers this data as 1 byte.

This function is offered only in character mode, and controlled by bit 0 of the mode register (R22) or by the AT pin. Any attribute functions are disabled when using the OR function.

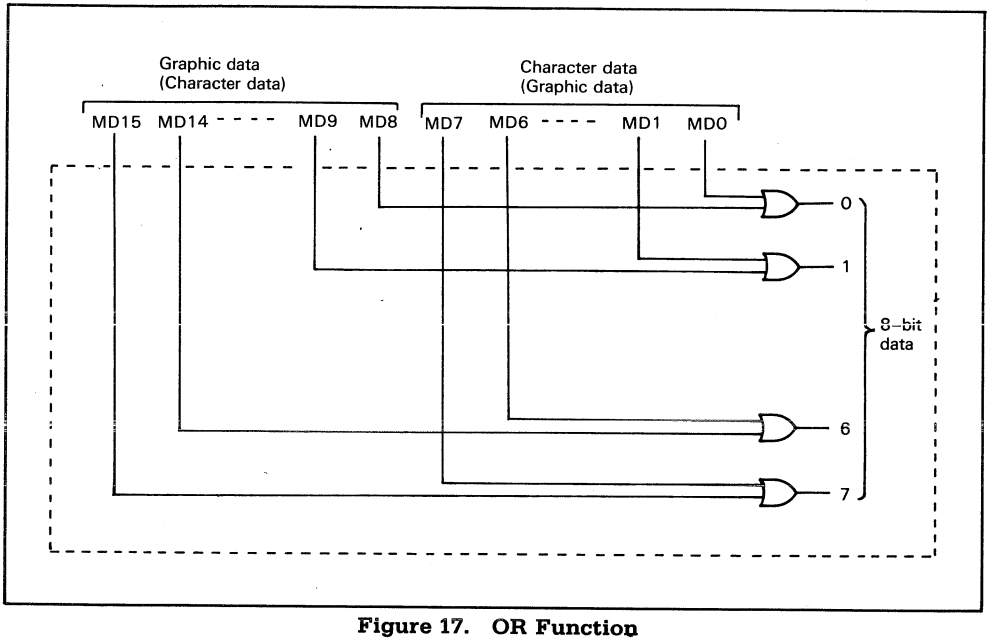


Figure 17. OR Function

DRAM Refresh Address Output Function

The LCTC outputs the address for DRAM refresh while CL1 is high, as shown in figure 18. The 16 refresh addresses per scanned line are output 16 times, from $00-$FF.

Skew Function

The LCTC can specify the skew (delay) for CUDISP, DISPTMG, CL2 outputs and MD inputs.

If buffer memory and character generator ROM cannot be accessed within one horizontal character display period, the access is retarded to the next cycle by inserting a latch to memory address output and buffer memory output. The skew function retards the CUDISP, DISPTMG, CL2 outputs, and MD inputs in the LCTC to match phase with the display data signal.

By utilizing this function, a low-speed memory can be used as a buffer RAM or a character generator ROM.

This function is controlled by pins SK0 and SK1 as shown in table 7.

Table 7. Skew Function

SK0	SK1	Skew Function
0	0	No skew
1	0	1 character time skew
0	1	2 character time skew
1	1	Inhibited combination

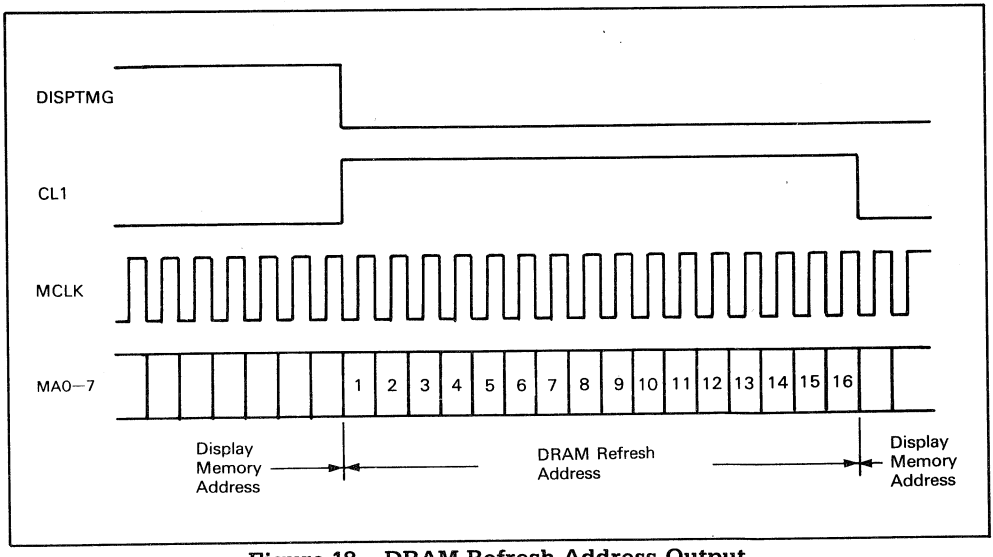


Figure 18. DRAM Refresh Address Output

Easy Mode

This mode utilizes software for systems using the CRTC (HD6845). By setting MODE pin to high, the display mode and screen format are fixed as shown in table 8. With this mode, software for a CRT screen can be utilized in a system using the LCTC, without changing the BIOS.

Automatic Correction of Down Panel Paster Address

When the LCTC mode is set for character display and dual screen, memory addresses (MA) and raster addresses (RA) are output in such a way as to keep continuity of display spreading over the two panels. Therefore users can use the LCTC without considering the multiplexing duty ratio (the number of vertical dots of a screen) or the character font. (See figure 19.)

Table 8. Fixed Values in Easy Mode

Reg. No.	Register Name	Fixed Value (decimal)
R9	Maximum raster address	7
R10	Cursor start raster	6
R11	Cursor end raster	7
R18	Horizontal virtual screen width	Same value as (R1)
R19	Multiplexing duty ratio (H)	99 (in dual screen mode)
R20	Multiplexing duty ratio (L)	199 (in single screen mode)
R21	Display start raster	0
R22	Mode register	0

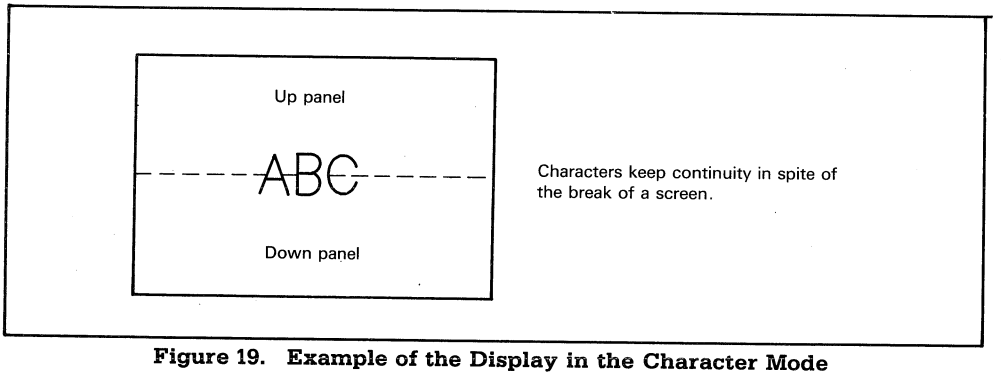


Figure 19. Example of the Display in the Character Mode

System Configuration and Mode Setting

LCD System Configuration

The screen configuration, single or dual, must be specified when using the LCD system (figure 20).

Using the single screen configuration, you can construct an LCD system with lower cost than a dual screen system, since the required number of column driversis smaller and the manufacturing process for mounting them is simpler. However, there are some limitations, such as duty ratio, breakdown voltage of a driver, and display quality of the liquid crystal, in single screen configuration. Thus, a dual screen configuration may be more suitable to an application.

The LCTC also offers an 8-bit LCD data transfer function to support an LCD screen with a smaller interval of signal input terminals. For a general size LCD screen, such as 640 × 200 single, or 640 × 400 dual, the usual 4-bit LCD data transfer is satisfactory.

Hardware Configuration and Mode Setting

The LCTC supports the following hardware configurations :

- Single or dual screen configuration
- 4-or 8-bit LCD data transfer

and the following screen format :

- Character, graphic 1, or graphic 2 display
- Normal or wide display (only in character mode)
- OR or attribute display (only in character mode)

Also, the LCTC supports up to 40 Mbits/s of large screeen mode (mode 13) for large screen display. This mode is provided only in graphic 1 mode.

Table 9 shows the mode selection method according to hardware configuration and screen format. Table 10 shows how they are specified.

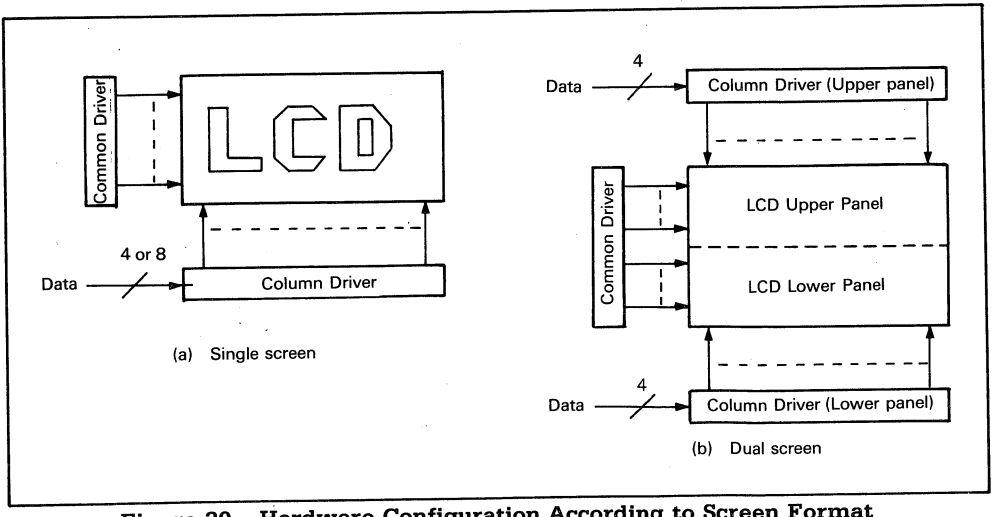


Figure 20. Hardware Configuration According to Screen Format

Table 9. Mode Selection

Hardware Configuration			Screen Format				
LCD Data Transfer	**Screen Configuration**	**Screen Size**	**Character/ Graphic**	**Normal/ Wide**	**Attribute/ OR**	**Maximum data transfer speed (MBPS)**	**Mode No.**
4-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	5
				Wide	$\frac{AT}{OR}$	10	6
			Graphic 1			20	7
			Graphic 2			20	8
	Dual	Normal	Character	Normal	$\frac{AT}{OR}$	20	1
				Wide	$\frac{AT}{OR}$	10	2
			Graphic 1			20	3
			Graphic 2			20	4
		Large	Graphic 1			40	13
8-bit	Single	Normal	Character	Normal	$\frac{AT}{OR}$	20	9
				Wide	$\frac{AT}{OR}$	10	10
			Graphic 1			20	11
			Graphic 2			20	12

Note : Maximum data transfer speed indicates amount of the data read out of a memory. Thus, the data transfer speed sent to the LCD driver in wide function is 20 Mbps.

Mode List

Table 10. Mode List

No.	Mode Name	Pin Name D/$\overline{S}$	G/$\overline{C}$	LS	WIDE	AT	Screen Confg.	Graphic/ Character	Data Transfer	Wide Display	Attribute
1	Dual-screen character	1	0	0	0	0	Dual screen	Character	4-bit × 2	Normal	OR
		1	0	0	0	1					AT
2	Dual-screen wide character	1	0	0	1	0				Wide	OR
		1	0	0	1	1					AT
3	Dual-screen graphic 1	1	1	0	0	1		Graphic		—	—
4	Dual-screen graphic 2	1	1	0	0	0					
5	Single-screen character	0	0	0	0	0	Single screen	Character	4-bit	Normal	OR
		0	0	0	0	1					AT
6	Single-screen wide character	0	0	0	1	0				Wide	OR
		0	0	0	1	1					AT
7	Single-screen graphic 1	0	1	0	0	1		Graphic		—	—
8	Single-screen graphic 2	0	1	0	0	0					
9	8-bit character	0	0	1	0	0		Character	8-bit	Normal	OR
		0	0	1	0	1					AT
10	8-bit wide character	0	0	1	1	0				Wide	OR
		0	0	1	1	1					AT
11	8-bit graphic 1	0	1	1	0	1		Graphic		—	—
12	8-bit graphic 2	0	1	1	0	0					
13	Large screen	1	1	1	0	1	Dual screen		4-bit × 2		

The LCTC display mode is determined by pins D/$\overline{S}$ (pin 55), G/$\overline{C}$ (pin 58), LS (pin 56), WIDE (pin 54), and AT (pin 57). As for G/C, WIDE, and AT, the OR is taken between data bits 0, 2, and 3 of the mode register (R22). The display mode can be controlled by either one of the external pins or the data bits of R22.

Note : The above 5 pins have 32 status combinations (high and low). Any combinations other than the above are inhibited, because they may cause malfunctions. If you set an inhibited combination, set the right combination again.

Internal Registers

The HD63645/HD64645 has one address register and fourteen data registers. In order to select one out of fourteen data registers, the address of the data register to be selected must be written into the address register. The MPU can transfer data to/from the data register corresponding to the written address.

To be software compatible with the CRTC (HD6845), registers R2-R8, R16, and R17, which are not necessary for an LCD are defined as invalid for the LCTC.

Address Register (AR)

AR register (figure 21) specifies one out of 14 data registers. Address data is written into the address register when RS is low. If no register corresponding to a specified address exists, the address data is invalid.

Horizontal Total Characters Register (R0)

R0 register (figure 22) specifies a horizontal scanning period. The total number of horizontal characters less 1 must be programmed into this 8-bit register in character units. The "Nht" indicates the horizontal scanning period including the period when the CPU occupies memory (total number of horizontal characters minus the number of horizontal displayed characters). Its unit is, then, converted from time into the number of characters. This value is to be specified according to the specification of the LCD system to be used.

Note the following restrictions

$$Nhd + \frac{16}{m} \leqq Nht + 1$$

Mode No.	m
5, 9	1
1, 6, 7, 8, 10, 11, 12, 13	2
2, 3, 4	4

Horizontal Displayed Characters Register (R1)

R1 register (figure 23) specifies the number of characters displayed per row. The horizontal character pitches are 8 bits for normal character display and 16 dots for wide character display and graphic display.

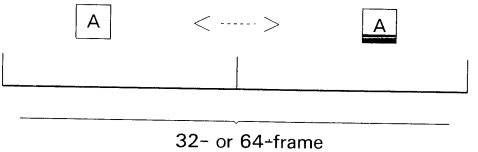
The "Nhd" must be less than the total number of horizontal characters.

Maximum Raster Address Register (R9)

R9 register (figure 24) specifies the number of rasters per row in characters mode, consisting of 5 bits. The programmable range is 0 (1 raster/row) to 31 (32 rasters/row).

Cursor Start Raster Register (R10)

R10 register (figure 25) specifies the cursor start raster address and its blink mode. Refer to table 11.



Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	—	W
—	—	—	Register address						

Figure 21. Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Character	W
Nht (Total characters − 1)									

Figure 22. Horizontal Total Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Character	W
Nhd (Displayed characters)									

Figure 23. Horizontal Displayed Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Raster	W
—	—	—	Nr						

Figure 24. Maximum Raster Address Register

Cursor End Raster Register (R11)

R11 register (figure 26) specifies the cursor end raster address.

Start Address Register (H/L)(R12/R13)

R12/R13 register (figure 27) specifies a buffer memory read start address. Updating this register facilitates paging and scrolling. R14/R15 register can be read and written to/from the MPU.

Cursor Address Register (H/L)(R14/R15)

R14/R15 register (figure 28) specifies a cursor display address. Cusor display requires setting R10 and R11, and CUDISP should be connected with MD12 (in character mode). This register can be read from and written to the MPU.

Horizontal Virtual Screen Width Register (R18)

R18 register (figure 29) specifies the memory width to determine the start address of the next row. By using this register, memory width can be specified larger than the number of horizontal displayed characters. Updating the display start address facilitates scrolling in any direction within a memory space.

The start address of the next row is that of the previous row plus Nir. If a larger memory width than display width is unnecessary, Nir should be set equal to the number of horizontal displayed characters.

Multiplexing Duty Ratio Register (H/L) (R19/R20)

R19/R20 register (figure 30) specifies the number of vertical dots of the display screen. The programmed value differs according to the LCD screen configuration.

In single screen configuration :

(Programmed value) = (Number of vertical dots) − 1.

In dual screen configuration :

$$\text{(Programmed value)} = \frac{\text{(Number of vertical dots)}}{2} - 1.$$

Display Start Raster Register (R21)

R21 register (figure 31) specifies the start raster of the character row displayed on the top of the screen. The programmed value should be equal or less than the maximum raster address. Updating this register allows smooth scrolling in character mode.

Mode register (R22)

The OR of the data bits of R22 (figure 32) register and the external terminals of the same name determines a particular mode. (figure 33)

Table 11 Cursor Blink Mode

B	P	Cursor blink mode
0	0	Cursor on ; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	B	P	Ncs (Raster address)					Raster	W

Figure 25. Cursor Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nce (Raster address)					Raster	W

Figure 26. Cursor End Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R12)								Memory address	R/W
Memory address (L) (R13)									

Figure 27. Start Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Memory address (H) (R14)								Memory address	R/W
Memory address (L) (R15)									

Figure 28. Cursor Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nir (No. of chars. of virtual width)								Character	W

Figure 29. Horizontal Virtual Screen Width Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	—	—	—	— (R19)	Ndh*	Raster	W
Ndl (Number of rasters − 1) (R20)									

* : Number of rasters

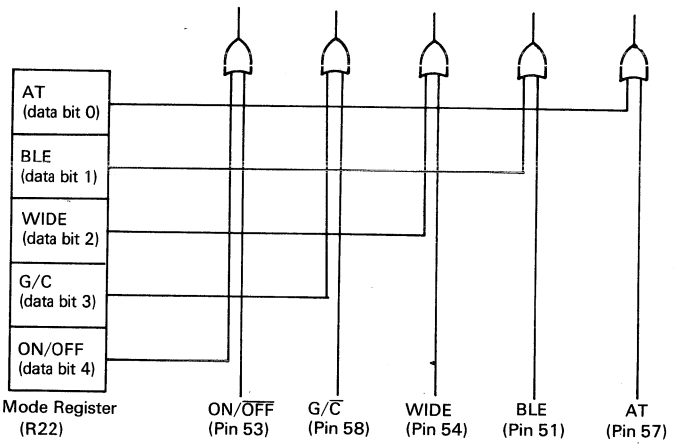
Figure 30. Multiplexing Duty Ratio Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Raster address					Raster	W

Figure 31. Display Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	ON/OFF	G/C	WIDE	BLE	AT	—	W

Figure 32. Mode Register



Notes: 1. AT (valid only when G/C is low (character mode))
AT = High: Attribute functions enabled, OR function disabled.
AT = Low: OR function enabled, attribute functions disabled.

2. BLE (valid only when G/C is low (character mode))
BLE = High: Blinking enable on the character specified by attribute RAM
BLE = Low: No blinking

3. WIDE (valid only when G/C is low (character mode))
WIDE = High: Wide display enabled
WIDE = Low: Normal display

4. G/C
G/C = High: Graphic 1 display (when AT = Low) or Graphic 2 display (when AT = High)
G/C = Low: Character display

5. ON/OFF
ON/OFF = High: Display on state
ON/OFF = Low: Display off state

Figure 33. Correspondence between Mode Register and External Pins

Restrictions on Programming Internal Registers

Note when programming that the values you can write into the internal registers is restricted as shown in Table 12.

Table 12. Restrictions on Writing Values into the Internal Registers

Function	Restrictions	Register
Display Format	$1 < Nhd < Nht + 1 \leqq 256$	R0, R1
	$Nhd + \frac{16}{m} * 1 \leqq Nht + 1$	
	(No. of vertical dots) x (no. of horizontal dots) x (frame frequency; f_{FRM}) $\leqq$ (data transfer speed; V)	R1, R19, R20
	$\left\{\begin{matrix}1\\2\end{matrix}\right\} * 2 \times (Nd + 1) \times Nhd \times \left\{\begin{matrix}8\\16\end{matrix}\right\} * 3\ f_{FRM} \leqq V$	
	$Nhd \leqq Nir$	R1, R18
	$0 \leqq Nd \leqq 511$	R19, R20
Cursor Control	$0 \leqq Ncs \leqq Nce$	R10, R11
	$Nce \leqq Nr$	R10, R9
Smooth Scroll	$Nsr \leqq Nr$	R21, R9
Memory Width Set	$0 \leqq Nir \leqq 255$	R18

*1 m varies according to the modes. See the following table.

Mode No.	m
5,9	1
1,6,7,8,10,11,12,13	2
2,3,4	4

*2 Set 1 when an LCD screen is a single screen, and set 2 when dual. Modes are classified as shown in the following table.

Mode No.	Value
5,6,7,8,9,10,11,12	1
1,2,3,4,13	2

*3 Set 8 when a character is constructed with 8 dots, and set 16 when with 16 dots. Modes are classified as shown in the following table.

Mode No.	Value
1,5,9	8
2,3,4,6,7,8,10,11,12,13	16

Reset

$\overline{RES}$ pin determines the internal state of LSI counters and the like. This pin does not affect register contents nor does it basically control output terminals.

"Reset" is defined as follows (Figure 34) :

- At reset: the time when $\overline{RES}$ goes low
- During reset: the period while $\overline{RES}$ remains low
- After reset: the period on and after the $\overline{RES}$ transition from low to high

Make sure to hold the reset signal low for at least 1 μs.

$\overline{RES}$ pin should be pulled high by users during operation.

Reset State of Pins

$\overline{RES}$ pin does not basically control output pins, and operates regardless of other input pins.

(1) Preserves states before reset :
LU0-LU3, LD0-LD3, FLM, CL1, RA0-RA4

(2) Fixed at high level :
MLCK

(3) Preserves states before reset or fixed at low level according to the timing when the reset signal is input :
DISPTMG, CUDISP, MA0-MA15

(4) Fixed at high or low according to mode :
CL2

(5) Unaffected :
DB_0-DB_7

Reset State of Registers

$\overline{RES}$ pin does not affect register contents. Therefore, registers can be read or written even during a reset state ; their contents will be preserved regardless of reset until they are rewritten to.

Notes for HD63645/HD64645

(1) The HD63645/HD64645 are CMOS LSIs, and it should be noted that input pins must not be left disconnected, etc.

(2) At power-on, the state of internal registers becomes undefined. The LSI operation is undefined until all internal registers have been programmed.

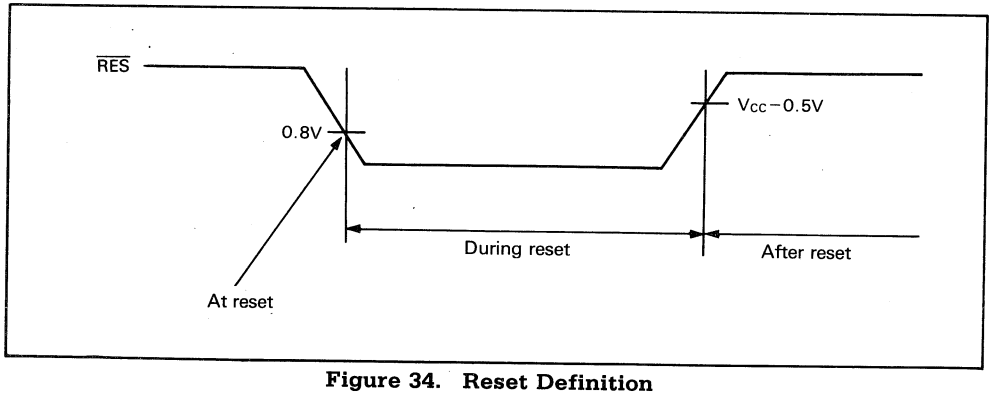


Figure 34. Reset Definition

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes : 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.
2. Width respect to GROUND (GND = 0 V)

Electrical Characteristics

DC characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$, MODE, SK0, SK1	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V	
	DCLK, ON/$\overline{OFF}$		2.2		V_{CC}+0.3	V	
	All others		2.0		V_{CC}+0.3	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL Interface[1]	V_{OH}	2.4			V	I_{OH} = −400μA
	CMOS Interface[1]		V_{CC}−0.8			V	I_{OH} = −400μA
Output low voltage	TTL Interface	V_{OL}			0.4	V	I_{OL} = 1.6mA
	CMOS Interface				0.8	V	I_{OL} = 400μA
Input leakage current	All inputs except DB_0−DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0−DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes: 1. TTL Interface ; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
C-MOS Interface ; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM
2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.
3. If the capacity loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface (HD63645 — 68 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
Enable cycle time	t_{CYCE}	500			ns	35
Enable pulse width (high)	P_{WEH}	220			ns	
Enable pulse width (low)	P_{WEL}	220			ns	
Enable rise time	t_{Er}			25	ns	
Enable fall time	t_{Ef}			25	ns	
$\overline{CS}$, RS, R/$\overline{W}$ setup time	t_{AS}	70			ns	
$\overline{CS}$, RS, R/$\overline{W}$ hold time	t_{AH}	10			ns	
DB_0-DB_7 setup time	t_{DS}	60			ns	
DB_0-DB_7 hold time	t_{DHW}	10			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

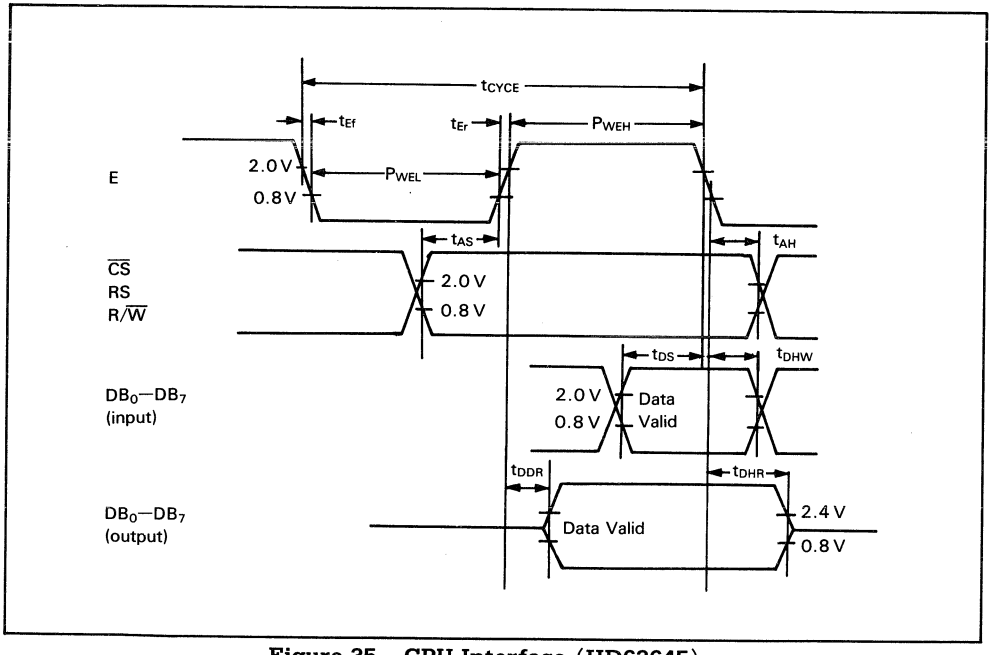


Figure 35. CPU Interface (HD63645)

CPU Interface (HD64645 — 80 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	36
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB_0-DB_7 setup time	t_{DSW}	100			ns	
DB_0-DB_7 hold time	t_{DHW}	0			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

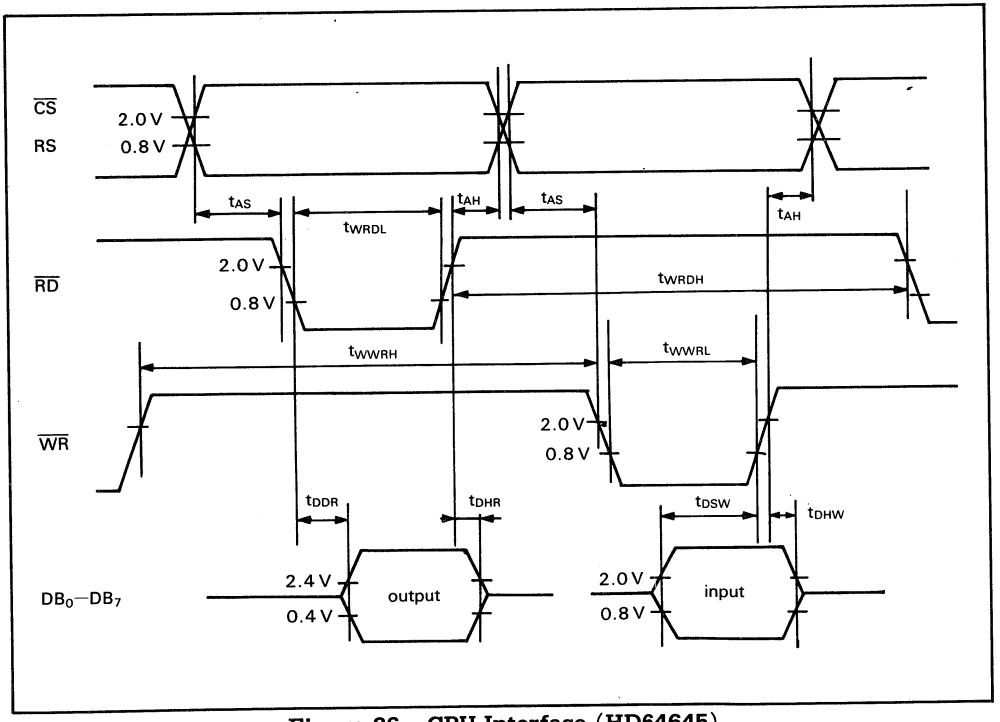


Figure 36. CPU Interface (HD64645)

AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100			ns	37
DCLK high level width	t_{WDH}	30			ns	
DCLK low level width	t_{WDL}	30			ns	
DCLK rise time	t_{Dr}			20	ns	
DCLK fall time	t_{Df}			20	ns	
MCLK delay time	t_{DMD}			60	ns	
MCLK rise time	t_{Mr}			30	ns	
MCLK fall time	t_{Mf}			30	ns	
MA0-MA15 delay time	t_{MAD}			150	ns	
MA0-MA15 hold time	t_{MAH}	10			ns	
RA0-RA4 delay time	t_{RAD}			150	ns	
RA0-RA4 hold time	t_{RAH}	10			ns	
DISPTMG delay time	t_{DTD}			150	ns	
DISPTMG hold time	t_{DTH}	10			ns	
CUDISP delay time	t_{CDD}			150	ns	
CUDISP hold time	t_{CDH}	10			ns	
CL1 delay time	t_{CL1D}			150	ns	
CL1 hold time	t_{CL1H}	10			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
MD0-MD15 setup time	t_{MDS}	30			ns	
MD0-MD15 hold time	t_{MDH}	15			ns	

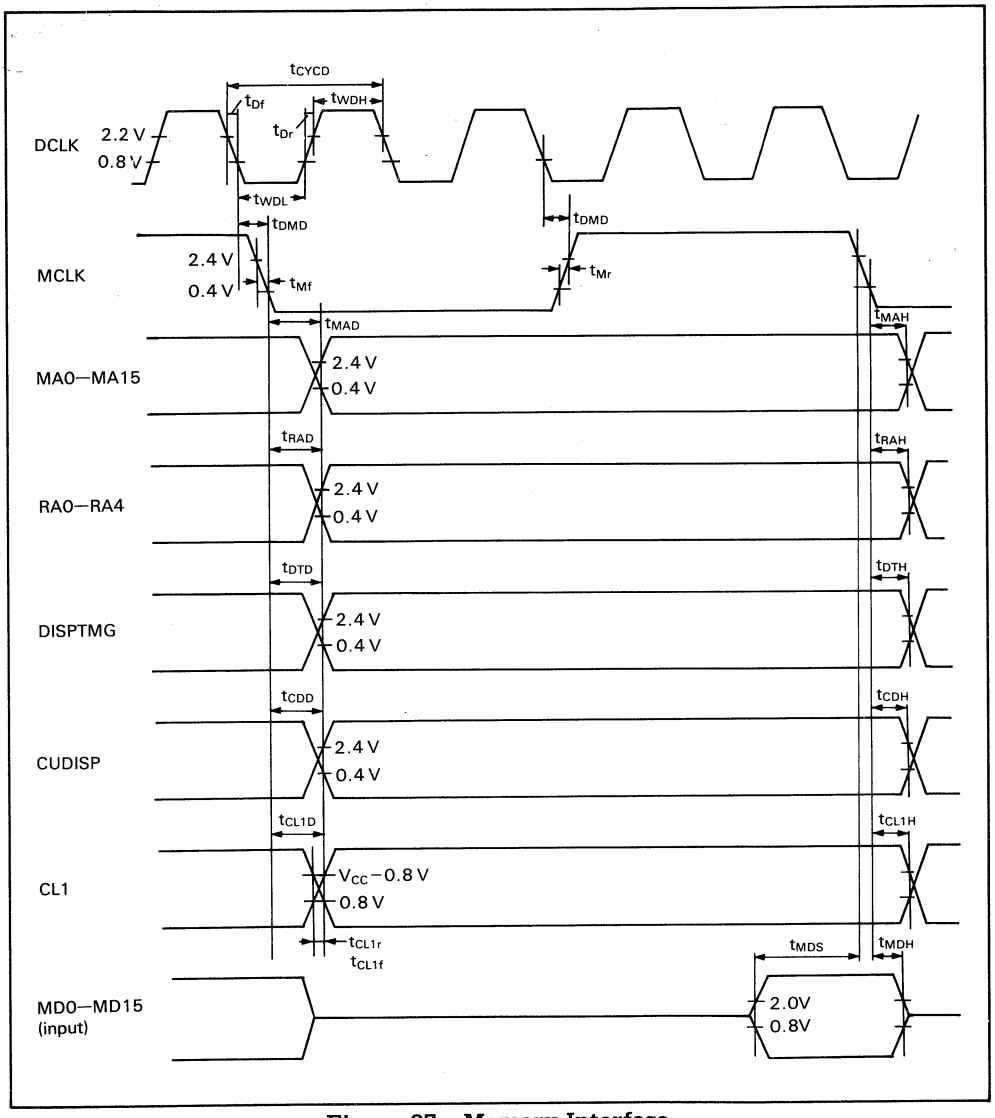


Figure 37. Memory Interface

AC Characteristics (Cont)

LCD Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
Display data setup time	t_{LDS}	50			ns	38
Display data hold time	t_{LDH}	100			ns	
CL2 high level width	t_{WCL2H}	100			ns	
CL2 low level width	t_{WCL2L}	100			ns	
FLM setup time	t_{FS}	500			ns	
FLM hold time	t_{FH}	300			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
CL2 rise time	t_{CL2r}			50	ns	
CL2 fall time	t_{CL2f}			50	ns	

Note : At fCL2 = 3 MHz

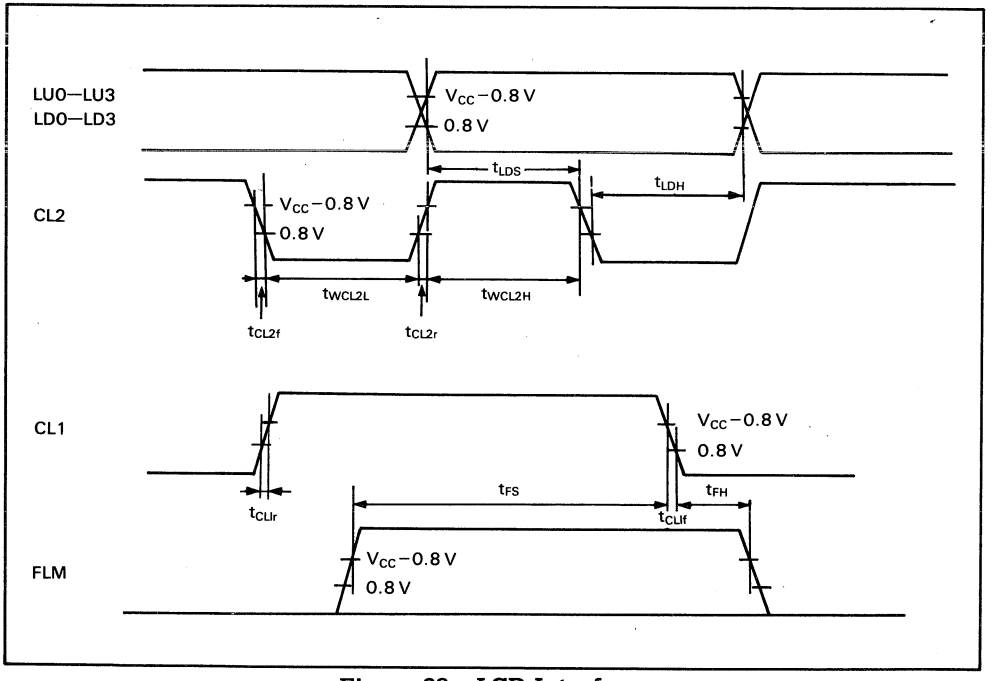
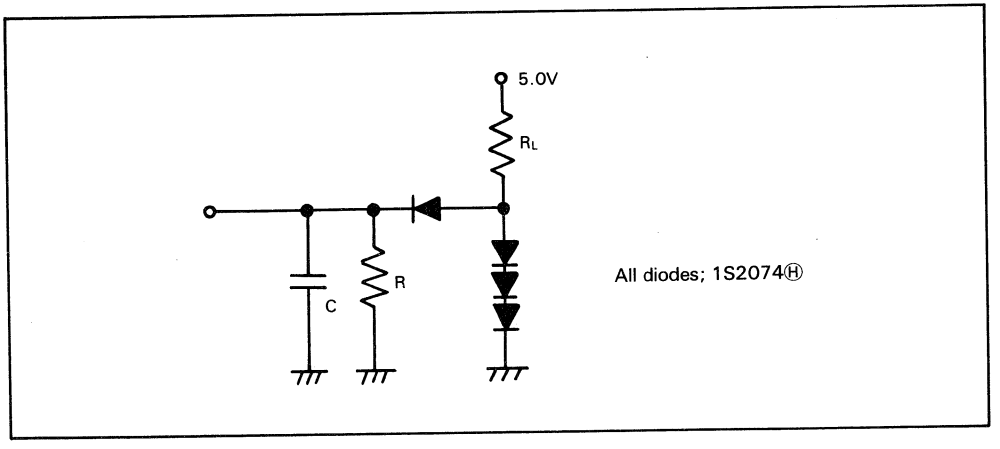


Figure 38. LCD Interface

AC Characteristics

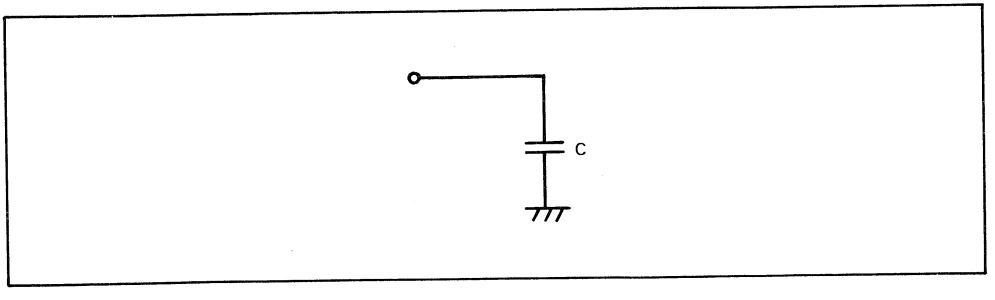
TTL Load

Terminal	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf : Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf : Specified



Capacity Load

Terminal	C	Remarks
CL2	150 pF	tr, tf : Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf : Not specified
FLM	50 pF	



Refer to user's manual (No. 68-1-160) and application note (No. ADE-502-003) for detail of this product.

HD64646

LCD Timing Controller (LCTC)

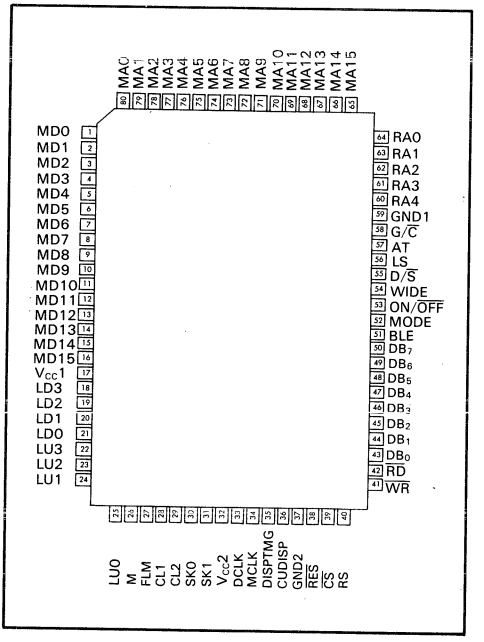
Description

The HD64646 LCTC is a modified version of the HD64645 LCTC with differente LCD interface timing.
The HD64646 is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Pin Arrangement



Features

- Software compatible with the HD6845 CRTC
- Programmable screen size:
  —Up to 1024 dots (height)
  —Up to 4096 dots (width)
- High-speed data transfer:
  —Up to 20 Mbits/sec in character mode
  —Up to 40 Mbits/sec in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font:
  —1-32 dots (height)
  —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical smooth scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver: HD61104 (column) and HD61105 (common), HD66106 and HD66107T (column/common)
- CPU interface:
  80 family
- CMOS process
- Single +5 V ±10%
- 80-pin plastic QFP (FP-80B)

Ordering Information

Type No.	Bus Timing	Bus Interface	Package
HD63645	2 MHz	68 System	FP-80
HD64645	4 MHz	80 System	FP-80
HD64646	4 MHz	80 System	FP-80B

Differences Between HD64645 and HD64646

Fig.1 and Fig.2 show the relation between display data transfer period, when display data shift clock CL2 changes, and display data latch clock CL1. Fig.1 shows the case without skew function and fig.2 shows the case with skew function.
In Fig.1 "High" period between CL2 and CL1 of HD64645 overlap.
HD64646 has no overlap like HD64645, and except for overlap parts HD64646 is the same as HD64645 functionally.
Besides, in case of skew function, phase relation between CL1 and CL2 changes. As Fig.2 shows, data transfer period and CL1 "High" period of HD64646 never overlap in case of skew function.

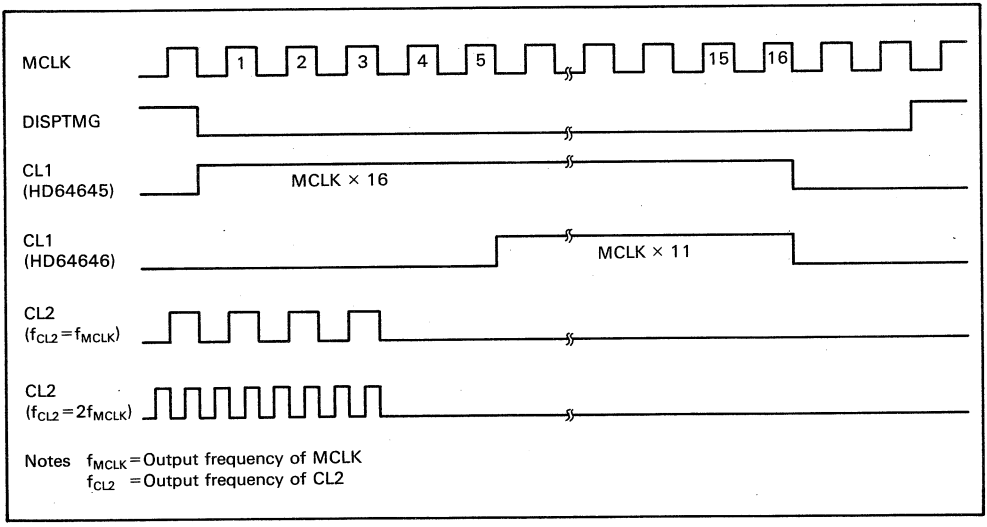


Figure 1. Differences between HD64645 and HD64646 (no skew)

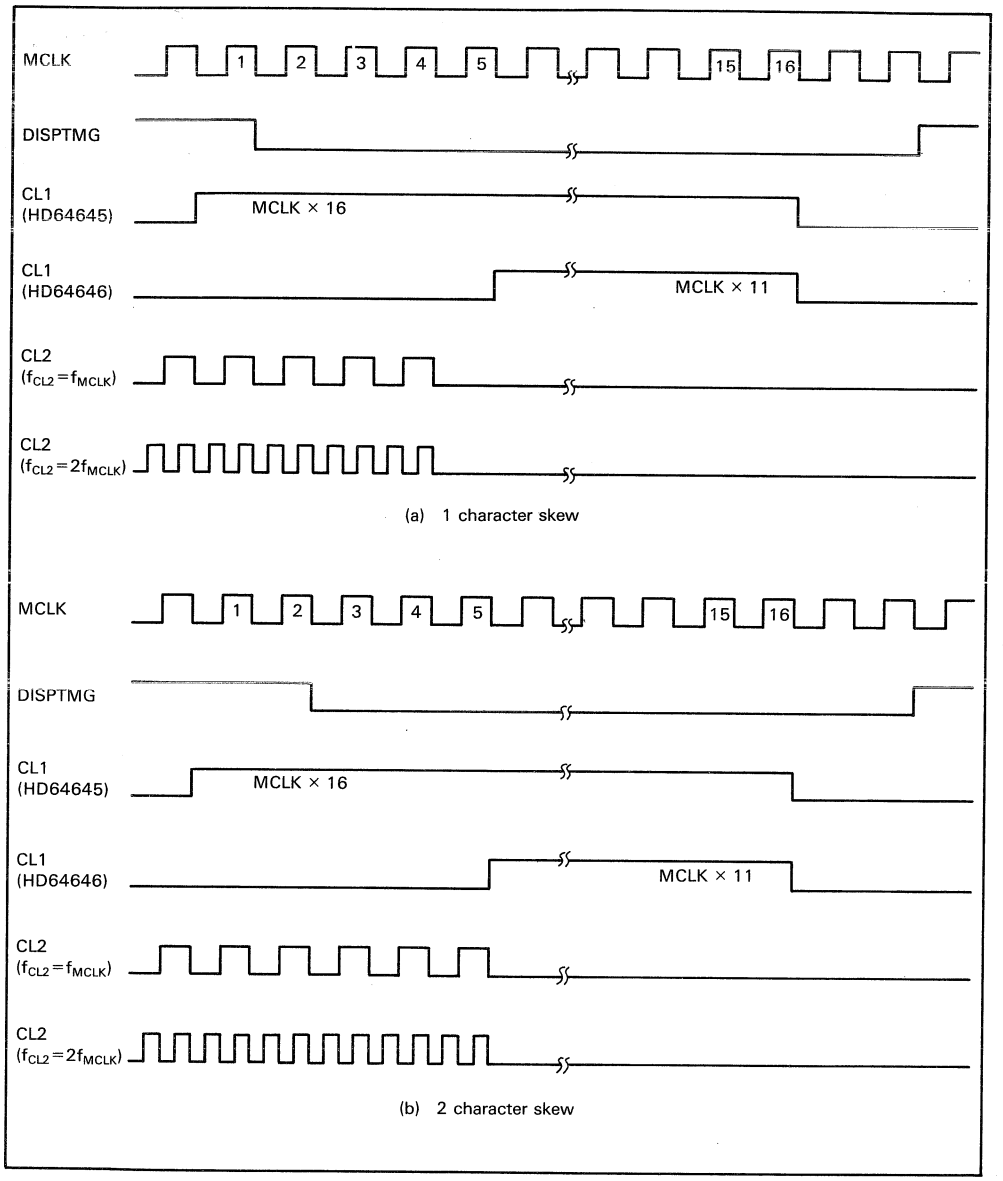


Figure 2. Differences between HD64645 and HD64646 (skew)

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes : 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.
2. With respect to GROUND (GND = 0 V)

Electrical Characteristics

DC characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$, MODE, SK0, SK1	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V	
	DCLK, ON/$\overline{OFF}$		2.2		V_{CC}+0.3	V	
	All others		2.0		V_{CC}+0.3	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL Interface[1]	V_{OH}	2.4			V	I_{OH} = −400μA
	CMOS Interface[1]		V_{CC}−0.8			V	I_{OH} = −400μA
Output low voltage	TTL Interface	V_{OL}			0.4	V	I_{OL} = 1.6mA
	CMOS Interface				0.8	V	I_{OL} = 400μA
Input leakage current	All inputs except DB_0−DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0−DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes : 1. TTL Interface ; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
C-MOS Interface ; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM
2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.
3. If the capacity loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	3
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB_0-DB_7 setup time	t_{DSW}	100			ns	
DB_0-DB_7 hold time	t_{DHW}	0			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

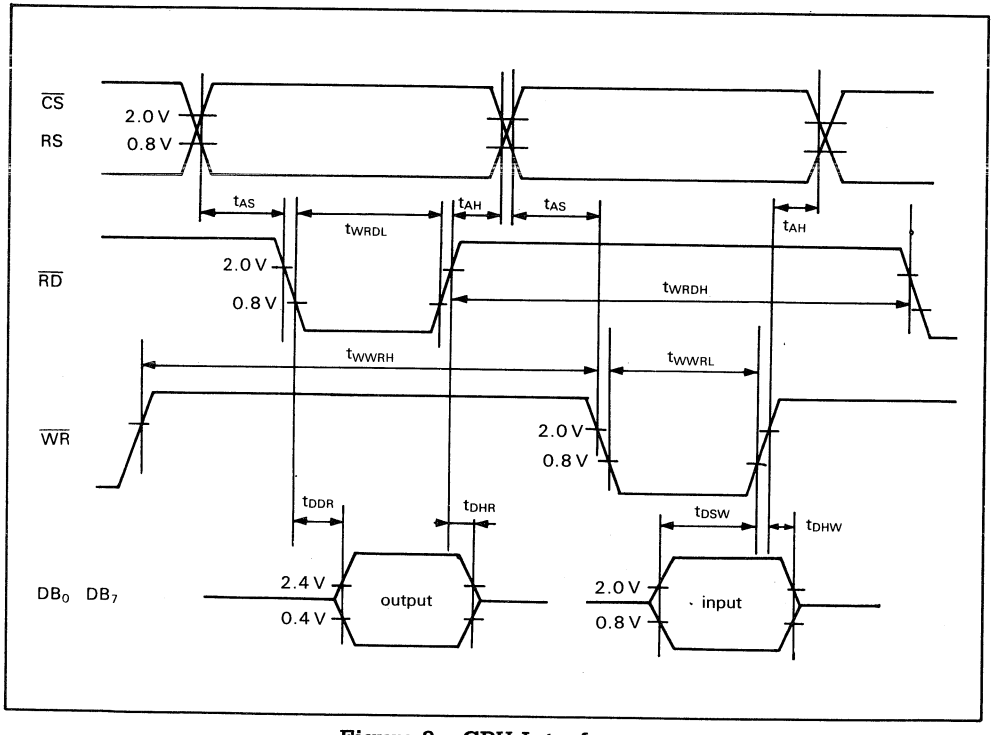


Figure 3. CPU Interface

AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100			ns	4
DCLK high level width	t_{WDH}	30			ns	
DCLK low level width	t_{WDL}	30			ns	
DCLK rise time	t_{Dr}			20	ns	
DCLK fall time	t_{Df}			20	ns	
MCLK delay time	t_{DMD}			60	ns	
MCLK rise time	t_{Mr}			30	ns	
MCLK fall time	t_{Mf}			30	ns	
MA0-MA15 delay time	t_{MAD}			150	ns	
MA0-MA15 hold time	t_{MAH}	10			ns	
RA0-RA4 delay time	t_{RAD}			150	ns	
RA0-RA4 hold time	t_{RAH}	10			ns	
DISPTMG delay time	t_{DTD}			150	ns	
DISPTMG hold time	t_{DTH}	10			ns	
CUDISP delay time	t_{CDD}			150	ns	
CUDISP hold time	t_{CDH}	10			ns	
CL1 delay time	t_{CL1D}			150	ns	
CL1 hold time	t_{CL1H}	10			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
MD0-MD15 setup time	t_{MDS}	30			ns	
MD0-MD15 hold time	t_{MDH}	15			ns	

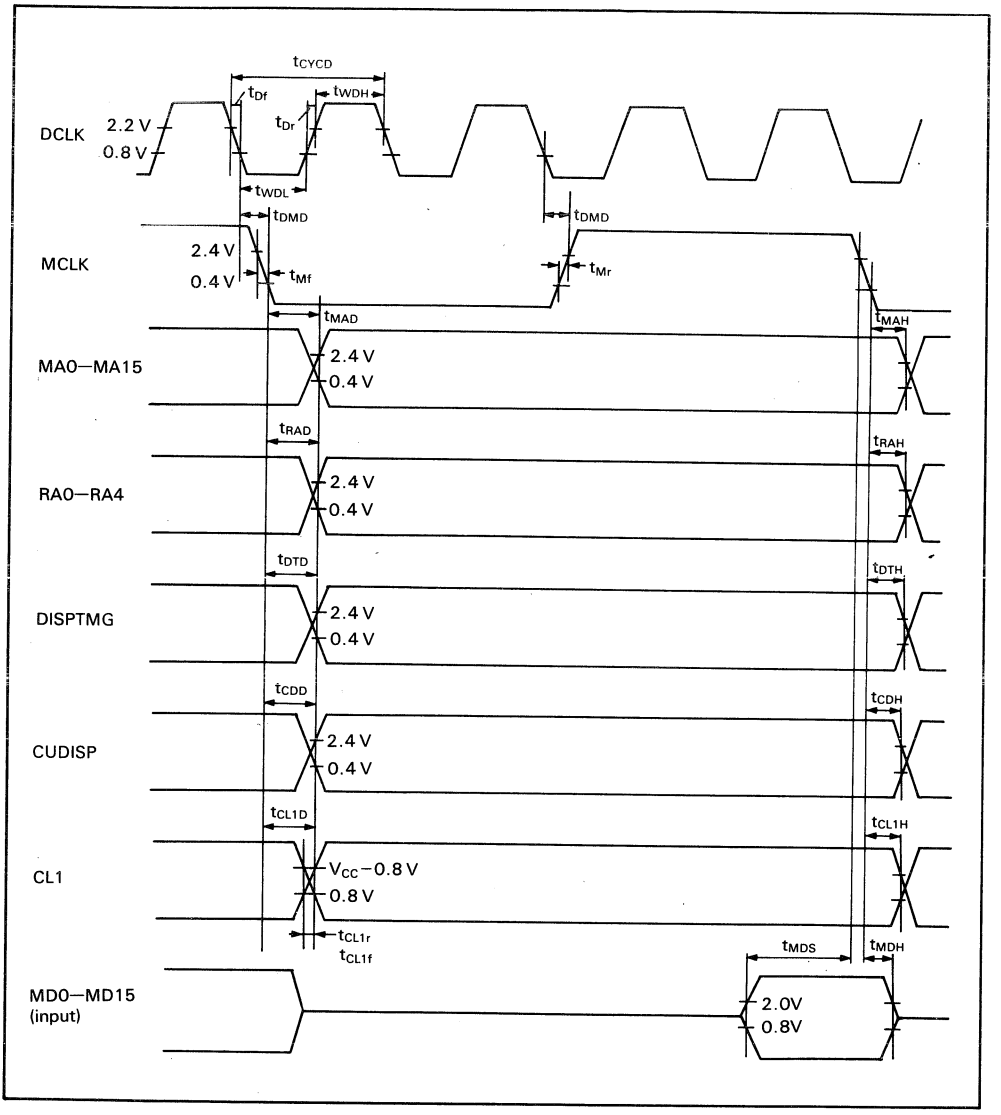


Figure 4. Memory Interface

AC Characteristics (Cont)

LCD Interface 1 (at f_{CL2}=3MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM stetup time	t_{Fs}	500	–	–	ns	5
FLM hold time	t_{FH}	300	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	100	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	100	–	–	ns	
CL2 low level width	t_{CL2L}	100	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	80	–	–	ns	
Display data hold time	t_{LDH}	100	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

LCD Interface 2 (at f_{CL2}=5MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{Fs}	500	–	–	ns	5
FLM hold time	t_{FH}	200	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	70	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	50	–	–	ns	
CL2 low level width	t_{CL2L}	50	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	30	–	–	ns	
Display data hold time	t_{LDH}	30	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

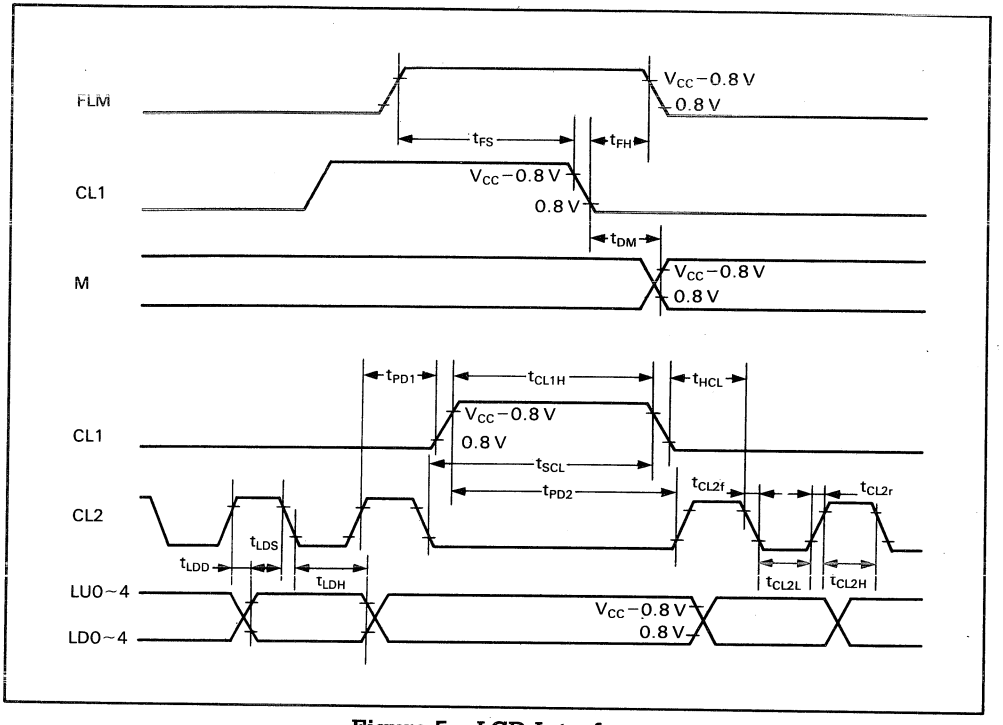
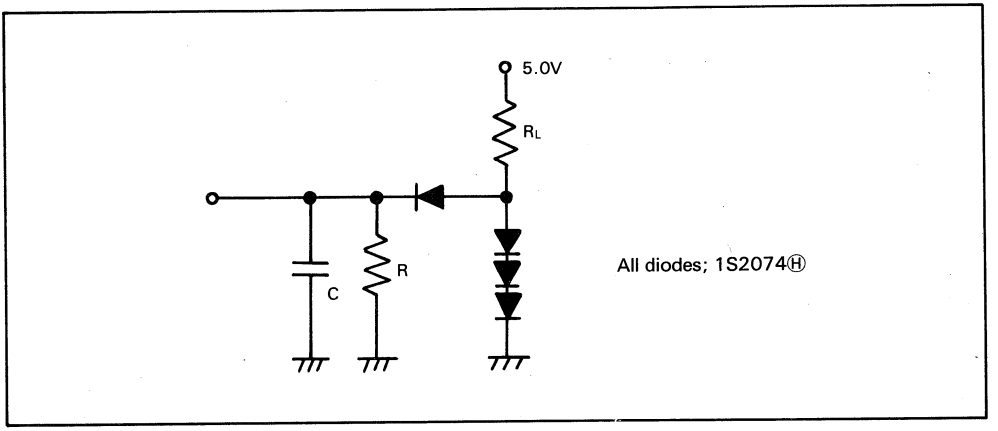


Figure 5. LCD Interface

AC Characteristics

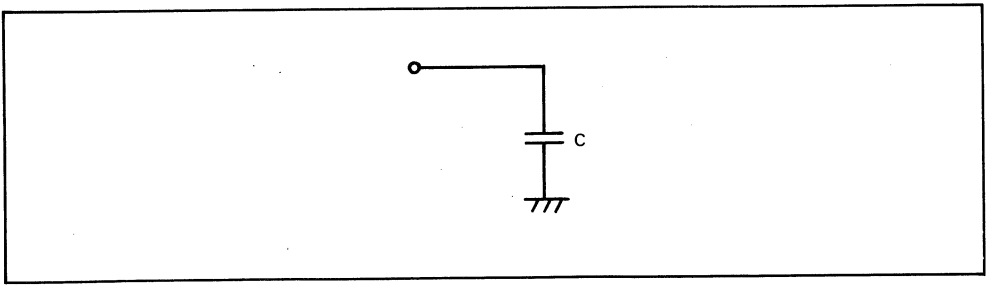
TTL Load

Terminal	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf : Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf : Specified



Capacity Load

Terminal	C	Remarks
CL2	150 pF	tr, tf : Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf : Not specified
FLM	50 pF	



Refer to user's manual (No. 68-1-160) and application note (No. ADE-502-003) for detail of this product.

HD66840

LCD Video Interface Controller (LVIC)

Description

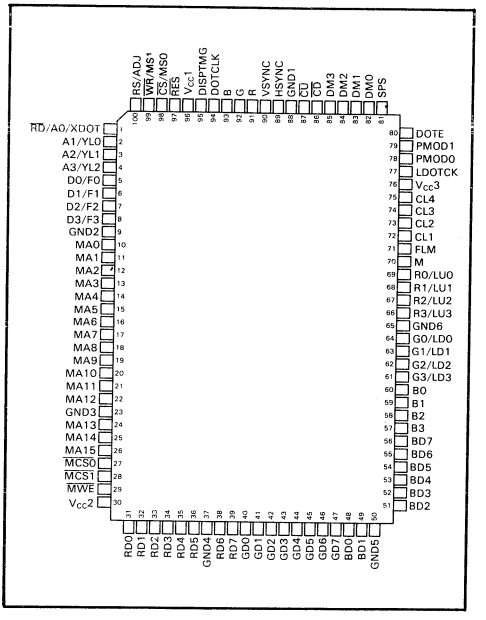
The HD66840 LVIC interface controller converts the standard video signals R, G, B for CRT display into LCD data. It enables a CRT display system to be replaced by an LCD system without any changes. It also enables the software originally intended for CRT display to control the LCD.

Since the LVIC can control TFT-type LCDs in addition to the current TN-type LCD, it can support color display as well as monochrome display. It can program screen size and can control a large-panel LCD of 720 dots × 512 dots (max).

Features

- Converts video R, G, B signals for CRT display into LCD data:
  - —Monochrome display data
  - —8-level gray scale display data
  - —8-color display data
- Can select LVIC control method:
  - —Pin programming method
  - —Internal register programming method (either with MPU or ROM)
- Can program screen size:
  - —200, 350, 400, 480, 512, or 540 dots (lines) in height and 640, or 720 dots (80, or 90 characters) in width by pin programming method
  - —4-1024 dots (lines) in height and 32-4048 dots (4-506 characters) in width by internal register programming method
- Can regenerate the display timing signal from HSYNC and VSYNC
- Internal PLL circuit can generate the dot clock (external charge pump, low pass filter (LPF), and voltage-controlled oscillator (VCO) required)
- Can control both TN-type LCD and TFT-type LCD
- Maximum operating frequency: 25, 30 MHz (dot clock for CRT display)
- LCD driver interface: 4-, 8-, or 12-bit (4 bits each for R, G, B) parallel data transfer
- Recommended LCD drivers: HD61104 (column) and HD61105 (common), HD66106 and HD66107T (column/common)
- CMOS 1.3 μm process
- Single power supply: +5 V ± 10 %
- 100-pin plastic QFP (FP-100A)

Pin Arrangement



HITACHI

Pin Description

Table 1 describes the pins.

Table 1. Pin Description

Symbol	Pin Number	Pin Name	I/O
$V_{CC}1$-$V_{CC}3$	96, 30, 76	$V_{CC}1$, V_{CC} 2, V_{CC} 3	—
GND1-GND6	88, 9, 23, 37, 50, 65	Ground 1-6	—
R, G, B[1]	91, 92, 93	Red, green, blue serial data	I
HSYNC	89	Horizontal synchronization	I
VSYNC	90	Vertical synchronization	I
DISPTMG[2]	95	Display timing	I
DOTCLK	94	Dot clock	I
R0-R3[3]	69-66	LCD red data 0-3	O
LU0-LU3[4]	69-66	LCD up panel data 0-3	O
G0-G3[3,5]	64-61	LCD green data 0-3	O
LD0-LD3[4,5]	64-61	LCD down panel data 0-3	O
B0-B3[3,6]	60-57	LCD blue data 0-3	O
CL1	72	LCD data line clock	O
CL2	73	LCD data shift clock	O
CL3[7]	74	Y-driver shift clock 1	O
CL4[7]	75	Y-driver shift clock 2	O
FLM	71	First line marker	O
M	70	LCD driving signal alternation	O
LDOTCK	77	LCD dot clock	I
$\overline{MCS0}$, $\overline{MCS1}$[8]	27, 28	Memory chip select 0, 1	O
$\overline{MWE}$[9]	29	Memory write enable	O
MA0-MA15[9]	10-22, 24-26	Memory address 0-15	O
RD0-RD7[9]	31-36, 38-39	Memory red data 0-7	I/O
GD0-GD7[9,10]	40-47	Memory green data 0-7	I/O
BD0-BD7[9,10]	48, 49 51-56	Memory blue data 0-7	I/O

Ordering Information

Type No.	Dot clock (MHz)	Package
HD66840F25	25MHz	100-pin
HD66840F30	30MHz	Plastic QFP (FP-100A)

Table 1. Pin Description (cont)

Symbol	Pin Number	Pin Name	I/O
PMOD0, PMOD1	78, 79	Program mode 0, 1	I
DOTE	80	Dot clock edge change	I
SPS	81	Synchronization polarity select	I
DM0-DM3	82-85	Display mode 0-3	I
$\overline{CS}$ (MPU programming)[11]	98	Chip select	I
$\overline{MS0}$ (pin programming)[11]	98	Memory select 0	I
$\overline{WR}$ (MPU programming)[11,12]	99	Write	I
MS1 (pin programming)[11]	99	Memory select 1	I
$\overline{RD}$ (MPU programming)[12]	1	Read	I
A0 (ROM programming)	1	Address 0	O
XDOT (pin programming)	1	X-dot	I
RS (MPU programming)[11]	100	Register select	I
ADJ (pin programming)[11]	100	Adjust	I
D0-D3 (MPU programming)	5-8	Data 0-3	I/O
D0-D3 (ROM programming)	5-8	Data 0-3	I
F0-F3 (pin programming)	5-8	Fine adjust 0-3	I
A1-A3 (ROM programming)[13]	2-4	Address 1-3	O
YL0-YL2 (pin programming)[13]	2-4	Y-line 0-2	I
$\overline{RES}$[14]	97	Reset	I
$\overline{CD}$	86	Charge down	O
$\overline{CU}$	87	Charge up	O

Notes: 1. When CRT display data is monochrome, G and B pins should be fixed low.
2. Fix high or low when regenerating the display timing signal internally.
3. For 8-color display modes.
4. For monochrome and 8-level gray scale display modes.
5. Leave disconnected in 4-bit/single screen data transfer modes.
6. Leave disconnected in monochrome and 8-level gray scale display modes.
7. Leave disconnected when controlling TN-type LCD.
8. Leave disconnected when using no buffer memories.
9. Leave disconnected when using no buffer memories.
10. In monochrome display modes, the LVIC writes the OR of R, G, B signals into R-plane RAMs. Thus, no RAMs are required for G and B planes in these modes.
Pull up these pins 20-kΩ resistance. If G and B plane RAMs are connected in monochrome display modes, the LVIC writes G and B signals into each RAM. However, it does not affect the display or the contents of R-plane RAM whether G- and B-plane RAMs are connected or not.
11. Fix high or low when controlling the LVIC by ROM programming method.
12. $\overline{WR}$ and $\overline{RD}$ must not be low at the same time.
13. Fix high or low when controlling the LVIC by MPU programming method.
14. Make sure to input $\overline{RES}$ signal after power-on.

Power Supply

$V_{CC}1$-$V_{CC}3$: Connect $V_{CC}1$-$V_{CC}3$ with +5 V.

GND1-GND6: Ground GND1-GND6.

CRT Display Interface

R, G, B: Input CRT display R, G, B signals on R, G and B respectively.

HSYNC: Input the CRT horizontal synchronization on HSYNC.

VSYNC: Input the CRT vertical synchronization on VSYNC.

DISPTMG: Input the display timing signal, which announces the horizontal or vertical display period, on DISPTMG.

DOTCLK: Input the dot clock for CRT display on DOTCLK.

LCD Interface

R0-R3: R0-R3 output R data for the LCD.

LU0-LU3: LU0-LU3 output LCD up panel data.

G0-G3: G0-G3 output G data for LCD.

LD0-LD3: LD0-LD3 output LCD down panel data.

B0-B3: B0-B3 output B data for LCD.

CL1: CL1 outputs the line select clock for LCD data.

CL2: CL2 outputs the shift clock for LCD data.

CL3: CL3 outputs the line select and shift clock when a Y-driver is set on one side of an LCD screen (see "LCD System Configuration").

CL4: CL4 outputs the line select and shift clock when Y-drivers are set on both sides of an LCD screen (see "LCD System Configuration").

FLM: FLM outputs the first line marker for a Y-driver.

M: The M output signal converts the LCD drive signal to AC.

LDOTCK: LDOTCK outputs the LCD dot clock.

Buffer Memory Interface

$\overline{MCS0}$, $\overline{MCS1}$: $\overline{MCS0}$ and $\overline{MCS1}$ output the buffer memory chip select signal.

$\overline{MWE}$: $\overline{MWE}$ outputs the write enable signal of buffer memories.

MA0-MA15: MA0-MA15 output buffer memory addresses.

RD0-RD7: RD0-RD7 transfer data between R data buffer memory and the LVIC.

GD0-GD7: GD0-GD7 transfer data between G data buffer memory and the LVIC.

BD0-BD7: BD0-BD7 transfer data between B data buffer memory and the LVIC.

Mode Setting

PMOD0, PMOD1: The PMOD0-PMOD1 input signals select a programming method (table 6).

DOTE: The DOTE input signal switches the timing of the data latch. The LVIC latches R, G, B signal at the falling edge of DOTCLK when DOTE is high, and at the rising edge when low.

SPS: The SPS input signal selects the polarity of VSYNC. (The polarity of HSYNC is fixed.) VSYNC is high active when SPS is high, and low active when low.

DM0-DM3: The DM0-DM3 input signals select a display mode (table 8).

MS0-MS1: The MS0-MS1 input signals select the kind of buffer memories (table 2).

XDOT: The XDOT input signal specifies the number of horizontal displayed characters. The number is 90 when XDOT is high, and 80 when low.

YL0-YL2: The YL0-YL2 input signals specify the number of vertical displayed lines (table 3).

ADJ: The ADJ input signal determines whether F0-F3 pins adjust the number of vertical displayed lines or the display timing signal. F0-F3 pins adjust the display timing signal when ADJ is high, and adjust the number of vertical displayed lines when low.

F0-F3: F0-F3 input data for adjusting the number of vertical displayed lines (table 4), or the display timing signal (see "Fine

Adjustment of Display Timing Signal").

MPU Interface

$\overline{CS}$: The MPU selects the LVIC when $\overline{CS}$ is low.

$\overline{WR}$: The MPU inputs the $\overline{WR}$ write signal to write data into internal registers of the LVIC. The MPU can write data when $\overline{WR}$ is low and cannot write data when high.

$\overline{RD}$: The MPU inputs the $\overline{RD}$ read signal to read data from internal registers of the LVIC. The MPU can read data when $\overline{RD}$ is low and cannot read data when high.

RS: The MPU inputs the RS signal together with $\overline{CS}$ to select internal registers. The MPU selects data registers (R0-R15) when RS is high and $\overline{CS}$ is low, and selects the address register (AR) when RS is low and $\overline{CS}$ is low.

D0-D3: D0-D3 transfer internal register data between the MPU and LVIC.

$\overline{RES}$: $\overline{RES}$ inputs the external reset signal.

ROM Interface

A0-A3: A0-A3 output address 0 to address 3 to an external ROM.

D0-D3: D0-D3 input data from an external ROM to internal registers.

PLL Circuit Interface

$\overline{CD}$: $\overline{CD}$ outputs the charge down signal to an external charge pump.

$\overline{CU}$: $\overline{CU}$ outputs the charge up signal to an external charge pump.

Table 2. Memory Type and MS1, MS0 Pins

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbyte memory
1	0	32-kbyte memory
1	1	64-kbyte memory

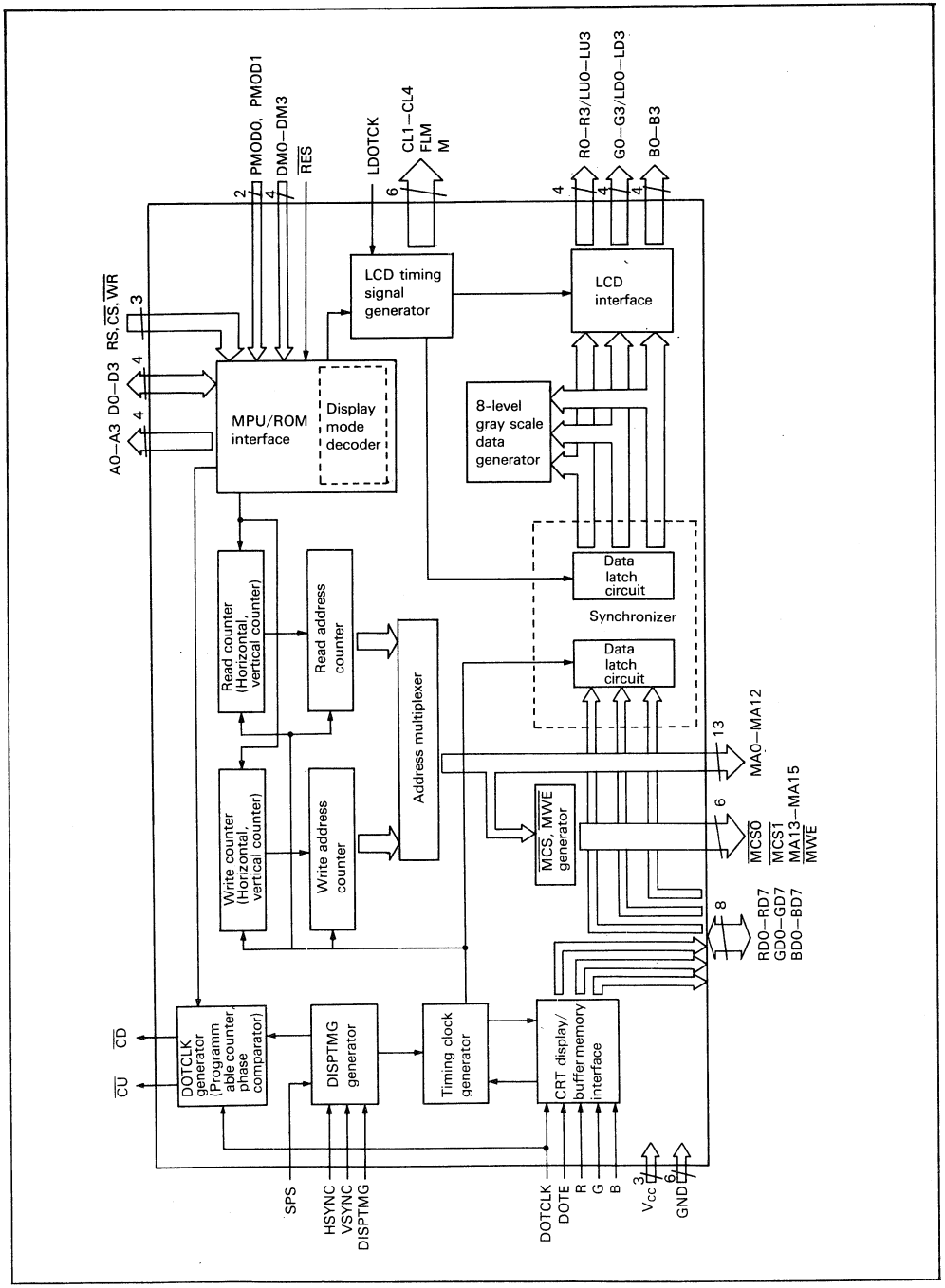
Table 3. Number of Vertical Displayed Lines and YL0-YL2 Pins

YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Prohibited
1	1	1	

Table 4. Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Lines Adjusted
0	0	0	0	± 0
0	0	0	1	+ 1
0	0	1	0	+ 2
⋮	⋮	⋮	⋮	⋮
1	1	1	0	+ 14
1	1	1	1	+ 15

Internal Block Diagram



Registers

Table 5 lists the internal registers and figure 1 illustrates the bit assignment to the registers.

Table 5. Register List

$\overline{CS}$	RS	Address Register 3	2	1	0	Reg. No.	Register Name	Program Unit	Read/ Write
1	—	—	—	—	—	—	Invalid	—	—
0	0	—	—	—	—	AR	Address register[1]	—	W
0	1	0	0	0	0	R0	Control register 1	—	R/W
0	1	0	0	0	1	R1	Control register 2	—	R/W
0	1	0	0	1	0	R2	Vertical displayed lines register (middle-order)[2]	Line	R/W
0	1	0	0	1	1	R3	Vertical displayed lines register (low-order)[2]	Line	R/W
0	1	0	1	0	0	R4	Vertical displayed lines register (high-order)[2]	Line	R/W
							CL3 period register (high-order)[3]	Char	R/W
0	1	0	1	0	1	R5	CL3 period register (low-order)[3]	Char	R/W
0	1	0	1	1	0	R6	Horizontal displayed characters register (high-order)[4]	Char	R/W
0	1	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Char	R/W
0	1	1	0	0	0	R8	CL3 pulse width register	Char	R/W
0	1	1	0	0	1	R9	Fine adjust register[5]	Dot	R/W
0	1	1	0	1	0	R10	PLL frequency-dividing ratio register (high-order)[6]	—	R/W
0	1	1	0	1	1	R11	PLL frequency-dividing ratio register (low-order)[6]	—	R/W
0	1	1	1	0	0	R12	Vertical backporch register (high-order)[2,7]	Line	R/W
0	1	1	1	0	1	R13	Vertical backporch register (low-order)[2,7]	Line	R/W
0	1	1	1	1	0	R14	Horizontal backporch register (high-order)[2,7]	Dot	R/W
0	1	1	1	1	1	R15	Horizontal backporch register (low-order)[2,7]	Dot	R/W

Notes: 1. If you attempt to read data from the register with RS = 0, the bus is driven to high-impedance state and the output data is indefinite.
2. (The specified value − 1) should be written into these registers.
3. Valid only in 8-color display modes with horizontal stripes.
4. The most significant bit is invalid in dual screen configuration modes.
5. Valid only when the display timing signal is supplied externally.
6. Valid only when generating the dot clock.
7. Valid only when generating the display timing signal internally.

Register No.	Data Bit 3	2	1	0	
—					
AR	Address register				
R0			DSP	DCK	← Control register 1
R1	MC	DON	MS1	MS0	← Control register 2
R2	Vertical displayed				
R3	lines register				
R4					
R5	CL3 period register				
R6	Horizontal displayed				
R7	characters register				
R8	CL3 pulse width register				
R9	Fine adjust register				
R10	PLL frequency-				
R11	dividing ratio register				
R12	Vertical Backporch				
R13	register				
R14	Horizontal Backporch				
R15	register				

Note: ▨ indicates invalid bits. Attempting to read data from these register bits returns indefinite output data.

Figure 1. Register Bit Assignment

System Configuration

Figure 2 is the block diagram of a system in which the LVIC is used outside of a personal computer.

The LVIC converts the R, G, B serial data sent from the personal computer into parallel data and writes them into the buffer memories once. It reads out the data in turn and outputs them to LCD drivers to drive an LCD. Here the latch clock of the serial data, namely the dot clock (DOTCLK) is generated by a PLL circuit, using HSYNC as a basic clock. The frequency of the dot clock is specified by the PLL frequency-dividing ratio register (R10, R11).

The user may also configure a system without VCO and LPF if supplying the dot clock externally and may configure a system without the MPU if the LVIC is controlled by the pin programming method.

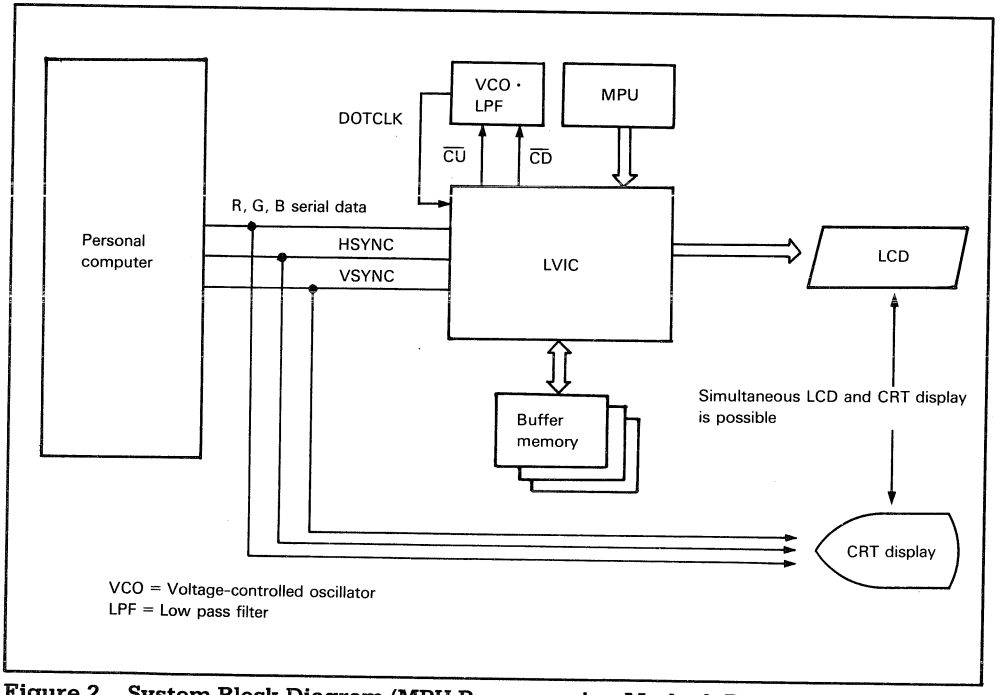


Figure 2. System Block Diagram (MPU Programming Method, Regenerates DOTCLK)

Functional Description

Programming Method

The user may select one of two methods to control the LVIC functions: by pin programming method or by internal registers (internal register programming method). The internal register programming method can be divided into the MPU programming method and the ROM programming method. The MPU writes data into internal registers in the MPU programming method and ROM writes the data in the ROM programming method. Table 6 lists the relation between programming method and pins.

Pin Programming Method: LVIC mode setting pins control functions in the pin programming method.

Internal Register Programming Method: In the internal register programming method, an MPU or ROM writes data into internal registers to control functions. Figure 3 illustrates the connections of MPU or ROM and the LVIC. Figure 3 (1) is an example of using a 4-bit microprocessor, but since the LVIC's MPU bus is compatible with the 4-MHz 80-family controller bus, it can also be connected directly with the bus of host MPU.

Table 6. Programming Method Selection

Pins			
PMOD1	**PMOD0**	**Programming Method**	
0	0	Pin programming	
0	1	Internal register Programming	With MPU
1	0		With ROM
1	1	Prohibited (Note)	

Note: This combination is for a test mode and disables display.

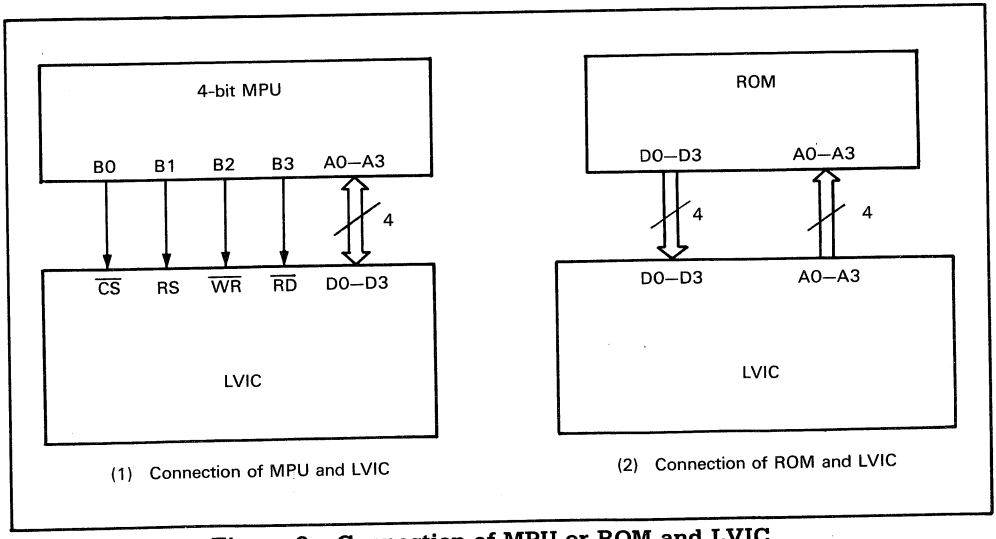


Figure 3. Connection of MPU or ROM and LVIC

Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, the user may select either 640 dots or 720 dots (80 characters or 90 characters) as the number of horizontal displayed characters with the XDOT pin, and 200, 350, 400, 480, 512, or 540 lines as the number of vertical displayed lines with YL2-YL0 pins. The number of vertical displayed lines can be adjusted with ADJ and F3-F0 pins within +0 to +15 lines.

In the internal register programming method, the user may select any even number from 32 dots to 4048 dots (= 4 characters up to 506 characters) with the horizontal displayed characters register (R6, R7), and any even number from 4 lines up to 1028 lines with the vertical displayed lines register (R2, R3 and the high-order two bits of R4). However, odd number of lines can also be selected when screen configuration is single and a Y-driver (scan driver) is set on one side of an LCD screen.

Figure 4 illustrates the relation between an LCD screen and pins and internal registers controlling screen size.

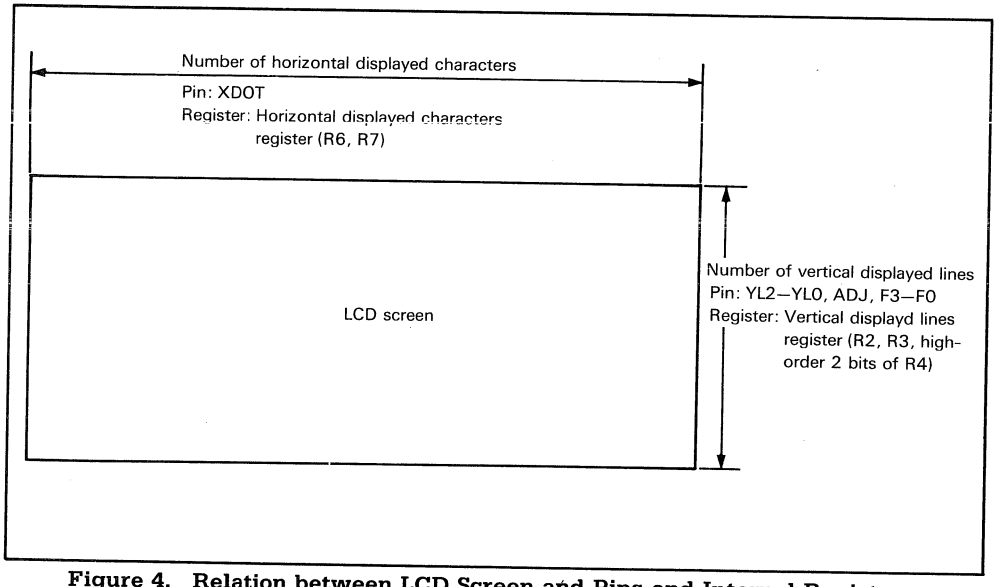


Figure 4. Relation between LCD Screen and Pins and Internal Registers

Memory Selection

The user may select 8-, 32-, or 64-kbyte SRAMs as buffer memory for the LVIC. Since the LVIC has a chip selector for these memories, no external decoder is required. The user selects the memory with pins MS1 and MS0 or with data bits MS1 and MS0 of the control register 2 (R1). Table 7 lists the kinds of memories and pin address assignments.

Memory capacity required depends on screen size and can be obtained with the following expression:

Memory capacity (bytes) = Nhd × Nvd

Nhd: number of horizontal displayed characters

Nvd: number of vertical displayed lines

For example, the screen of 640 × 200 dots requires 16-kbyte memory capacity since 80 characters × 200 lines is 16 kbytes. (8 dots compose a character.)
Therefore, each plane needs two HM6264s, which has 8-kbyte memory capacity, in 8-level gray scale display modes. Conncet $\overline{MCS0}$ with one of the memories of each plane and $\overline{MCS1}$ with the other (figure 5 (a)).,

When the screen size is 640 × 400 dots, 32-kbyte memory capacity is required (figure 5 (b)).
Therefore, each plane needs a HM62256, which has 32-kbyte memory capacity.
Connect $\overline{MCS0}$ with $\overline{CS}$ of the memories here.

Table 7. Memories and Pin Address Assignment

Pins or Bits					
MS1	**MS0**	**Memory**	**Address Output Pins**	**Chip Select Pins**	**Address Assignment**
0	0	No memory[1]	—	—	—
0	1	8-kbyte	MA0-MA12	$\overline{MCS0}$	$0000-$1FFF
				$\overline{MCS1}$	$2000-$3FFF
				MA13	$4000-$5FFF
				MA14	$6000-$7FFF
				MA15	$8000-$9FFF
1	0	32-kbyte	MA0-MA14	$\overline{MCS0}$	$00000-$07FFF
				$\overline{MCS1}$	$08000-$0FFFF
				MA15	$10000-$17FFF
1	1	64-kbyte	MA0-MA15	$\overline{MCS0}$	$00000-$0FFFF
				$\overline{MCS1}$	$10000-$1FFFF

Note: 1. There are some limitations when the user uses no memory. Refer to "User Precautions."

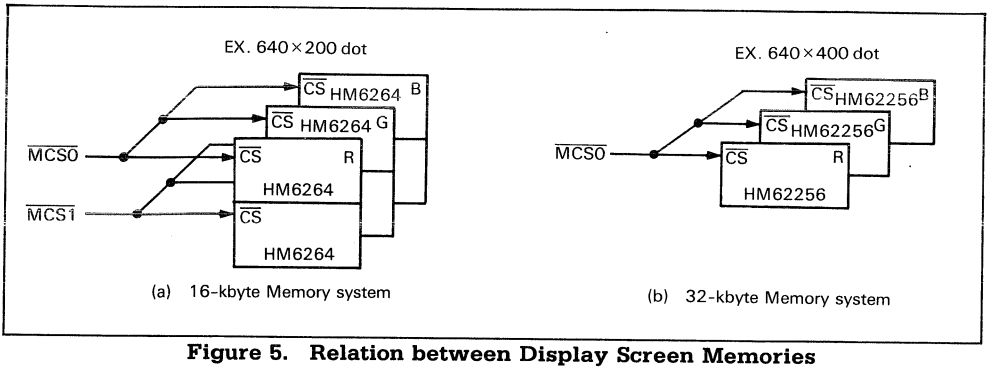


Figure 5. Relation between Display Screen Memories

Display Modes

The LVIC supports 16 display modes, depending on the state of the DM3-DM0 pins. The display mode consists of display color, type of LCD data output, how to set LCD drivers around an LCD screen, how to arrange color data (= type of stripes), and how to output M signal (= type of alternating signal). Table 8 lists display modes.

Table 8. Modes List

Mode	Pins				Display	LCD Data Output		LCD Driver Setting			
						Data	Screen				
No.	DM3	DM2	DM1	DM0	Color	Transfer	Config.	X-Driver[2]	Y-Driver[3]	Stripe[4]	Alternating
1	0	0	0	0	Monochrome	4-bit	Dual	One side	One side	—	Per frame
2	0	0	0	1			Single				
3[1]	0	0	1	0					Both sides		
4	0	0	1	1		8-bit			One side		
5[1]	0	1	0	0					Both sides		
6	0	1	0	1	8-level	4-bit	Dual		One side		
7	0	1	1	0	gray scale		Single				
8	0	1	1	1		8-bit					
9[1]	1	0	0	0	8-color	12-bit				Vertical	Per line
10[1]	1	0	0	1		(4 bits			Both sides		
11[1]	1	0	1	0		for R,G,B		Both sides	One side		
12[1]	1	0	1	1		each)			Both sides		
13[1]	1	1	0	0				One side	One side	Horizontal	
14[1]	1	1	0	1					Both sides		
15[1]	1	1	1	0				Both sides	One side		
16[1]	1	1	1	1					Both sides		

Notes: 1. For TFT-type LCD.
2. Data output driver
3. Scan driver
4. Refer to "Display Color, 8-Color Display."

Display Color

The LVIC converts R, G, B, the color data for CRT display, into the monochrome, 8-level gray scale, or 8-color display data.

Monochrome Display (Mode 1 to Mode 5): In monochrome modes 1-5, the LVIC displays two colors, namely black (= display on) and white (= display off). As shown in table 9, the OR of CRT display R, G, B data determines the display color.

8-Level Gray Scale Display (Mode 6 to Mode 8): In 8-level gray scale modes 6-8, the LVIC thins out data on certain lines to display an 8-level gray scale according to CRT display color (luminosity). Table 10 shows the relation between CRT display color (luminosity) and LCD color (contrast).

8-Color Display (Mode 9 to Mode 16): In 8-color modes 9-16, the LVIC displays 8 colors with red (R), green (G), and blue (B) filters on liquid crystal cells. The eight colors are the same as those provided by CRT display. As illustrated in figure 5, 8-color display has of two stripe modes: horizontal stripe mode and vertical stripe mode. In the former mode, the LVIC arranges R, G, B data horizontally, with horizontal filters. In the latter mode, the LVIC arranges R, G, B data vertically, with vertical filters. Three cells express a dot in both modes.

Table 9. Monochrome Display

CRT Display Data				LCD	
R	G	B	CRT Display Color	On/Off	Color
1	1	1	White	On	Black
1	1	0	Yellow	On	Black
0	1	1	Cyan	On	Black
0	1	0	Green	On	Black
1	0	1	Magenta	On	Black
1	0	0	Red	On	Black
0	0	1	Blue	On	Black
0	0	0	Black	Off	White

Table 10. 8-Level Gray Scale Display

CRT Display Data			CRT		LCD	
R	G	B	Color	Luminosity	Color	Contrast
1	1	1	White	High	Black	Strong
1	1	0	Yellow			
0	1	1	Cyan			
0	1	0	Green			
1	0	1	Magenta			
1	0	0	Red			
0	0	1	Blue			
0	0	0	Black	Low	White	Weak

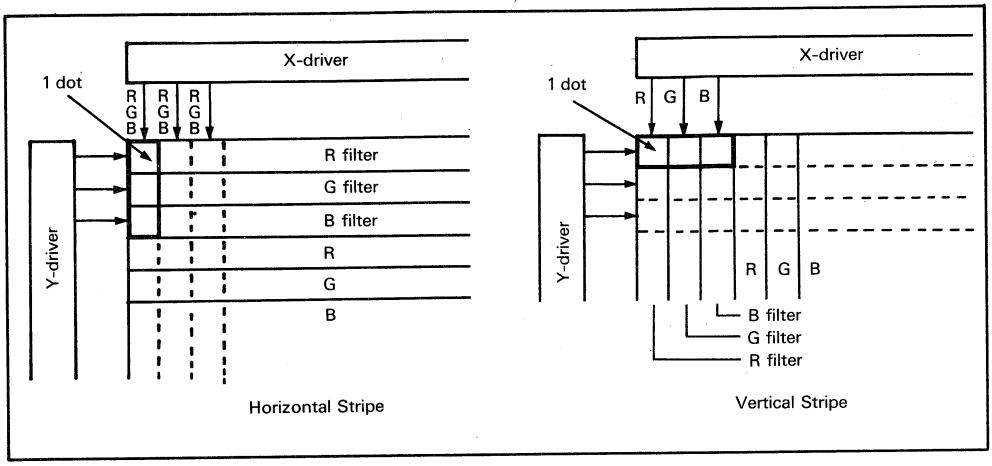


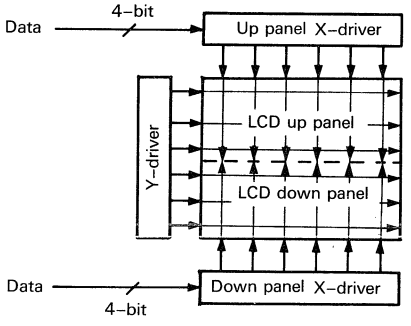
Figure 6. Stripe Modes in 8-Color Display

LCD System Configuration

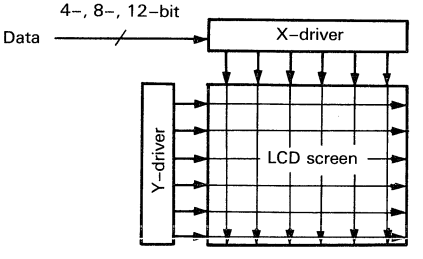
The LVIC supports the following system configurations for LCD:

- Types of LCD data output:
  —Data transfer: 4-bit, 8-bit, or 12-bits (4 bits for R, G, B each)
  —Screen configuration: Single or dual
- How to set LCD drivers around LCD screen:
  —X-driver: On one side or on both sides
  —Y-driver: On one side or on both sides

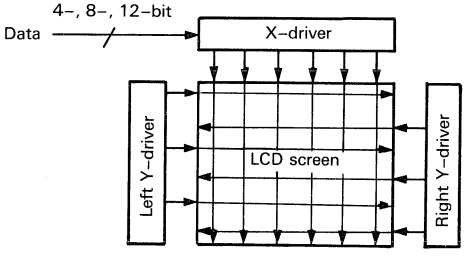
Figure 7 illustrates these system configurations by mode.



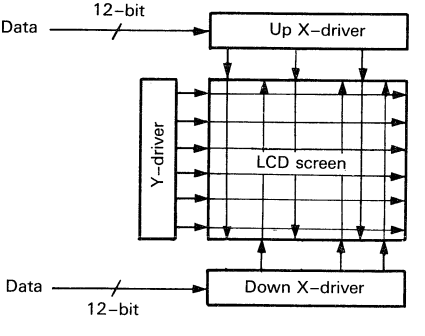
System Configuration for Mode 1 and Mode 6 (4–Bit Data Transfer, Dual Screen, X–Driver and Y–Driver on One Side Each) (Note)



System Configuration for Modes 2, 4, 7, 8, 9, and 13 (4–, 8–, or 12–Bit Data Transfer, Single Screen, X–Driver and Y–Driver on One Side Each)



System Configuration for Modes 3, 5, 10, and 14 (4–, 8–, or 12–Bit Data Transfer, Single Screen, X–Driver on One Side and Y–Driver on Both Sides)



System Configuration for Mode 11 and Mode 15 (12–Bit Data Transfer, Single Screen, X–Driver on Both Sides and Y–Driver on One Side)

Note: Although there are two X-drivers, the X-driver is considered to be set on one side, not on both sides, because the LCD up panel and down panel are each regarded as one screen.

Figure 7. System Configurations by Mode

Calculation of LDOTCK

LDOTCK frequency f_L is calculated from the following expression:

$f_L = (Nhd + 6) \times 8 \times Nvd \times f_F$

Nhd : number of horizontal characters displayed on LCD

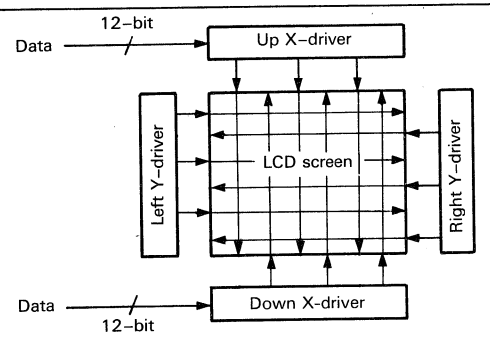
Nvd : number of virtical displayed lines on LCD

f_F : FLM frequency

Here f_L must hold the following relation, where f_D is frequency of dot clock for CRT display (= DOTCLK).

$f_L < f_D \times 15/16$ or

$f_L = f_D$ (The LDOTCK phase must be inverse of the DOTCLK phase in this case)



System Configuration for Mode 12 and Mode 16 (12–Bit Data Transfer, Single Screen, X–Driver and Y–Driver on Both Sides Each)

Notes: 1. X-drivers on both sides: Data output wires run from up and down X-drivers alternately, which widens the interval between wires to twice that in case of an X-driver an one side (figure 8).

2. Y-drivers on both sides: Line select signal output wires run from right and left Y-drivers alternately, which widens the interval between wires to twice that in case of Y-driver on one side (figure 9).

Figure 7. System Configurations by Mode (cont)

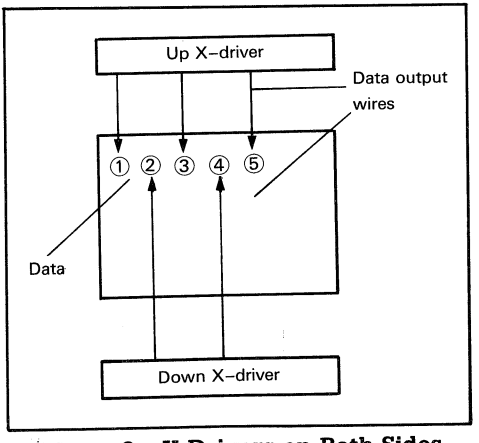


Figure 8. X-Drivers on Both Sides

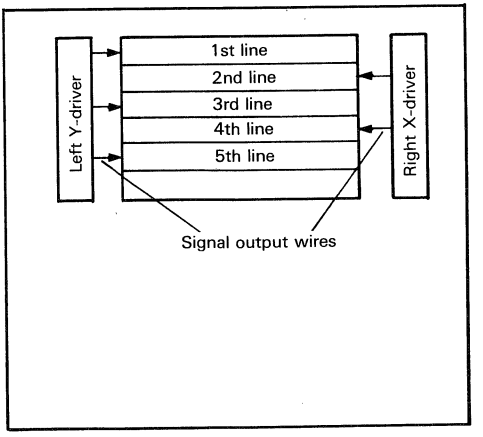


Figure 9. Y-Drivers on Both Sides

Display Timing Signal Generation

CRT display data is classified into display period data and retrace period data. Only display period data is necessary for LCD. Therefore, the LVIC needs a signal announcing whether the CRT display data transferred is for the display period or not. This signal is the display timing signal.

The LVIC can generate the display timing signal from HSYNC and VSYNC. Figure 10 illustrates the relation between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal backporch register (R14, R15) respectively.

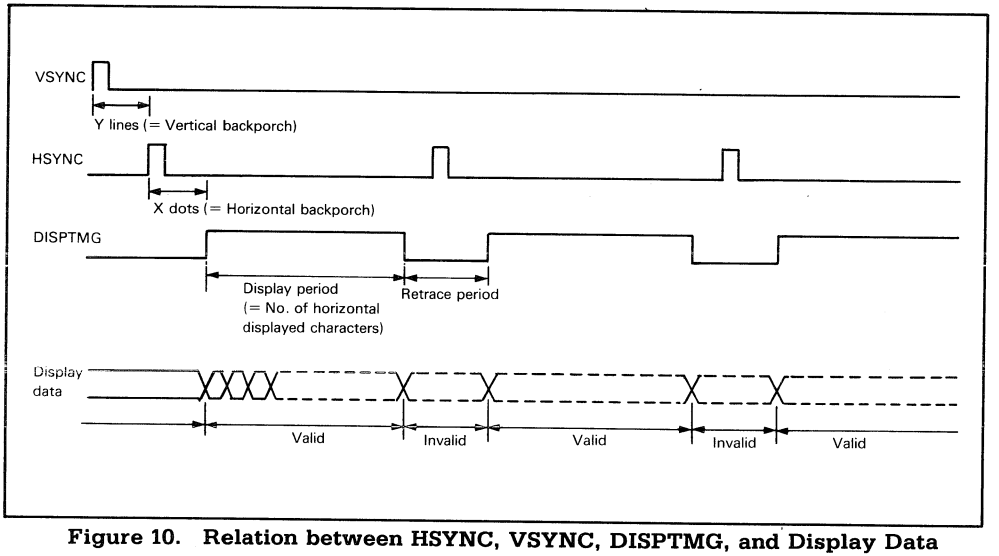


Figure 10. Relation between HSYNC, VSYNC, DISPTMG, and Display Data

Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal and does not appear from the CRT display plug. Thus it is necessary to generate the dot clock. The LVIC has a programmable counter and a phase comparator which are parts of a PLL circuit, and can generate the dot clock from HSYNC if a charge pump, a low pass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

Figure 11 is a block diagram of a PLL circuit. A PLL (phase-locked loop) circuit is a feedback controller regenerating a clock whose frequency and phase are the same as those of a basic clock. The basic clock is HSYNC here.

At power-on, VCO outputs to the programmable counter a signal whose frequency depends on the voltage at the time. The counter divides the frequency of the signal according to the value in the PLL frequency-dividing ratio register (R10, R11) and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock and HSYNC and outputs $\overline{CU}$ or $\overline{CD}$ signal to the charge pump and LPF according to the result. The comparator outputs $\overline{CU}$ when the frequency of the clock is lower than that of HSYNC or when the phase of the clock is behind that of HSYNC, while it outputs $\overline{CD}$ in the contrary case. The charge pump and LPF apply voltage to the VCO according to $\overline{CU}$ or $\overline{CD}$ signal.

This operation is repeated until the phase and the frequency of the frequency-divided clock coincide with those of HSYNC, making it a stable dot clock.

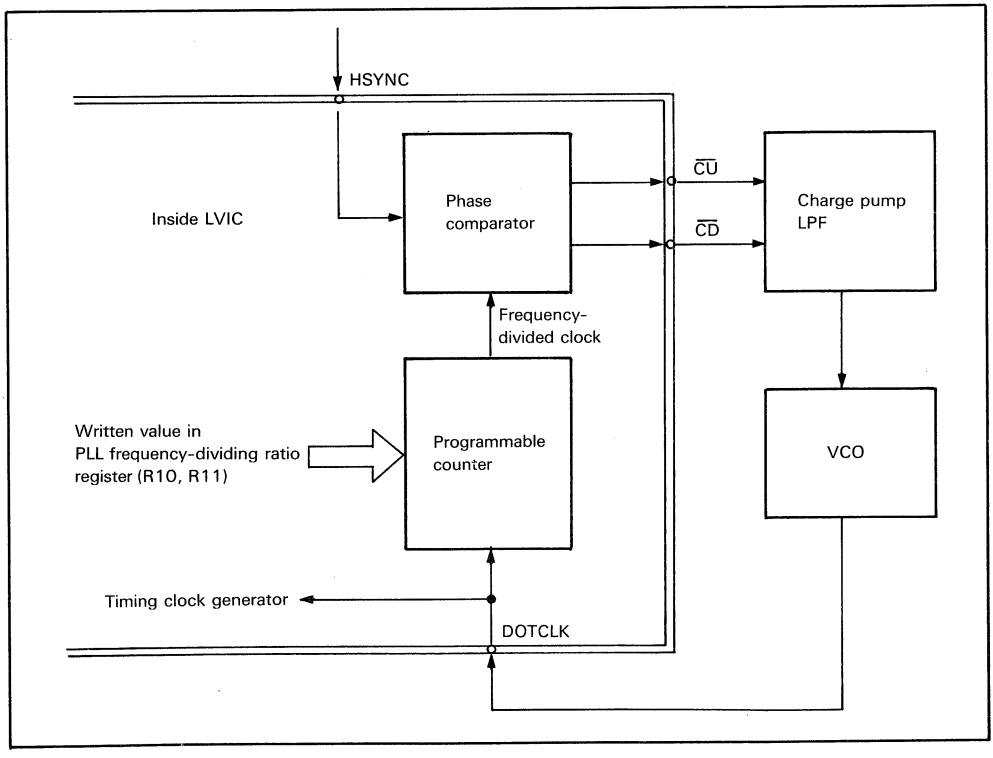


Figure 11. PLL Circuit Block Diagram

Doubled-in-Height Display

Doubled-in-height display doubles characters and pictures in height as illustrated in figure 12.

In TN-type LCD modes (= modes 1, 2, 4, 6, 7, and 8), CL3 frequency is twice as high as CL1 frequency (figure 13). As a result, using CL3 instead of CL1 as a shift clock (figure 14) enables two lines to be selected while an X-driver (data output driver) is outputting the same data, realizing doubled-in height display. However, the following procedures are necessary in this display since multiplexing duty ratio becomes twice as great as the value specified as the number of vertical displayed lines.

1. Halve the frequency of the LCD dot clock (= LDOTCK)
2. Halve the number of vertical displayed lines

This function is provided only for TN-type LCD.

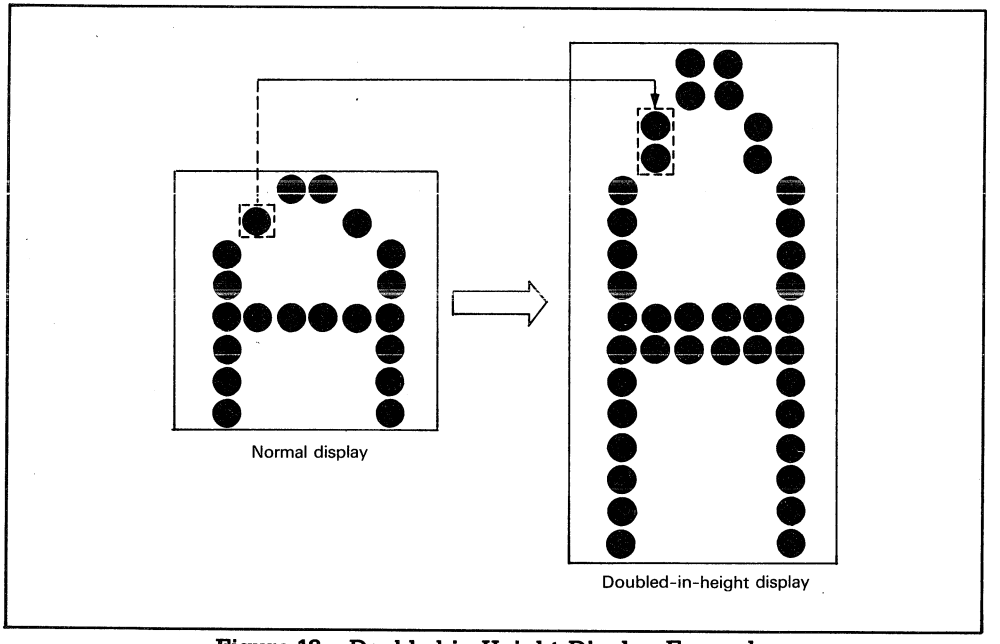


Figure 12. Doubled-in-Height Display Example

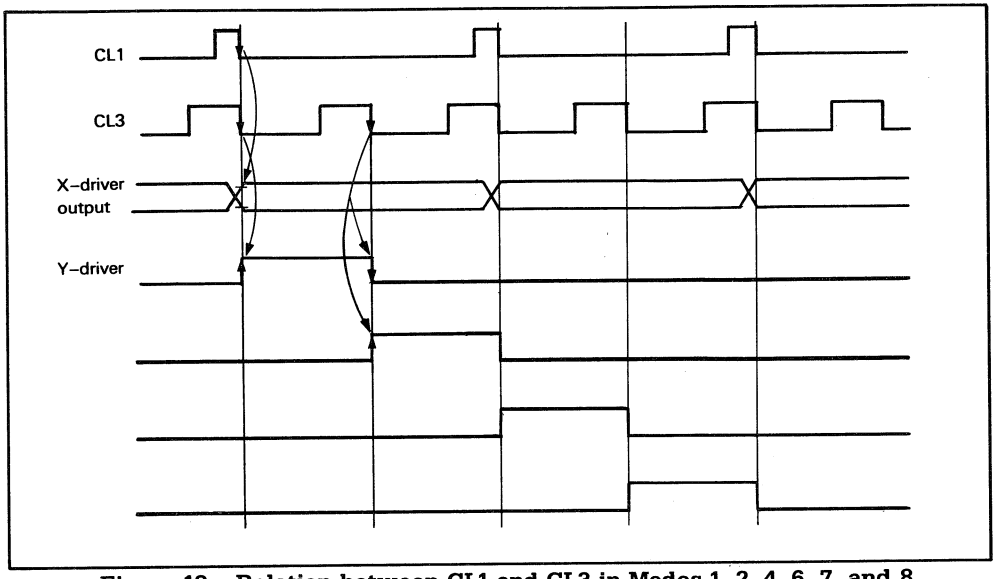


Figure 13. Relation between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

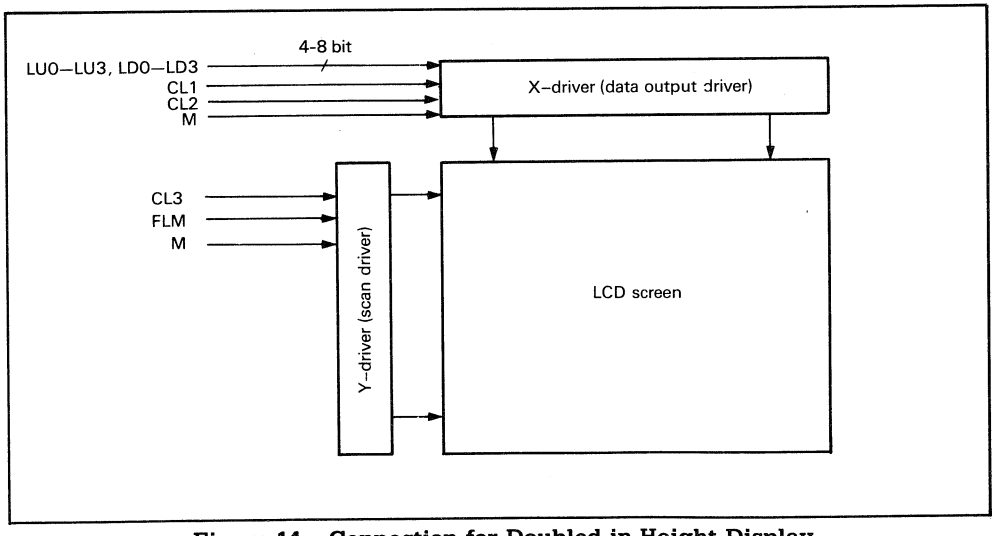


Figure 14. Connection for Doubled-in-Height Display

Display Timing Signal Fine Adjusment

When the display timing signal is supplied externally, a phase shift might appear between CRT data and the display timing signal. This is because each signal has its own peculiar lag. The LVIC can adjust the display timing signal with the F0-F3 pins or the fine adjust register (R9) to correct this phase shift.

Table 11 shows the relation between F3-F0 pins, data bit 3 to data bit 0 of the fine adjust register, and fine adjustment. Concerning the polarity of the number of dots adjusted, − indicates advancing the phase of the display timing signal and + indicates delaying it. F3 pin or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Figure 15 shows examples of adjusting the display timing signal. Since the signal is two dots ahead of the display start position in case (1), (F3, F2, F1, F0) or (data bits 3, 2, 1, 0 of R9) should be set to (1, 0, 1, 0) to delay the signal for two dots. Since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal for two dots. When there is no need to adjust the signal, settings of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 11. Pins, Data Bits of R9, and Fine Adjustment

Pin:	F3	F2	F1	F0	Number of Dots
R9 Bit:	3	2	1	0	Adjusted
	0	0	0	0	0
		0	0	1	− 1
		⋮	⋮	⋮	⋮
		1	1	0	− 6
		1	1	1	− 7
	1	0	0	0	0
		0	0	1	+ 1
		⋮	⋮	⋮	⋮
		1	1	0	+ 6
		1	1	1	+ 7

Note: When adjusting the display timing signal with pins, set ADJ pin to 1.

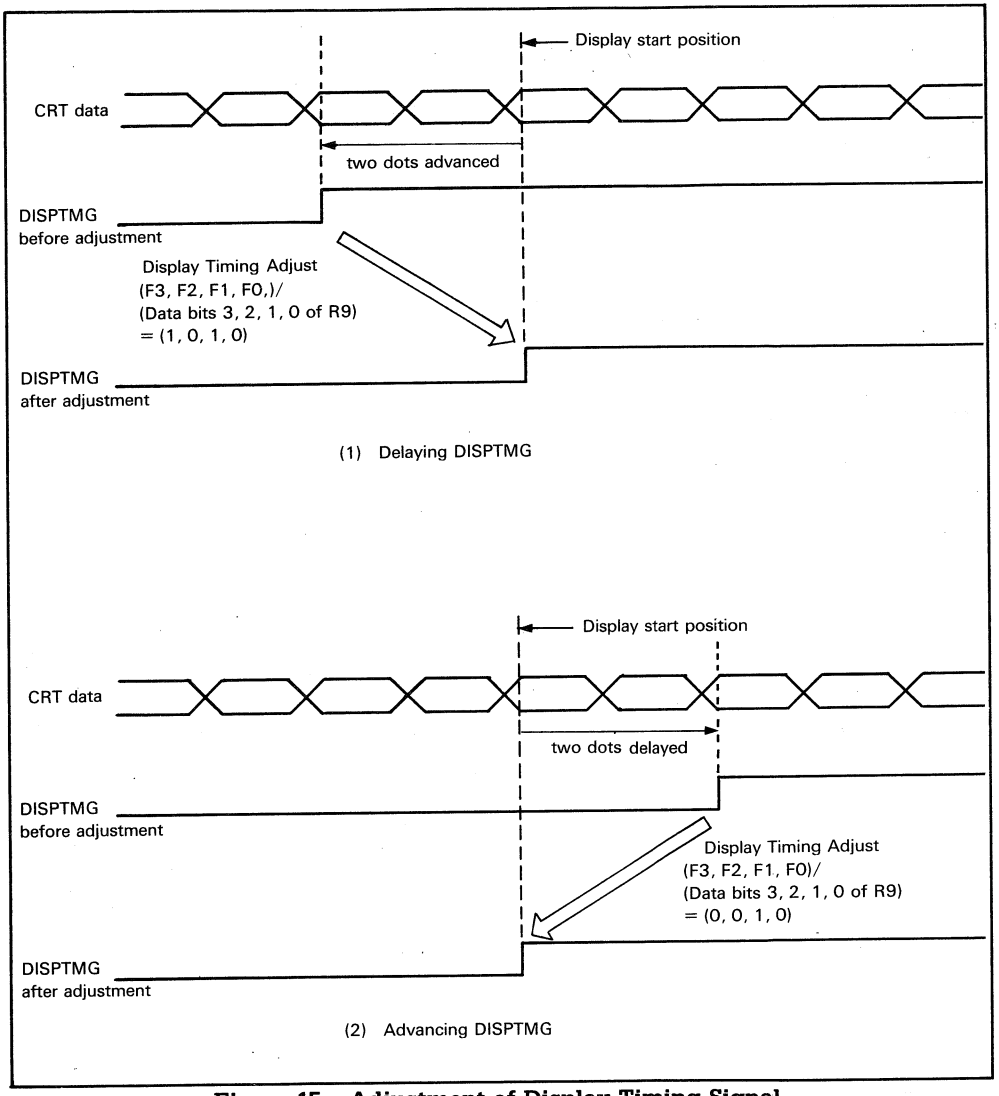


Figure 15. Adjustment of Display Timing Signal

Internal Registers

The LVIC has an address register (AR) and sixteen data registers (R0-R15). In order to specify one of the sixteen data registers, write its register address into the address register. The MPU transfers data to the data register corresponding to the written address.

All the registers are valid only when the LVIC is controlled by the internal register programming method and are invalid (don't care) when by the pin programming method.

Address Register (AR)

The address register (figure 16) is composed of four bits and specifies one data register out of sixteen. This register is selected by the MPU when RS pin is low and specifies any data register with the register address written by the MPU.

Control Register 1 (R0)

Control register 1 (figure 17) is composed of four bits, including two invalid bits. Each of two valid bits has its own function. Reading from and writing into invalid bits are passible. However, these operation does not affect the LSI function.

- DSP Bit
  - —DSP = 1: LVIC generates the display timing signal
  - —DSP = 0: LVIC does not generate the display timing signal
    (If DCK = 1, the display timing signal is generated in spite that DSP = 0)
- DCK Bit
  - —DCK = 1: LVIC generates the dot clock
  - —DCK = 0: LVIC does not generate the dot clock

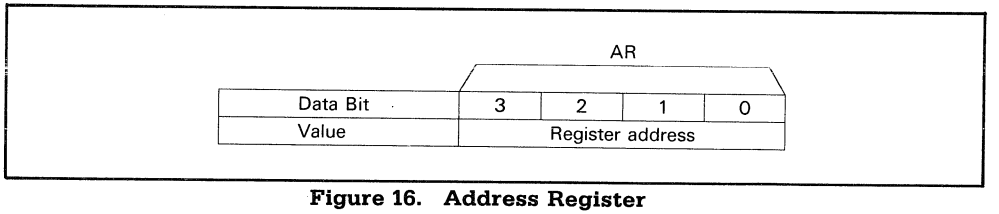


Figure 16. Address Register

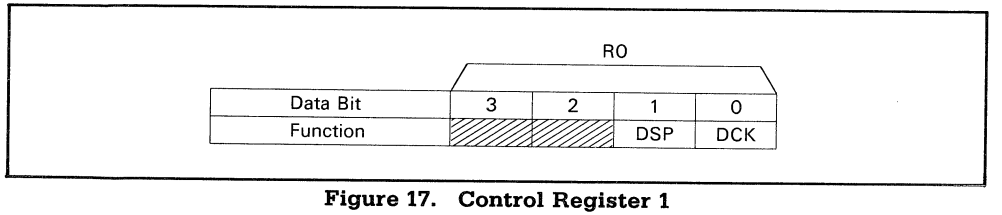


Figure 17. Control Register 1

Control Register 2 (R0)

Control register 2 (figure 18) is composed of four bits and has three functions.

- MC Bit
  —MC = 1: M signal alternates per line
  —MC = 0: M signal alternates per frame
- DON Bit
  —DON = 1: Display on
  —DON = 0: Display off
- MS1 and MS0 Bits
  —Select the memory type (table 12)

Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4), CL3 Period Register (Low-order 2 Bits of R4, R5)

The vertical displayed lines register (figure 19) is composed of ten bits (R2 + R3 + high-order two bits of R4) and specifies the number of vertical displayed lines. This register can specify both even and odd numbers in modes for a Y-driver on one side and single screen configuration, but even numbers only in the other modes. The value to be written into this register is (Nvd − 1), where Nvd = number of vertical displayed lines.

The CL3 period register is composed of six bits (low-order two bits of R4 + R5) and specifies the period of CL3 in 8-color display modes with horizontal stripes. Thus this register is invalid in the other modes. CL3 is a clock for the LVIC to output R, G, B data separately to LCD drivers. The value to be written into this register is (Nhd + 6) × 1/3 − 1, where Nhd = number of horizontal displayed characters. When (Nhd + 6) is not divisible by 3, the quotient should be rounded up or rounded down.

Table 12. Memory Type and MS1, MS0

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbyte
1	0	32-kbyte
1	1	64-kbyte

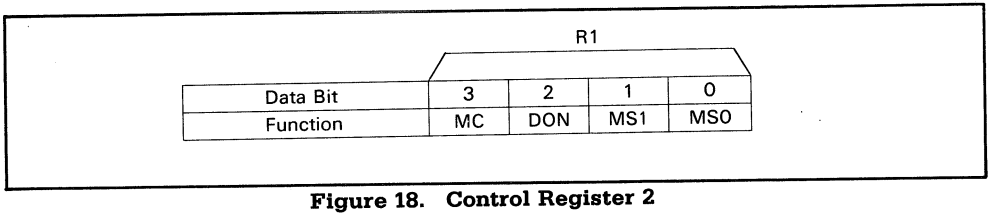


Figure 18. Control Register 2

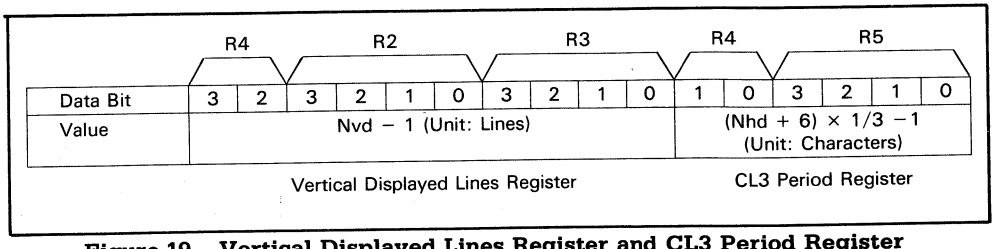


Figure 19. Vertical Displayed Lines Register and CL3 Period Register

Horizontal Displayed Characters Register (R6, R7)

The horizontal displayed characters register (figure 20) is composed of eight bits (R6 + R7) and specifies the number of horizontal displayed characters. This register can specify even numbers only. The most significant bit of R6 is invalid in the modes for dual screen configuration. When writing into this register, shift (Nhd − 1) in the low-order direction for one bit to cut off the least significant bit. Figure 20 shows how to write a value into the register when Nhd = 90.

CL3 Pulse Width Register (R8)

The CL3 period register (figure 22) is composed of four bits and specifies the high-level pulse width of CL3. When controlling TFT-type LCDs, each gate of the LCD has to hold data from the time a Y-driver outputs the line select and shift signal to the time an X-driver the outputs next display data. Data must be held while CL3 is high. However, even when the LVIC is not controlling TFT-type LCDs, CL3 appears with the high-level pulse width specified by this register.

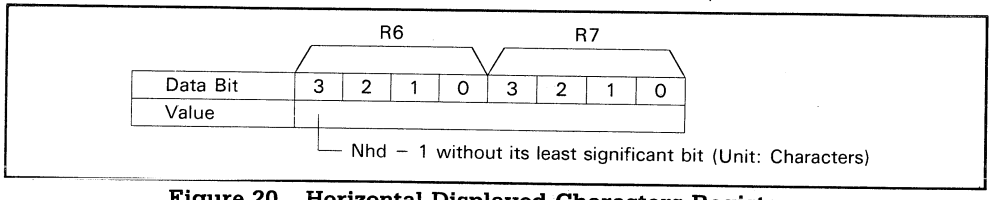


Figure 20. Horizontal Displayed Characters Register

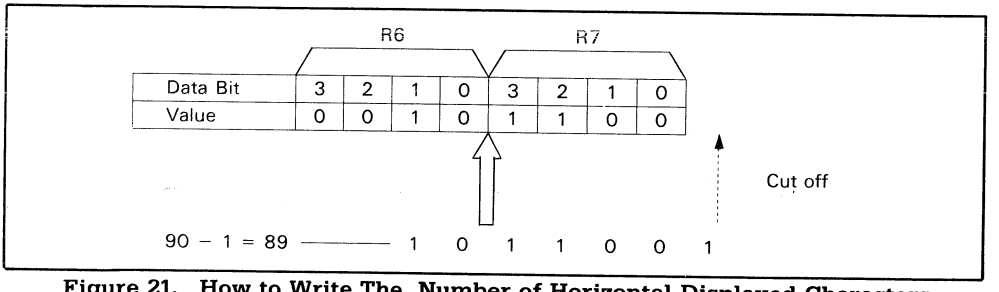


Figure 21. How to Write The Number of Horizontal Displayed Characters

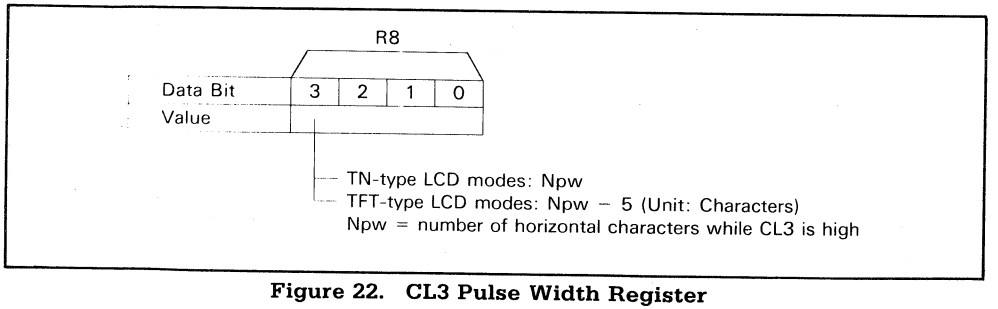


Figure 22. CL3 Pulse Width Register

Fine Adjust Register (R9)

The fine adjust register (figure 23) is composed of four bits and adjusts the externally supplied display timing signal to synchronize its phase with that of LCD data. The value to be written into this register is determined by the interval between the positive edge of the display timing signal and the display start position. For more details, refer to "Display Timing Signal Fine Adjustment." This register is invalid when the display timing signal is generated internally.

PLL Frequency-Dividing Ratio Register (R10, R11)

The PLL frequency-dividing ratio register (figure 24) is composed of eight bits (R10 + R11) and specifies the PLL frequency-dividing ratio for generating a dot clock by a PLL circuit. The value to be written into this register is determined by the ratio of the frequency of HSYNC to that of the dot clock which the user wants. This register is invalid when the dot clock is supplied externally and is valid only when the LVIC is controlled by the internal register programming method and the DCK bit of control register 1 (R0) is 1. The written value in this register (N_{PLL}) is obtained with the following expression:

N_{PLL} = Ncht × 8 − 731

Ncht: total number of characters for CRT

Ncht can be obtained as follows from the specifications of a CRT monitor:

Ncht = 1/8 × (DOTCLK frequency)/(HSYNC frequency)

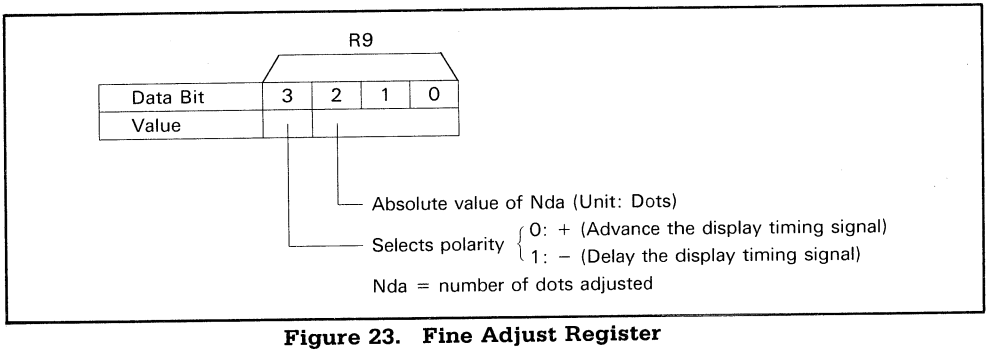


Figure 23. Fine Adjust Register

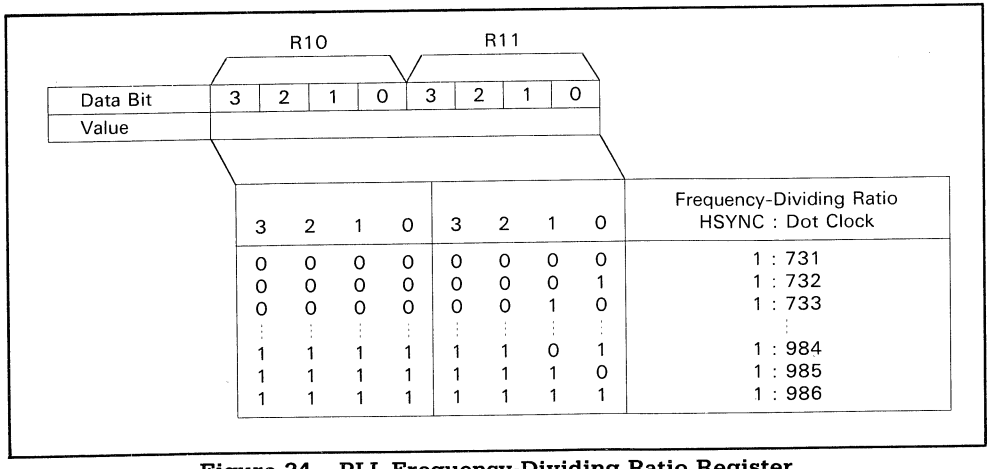


Figure 24. PLL Frequency-Dividing Ratio Register

Vertical Backporch Register (R12, R13)

The vertical backporch register (figure 25) is composed of eight bits (R12 + R13) and specifies the vertical backporch. The vertical backporch is the number of lines between the positive edge of VSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation." This register is invalid when the display timing signal is supplied externally and is valid only is a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be regenerated and the register is enabled even when DSP = 0.)

Horizontal Backporch Register (R14, R15)

The horizontal backporch register (figure 26) is composed of eight bits (R14 + R15) and specifies the horizontal backporch. The horizontal backporch is the number of characters between the positive edge of HSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation". This register is invalid when the display timing signal is supplied externally and is valid only in a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be generated and this register is enabled even when DSP = 0.)

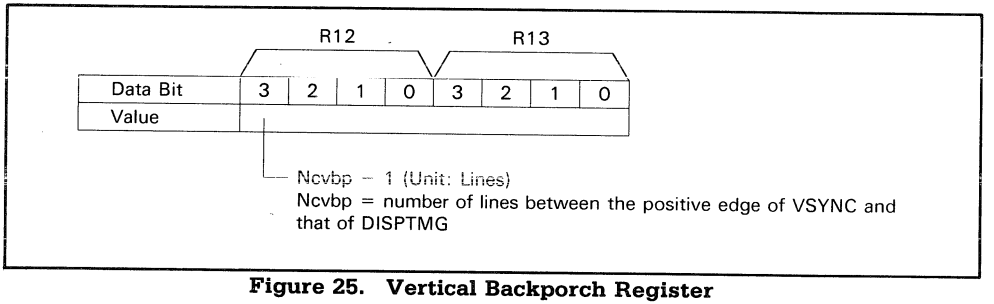


Figure 25. Vertical Backporch Register

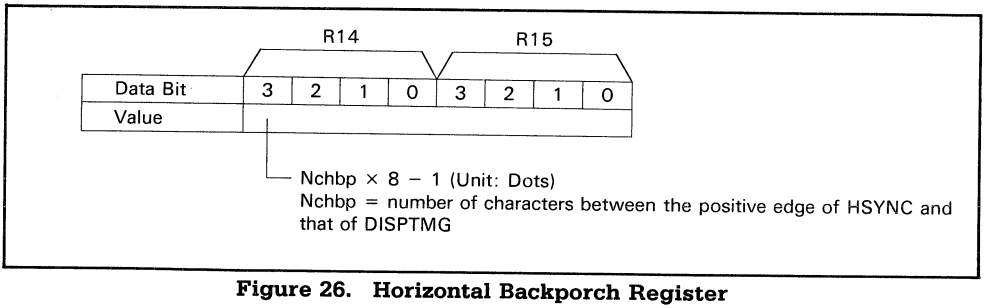


Figure 26. Horizontal Backporch Register

Reset

$\overline{RES}$ pin resets and starts the LVIC. Make sure to hold the reset signal low for at least 1 μs after power-on.

Reset is defined as shown in figure 27.

State of Pins During Reset

$\overline{RES}$ basically does not control output pins and operates regardless of the other input pins. Output pins can be classified into the following five groups depending on their reset state.

1. Keeps state before reset: CL2
2. Driven to high-impedance state (fixed low when using no memory): RD0-RD7, GD0-GD7, BD0-BD7
3. Fixed high: $\overline{MWE}$, CL4, M, $\overline{CD}$, $\overline{MCS1}$
4. Fixed low: MA0-MA12, R0-R3, G0-G3, B0-B3, $\overline{CS}$, CL1, CL3, FLM, A0-A3, $\overline{CU}$
5. Fixed high or low depending on the memory in use (table 13): MA13-MA15, $\overline{MCS0}$

State of Registers During Reset

$\overline{RES}$ pin does not affect register contents. Therefore, registers can be both read and written by the MPU even during reset. Registers keep the contents they had before reset until they are rewritten.

Memory Clear Function

After reset, the LVIC writes 0 in the memory area specified by MSEL0 and MSEL1 (table 7) regardless of R, G, B data.

Table 13. Memory Type and State of Pins During Reset

Kind of Memories	MA13	MA14	MA15	$\overline{MCS0}$
No memory	Low	Low	High	High
8-kbyte memory	High	High	High	Low
32-kbyte memory	Low	Low	High	Low
64-kbyte memory	Low	Low	Low	Low

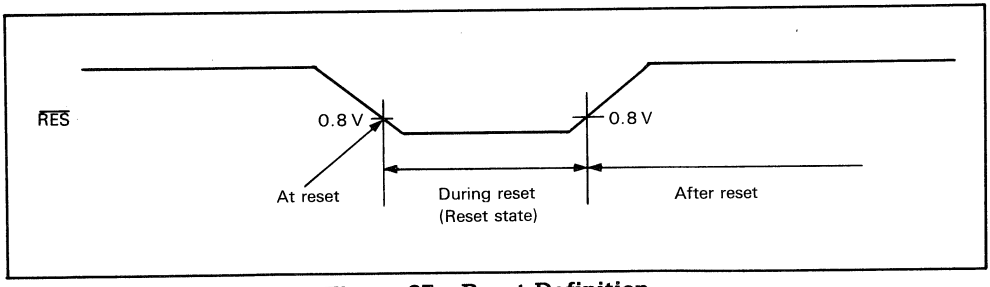


Figure 27. Reset Definition

User Precautions

1. There are following limitations when the user uses no memory. (MSEL0 = 0, MSEL1 = 1)

   - The display modes for dual screen configuration (= mode 1 and mode 6) are disabled.
   - The LVIC cannot support the LCD systems with Y-drivers on both sides. Even if the user selects the mode for the system with Y-drivers on both sides (= mode 3, 5, 10, 12, 14, or 16), the operation of the LVIC is exactly the same as that in the mode for the system with Y-driver on one side (= mode 2, 4, 9, 11, 13, or 15).
     And leave CL4 terminal disconnected in this usage.
   - The doubled-in-height function does not work in this condition.
   - The LVIC in the pin program mode can not support 8-color horizontal stripe display (=mode 13, 14, 15, 16).

2. The LVIC might operate irregularly until the internal registers have been written after reset in the system which controls the LVIC by internal register programming method.

3. Memory clear function might not work normally at power-on or after reset if MSEL0 and MSEL1 are not properly set to the value corresponding to the memories in use.

4. Since the LVIC is a CMOS LSI, input pins must not be left disconnected. Refer to table 1 concerning how to deal with each pin.

Programming

The values written in internal registers have the limit listed in table 14. The symbols in the table are difined as shown in table 15 and figure 27.

Table 14. Limit on Values Written in Registers

Function	Limit	Notes	Applicable Registers
Screen Configuration	$4 \leqq Nvd \leqq (Ncvbp + Ncvsp) - 1 \leqq 1024$	1, 8	R2, R3, R4, R6, R7
	$4 \leqq Nhd \leqq (Nchbp \times 1/n + Nchsp) - 1 \leqq 506$		
	$(Nhd + 6) \times n \times Nvd \times f_F \leqq f_D \leqq 30$ MHz	2, 8	R2, R3, R4, R6, R7
CL3 Control	$1 \leqq Npw \leqq (Nhd + 6) \times 1/2 - 1$	3	R4, R5, R6, R7, R8
	$1 \leqq Npw \leqq Nhd$	4	
	$1 \leqq Npw \leqq Npc - 1$	5	
	$Npc \leqq (Nhd + 6)/2 - 1$	5	
DISPTMG Regeneration	$1 \leqq Nchbp \leqq 256$	6	R12, R13, R14, R15
	$1 \leqq Ncvbp \leqq 256$	6	
Without Buffer Memory	$4 \leqq Nhd \leqq Nchsp - 4$	7	R2, R3, R4, R6, R7
	$4 \leqq Nvd \leqq Ncvsp - 4$	7	

Notes:
1. $Nhd \leqq 256$ in dual screen configuration (= mode 1 and mode 6)
2. f_F: FLM frequency, f_D: frequency of CRT dot clock, f_L: frequency of LCD dot clock for LCD
   $f_L < f_D \times 15/16$, or $f_L = f_D$
3. In modes 1, 2, 4, 6, 7, and 8
4. In modes 3, 5, 9, 10, 11, and 12 (Npw = (value in R8) + 5)
5. In modes 13, 14, 15, and 16 (Npw = (value in R8) + 5)
6. Value in R14, R15 $\leqq$ (Nchsp $\times$ n + Nchbp) $-$ Nhd $\times$ n $-$ 2
   Value in R12, R13 $\leqq$ (Ncvsp + Ncvbp) $-$ Nvd $-$ 2
7. Nht = Nchsp + Nchbp $\times$ 1/n, Nd = Ncvbp + Ncvsp
   (Nht = Nhd + 6, Nd = Nvd when using buffer memory)
8. n: Horizontal character pitch (the number of horizontal dots in one character).

Table 15. Symbol Definition

Symbol	Definition
Nchd	Number of horizontal displayed characters on CRT display
Nchsp	Number of characters between the positive edge of DISPTMG and that of HSYNC (= Horizontal sync position)
Nchbp	Number of dots between the positive edge of HSYNC and that of DISPTMG (= horizontal backporch)
Ncvbp	Number of lines between the negative edge (positive edge when VSYNC is high in active state) of VSYNC and the first positive edge of DISPTMG (= vertical backporch)
Ncvsp	Number of lines between the first positive edge of DISPTMG and the next negative edge of VSYNC (= vertical sync position)
Ncvd	Number of vertical displayed lines on CRT display
Nhd	Number of horizontal displayed characters (on LCD)
Npc	Number of characters during CL3 period (= CL3 pulse cycle)
Npw	Number of characters while CL3 is high (= CL3 pulse width)
Nht	Total number of horizontal characters
Nvd	Number of vertical displayed lines (on LCD)

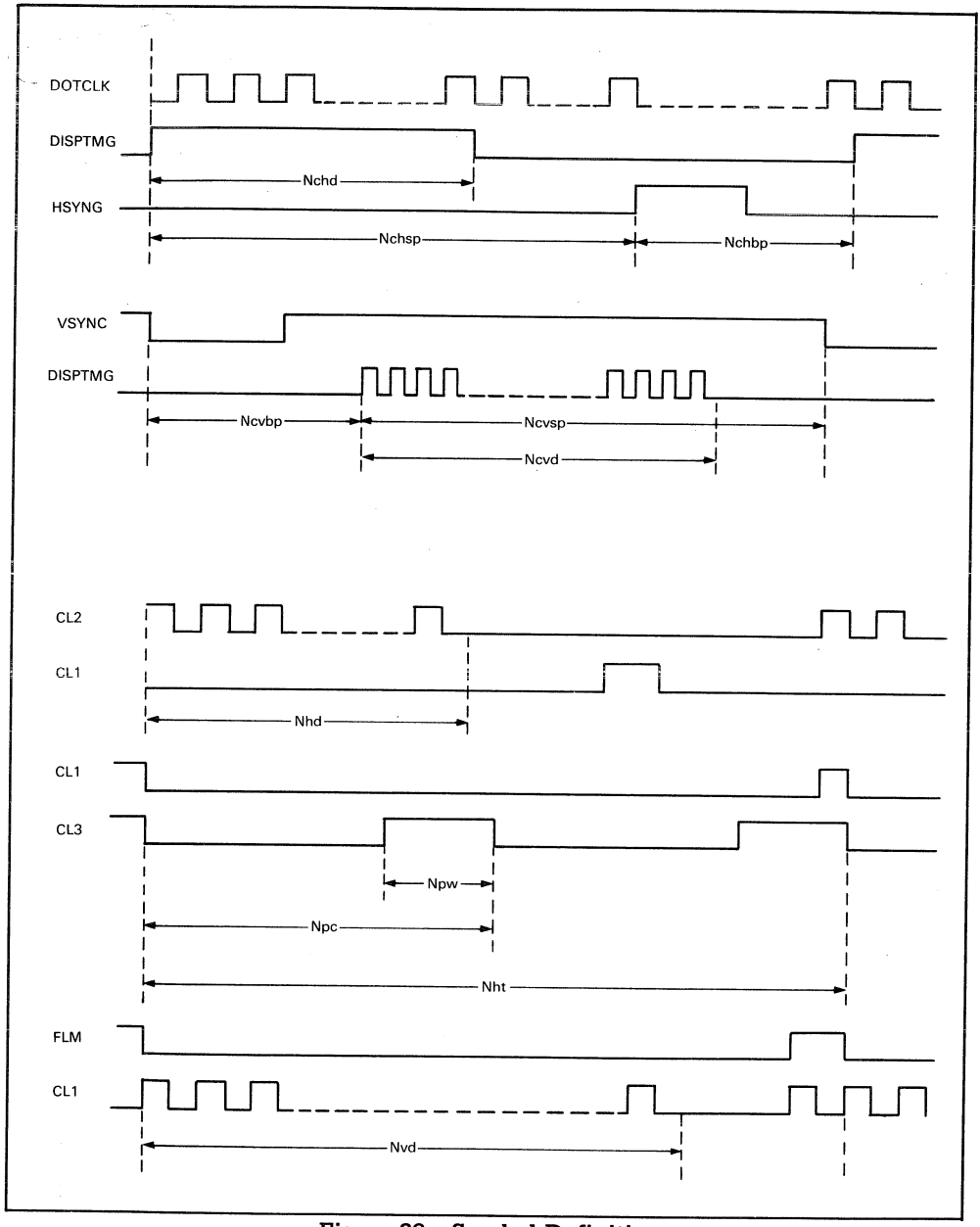


Figure 28. Symbol Definition

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{in}	− 0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	− 20 to + 75	°C
Storage temperature	T_{stg}	− 55 to + 125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of the LSI.
2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Conditions
Input high voltage	$\overline{RES}$	V_{IH}	V_{CC} − 0.5	V_{CC} + 0.3	V	
	TTL interface[1]		2.0	V_{CC} + 0.3		
	TTL interface[4]		2.2	V_{CC} + 0.3		
	CMOS interface[1]		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface[1], $\overline{RES}$	V_{IL}	−0.3	0.8	V	
	TTL interface[5]		−0.3	0.6		
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		V_{CC} − 0.8	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 30 MHz Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{RD}$/XDOT, $\overline{RS}$/ADJ, $\overline{CS}$/MS0
CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2
2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$
CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4
3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG
4. TTL interface: $\overline{WR}$/MS1, LDOTCK, DOTCLK
5. TTL interface: $\overline{WR}$/MS1

DC Characteristics 2 (V_{CC} = 5.0 V ± 5 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Conditions
Input high voltage	$\overline{RES}$	V_{IH}	V_{CC} − 0.5	V_{CC} + 0.3	V	
	TTL interface[1], $\overline{RES}$		2.0	V_{CC} + 0.3		
	CMOS interface[1]		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface[1]	V_{IL}	−0.3	0.8	V	
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		V_{CC} − 0.8	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 30 MHz Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, DOTCLK, LDOTCK, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{RD}$/XDOT, $\overline{RS}$/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1
CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2

2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$
CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4

3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

AC Characteristics (V_{CC} = 5.0 V ±10 %, GND = 0 V, Ta = −20 °C to +75 °C, unless otherwise noted)

Video Signal Interface (1) (HD66840F30: 30 MHz) (V_{CC} = 5.0 V ± 5 %)

Item	Symbol	Min	Max	Unit	Remark
DOTCLK cycle time	t_{CYCD}	33	1000	ns	
DOTCLK high-level pulse width	t_{WDH}	16.5	—	ns	
DOTCLK low-level pulse width	t_{WDL}	16.5	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
R, G, B, setup time	t_{VDS}	10	—	ns	
R, G, B, hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Except DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	Except DOTCLK

Video Signal Interface (2) (HD66840F25 : 25MHz)

Item	Symbol	Min	Max	Unit	Remark
DOTCLK cycle time	t_{CYCD}	40	1000	ns	
DOTCLK high-level pulse width	t_{WDH}	20	—	ns	
DOTCLK low-level pulse width	t_{WDL}	20	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
R, G, B, setup time	t_{VDS}	10	—	ns	
R, G, B, hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Except DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	Except DOTCLK

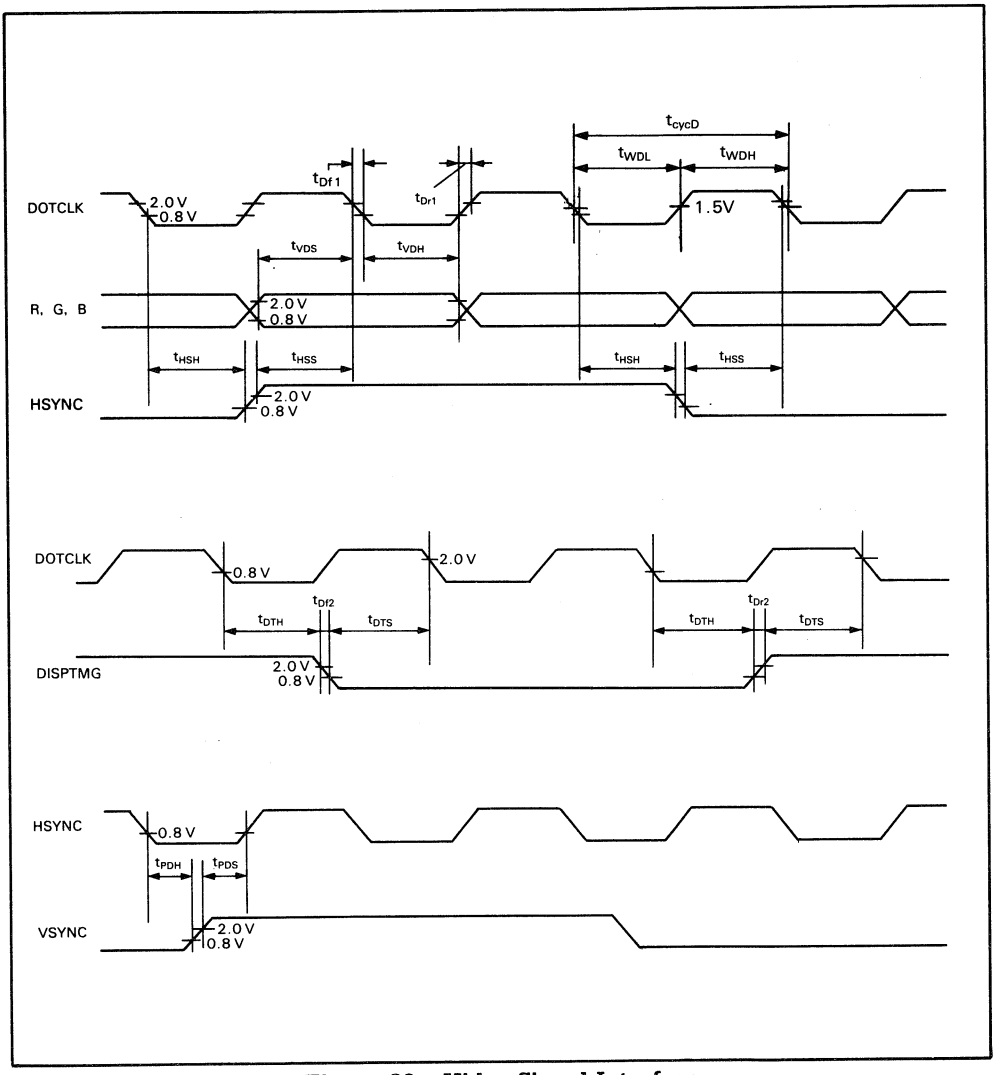


Figure 29. Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	5 t_{CYCD} – 50	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data setup time	t_{SMD}	25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data hold time	t_{HMD}	0	—	ns
Write cycle time	t_{WC}	6 t_{CYCD} – 50	—	ns
Address setup time	t_{AS}	t_{CYCD} – 30	—	ns
Address hold time	t_{WR}	t_{CYCD} – 30	—	ns
Chip select time	t_{CW}	4 t_{CYCD} – 40	—	ns
Write pulse width	t_{WP}	4 t_{CYCD} – 40	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output setup time	T_{SMDW}	2 t_{CYCD} – 25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output hold time	t_{HMDW}	0	—	ns

Note: t_{CYCD} indicates DOTCLK cycle time (min 33 ns, max 1000 ns).

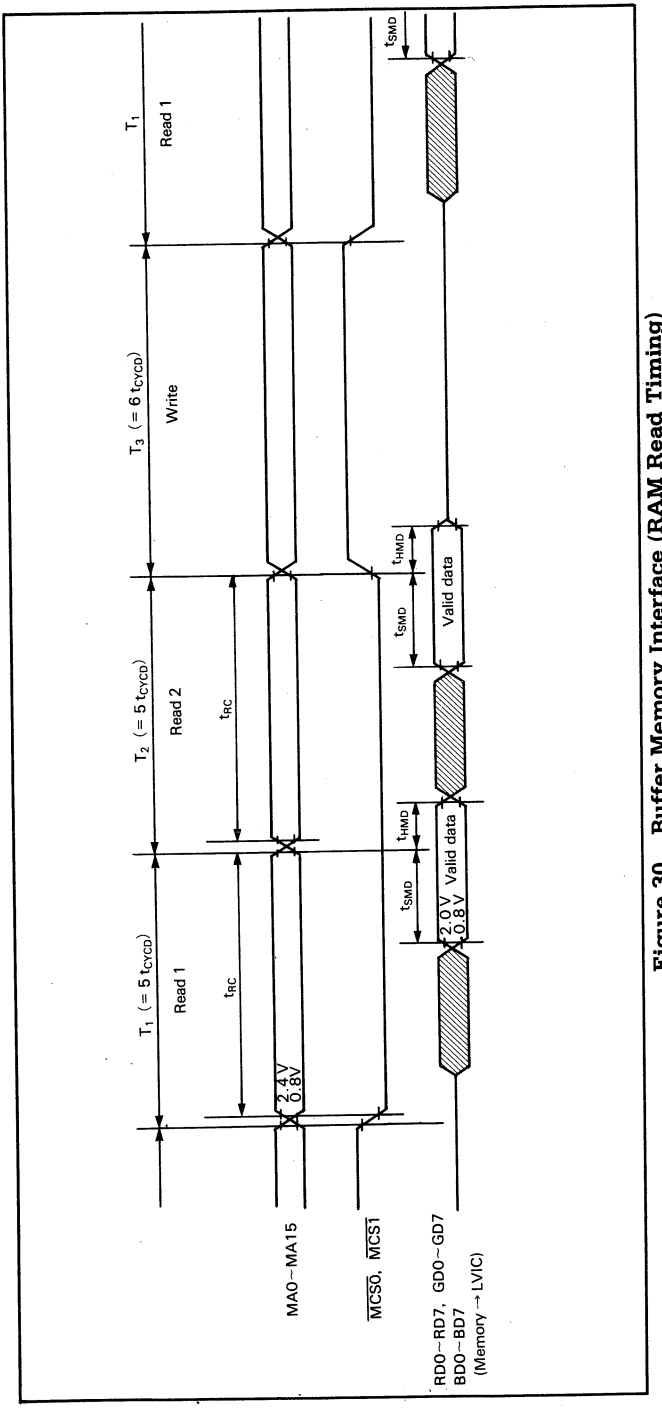


Figure 30. Buffer Memory Interface (RAM Read Timing)

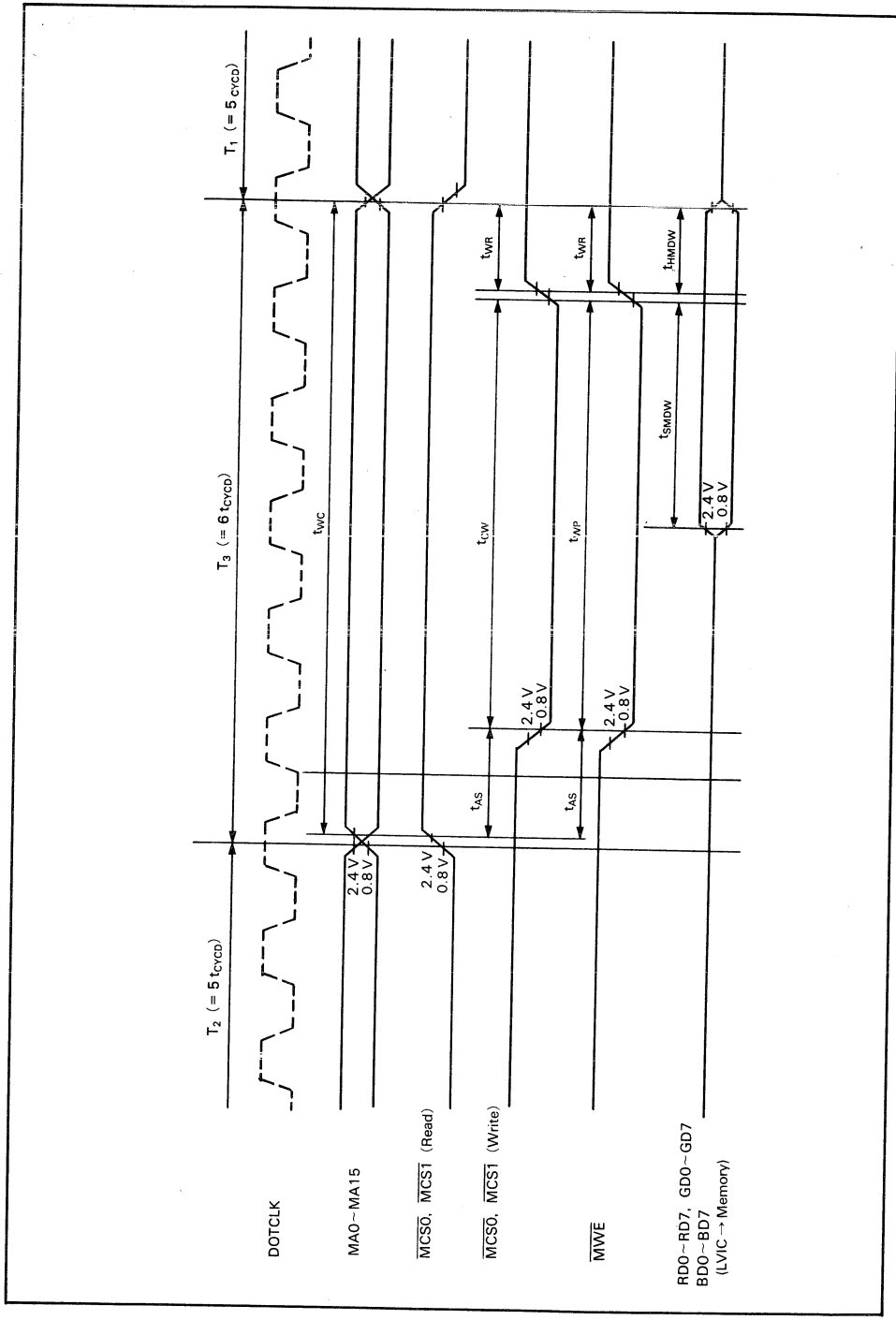


Figure 31. Buffer Memory Interface (RAM Write Timing)

LCD Driver Interface (TN-Type LCD Driver)

Item	Symbol	Min	Max	Unit
CL2 cycle time	t_{WCL2}	166	—	ns
CL2 high-level pulse width	t_{WCL2H}	50	—	ns
CL2 low-level pulse width	t_{WCL2L}	50	—	ns
CL2 rise time	t_{CL2r}	—	30	ns
CL2 fall time	t_{CL2f}	—	30	ns
CL1 high-level pulse width	t_{WCL1H}	200	—	ns
CL1 rise time	t_{CL1r}	—	30	ns
CL1 fall time	t_{CL1f}	—	30	ns
CL1 setup time	t_{SCL1}	500	—	ns
CL1 hold time	t_{HCL1}	200	—	ns
FLM hold time	t_{HF}	200	—	ns
M output delay time	t_{DM}	—	300	ns
Data delay time	t_{DD}	− 20	20	ns
LDOTCK cycle time	t_{WLDOT}	41	—	ns

Note: All the values are measured at f_{CL2} = 6 MHz.

LCD Driver Interface (TFT-Type LCD Driver)

Item	Symbol	Min	Max	Unit	Remark
CL2 cycle time (X drivers on one side)	t_{TCL2S}	133		ns	Figure 34,35
CL2 high-level width (X drivers on one side)	t_{TCL2HS}	30		ns	
CL2 low-level width (X drivers on one side)	t_{TCL2LS}	30		ns	
CL2 cycle time (X drivers on both side)	t_{TCL2D}	266		ns	
CL2 high-level width (X drivers on both side)	t_{TCL2HD}	80		ns	
CL2 low-level width (X drivers on both side)	t_{TCL2LD}	80		ns	
CL2 rise time	t_{CL2r}		30	ns	
CL2 fall time	t_{CL2f}		30	ns	
CL1 high-level width	t_{TCL1H}	200		ns	
CL1 rise time	t_{CL1r}		30	ns	
CL1 fall time	t_{CL1f}		30	ns	
Data delay time	t_{DD1}	−20	20	ns	
Data set up time	t_{LDS}	15		ns	
Data hold time	t_{LDH}	15		ns	
CL1 setup time	t_{TSCL1}	500		ns	
CL1 hold time	t_{THCL1}	200		ns	
CL3 delay time	t_{DCL3}	50		ns	
M delay time	t_{DM}		300	ns	
FLM hold time	t_{TFH}	200		ns	
LDOTCK cycle time	t_{WLDOT}	33		ns	

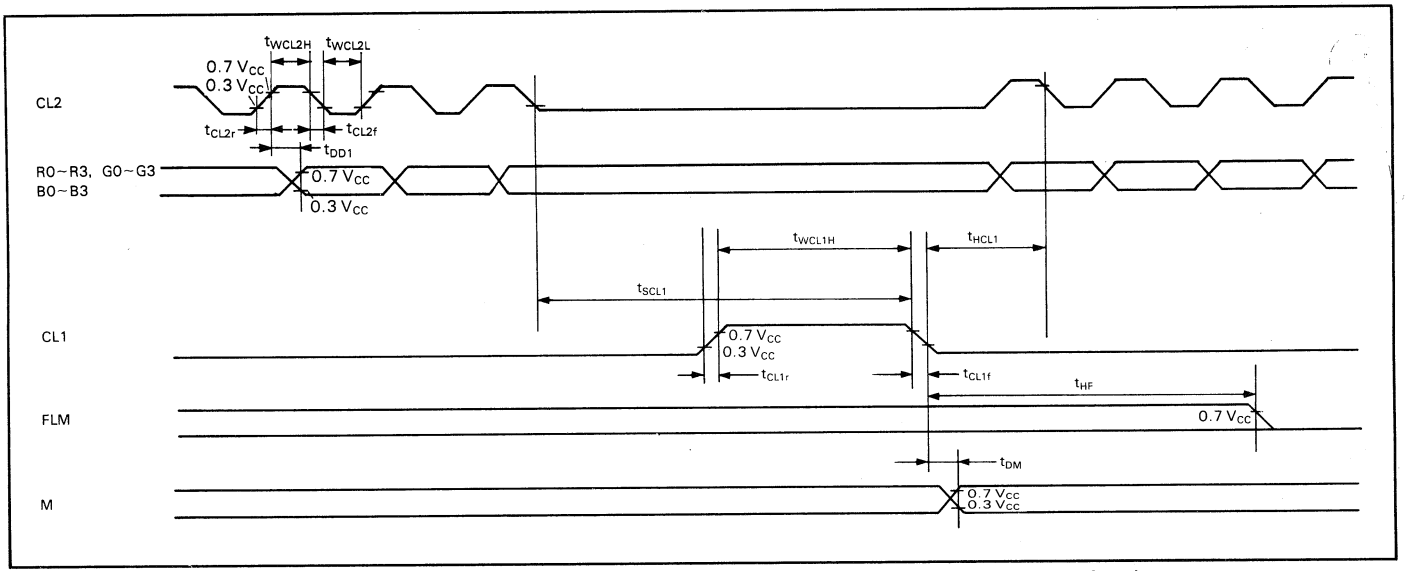


Figure 32. LCD Driver Interface (TN-Type LCD Driver Interface)

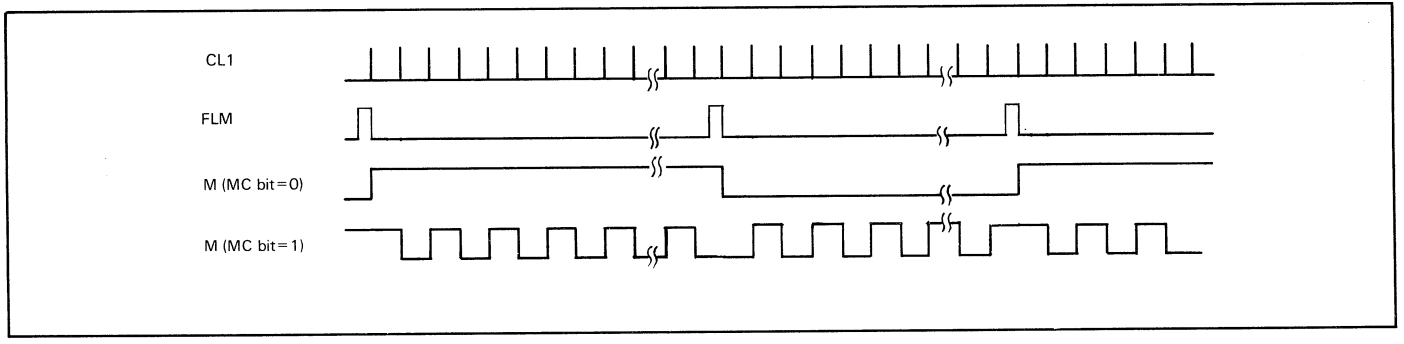


Figure 33. CL1, FLM and M (Reduced View of Figure 32)

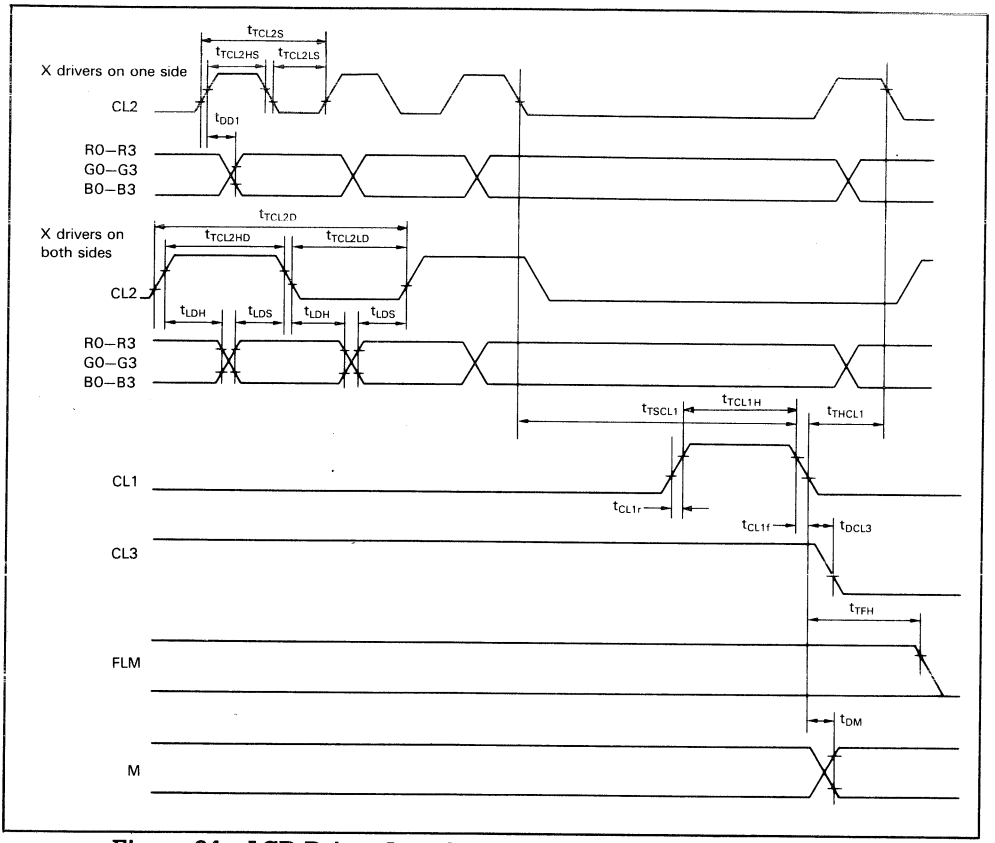


Figure 34. LCD Driver Interface (TFT-type LCD Driver Interface)

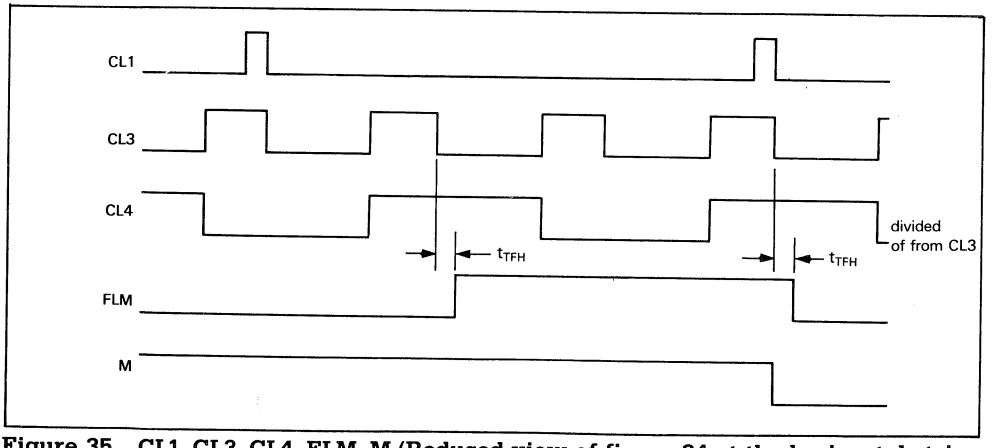


Figure 35. CL1, CL3, CL4, FLM, M (Reduced view of figure 34 at the horizontal stripe mode)

Register Programming, MPU Write

Item	Symbol	Min	Max	Unit
$\overline{RD}$ high-level pulse width	t_{WRDH}	190	—	ns
$\overline{RD}$ low-level pulse width	t_{WRDL}	190	—	ns
$\overline{WE}$ high-level pulse width	t_{WWEH}	190	—	ns
$\overline{WE}$ low-level pulse width	t_{WWEL}	190	—	ns
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns
D0-D3 setup time	t_{DSW}	100	—	ns
D0-D3 hold time	t_{DHW}	0	—	ns
D0-D3 output delay time	t_{DDR}	—	150	ns
D0-D3 output hold time	t_{DHR}	10	—	ns

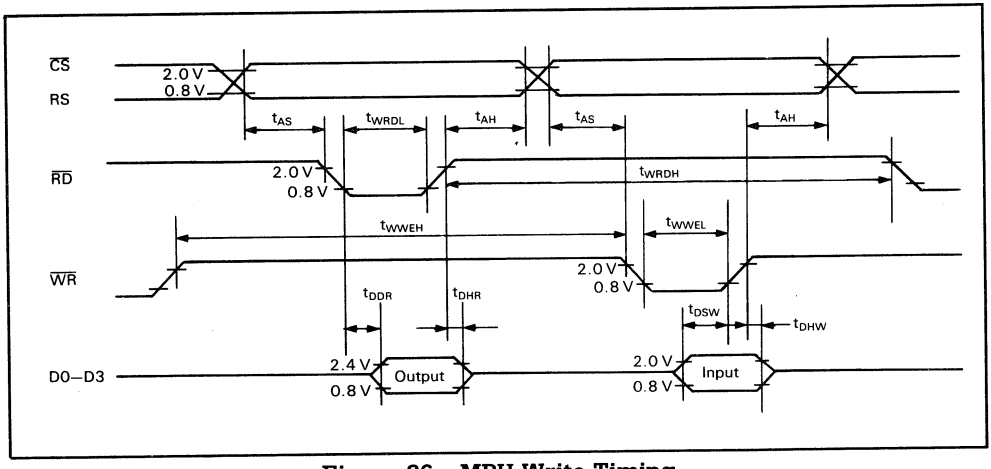


Figure 36. MPU Write Timing

Register Programming, ROM Write

Item	Symbol	Min	Max	Unit
A cycle time	t_{CYCA}	528	—	ns
A rise time	t_{Ar}	—	100	ns
A fall time	t_{Af}	—	100	ns
D ROM data setup time	t_{DSWD}	120	—	ns
D ROM data hold time	t_{DHWD}	0	—	ns

Note: $t_{CYCA} = 16\ t_{CYCD}$

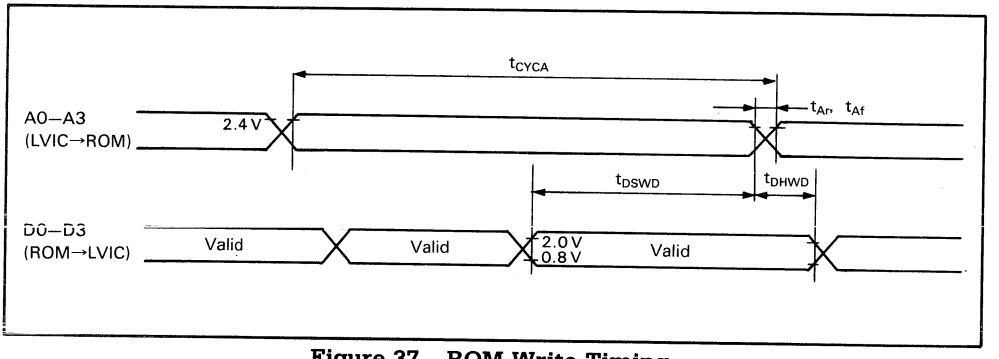


Figure 37. ROM Write Timing

PLL Interface

Item	Symbol	Min	Max	Unit
$\overline{CU}$ fall delay time	t_{Uf}	—	80	ns
$\overline{CU}$ rise delay time	t_{Ur}	—	80	ns
$\overline{CD}$ fall delay time	t_{Df}	—	80	ns
$\overline{CD}$ rise delay time	t_{Dr}	—	80	ns

Reset Input

Item	Symbol	Min	Max	Unit
$\overline{RES}$ input pulse width	$t_{\overline{RES}}$	1	—	μs

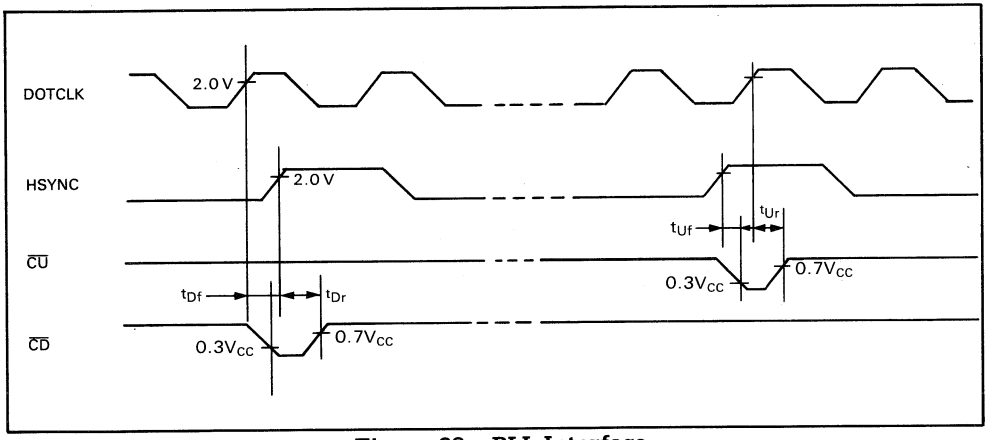


Figure 38. PLL Interface

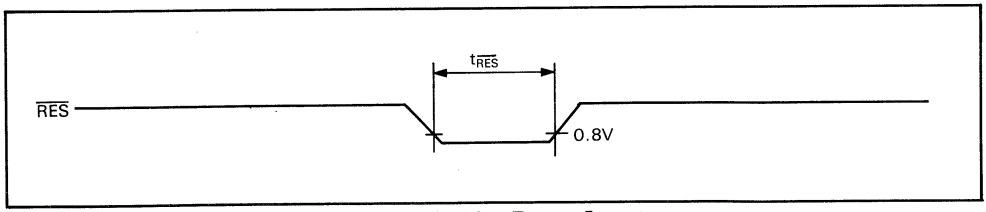


Figure 39. Reset Input

Load Circuits

TTL Load

Pin	R_L	R	C_L	Remarks
MA0-MA15, $\overline{MWE}$, $\overline{MCS0}$, $\overline{MCS1}$, RD0-RD7, GD0-GD7, BD0-BD7	2.4 kΩ	11 kΩ	40 pF	tr, tf: Not specified
A0/RD/XDOT, A1/YL0-A3/YL2	2.4 kΩ	11 kΩ	40 pF	tr, tf: Specified

Capacitive Load

Pin	C	Remarks
CL1, CL2, CL3, CL4	40 pF	tr, tf: Specified
R0-R3, G0-G3, B0-B3, FLM $\overline{CU}$, $\overline{CD}$	40 pF	tr, tf: Not specified

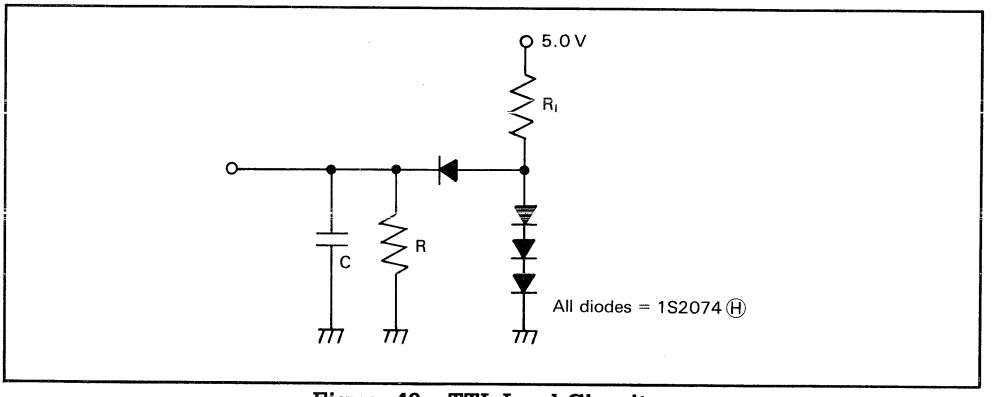


Figure 40. TTL Load Circuit

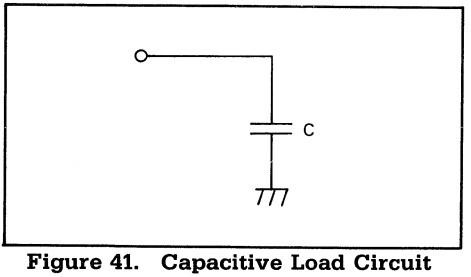


Figure 41. Capacitive Load Circuit

Refer to application note (No. ADE-502-011) for detail of this product.

Preliminary

HD66841

LCD Video Interface Controller (LVIC)

Description

The HD66841 LCD video interface controller (LVIC) converts standard RGB video signals for CRT display into LCD data. It enables a CRT display system to be replaced by an LCD system without any changes, and it also enables software originally intended for CRT display to control an LCD.

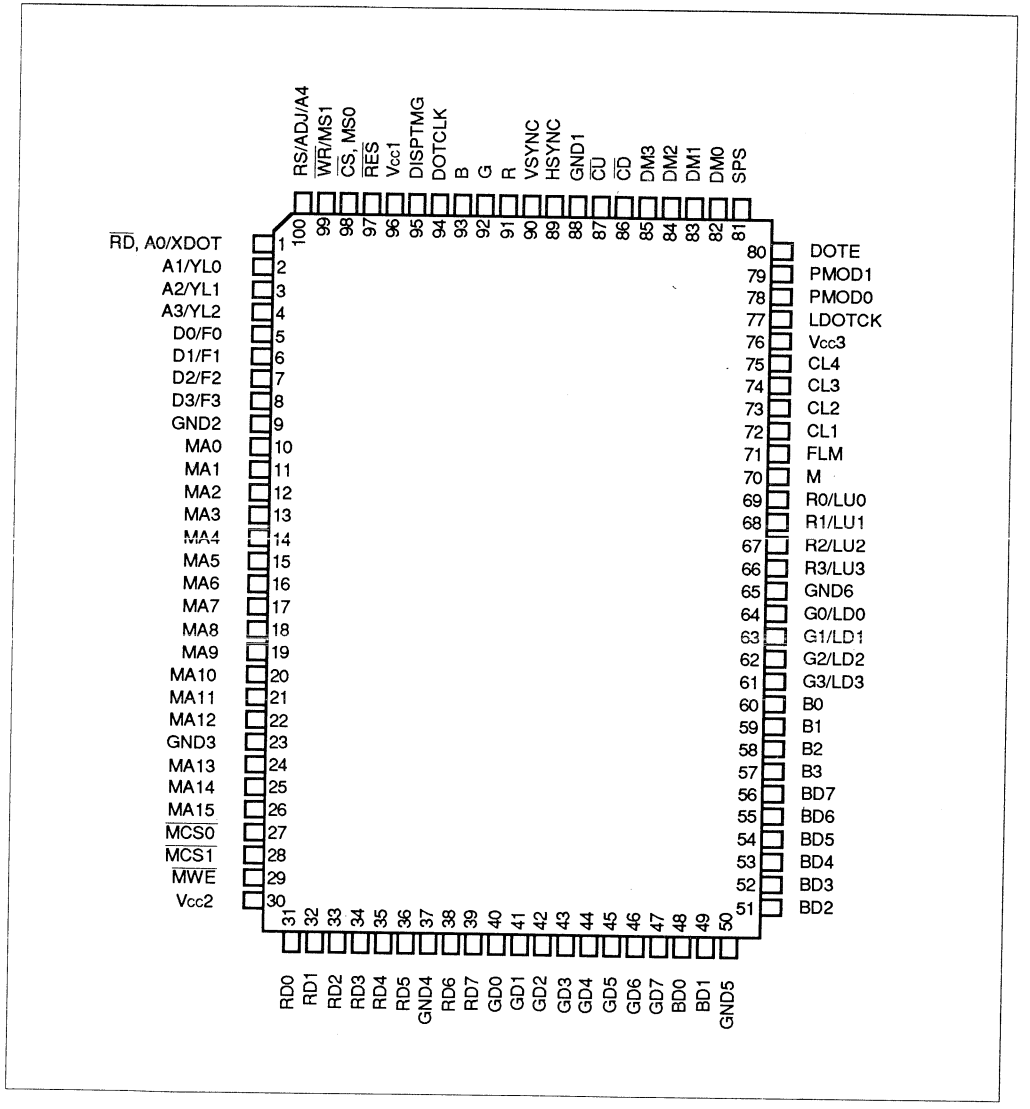
Since the LVIC can control TFT-type LCDs in addition to current TN-type LCDs, it can support monochrome, 8-level gray-scale, and 8-color displays. Thanks to a gray-scale palette, any 8 levels can be selected from 13 gray-scale levels, depending on the LCD panel used.

The LVIC also features a programmable screen size and can control a large-panel LCD of up to 720 × 512 dots.

Features

- Conversion of RGB video signals used for CRT display into LCD data:
  - Monochrome display data
  - 8-level gray-scale data
  - 8-color display data
- Selectable LVIC control method:
  - Pin programming method
  - Internal register programming method (either with MPU or ROM)
- Programmable screen size:
  - 640 or 720 dots (80 or 90 characters) wide by 200, 350, 400, 512, or 540 dots (lines) high, using the pin programming method
  - 32 to 4048 dots (4 to 506 characters) wide by 4 to 1024 dots (lines) high, using the internal register programming method
- Double-height display capability
- Generation of display timing signal (DISPTMG) from horizontal synchronization (HSYNC) and vertical synchronization (VSYNC) signals
- Internal PLL circuit capable of generating a CRT display dot clock (DOTCLK) (external charge pump, low pass filter (LPF), and voltage-controlled oscillator (VCO) required)
- Control of both TN-type LCDs and TFT-type LCDs
- Gray-scale level selection from gray-scale palette
- Maximum operating frequency: 30MHz (DOTCLK)
- LCD driver interface: 4-, 8-, or 12-bit (4 bits each for R, G, and B) parallel data transfer
- Recommended LCD drivers: HD61104 (column), HD61105 (row), HD66106 and HD66107 (column/row)
- Direct interface with buffer memory (no external decoder required)
- 1.3-µm CMOS processing
- Single power supply: +5V ± 5%
- Package: 100-pin plastic QFP (FP-100A)

Pin Arrangement



Pin Description

The LVIC's pins are listed in table 1 and their functions are described below.

Table 1 Pin List

Classification	Symbol	Pin Number	Pin Name	I/O	Note(s)
Power supply	$V_{CC}1$–$V_{CC}3$	96, 30, 76	$V_{CC}1$ to $V_{CC}3$	—	
	GND1–GND6	88, 9, 23, 37, 50, 65	Ground 1 to ground 6	—	
Video signal interface	R, G, B	91, 92, 93	Red, green, and blue serial data	I	1
	HSYNC	89	Horizontal synchronization	I	
	VSYNC	90	Vertical synchronization	I	
	DISPTMG	95	Display timing	I	2
	DOTCLK	94	Dot clock	I	
LCD interface	R0–R3	69–66	LCD red data 0–3	O	3
	LU0–LU3	69–66	LCD upper panel data 0–3	O	4
	G0–G3	64–61	LCD green data 0–3	O	3, 5
	LD0–LD3	64–61	LCD lower panel data 0–3	O	4, 5
	B0–B3	60–57	LCD blue data 0–3	O	3, 6
	CL1	72	LCD data line select clock	O	
	CL2	73	LCD data shift clock	O	
	CL3	74	Y-driver shift clock 1	O	7
	CL4	75	Y-driver shift clock 2	O	7
	FLM	71	First line marker	O	
	M	70	LCD driving signal alternation	O	
	LDOTCK	77	LCD dot clock	I	
Buffer memory interface	$\overline{MCS0}$, $\overline{MCS1}$	27, 28	Memory chip select 0, 1	O	8
	$\overline{MWE}$	29	Memory write enable	O	8
	MA0–MA15	10–22, 24–26	Memory address 0–15	O	8
	RD0–RD7	31–36, 38, 39	Memory red data 0–7	I/O	8
	GD0–GD7	40–47	Memory green data 0–7	I/O	8, 9
	BD0–BD7	48, 49, 51–56	Memory blue data 0–7	I/O	8, 9
Mode setting	PMOD0, PMOD1	78, 79	Program mode 0, 1	I	
	DOTE	80	Dot clock edge change	I	
	SPS	81	Synchronization polarity select	I	
	DM0–DM3	82–85	Display mode 0–3	I	
	MS0, MS1	98, 99	Memory select 0, 1	I	10, 11
	XDOT	1	X-dot	I	10
	YL0–YL2	2–4	Y-line 0–2	I	10, 12

Table 1 Pin List (cont)

Classification	Symbol	Pin Number	Pin Name	I/O	Note(s)
Mode setting	ADJ	100	Adjust	I	10
	F0–F3	5–8	Fine adjust 0–3	I	10
MPU interface	$\overline{CS}$	98	Chip select	I	10, 11
	$\overline{WR}$	99	Write	I	10, 11, 13
	$\overline{RD}$	1	Read	I	10, 13
	RS	100	Register select	I	10
	D0–D3	5–8	Data 0–3	I/O	10
	$\overline{RES}$	97	Reset	I	14
ROM interface	A0–A4	1–4, 100	Address 0–4	O	10
	D0–D3	5–8	Data 0–3	I	10
PLL interface	$\overline{CD}$	86	Charge down	O	
	$\overline{CU}$	87	Charge up	O	

Notes:
1. Fix G and B pins low if CRT display data is monochrome.
2. Fix high or low if the display timing signal is generated internally.
3. For 8-color display modes.
4. For monochrome or 8-level gray-scale display modes.
5. Leave disconnected in 4-bit/single-screen data transfer modes.
6. Leave disconnected in monochrome or 8-level gray-scale display modes.
7. Leave disconnected in TN-type LCD modes.
8. Leave disconnected if no buffer memory is used.
9. Pull up with a resister of about 20kΩ in monochrome display modes.
   The LVIC writes the OR of RGB signals into R-plane RAM, so no RAM is required for the G and B planes in these modes. (If G- or B-plane RAM is connected in monochrome display modes, the LVIC writes G or B signals into each RAM. However, this does not affect the display or the contents of R-plane RAM.)
10. Multiplexed pins.
11. Fix high or low when using the ROM programming method.
12. Fix high or low when using the MPU programming method.
13. Do not set pins $\overline{WR}$ and $\overline{RD}$ low simultaneously.
14. A reset signal must be input after power-on.

Power Supply

$V_{CC}1$–$V_{CC}3$: Must be connected to a +5V power supply.

GND1–GND6: Must be grounded.

CRT Display Interface

R, G, B: Input R, G, and B signals for CRT display.

HSYNC: Inputs the CRT horizontal synchronization signal.

VSYNC: Inputs the CRT vertical synchronization signal.

DISPTMG: Inputs the display timing signal which indicates the horizontal or vertical display period.

DOTCLK: Inputs dot clock pulses used for CRT display.

LCD Interface

R0–R3: Output LCD R data

LU0–LU3: Output LCD upper panel data.

G0–G3: Output LCD G data.

LD0–LD3: Output LCD lower panel data.

B0–B3: Output LCD B data.

CL1: Outputs line select clock pulses for LCD data.

CL2: Outputs shift clock pulses for LCD data.

CL3: Outputs line select and shift clock pulses for LCD data if Y-drivers are positioned on one side of the LCD screen. Refer to the LCD System Configuration section for details.

CL4: Outputs line select and shift clock pulses for LCD data if Y-drivers are positioned on both sides of the LCD screen. Refer to the LCD System Configuration section for details.

FLM: Outputs a first line marker for Y-drivers.

M: Outputs an alternation signal for converting convert LCD driving signals to AC.

LDOTCK: Inputs LCD dot clock pulses.

Buffer Memory Interface

$\overline{MCS0}$, $\overline{MCS1}$: Output buffer memory chip select signals.

$\overline{MWE}$: Outputs the buffer memory write enable signal.

MA0–MA15: Output buffer memory addresses.

RD0–RD7: Transfer data between R-data buffer memory and the LVIC.

GD0–GD7: Transfer data between G-data buffer memory and the LVIC.

BD0–BD7: Transfer data between B-data buffer memory and the LVIC.

Mode Setting

PMOD0, PMOD1: Select the programming method for the LVIC (table 2).

DOTE: Switches data latch timing. The LVIC latches RGB signals at the falling edge of DOTCLK pulses if the DOTE pin is set high, or at the rising edge if it is set low.

SPS: Selects the polarity of the VSYNC signal. (The HSYNC signal's polarity is fixed.) The VSYNC signal is active-high if SPS is set high, or active-low if it is set low.

DM0–DM3: Select the display mode (table 8).

MS0–MS1: Select the buffer memory type (table 3).

XDOT: Specifies the number of characters displayed on the LCD screen in the horizontal direction (called the horizontal displayed characters). The number is 90 (720 dots) if XDOT is set high, or 80 (640 dots) if it is set low.

YL0–YL2: Specify the number of lines displayed on the LCD screen in the vertical direction (called the vertical displayed lines) (table 4).

ADJ: Determines whether the F0–F3 pins adjust the display timing signal or the number of vertical displayed lines. The pins adjust the display timing signal if ADJ is set high, or the number of vertical displayed lines if it is set low.

F0–F3: Adjust the number of vertical displayed lines (table 5) or the display timing signal. Refer to the Display Timing Signal Fine Adjustment section for details.

MPU Interface

$\overline{CS}$: An MPU inputs the $\overline{CS}$ signal through this pin to select the LVIC. The MPU can access the LVIC while this signal is low.

$\overline{WR}$: An MPU inputs the $\overline{WR}$ signal through this pin to write data into the LVIC's internal registers. The MPU can write data while this signal is low.

$\overline{RD}$: An MPU inputs the $\overline{RD}$ signal through this pin to read data from the LVIC's internal registers. The MPU can read data while this signal is low.

RS: An MPU inputs the RS signal through this pin to select the LVIC's internal registers. The MPU can access data registers (R0–R15) while this signal is high and the $\overline{CS}$ signal is low, and can select the address register (AR) while both this signal and the $\overline{CS}$ signal are low.

D0–D3: Transfer LVIC internal register data between an MPU and the LVIC.

$\overline{RES}$: Externally resets the LVIC.

ROM Interface

A0–A4: Output external ROM addresses.

D0–D3: Input external ROM data to the LVIC's internal registers.

PLL Circuit Interface

$\overline{CD}$: Outputs charge-down signals to an external charge pump.

$\overline{CU}$: Outputs charge-up signals to an external charge pump.

Table 2 Programming Method Selection

PMOD1	PMOD0	Programming Method	
0	0	Pin programming	
0	1	Internal register programming	MPU
1	0		ROM
1	1	Inhibited (Note)	

Note: This combination is for test mode: it disables display.

Table 3 Memory Type Selection

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbyte memory
1	0	32-kbyte memory
1	1	64-kbyte memory

Table 4 Number of Vertical Displayed Lines

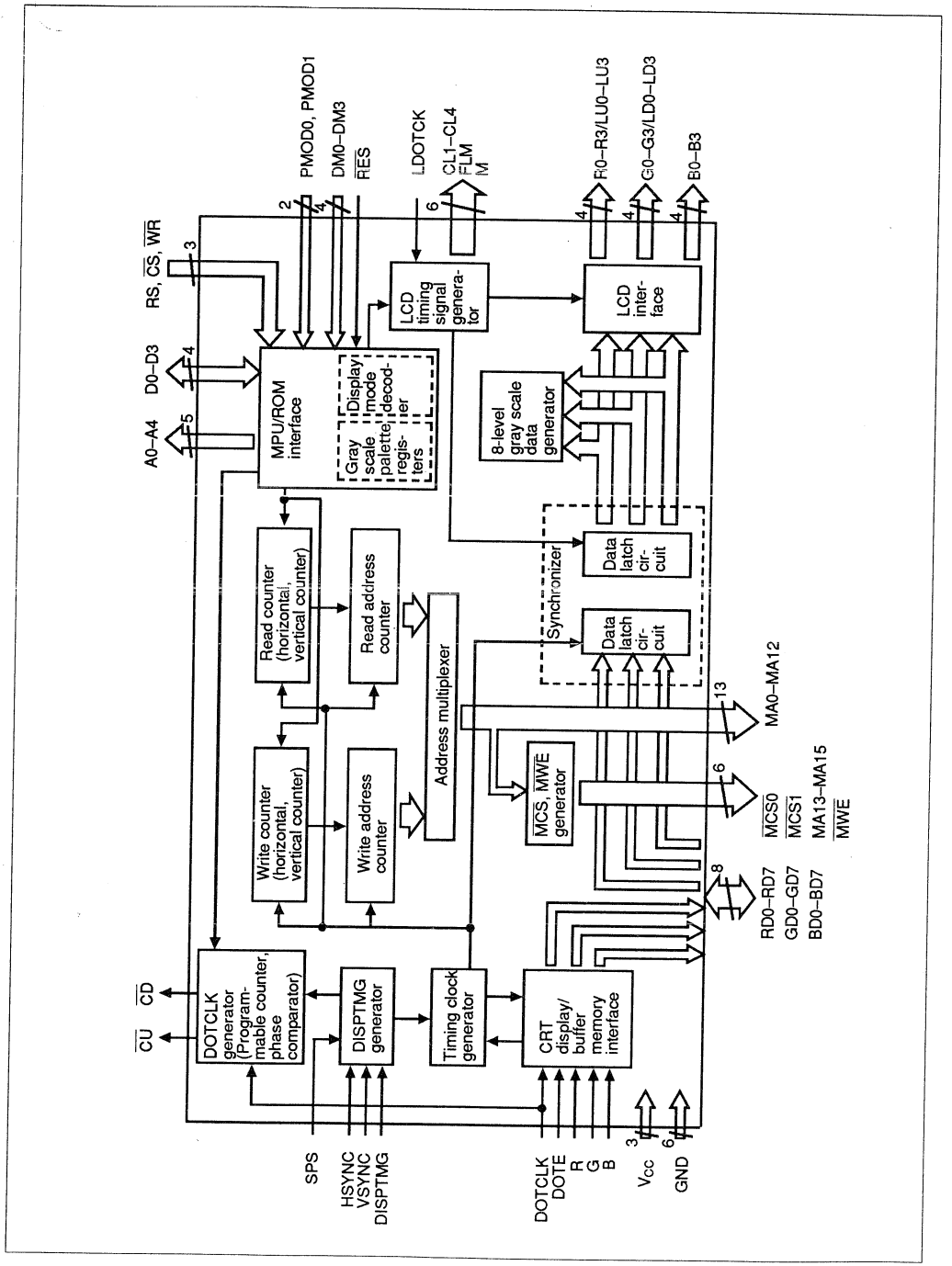
YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Inhibited (Note)
1	1	1	

Note: 480 lines are displayed, but they are practically indistinguishable.

Table 5 Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Adjusted Lines
0	0	0	0	±0
0	0	0	1	+1
0	0	1	0	+2
⋮	⋮	⋮	⋮	⋮
1	1	1	0	+14
1	1	1	1	+15

Block Diagram



Registers

The LVIC's registers are listed in table 6 and the bit assignments within the registers are shown in figure 1

Table 6 Register List

$\overline{CS}$	RS	PS[1]	Reg. Address 3	2	1	0	Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/ Write[2]	Note(s)
1	—		—	—	—	—	—	—	—	—	—	
0	0		—	—	—	—	AR	Address register	—	—	W	3
0	1	0	0	0	0	0	R0	Control register 1	—	—	R/W	
0	1	0	0	0	0	1	R1	Control register 2	—	—	R/W	
0	1	0	0	0	1	0	R2	Vertical displayed lines register (middle-order)	Lines	Nvd	R/W	4
0	1	0	0	0	1	1	R3	Vertical displayed lines register (low-order)	Lines	Nvd	R/W	4
0	1	0	0	1	0	0	R4	Vertical displayed lines register (high-order)/ CL3 period register (high-order)	Lines/ Chars.	Nvd/ Npc	R/W	4, 5, 6
0	1	0	0	1	0	1	R5	CL3 period register (low-order)	Chars.	Npc	R/W	4, 5, 6
0	1	0	0	1	1	0	R6	Horizontal displayed characters register (high-order)	Chars.	Nhd	R/W	6
0	1	0	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Chars.	Nhd	R/W	6
0	1	0	1	0	0	0	R8	CL3 pulse width register	Chars.	Npw	R/W	6
0	1	0	1	0	0	1	R9	Fine adjust register	Dots	Nda	R/W	7
0	1	0	1	0	1	0	R10	PLL frequency-division ratio register (high-order)	—	N_{PLL}	R/W	8
0	1	0	1	0	1	1	R11	PLL frequency-division ratio register (low-order)	—	N_{PLL}	R/W	8
0	1	0	1	1	0	0	R12	Vertical backporch register (high-order)	Lines	Ncvbp	R/W	4, 9
0	1	0	1	1	0	1	R13	Vertical backporch register (low-order)	Lines	Ncvbp	R/W	4, 9
0	1	0	1	1	1	0	R14	Horizontal backporch register (high-order)	Dots	Nchbp	R/W	4, 9
0	1	0	1	1	1	1	R15	Horizontal backporch register (low-order)	Dots	Nchbp	R/W	4, 9

Table 6 Register List (cont)

$\overline{CS}$	RS	PS[1]	Reg. Address 3	2	1	0	Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/ Write[2]	Note(s)
0	1	1	0	0	0	1	P1	Black palette register	—	—	R/W	
0	1	1	0	0	1	0	P2	Blue palette register	—	—	R/W	
0	1	1	0	0	1	1	P3	Red palette register	—	—	R/W	
0	1	1	0	1	0	0	P4	Magenta palette register	—	—	R/W	
0	1	1	0	1	0	1	P5	Green palette register	—	—	R/W	
0	1	1	0	1	1	0	P6	Cyan palette register	—	—	R/W	
0	1	1	0	1	1	1	P7	Yellow palette register	—	—	R/W	
0	1	1	1	0	0	0	P8	White palette register	—	—	R/W	
0	1	1	1	0	0	1		Reserved				
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮				
0	1	1	1	1	1	1		Reserved				

Notes:
1. Corresponds to bit 2 of control register 1 (R0)
2. W indicates that the register can only be written to; R/W indicates that the register can both be read from and written to.
3. Attempting to read data from this register when RS = 0 drives the bus to high-impedance state; output data becomes undefined.
4. Write (the specified value – 1) into this register.
5. Valid only in 8-color display modes with horizontal stripes.
6. One character consists of eight horizontal dots.
7. Valid only if the display timing signal is supplied externally.
8. Valid only if the dot clock signal is generated internally.
9. Valid only if the display timing signal is generated internally.

$\overline{CS}$	RS	PS[1]	Reg. Address 3	2	1	0	Reg. No.	Data Bits 3	2	1	0	
1	—	—	—	—	—	—	—	– [2]				
0	0	—	—	—	—	—	AR					← Address register
0	1	—	0	0	0	0	R0	DIZ	PS	DSP	DCK	← Control register 1
0	1	0	0	0	0	1	R1	MC	DON	MS1	MS0	← Control register 2
0	1	0	0	0	1	0	R2					← Vertical displayed lines register
0	1	0	0	0	1	1	R3					
0	1	0	0	1	0	0	R4					
0	1	0	0	1	0	1	R5					← CL3 period register
0	1	0	0	1	1	0	R6[3]					← Horizontal displayed characters register
0	1	0	0	1	1	1	R7					
0	1	0	1	0	0	0	R8					← CL3 pulse width register
0	1	0	1	0	0	1	R9					← Fine adjust register
0	1	0	1	0	1	0	R10					← PLL frequency-division ratio register
0	1	0	1	0	1	1	R11					
0	1	0	1	1	0	0	R12					← Vertical backporch register
0	1	0	1	1	0	1	R13					
0	1	0	1	1	1	0	R14					← Horizontal backporch register
0	1	0	1	1	1	1	R15					
0	1	1	0	0	0	1	P1[4]	0	0	0	0	← Black palette register
0	1	1	0	0	1	0	P2[4]	0	0	1	0	← Blue palette register
0	1	1	0	0	1	1	P3[4]	0	1	0	1	← Red palette register
0	1	1	0	1	0	0	P4[4]	0	1	1	0	← Magenta palette register
0	1	1	0	1	0	1	P5[4]	0	1	1	1	← Green palette register
0	1	1	0	1	1	0	P6[4]	1	0	0	0	← Cyan palette register
0	1	1	0	1	1	1	P7[4]	1	0	1	0	← Yellow palette register
0	1	1	1	0	0	0	P8[4]	1	1	0	0	← White palette register
0	1	1	1	0	0	1	—	– [5]				← Reserved registers
⋮	⋮	⋮		⋮								
0	1	1	1	1	1	1	—					

Notes:
1. Corresponds to bit 2 of control register 1 (R0).
2. Invalid bits. Attempting to read data from these bits returns undefined data.
3. The most significant bit is invalid in dual-screen configuration modes.
4. Bit values shown are default values at reset.
5. Reserved bits. Any attempt to write data into the register is invalid, although it has no affect on LSI operations. Any attempt to read data from the register returns undefined data.

Figure 1 Register Bit Assignment

System Description

Figure 2 is a block diagram of a system in which the LVIC is used outside a personal computer.

The LVIC converts the RGB serial data sent from the personal computer into parallel data and temporarily writes it to the buffer memory. It then reads out the data in order and outputs it to LCD drivers to drive the LCD. In this case, the CRT display dot clock (DOTCLK), which is a latch clock for serial data, is generated by the PLL circuit from the horizontal synchronization signal (HSYNC). The DOTCLK signal frequency is specified by the PLL frequency-division ratio register (R10, R11).

The system can be configured without a VCO and LPF if the DOTCLK signal is supplied externally, and it can be configured without an MPU if the LVIC is controlled by the pin programming method.

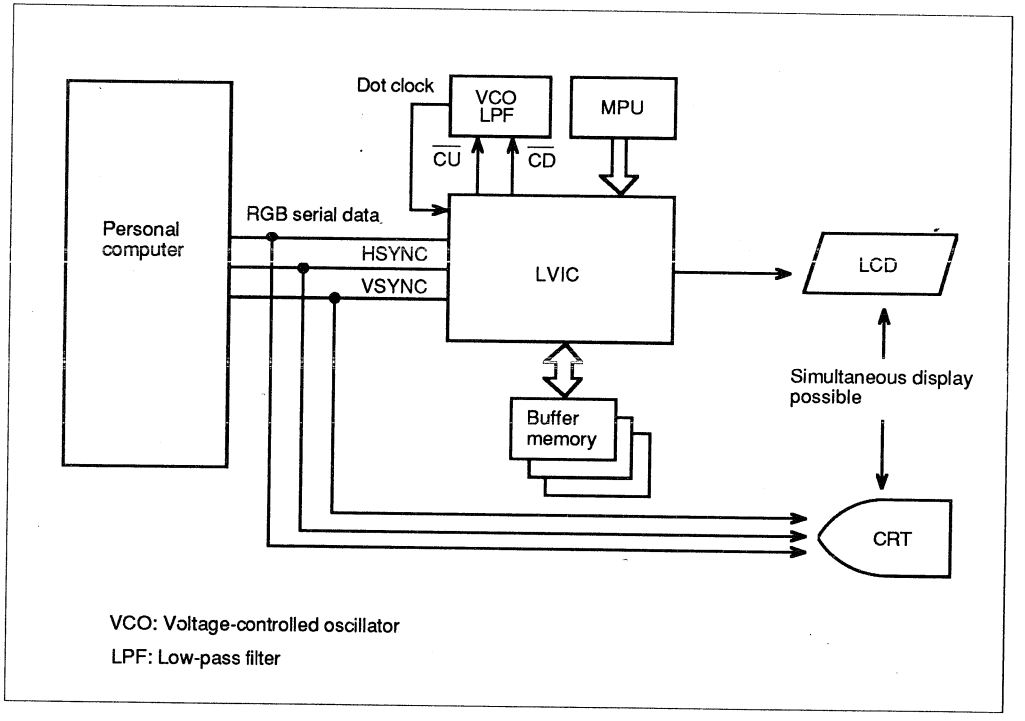


Figure 2 System Block Diagram (with MPU programming method and DOTCLK generated internally)

Functional Description

Programming Method

One of two methods of controlling LVIC functions can be selected by setting pins PMOD0 and PMOD1. Control by pins is called the pin programming method and control by internal registers is called the internal register programming method. The internal register programming method can be further divided into the MPU programming method and the ROM programming method; an MPU is used to write data into internal registers in the MPU programming method and ROM is used to write data into internal registers in the ROM programming method.

Pin Programming Method: The LVIC's mode-setting pins control functions.

Internal Register Programming Method: An MPU or ROM is used to write data into the LVIC's internal registers to control functions. Figure 3 shows the connection of either an MPU or ROM to the LVIC. Although figure 3 (1) shows an example of the use of a 4-bit microprocessor, the LVIC can also be connected directly to the host MPU bus since the LVIC MPU bus is compatible with the 4-MHz bus of 80-series microcomputers.

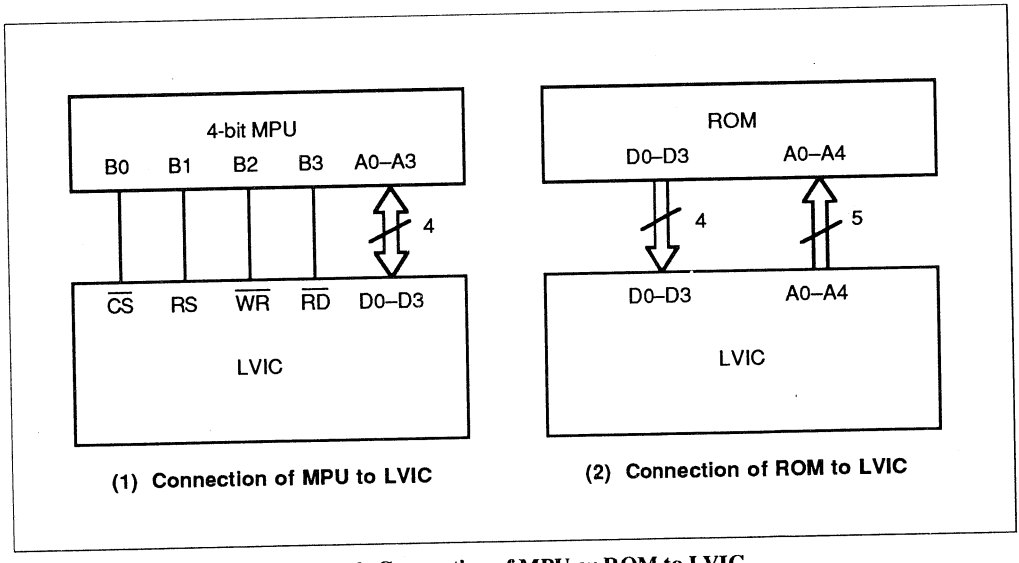


Figure 3 Connection of MPU or ROM to LVIC

Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, either 640 dots or 720 dots (80 characters or 90 characters) can be selected with the XDOT pin as the number of horizontal displayed characters, and either 200, 350, 400, 480, 512, or 540 lines can be selected with the YL2–YL0 pins as the number of vertical displayed lines. The number of vertical displayed lines can be adjusted by from +0 to +15 lines with the ADJ and F3–F0 pins.

In the internal register programming method, any even number of characters form 4 to 506 (from 32 to 4048 dots) can be selected with the horizontal displayed characters register (R6, R7), and any even number of lines from 4 to 1028 can be selected with the vertical displayed lines register (R2, R3, and the high-order two bits of R4). However, note that an odd number of lines can also be selected if the screen configuration is single-screen and Y-drivers (scan drivers) are positioned on one side of the LCD screen.

The relationship between the LCD screen and the pins and internal registers controlling screen size is shown in figure 4.

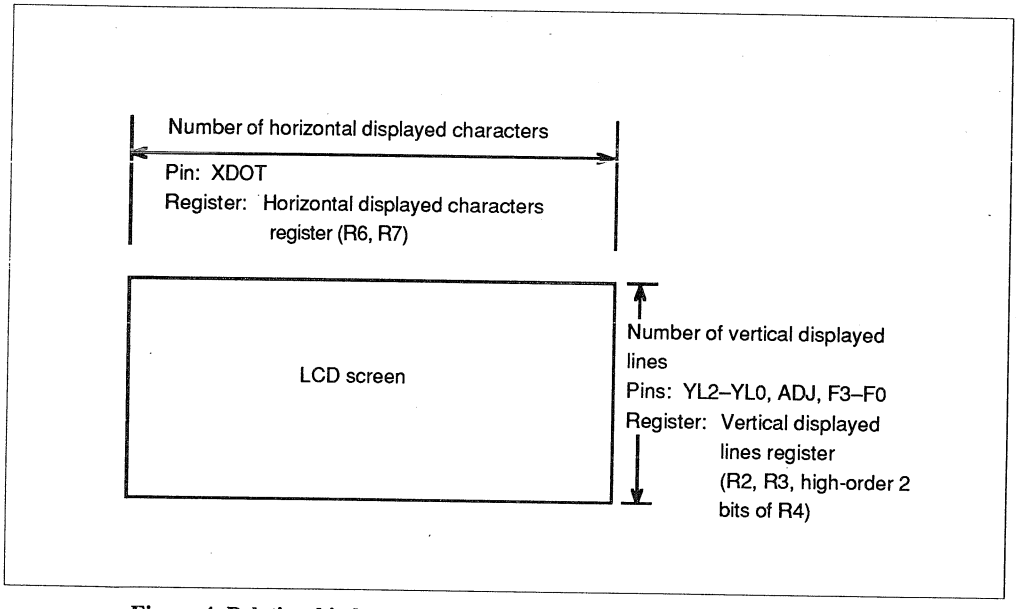


Figure 4 Relationship between LCD Screen and Pins and Internal Registers

Memory Selection

8-, 32-, or 64-kbyte SRAMs can be selected as buffer memory for the LVIC. Since the LVIC has a chip select circuit for memory, no external decoder is required. The memory type can be selected with the MS1 and MS0 pins or the MS1 and MS0 bits of control register 2 (R1). Memory types and corresponding pin address assignments are listed in table 7.

The memory capacity required depends on screen size and can be obtained from the following equation:

Memory capacity (bytes) = Nhd × Nvd

Nhd: Number of horizontal displayed characters (where one character consists of 8 horizontal dots)

Nvd: Number of vertical displayed lines

For example, a screen of 640 × 200 dots requires a 16-kbyte memory capacity since 80 characters × 200 lines is 16 kbytes. Consequently, each plane requires two HM6264s (8-kbyte memories) in 8-level gray-scale display modes. The $\overline{MCS0}$ pin must be connected to the $\overline{CS}$ pin of one of the memory chips in each plane, and the $\overline{MCS1}$ pin must be connected to the $\overline{CS}$ pin of the remaining memory chip in each plane (figure 5 (a)).

A screen of 640 × 400 dots requires a 32-kbyte (256-kbit) memory capacity, so each plane requires an HM62256, which is a 32-kbyte memory. In this case, the $\overline{MCS0}$ pin must be connected to the $\overline{CS}$ pin of each memory chip. (figure 5 (b)).

Table 7 Memories and Pin Address Assignments

Pins or Bits					Address
MS1	MS0	Memory	Address Pins	Chip Select Pins	Assignment
0	0	No memory [Note]	—	—	—
0	1	8-kbyte	MA0–MA12	$\overline{MCS0}$	$0000–$1FFF
				$\overline{MCS1}$	$2000–$3FFF
				MA13	$4000–$5FFF
				MA14	$6000–$7FFF
				MA15	$8000–$9FFF
1	0	32-kbyte	MA0–MA14	$\overline{MCS0}$	$00000–$07FFF
				$\overline{MCS1}$	$08000–$0FFFF
				MA15	$10000–$17FFF
1	1	64-kbyte	MA0–MA15	$\overline{MCS0}$	$00000–$0FFFF
				$\overline{MCS1}$	$10000–$1FFFF

Note: There are some limitations if no memory is used. Refer to the User Notes section for details.

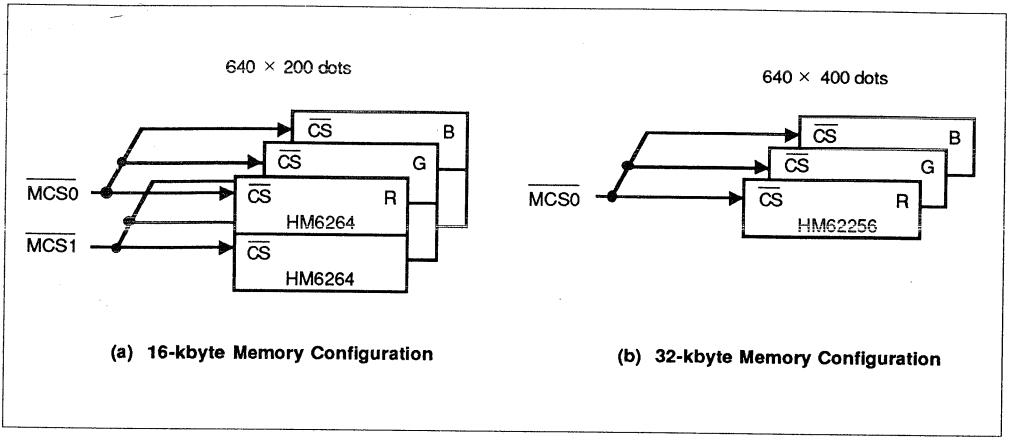


Figure 5 Screen Size and Memory Configuration

Display Modes

The LVIC supports 16 display modes, depending on the states of the DM3–DM0 pins. The display mode controls display color, type of LCD data output, positions of LCD drivers for the LCD screen, arrangement of color data (type of stripes), and method of M signal output (type of alternation signal). Display modes are listed in table 8.

Table 8 Display Mode List

Mode No.	Pins DM3	DM2	DM1	DM0	Display Color	Data Transfer Type	Screen Config.	LCD Driver Positions X-driver[2]	Y-Driver[3]	Stripe[4]	Alternation
1	0	0	0	0	Mono-	4-bit	Dual	One side	One side	—	Every frame
2	0	0	0	1	chrome		Single				
3[1]	0	0	1	0					Both sides		
4	0	0	1	1		8-bit			One side		
5[1]	0	1	0	0					Both sides		
6	0	1	0	1	8-level	4-bit	Dual		One side		
7	0	1	1	0	gray scale		Single				
8	0	1	1	1		8-bit					
9[1]	1	0	0	0	8-color	12-bit				Vertical	Every line
10[1]	1	0	0	1		(4 bits each			Both sides		
11[1]	1	0	1	0		for R, G, and B)		Both sides	One side		
12[1]	1	0	1	1					Both sides		
13[1]	1	1	0	0				One side	One side	Horizontal	
14[1]	1	1	0	1					Both sides		
15[1]	1	1	1	0				Both sides	One side		
16	1	1	1	1			Dual	One side		Vertical	Every frame

Notes: 1. For TFT-type LCDs.
2. Data output driver.
3. Scan driver.
4. Refer to the 8-Color Display section.

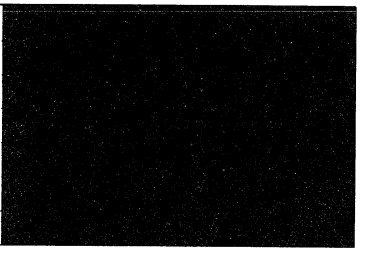
Display Color

The LVIC converts the RGB color data normally used for CRT display into monochrome, 8-level gray-scale, or 8-color display data.

Monochrome Display (Modes 1 to 5): The LVIC displays two colors: black (display on) and white (display off). As shown in table 9, the CRT display RGB data is ORed to determine display on/off.

Table 9 Monochrome Display

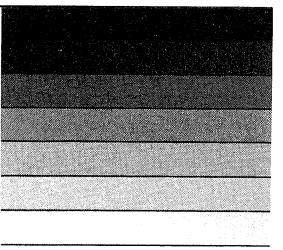
CRT Display Data				LCD	
R	G	B	CRT Display Color	On/Off	Color
1	1	1	White	On	Black
1	1	0	Yellow	On	Black
0	1	1	Cyan	On	Black
0	1	0	Green	On	Black
1	0	1	Magenta	On	Black
1	0	0	Red	On	Black
0	0	1	Blue	On	Black
0	0	0	Black	Off	White



8-Level Gray Scale Display (Modes 6 to 8): The LVIC thins out data on certain lines or dots to provide an 8-level gray-scale display based on CRT display color (luminosity). The relationship between CRT display color (luminosity) and LCD gray scale (contrast) is shown in table 10. This relationship corresponds to the default values in palette register. The correspondence between color and gray scale can be changed by writing data into palette registers.

Table 10 8-Level Gray-Scale Display

CRT Display Data			CRT		LCD	
R	G	B	Color	Luminosity	Gray Scale	Contrast
1	1	1	White	High	Black	Strong
1	1	0	Yellow			
0	1	1	Cyan			
0	1	0	Green			
1	0	1	Magenta			
1	0	0	Red			
0	0	1	Blue			
0	0	0	Black	Low	White	Weak



8-Color Display (Modes 9 to 16): The LVIC displays 8 colors through red (R), green (G), and blue (B) filters placed on liquid-crystal cells. The eight colors are the same as those provided by a CRT display. As shown in figure 6, 8-color display has two stripe modes: horizontal stripe mode in which the LVIC arranges RGB data horizontally for horizontal filters and vertical stripe mode in which it arranges RGB data vertically for vertical filters. Three cells express one dot in both modes.

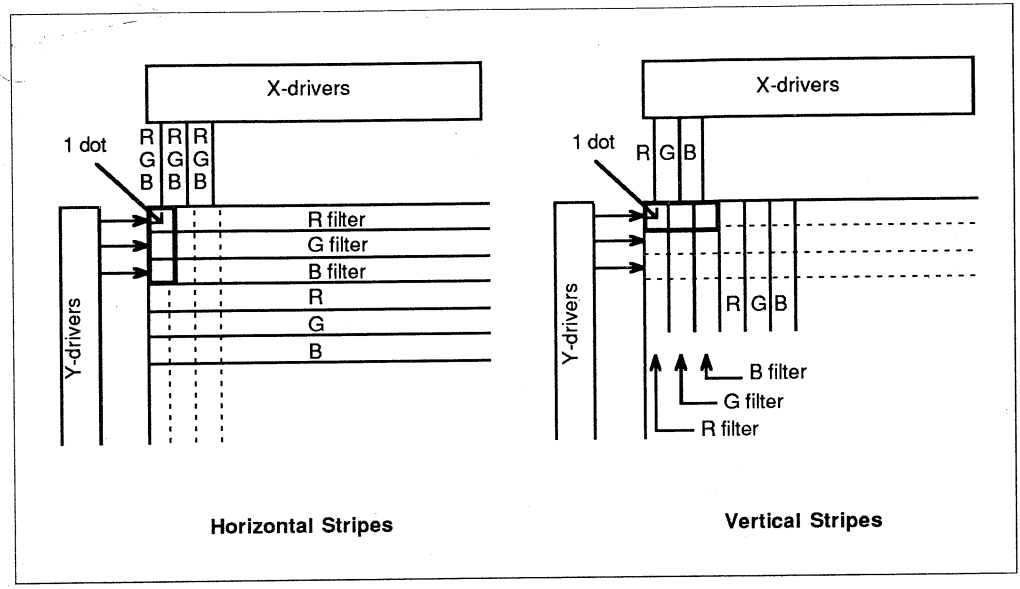


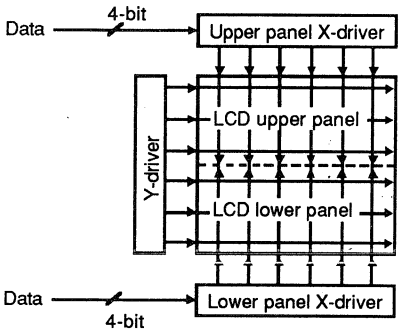
Figure 6 Stripe Modes in 8-Color Display

LCD System Configuration

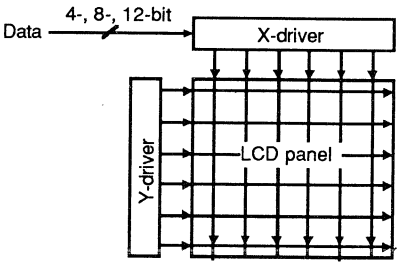
The LVIC supports the following LCD system configurations:

- Types of LCD data output:
  - Data transfer: 4-bit, 8-bit, or 12-bit (4 bits each for R, G, and B)
  - Screen configuration: Single or dual
- LCD driver positions around LCD screen:
  - X-drivers: On one side or on both sides
  - Y-drivers: On one side or on both sides

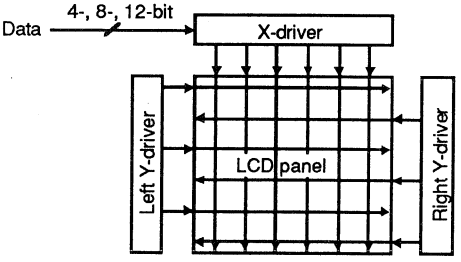
System configurations for different modes are shown in figure 7, and configurations of X- and Y-drivers positioned on both sides of an LCD screen are shown in figure 8.



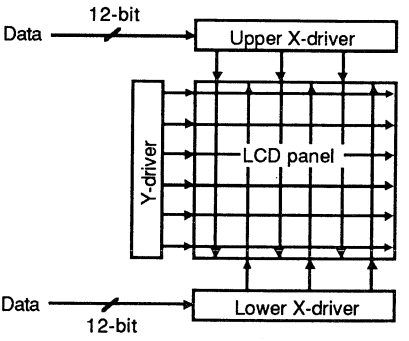
System configuration for mode 1 and mode 6 (4-bit data transfer, dual screen, X-driver and Y-driver each on one side)Note



System configuration for modes 2, 4, 7, 8, 9, and 13 (4-, 8-, or 12-bit data transfer, single screen, X-driver and Y-driver each on one side)



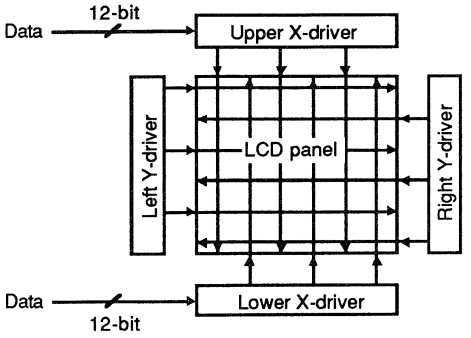
System configuration for modes 3, 5, 10, and 14 (4-, 8-, or 12-bit data transfer, single screen, X-driver on one side and Y-driver on both sides)



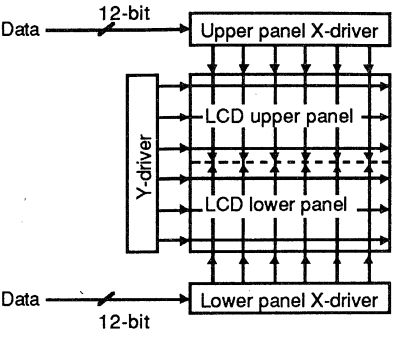
System configuration for mode 11 and mode 15 (12-bit data transfer, single screen, X-driver on both sides and Y-driver on one side)

Note: Since the LCD upper panel and lower panel are each regarded as one screen, the X-drivers are considered to be positioned on one side, not on both sides.

Figure 7 System Configurations by Mode



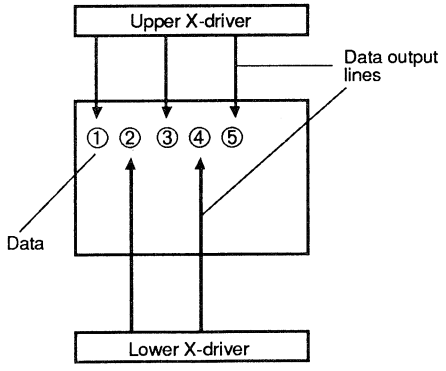
System configuration for mode 12 (12-bit data transfer, single screen, X-driver and Y-driver each on both sides)



System configuration for mode 16 (12-bit data transfer, dual screen, X-driver and Y-driver each on one side)Note

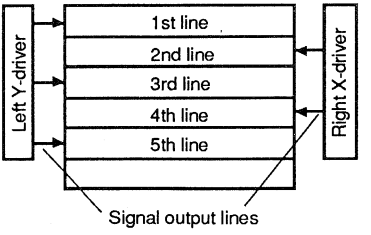
Note: Since the LCD upper panel and lower panel are each regarded as one screen, the X-drivers are considered to be positioned on one side, not on both sides.

Figure 7 System Configurations by Mode (cont)



(1) X-drivers set on both sides

Data output lines run alternately from upper and lower X-drivers, increasing the pitch of the lines to twise that X-drivers positioned on one side.



(2) Y-drivers set on both sides

Line select signal output lines run alternately from right and left Y-drivers, increasing the pitch of the lines to twice that for Y-drivers positioned on one side.

Figure 8 X- and Y-Drivers Set on Both Sides

LDOTCK Frequency Calculation

The frequency f_L of the LCD dot clock (LDOTCK) can be obtained from the following equation:

$f_L = (Nhd + 6) \times 8 \times Nvd \times f_F$

Nhd: Number of horizontal displayed characters on LCD = (number of horizontal displayed dots on LCD) × 1/8
Nvd: Number of vertical displayed lines on LCD
f_F: Frame frequency (FLM frequency)

In this case, f_L must satisfy the following relationships, where f_D is the frequency of the dot clock for CRT display (DOTCLK):

$f_L < f_D \times 15/16$ or

$f_L = f_D$ (the phase of LDOTCK must be opposite to that of DOTCLK in this case)

Display Timing Signal Generation

CRT display data is divided into display period data and retrace period data, so the LVIC needs a signal indicating whether the CRT display data that has just been transferred is display period data or not. This signal is called the display timing signal.

The LVIC can generate the display timing signal from the HSYNC and VSYNC signals. The relationships between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data are shown in figure 9. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal backporch register (R14, R15), respectively.

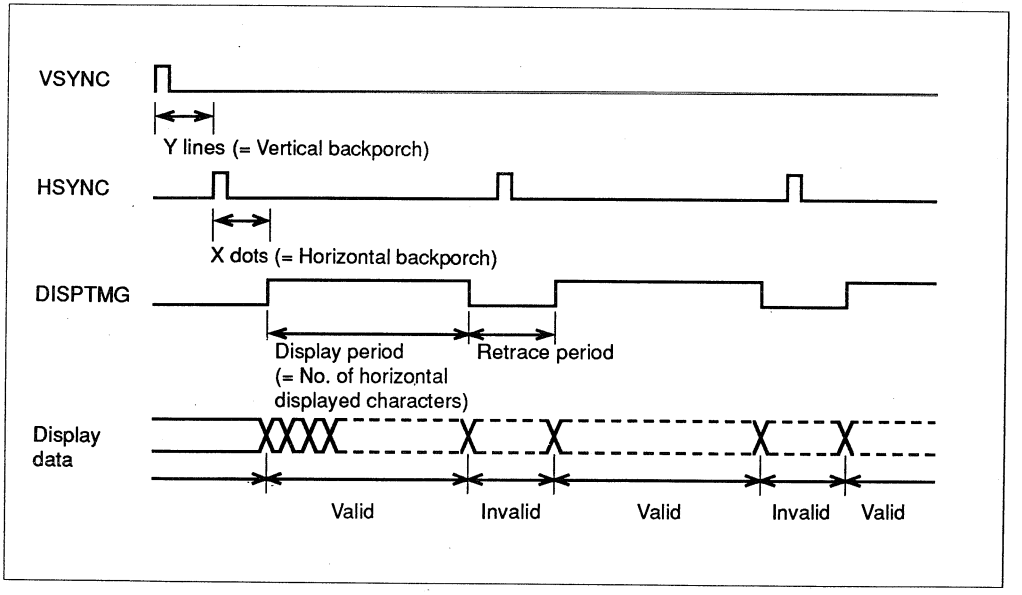


Figure 9 Relationships between HSYNC, VSYNC, DISPTMG, and Display Data

Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal, so it is not usually output from the CRT display plug. Therefore, the LVIC must generate it. The LVIC has a programmable counter and a phase comparator which are parts of a phase-locked loop (PLL) circuit, and it can generate the dot clock from the HSYNC signal if a charge pump, a low-pass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

A block diagram of the PLL circuit is shown in figure 10. A PLL circuit is a feedback controller that generates a clock whose frequency and phase are the same as those of a basic clock. The basic clock is the HSYNC signal in this case.

At power-on, the VCO outputs to the programmable counter a signal whose frequency is determined by the voltage at that time. The counter divides the frequency of the signal according to the value in the PLL frequency-division ratio register (R10, R11), and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock pulses and the HSYNC signal pulses and outputs the $\overline{CU}$ or $\overline{CD}$ signal to the charge pump and LPF according to the result. The comparator outputs the $\overline{CU}$ signal if the frequency of the clock is lower than that of the HSYNC signal or if the phase of the clock is behind that of the HSYNC signal; otherwise it outputs the $\overline{CD}$ signal. The charge pump and LPF apply a voltage to the VCO according to the $\overline{CU}$ or $\overline{CD}$ signal.

This operation is repeated until the phase and frequency of the frequency-divided clock match those of the HSYNC signal, making it a stable dot clock.

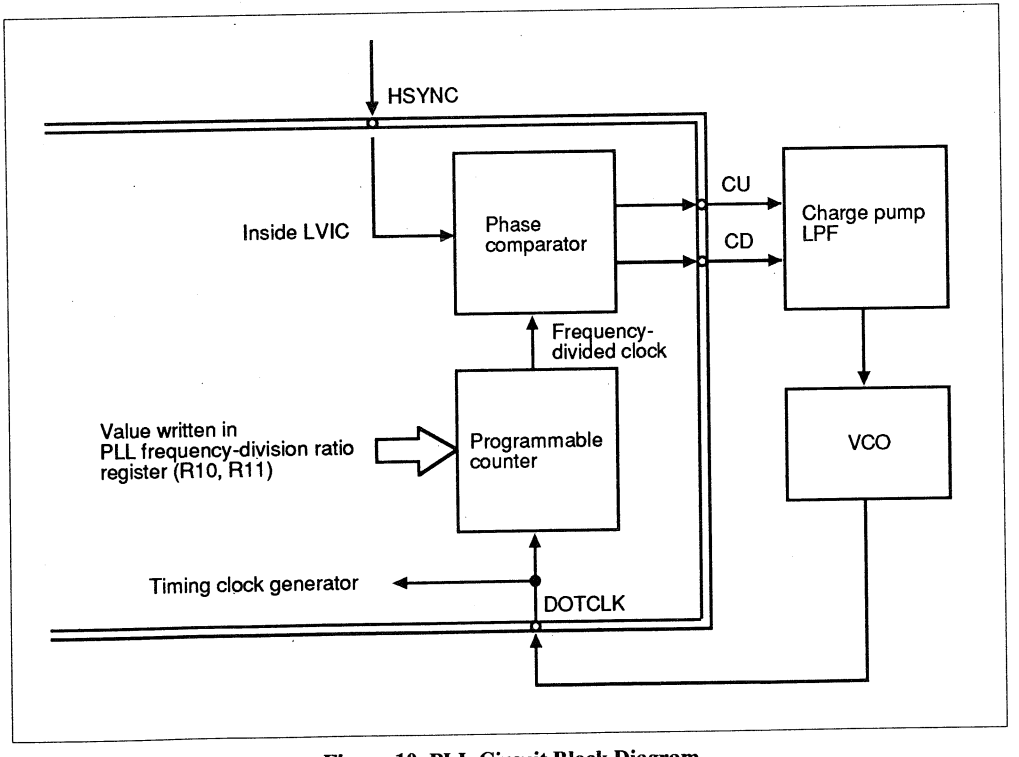


Figure 10 PLL Circuit Block Diagram

Gray-Scale Palette

The HD66841 thins out LCD data on certain dots or lines of an LCD panel every frame, changing integral voltages applied to liquid-crystal cells, to generate intermediate levels of luminosities. Consequently, the difference in depth between adjacent gray-scale shades may not be uniform in some cases since voltage-transmittance characteristics vary with different panels. To allow for this, the HD66841 is designed to generate 13 gray-scale levels and provide palette registers that assign desired levels to certain of the eight CRT display colors.

The relationships between gray scales and corresponding effective applied voltages are shown in figure 11 (a). Each gray scale is displayed according to the characteristics of its effective applied voltage and the optical transmittance of the panel (figure 11 (b)). Using the palette registers to select any 8 out of 13 levels of applied voltages enables an optimal gray-scale display conforming to the characteristics of the LCD panel. The palette registers can also be used to provide 4-level gray-scale display and reverse display.

Table 11 Default Values of Palette Registers

Register No.	CRT Display Data R	G	B	Register Name	Default Value			
P1	0	0	0	Black palette	0	0	0	0
P2	0	0	1	Blue palette	0	0	1	0
P3	1	0	0	Red palette	0	1	0	1
P4	1	0	1	Magenta palette	0	1	1	0
P5	0	1	0	Green palette	0	1	1	1
P6	0	1	1	Cyan palette	1	0	0	0
P7	1	1	0	Yellow palette	1	0	1	0
P8	1	1	1	White palette	1	1	0	0

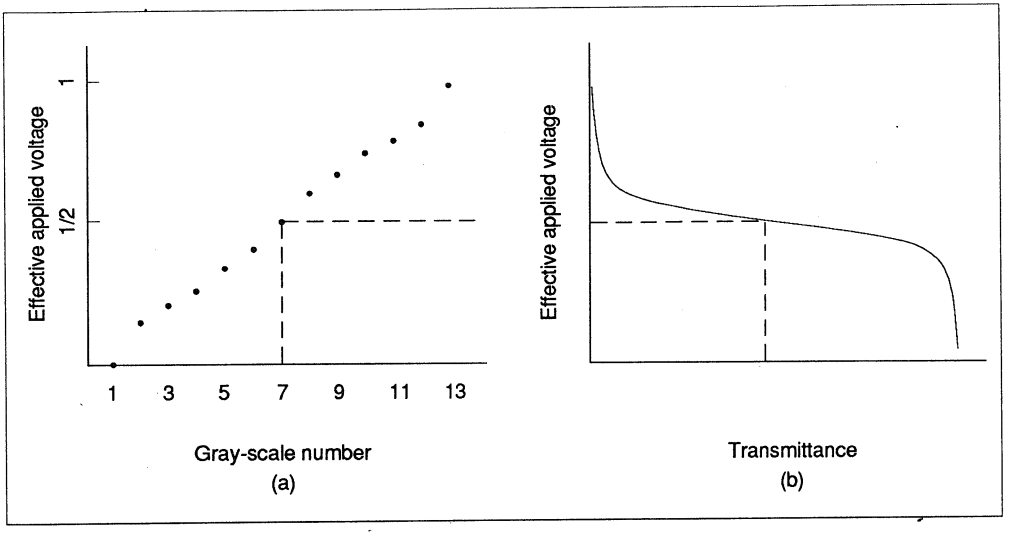


Figure 11 Relationships between Gray Scale, Transmittance, and Effective Applied Voltage

Pin Programming Method

The palette registers cannot be used in the pin programming method.

MPU Programming Method

To change the contents of palette registers in the MPU programming method, set bit 2 (the PS bit) of control register 1 (R0), to 1. Since data registers (R1–R15) cannot be accessed while this bit is 1, set in to 0 before accessing the data registers again. However, note that control register 1 (R0) can be accessed regardless of the setting of the PS bit if $0 is set in the address register (AR).

ROM Programming Method

In the ROM programming method, the HD66841 accesses ROM sequentially from address $0000 to $001F. In this case, write 0 to bit 2 of address $0000 (PS bit) before writing data register values to addresses $0001–$000F, and write 1 to bit 2 of address $0010 (PS bit) before writing palette register values to addresses $0011–$0018.

DIZ Function

The HD66841 thins out data on certain lines or dots every frame to enable gray-scale display. If a checker-board pattern consisting of alternately arranged gray scales of different levels (figure 12) is displayed by a simple dot-basis gray-scale display control method, the display might sometimes seem to "flow" horizontally, depending on the gray-scale and LCD panel characteristics.

The HD66841 automatically checks for such a checker-board section and changes the gray-scale display control method of dot-based data thinning to that of frame-based data thinning, to reduce display flow. Setting bit 3 (DIZ) of control register 1 (R0) to 1 enables this function. In frame-based data thinning, however, flickering might appear with some LCD panels; in that case, select the control method that generates the better display.

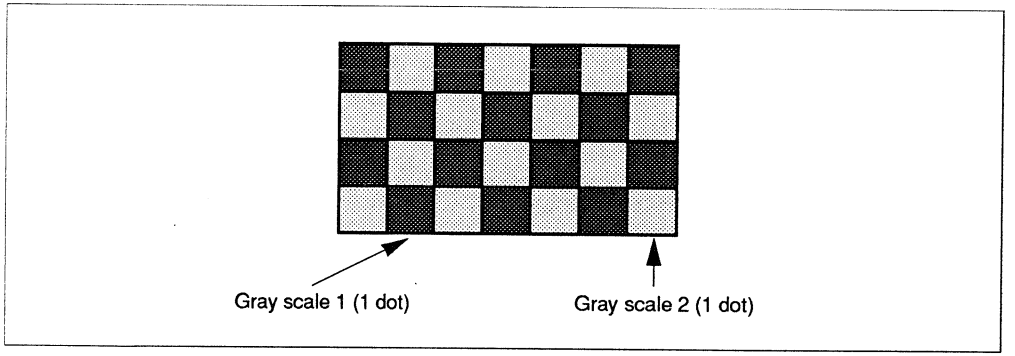


Figure 12 Checker-Board Display

Double-Height Display

The LVIC provides double-height display which doubles the vertical size of characters and pictures (figure 13).

In the TN-type LCD modes (display modes 1, 2, 4, and 6-8), the CL3 signal period is half as long as the CL1 signal period, as shown in figure 14. Consequently, using the CL3 signal instead of the CL1 signal (figure 15) as a line shift clock enables two lines to be selected while X-drivers (data output drivers) are outputting identical data, thus realizing double-height display. However, it should be noted that this display requires the following procedure since the LVIC displays twice as many lines as specified by pins or internal registers:

1. Halve the LCD dot clock (LDOTCK) frequency calculated from the number of vertical displayed lines of the LCD panel.
2. Specify half the number of vertical displayed lines of the LCD panel as the number of vertical displayed lines. (For instance, if the number of vertical displayed lines of the LCD panel is 400, specify 200 with the YL2–YL0 pins or the vertical displayed lines register.)

This function is available only in the TN-type LCD modes; it is disabled in the TFT-type LCD modes.

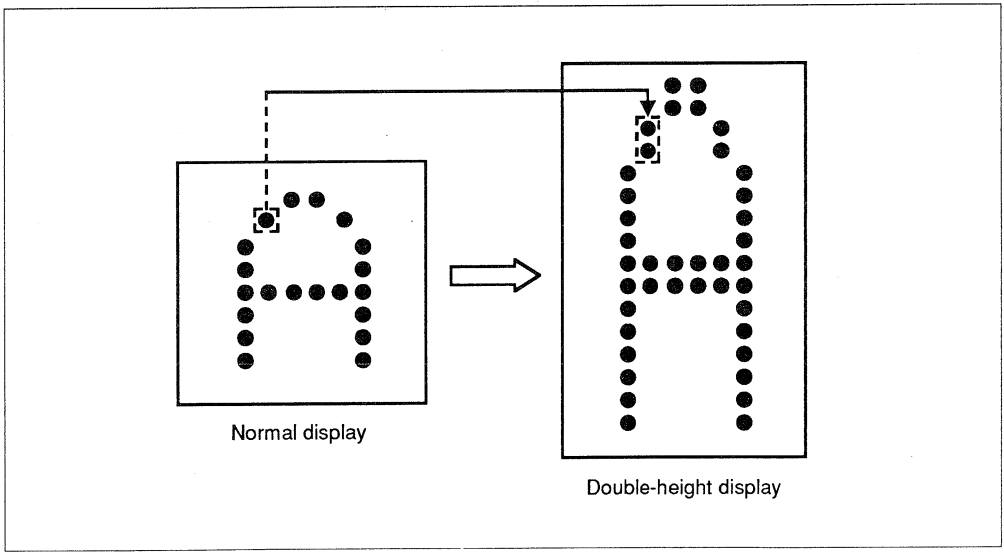


Figure 13 Double-Height Display Example

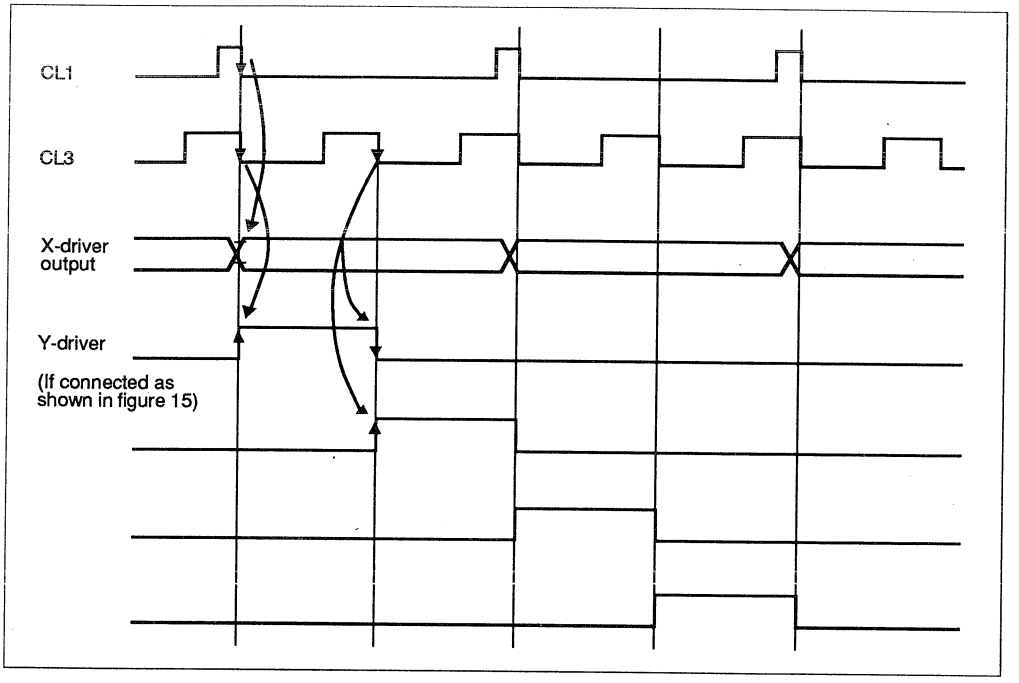


Figure 14 Relationship between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

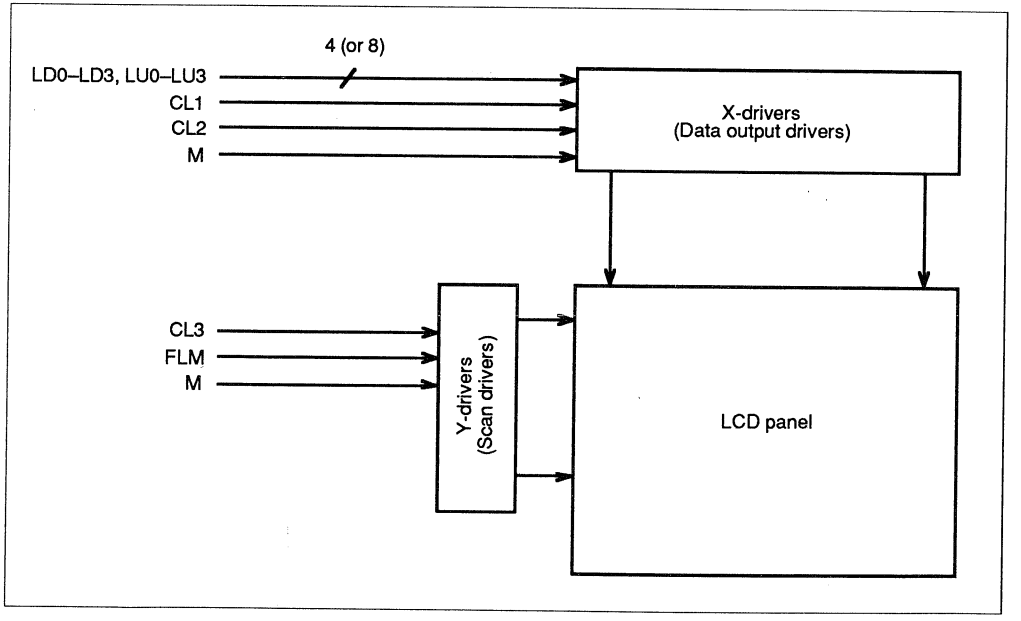


Figure 15 Connection for Double-Height Display

Display Timing Signal Fine Adjustment

If the display timing signal is supplied externally, a phase shift between CRT data and the display timing signal may appear. This is because each signal has its own specific lag. The LVIC can adjust the display timing signal according to pins F0–F3 or the fine adjust register (R9) to correct the phase shift.

The relationships between pins F3–F0, data bits 3 to 0 of the fine adjust register, and the resultant fine adjustments are shown in table 12. The polarity of the number of dots adjusted is given by – (minus) indicating advancing the phase of the display timing signal or + (plus) indicating delaying it. Pin F3 or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Examples of adjusting the display timing signal are shown in figure 16. Since the signal is two dots ahead of the display start position in case (1), F3, F2, F1, and F0 or data bits 3, 2, 1, and 0 of R9 should be set to (1, 0, 1, 0) to delay the signal by two dots. Conversely, since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal by two dots. If there is no need to adjust the signal, a setting of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 12 Pins, Data Bits of R9, and Fine Adjustment

Pin	F3	F2	F1	F0	Number of Dots
R9 Bit	3	2	1	0	Adjusted
	0	0	0	0	0
		0	0	1	–1
		⋮	⋮	⋮	⋮
		1	1	0	–6
		1	1	1	–7
	1	0	0	0	0
		0	0	1	+1
		⋮	⋮	⋮	⋮
		1	1	0	+6
		1	1	1	+7

Note: To use pins to adjust the display timing signal, set the ADJ pin to 1.

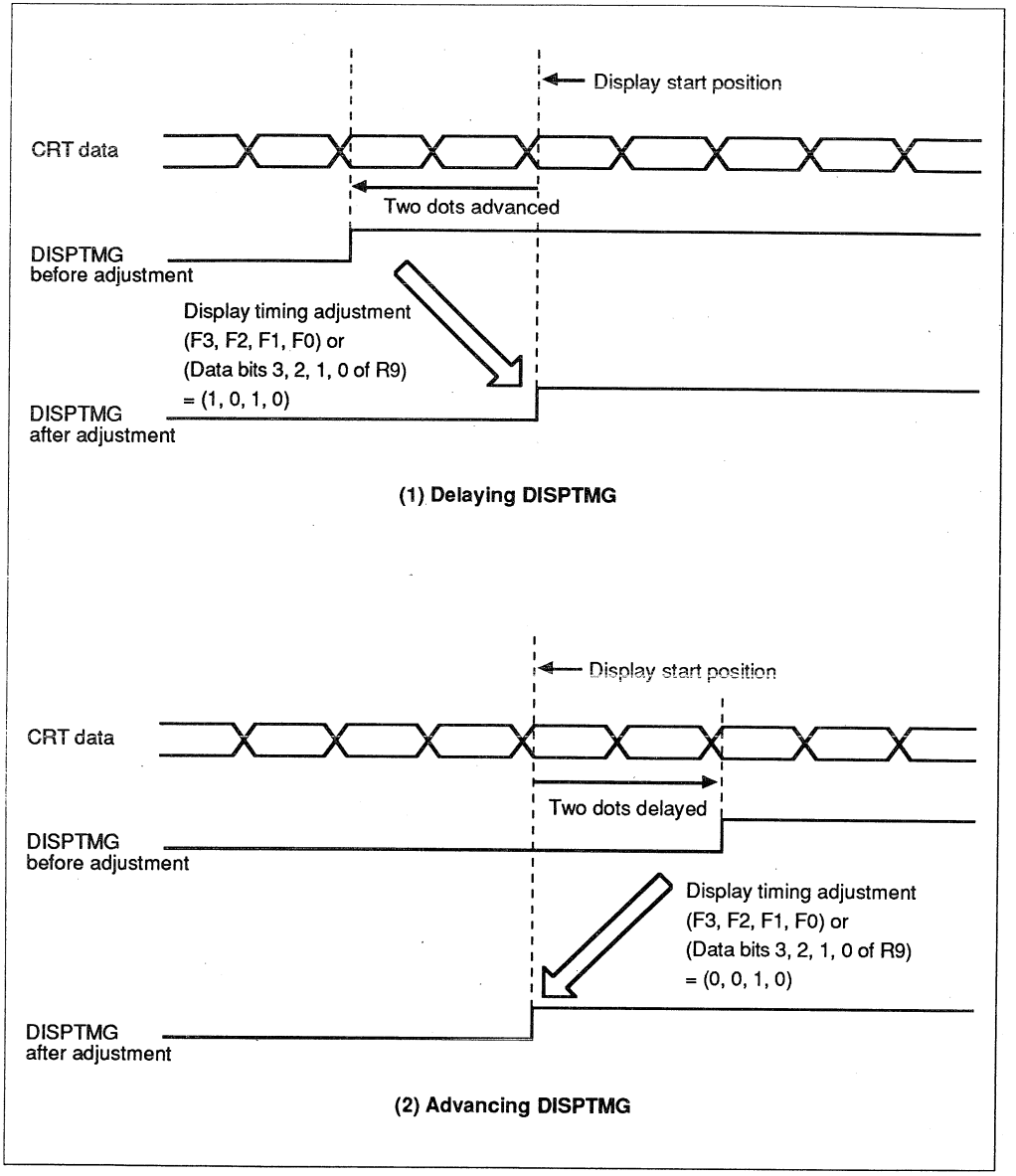


Figure 16 Adjustment of Display Timing Signal

Internal Registers

The HD66841 has an address register (AR), 16 data registers (R0–R15), and 8 palette registers (P1–P8). Write the address of a register to be used into the address register (AR), but only after setting the PS bit of control register 1 (R0) to 0 for a data register or 1 for a palette register. The MPU transfers data to the register corresponding to the written address.

Registers are valid only in the internal register programming method, they are invalid (don't care) in the pin programming method.

Address Register (AR)

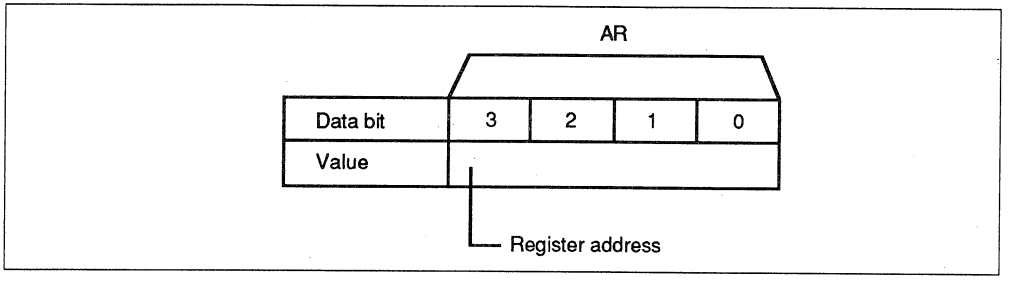


Figure 17 Address Register

The 4-bit address register (figure 17) is used to select one of the 16 data registers or 8 palette registers. It can select any data register or palette register according to the register address written to it by the MPU. The address register itself is selected if the RS signal is set low.

Control Register 1 (R0)

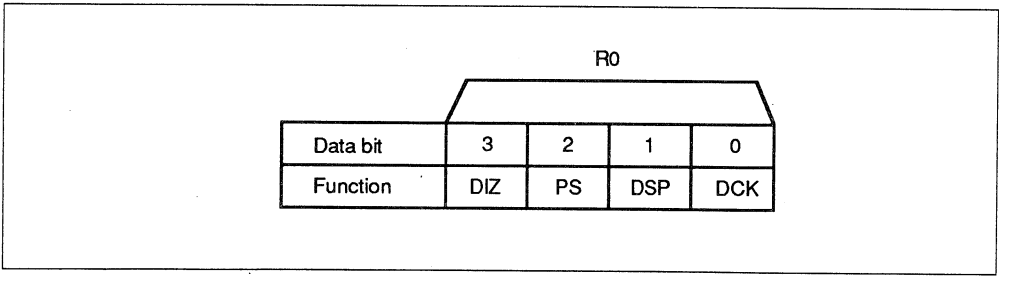


Figure 18 Control Register 1

Control register 1 (figure 18) is composed of four bits whose functions are described below.

- DIZ bit: Changes the method used to control the gray-scale display of a checker-board pattern.
  - DIZ = 0: Data thinned out on a dot basis every frame
  - DIZ = 1: Data thinned out on a frame basis every frame
- PS bit: Specifies access to data registers (R0–R15) or palette registers (P1–P8).

  In MPU programming mode:
  - PS = 0: Specifies access to data registers (R0–R15) only.
  - PS = 1: Specifies access to palette registers (P1–P8) only.

This register can be always accessed regardless of the PS bit setting, but it cannot be read after the PS bit is set to 1. Read it when PS is 0.

In ROM programming mode: Data for LVIC internal data registers can be written into $0001 to $000F when bit 2 (the PS bit) of $0000 is set to 0. Data to be set into palette registers can be written into $0011 to $0018 when the PS bit of $0010 is set to 1 (figure 19 (a)).

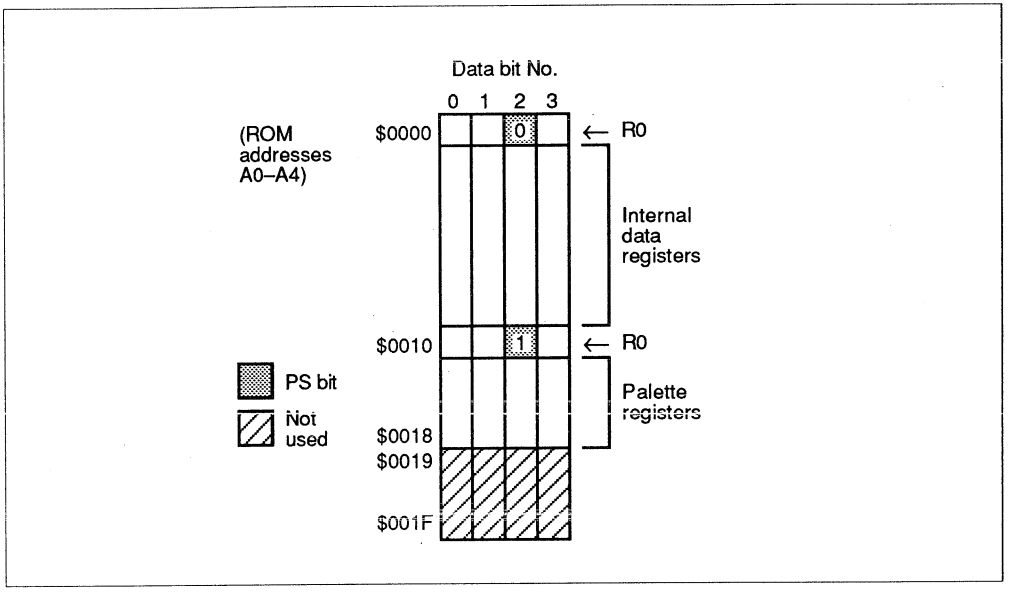


Figure 19 PS Bit Functions in ROM Programming Method

- DSP bit
  - DSP = 1: The DISPTMG signal is generated internally.
  - DSP = 0: The DISPTMG signal is supplied externally. (However, note that if DCK is 1, the DISPTMG signal is generated internally even if DSP is 0.)
- DCK bit
  - DCK = 1: The DOTCLK signal is generated internally.
  - DCK = 0: The DOTCLK signal is supplied externally.

Control Register 2 (R1)

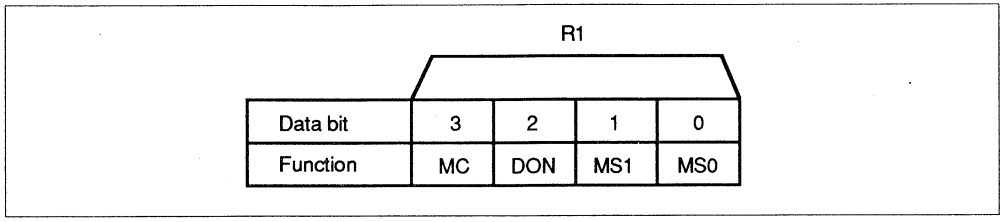


Figure 20 Control Register 2

Control register 2 (figure 20) is composed of four bits whose functions are described below.

- MC bit: Specifies M signal alternation.
  - MC = 1: The M signal alternates every line.
  - MC = 0: The M signal alternates every frame.
- DON bit: Specifies whether the LCD is on or off.
  - DON = 1: LCD on
  - DON = 0: LCD off
- MS1, MS0 bits: Specify buffer memory type.
  - (MS1, MS0) = (0, 0): No memory
  - (MS1, MS0) = (0, 1): 8-kbyte memory
  - (MS1, MS0) = (1, 0): 32-kbyte memory
  - (MS1, MS0) = (1, 1): 64-kbyte memory

Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4)

The vertical displayed lines register (figure 21) is composed of ten bits (R2, R3, and the high-order two bits of R4). It specifies the number of lines displayed from top to bottom of the screen, called the number of vertical displayed lines. This register can specify both even and odd numbers in single screen modes with Y-drivers positioned on one side, i.e., in display modes 2, 4, and 7–9, but can specify only even numbers in other modes. The value to be written into this register is Nvd – 1, where Nvd is the number of vertical displayed lines.

CL3 Period Register (Low-Order 2 Bits of R4, R5)

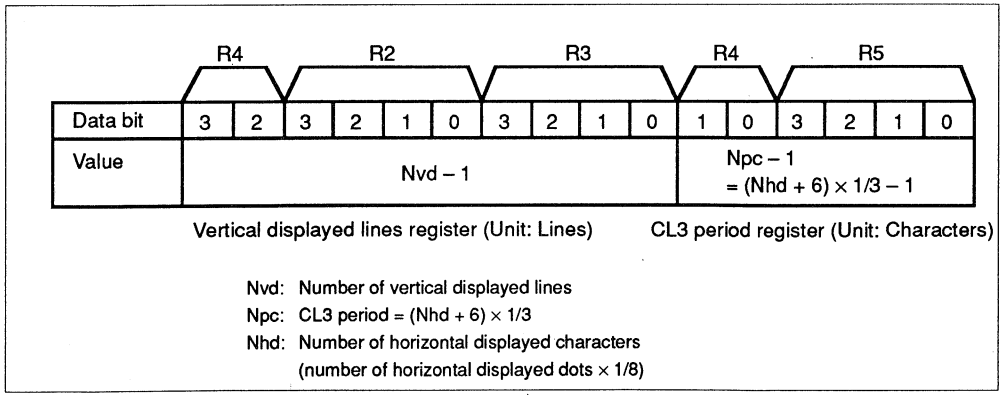


Figure 21 Vertical Displayed Lines Register and CL3 Period Register

The CL3 period register (figure 21), is composed of six bits (R5 and the low-order two bits of R4). It specifies the CL3 signal period in 8-color display modes with horizontal stripes (display modes 13–15), so it is invalid in other modes. CL3 is the clock signal used by the LVIC to output RGB data separately to LCD drivers. The value to be written into this register is Npc – 1, i.e., (Nhd + 6) × 1/3 – 1, where Nhd is the number of horizontal displayed dots × 1/8. If (Nhd + 6) is not divisible by 3, round it off.

Horizontal Displayed Characters Register (R6, R7)

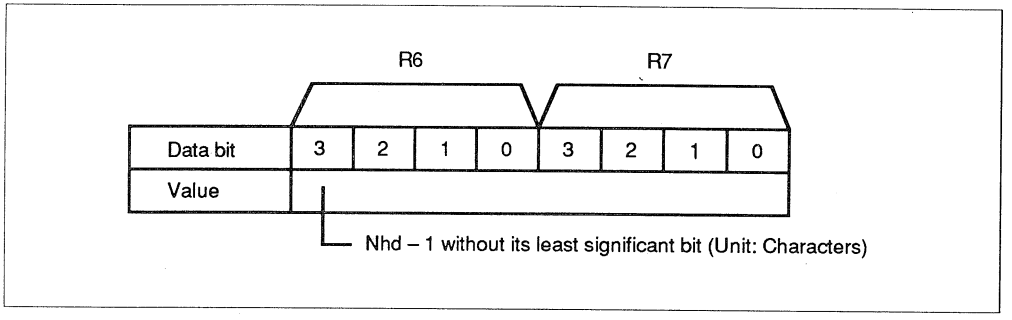


Figure 22 Horizontal Displayed Characters Register

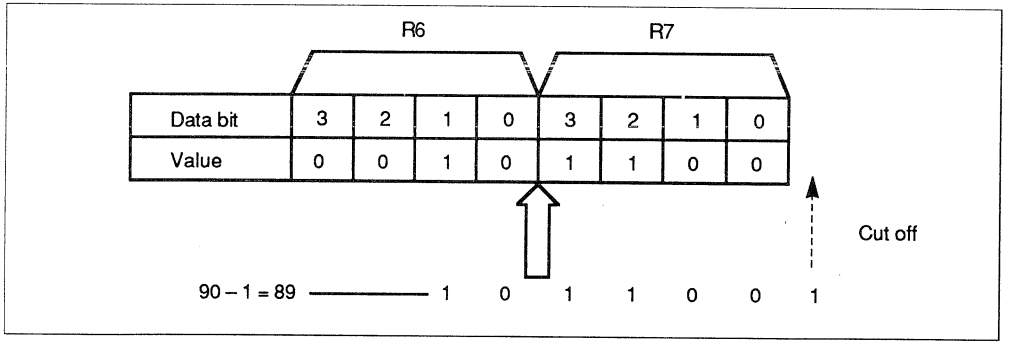


Figure 23 How to Write the Number of Horizontal Displayed Characters

The horizontal displayed characters register (figure 22) is composed of eight bits (R6, R7). It specifies the number of characters displayed on one horizontal line, called the number of horizontal displayed characters.

This register can specify even numbers only. In dual-screen modes (display modes 1, 6, and 16), the most significant bit of this register is invalid. When writing into this register, shift (Nhd – 1) in the low-order direction for one bit to cut off the least significant bit. Figure 22 shows how to write a value into the register when Nhd = 90.

CL3 Pulse Width Register (R8)

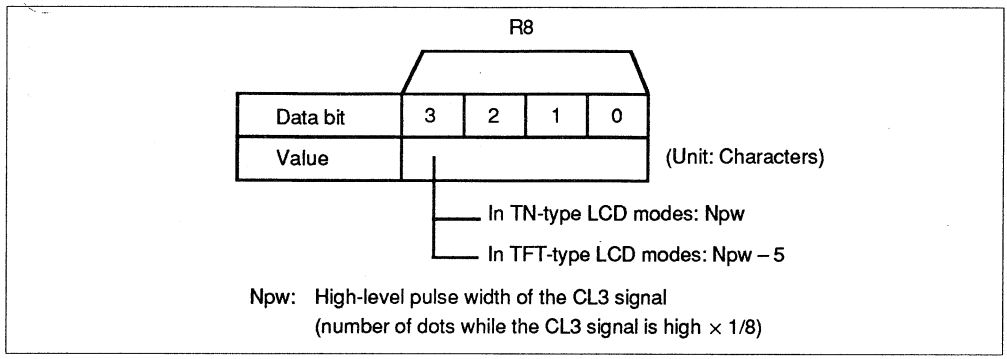


Figure 24 CL3 Pulse Width Register

The 4-bit CL3 pulse width register (figure 24) specifies the high-level pulse width of the CL3 signal. In TFT-type LCD modes, a data hold time is necessary and it is determined by the high-level pulse width of the CL3 signal. The CL3 signal is output with the high-level pulse width specified by this register even when the LVIC is not in a TFT-type LCD mode.

Fine Adjust Register (R9)

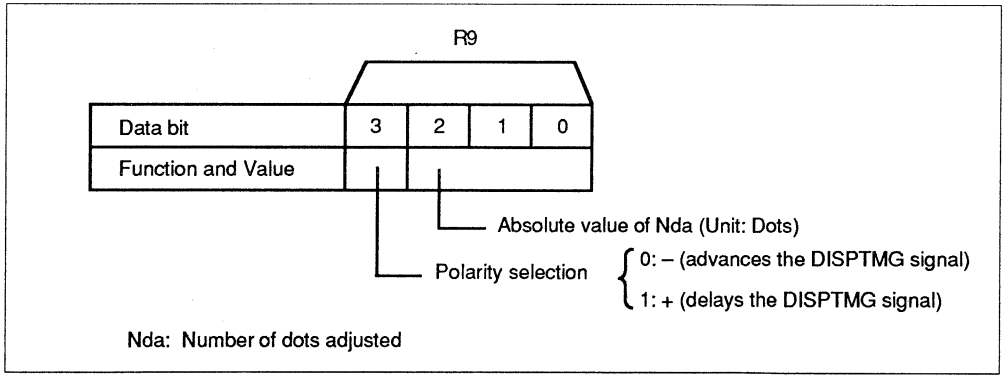


Figure 25 Fine Adjust Register

The 4-bit fine adjust register (figure 25) adjusts the externally supplied display timing signal (DISPTMG) to synchronize its phase with that of LCD data. The value to be written into this register depends on the interval between the rising edge of the DISPTMG signal and the display start position. For more details, refer to the Display Timing Signal Fine Adjustment section and table 12. This register is invalid if the DISPTMG signal is generated internally, that is, if either the DCK bit or the DSP bit of control register 1 (R0) is 1.

PLL Frequency-Division Ratio Register (R10, R11)

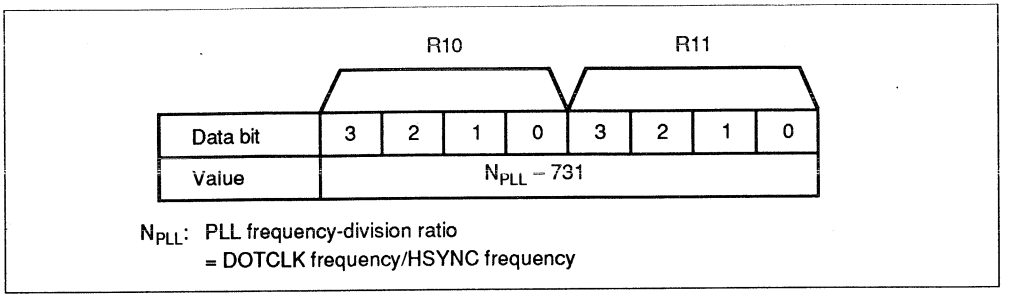


Figure 26 PLL Frequency-Division Ratio Register

The 8-bit PLL frequency-division ratio register (figure 26) specifies the PLL frequency-division ratio used for generating dot clock pulses by a PLL circuit. The PLL frequency-division ratio is the ratio of the DOTCLK signal's frequency to the horizontal synchronization signal's (HSYNC) frequency. The LVIC generates the DOTCLK signal according to this ratio. This register is invalid if the DOTCLK signal is supplied externally, i.e., it is valid only in the internal register programming method when the DCK bit of control register 1 (R0) is 0.

The value to be written into this register is N_{PLL} – 731, where N_{PLL} is the PLL frequency-division ratio, which can be obtained from the following equation:

$$N_{PLL} - 731 = Ncht \times n - 731$$

Ncht: Total number of horizontal characters on CRT (Total number of horizontal dots on CRT × 1/n)

n: horizontal character pitch (number of horizontal dots making up a character)

Ncht can be also obtained from the CRT monitor specifications as follows;

$$Ncht = 1/n \times (\text{DOTCLK frequency/HSYNC frequency})$$

Vertical Backporch Register (R12, R13)

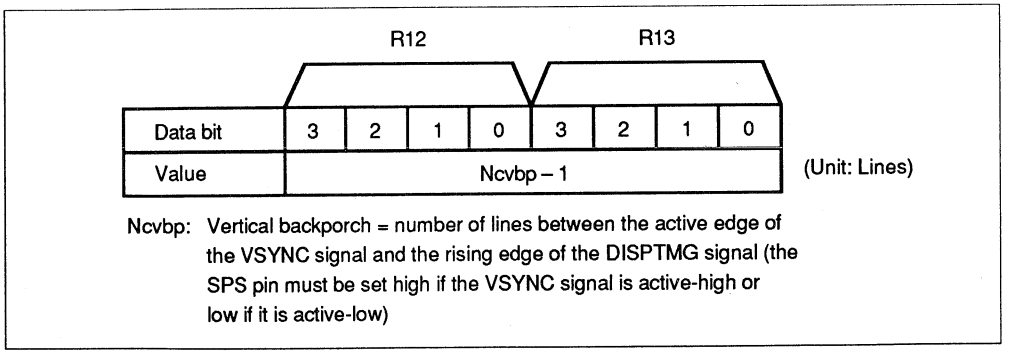


Figure 27 Vertical Backporch Register

The 8-bit vertical backporch register (figure 27) specifies the vertical backporch which is the number of lines between the active edge of the vertical synchronization signal (VSYNC) and the rising edge of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the vertical backporch, refer to the Display Timing Signal Generation section and figure 9.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be generated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

Horizontal Backporch Register (R14, R15)

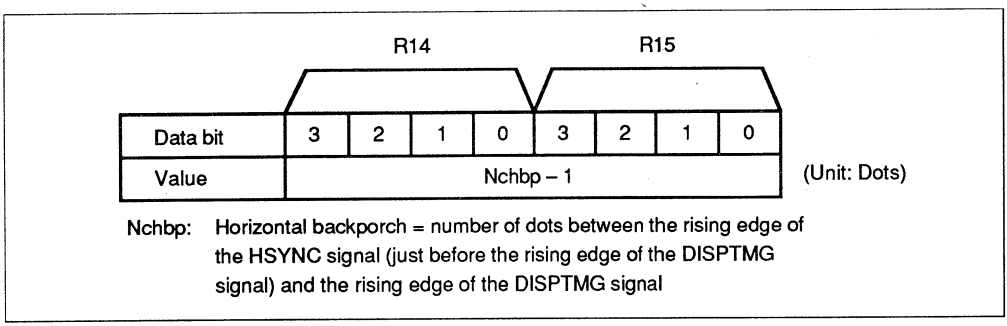
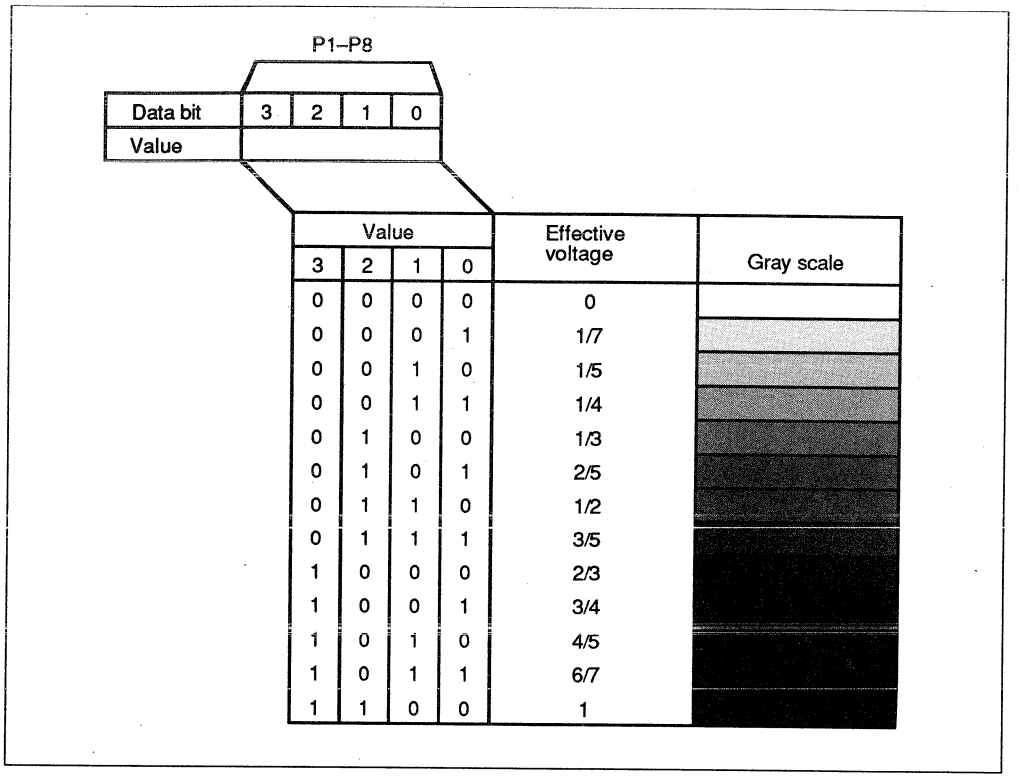


Figure 28 Horizontal Backporch Register

The 8-bit horizontal backporch register (figure 28) specifies the horizontal backporch which is the number of dots between the rising edge of the HSYNC signal and that of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the horizontal backporch, refer to the Display Timing Signal Generation section and figure 9.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be generated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

Palette Registers (P1–P8)



Value 3	2	1	0	Effective voltage	Gray scale
0	0	0	0	0	
0	0	0	1	1/7	
0	0	1	0	1/5	
0	0	1	1	1/4	
0	1	0	0	1/3	
0	1	0	1	2/5	
0	1	1	0	1/2	
0	1	1	1	3/5	
1	0	0	0	2/3	
1	0	0	1	3/4	
1	0	1	0	4/5	
1	0	1	1	6/7	
1	1	0	0	1	

Figure 29 Palette Registers

The eight 4-bit palette registers (figure 29) each specify one of 13 gray-scale levels for one of the eight colors provided by RGB signals. Use these registers to enable an 8-level gray-scale display appropriate to the characteristics of the LCD panel.

Reset

The $\overline{RES}$ signal resets and starts the LVIC. The reset signal must be held low for at least 1µs after power-on.
Reset is defined as shown in figure 30.

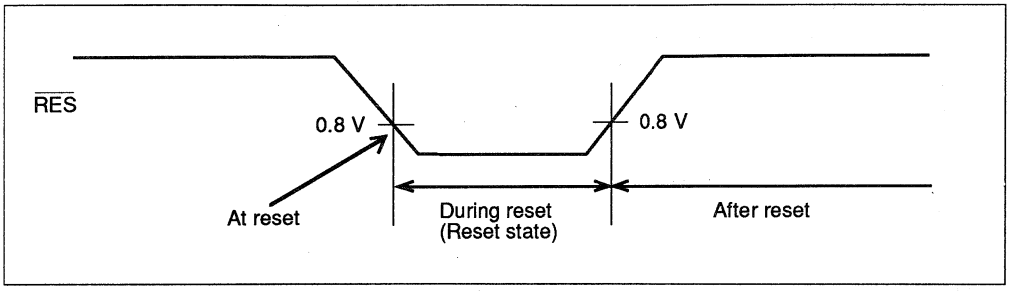


Figure 30 Reset Definition

State of Pins after Reset

In principle, the $\overline{RES}$ signal does not control output signals and it operates regardless of other input signals. Output signals can be classified into the following five groups, depending on their reset states:

- Retains pre-reset state: CL2, A0–A4
- Driven to high-impedance state (or fixed low if no memory is used): RD0–RD7, GD0–GD7, BD0–BD7
- Fixed high: $\overline{MWE}$, CL4, M, $\overline{CU}$, $\overline{CD}$, $\overline{MCS1}$,
- Fixed low: MA0–MA12, R0–R3, G0–G3, B0–B3, CL3, FLM
- Fixed high or low, depending on memory used (table 13): MA13–MA15, $\overline{MCS0}$

Table 13 State of Pins after Reset and Memory Type

Memory Type	MA13	MA14	MA15	$\overline{MCS0}$
No memory	Low	Low	High	High
8-kbyte memory	High	High	High	Low
32-kbyte memory	Low	Low	High	Low
64-kbyte memory	Low	Low	Low	Low

State of Registers after Reset

The $\overline{RES}$ signal does not affect data register contents, so the MPU can both read from and write to data registers, even after reset. Registers will retain their pre-reset contents until they are rewritten.

The palette registers, however, are usually set to their default values by a reset. For the default values, refer to the Gray-Scale Palette section and table 11.

Memory Clear Function

After a reset, the LVIC writes 0s in the memory area specified by pins or register bits MS0 and MS1 (table 7).

User Notes

1. The following limitations are imposed if no memory is used (MS0 = 0, MS1 = 0).
   - Dual-screen display modes (modes 1, 6, and 16) are disabled.
   - LCD systems with Y-drivers on both sides are disabled, even if a mode for a system with Y-drivers on both sides (mode 3, 5, 10, 12, or 14) is selected; the LVIC operates in exactly the same way as in the corresponding mode for a system with Y-drivers on one side (mode 2, 4, 9, 11, or 13). The CL4 pin must be left disconnected in this case.
2. With the internal register programming method, the operation of the LVIC after a reset cannot be guaranteed until its internal registers have been written to.
3. The memory clear function might not work normally at power-on or after a reset if the MS0 and MS1 pins or bits are not set correctly to the value corresponding to the type of memory being used.
4. Since the LVIC is a CMOS LSI, input pins must not be left disconnected. Refer to the Pin Description and table 1 for details on pin handling.

Programming Restrictions

The values written into the LVIC's internal registers have the limits listed in table 14. The symbols used in table 14 are defined in table 15 and figure 31.

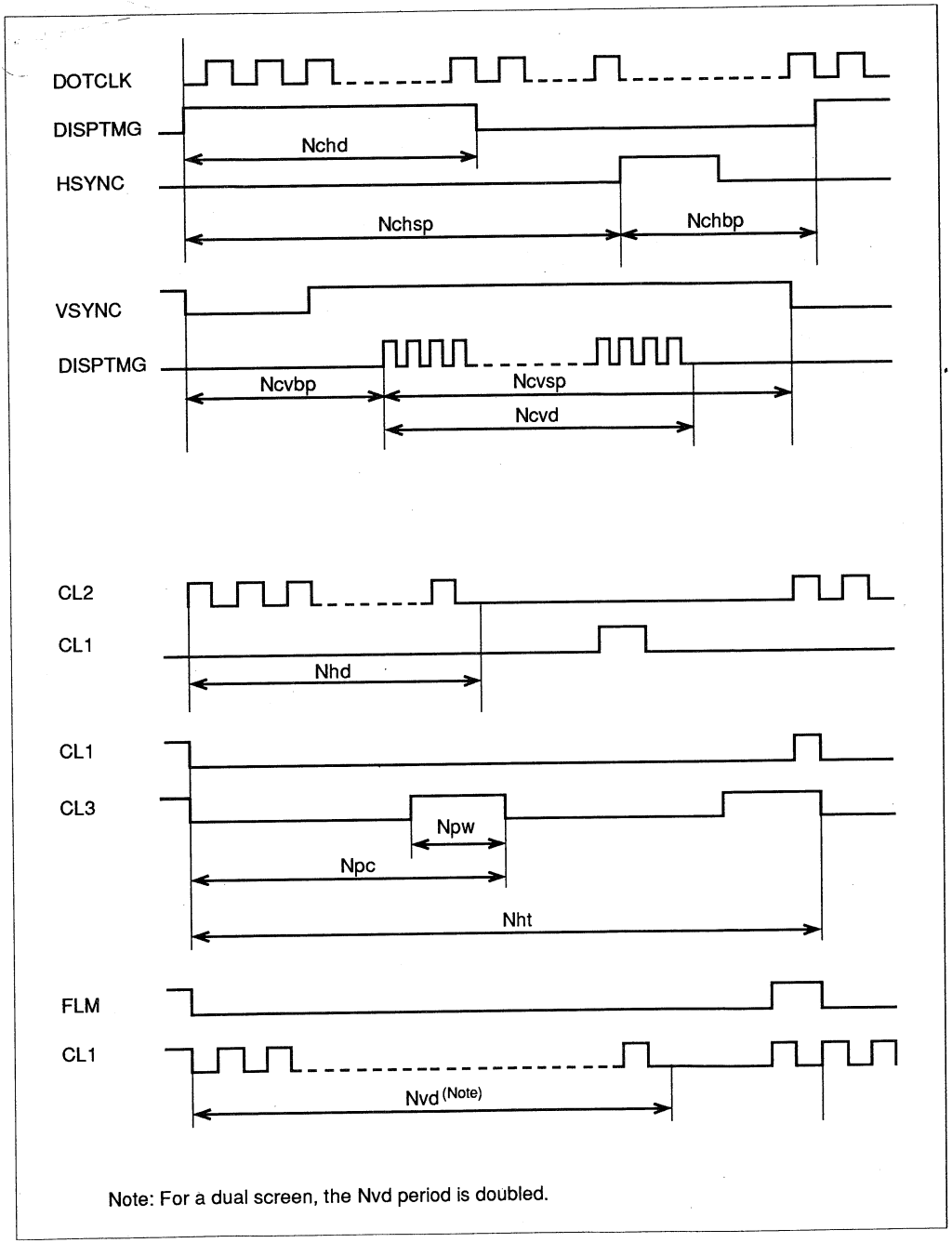
Table 14 Limits on Register Values

Item	Limits	Notes	Applicable Registers
Screen configuration	$4 \leqq Nvd \leqq (Ncvbp + Ncvsp) - 1 \leqq 1024$		R2, R3, R4,
	$4 \leqq Nhd \leqq (Nchbp \times 1/n + Nchsp) - 1 \leqq 506$	1, 2	R6, R7
	$(Nhd + 6) \times n \times Nvd \times f_{FLM} \leqq f_{DOTCLK} \leqq$ 30MHz	1, 3	R2, R3, R4, R6, R7
CL3 signal control	$1 \leqq Npw \leqq (Nhd + 6)/2 - 1$	4	R4, R5, R6,
	$1 \leqq Npw \leqq Nhd$	5	R7, R8
	$1 \leqq Npw \leqq Npc - 1$	6	
DISPTMG signal generation	$1 \leqq Nchbp \leqq 256$	7	R12, R13
	$1 \leqq Ncvbp \leqq 256$	7	R14, R15
No memory	$4 \leqq Nhd \leqq Nchsp - 4$	8	R2, R3, R4,
	$4 \leqq Nvd \leqq Ncvsp - 1$	8	R6, R7

Notes:
1. Lowercase n indicates the horizontal character pitch which is the number of horizontal dots composing a character.
2. Nhd ≦ 250 in the dual screen modes (display modes 1, 6, and 16).
3. f_{FLM} is the FLM signal frequency and f_{DOTCLK} is the CRT display dot clock (DOTCLK) frequency.
   $f_{LDOTCK} < f_{DOTCLK} \times 15/16$ or $f_{LDOTCK} = f_{DOTCLK}$
   (f_{LDOTCK} is the LCD dot clock (LDOTCK) frequency)
4. In display modes 1, 2, 4, and 6–8
5. In display modes 3, 5, and 9–12 when Npw = (value in R8) + 5
6. In display modes 13–15 when Npw = (value in R8) + 5
7. Value in R14 and R15 ≦ (Nchsp × n + Nchbp) – Nhd × n – 2
   (n = horizontal character pitch)
   Value in R12 and R13 ≦ (Ncvsp + Ncvbp) – Nvd – 2
8. Nht = Nchsp + (Nchbp × 1/n), Nvd < Ncvbp + Ncvsp
   (Nht = (Nhd + 6) if buffer memory is used)
   (n = horizontal character pitch)

Table 15 Symbol Definitions

Symbol	Definition
Nchd	Number of horizontal displayed characters on the CRT display (number of horizontal displayed dots on the CRT display × 1/8)
Nchsp	Number of characters between the rising edge of the DISPTMG signal and that of the HSYNC signal (number of dots between the rising edge of the DISPTMG signal and that of the HSYNC signal × 1/8) (= horizontal synchronization position)
Nchbp	Number of dots between the rising edge of the HSYNC signal and that of the DISPTMG signal (just after the rising edge of the HSYNC signal) (= horizontal backporch)
Ncvbp	Number of lines between the active edge of the VSYNC signal and the rising edge of the DISPTMG signal (just after the active edge of the VSYNC signal) (= vertical backporch)
Ncvsp	Number of lines between the rising edge of the DISPTMG signal and the active edge of the VSYNC signal (= vertical synch position)
Ncvd	Number of vertical displayed lines on the CRT display
Nhd	Number of horizontal displayed characters on the LCD (number of horizontal displayed dots on the LCD × 1/8)
Npc	Number of characters during one CL3 signal period (number of dots during one CL3 signal period × 1/8)
Npw	Number of characters while the CL3 signal is high (number of dots while the CL3 signal is high × 1/8)
Nht	Number of characters during a CL1 signal period (number of dots during a CL1 signal period × 1/8)
Nvd	Number of vertical displayed lines on the LCD



Note: For a dual screen, the Nvd period is doubled.

Figure 31 Symbol Definitions

Comparisons with HD66840

Gray-Scale Generation Method

The HD66840 shifts display data so that data on different lines will be thinned out in different frames, but the HD66841 shifts display data further so that data on different dots will be thinned out in different frames. This reduces deterioration of display contrast.

Gray-Scale Palette

	HD66840	HD66841
Numbers of registers	16	24 (palette registers have been added to the HD66840's registers)
Selection of correspondence between CRT display colors and gray-scale levels	Impossible	Possible (any of 13 levels assignable to each of 8 colors)

Display Mode

Mode 16 of the HD66840 (for 8-color display with horizontal stripes and X- and Y-drivers positioned on both sides of the LCD) has been modified into the following new mode in the HD66841:

Mode number: 16
Pin setting: (DM3, DM2, DM1, DM0) = (1, 1, 1, 1)
Display colors: 8 colors

LCD data output: – 12-bit-based data transfer
– Dual screen configuration
Lcd driver settings: X-drivers and Y-drivers set on one side
Stripe: Vertical
Alternation mode: Every frame

In this mode, the HD66841 outputs upper screen data and lower screen data alternately, as shown in figure 32. In this case, the CL2 frequency is one quarter of the LDOTCK frequency.

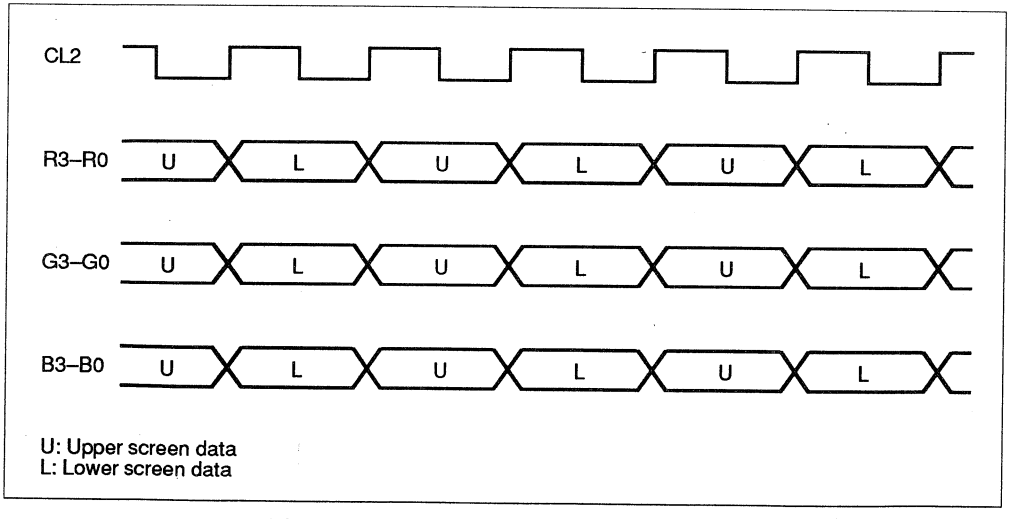


Figure 32 Operation in New HD66841 Mode 16

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	–0.3 to 7.0	V
Input voltage	V_{in}	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = –20°C to +75°C). If these conditions are exceeded, LSI reliability may be affected.
2. All voltages are referenced to GND = 0V.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Max	Unit	Test Conditions	Note(s)
Input high voltage						
$\overline{RES}$ pin	V_{IH}	V_{CC} – 0.5	V_{CC} + 0.3	V		
TTL interface pins		2.0	V_{CC} + 0.3			1
TTL interface pins		2.2	V_{CC} + 0.3			4
CMOS interface pins		0.7 V_{CC}	V_{CC} + 0.3			1
Input low voltage						
TTL interface pins, $\overline{RES}$ pin	V_{IL}	–0.3	0.8	V		1
TTL interface pins		–0.3	0.6			5
CMOS interface pins		–0.3	0.3 V_{CC}			1
Output high voltage						
TTL interface pins	V_{OH}	2.4	—	V	I_{OH} = –200µA	2
CMOS interface pins		V_{CC} – 0.8	—		I_{OH} = –200µA	
Output low voltage						
TTL interface pins	V_{OL}	—	0.4	V	I_{OL} = 1.6mA	2
CMOS interface pins		—	0.8		I_{OL} = 200µA	
Input leakage current						
All inputs expect I/O common pins	I_{IL}	–2.5	2.5	µA		3
Three-state (off-state) leakage current						
I/O common pins	I_{TSL}	–10.0	10.0	µA		3
Power dissipation	I_{CC}	—	250	mW	f_{DOTCLK} = 25MHz, output pins left disconnected	

Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, RD0–RD7, GD0–GD7, BD0–BD7, D0–D3, A0/$\overline{RD}$/XDOT, RS/ADJ/A4, $\overline{CS}$/MS0
CMOS interface inputs: DM0–DM3, DOTE, PMOD0, PMOD1, A1/YL0–A3/YL2

2. TTL interface inputs: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, MA0–MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$, RS/ADJ/A4
CMOS interface inputs: $\overline{CU}$, $\overline{CD}$, R0/LU0–R3/LU3, G0/LD0–G3/LD3, B0–B3, M, FLM, CL1, CL2, CL3, CL4

3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, RS/ADJ/A4
Inputs other than I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE , DM0–DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

4. TTL interface inputs: $\overline{WR}$/MS1, LDOTCK, DOTCLK

5. TTL interface inputs: $\overline{WR}$/MS1

DC Characteristics 2 (V_{CC} = 5.0V ± 5%, GND = 0V, Ta = –20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Max	Unit	Test Conditions	Note(s)
Input high voltage						
$\overline{RES}$ pin	V_{IH}	V_{CC} – 0.5	V_{CC} + 0.3	V		
TTL interface pins		2.0	V_{CC} + 0.3			1
CMOS interface pins		0.7 V_{CC}	V_{CC} + 0.3			1
Input low voltage						
TTL interface pins, $\overline{RES}$ pin	V_{IL}	–0.3	0.8	V		1
CMOS interface pins		–0.3	0.3 V_{CC}			1
Output high voltage						
TTL interface pins	V_{OH}	2.4	—	V	I_{OH} = –200µA	2
CMOS interface pins		V_{CC} – 0.8	—		I_{OH} = –200µA	2
Output low voltage						
TTL interface pins	V_{OL}	—	0.4	V	I_{OL} = 1.6mA	2
CMOS interface pins		—	0.8		I_{OL} = 200µA	2
Input leakage current						
All inputs expect	I_{IL}	–2.5	2.5	µA		
I/O common pins						3
Three-state (off-state) leakage current						
I/O common pins	I_{TSL}	–10.0	10.0	µA		3
Power dissipation	I_{CC}	—	250	mW	f_{DOTCLK} = 30MHz, output pins left disconnected	

Notes:
1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, DOTCLK, LDOTCK, RD0–RD7, GD0–GD7, BD0–BD7, D0–D3, A0/$\overline{RD}$/XDOT, RS/ADJ/A4, $\overline{CS}$/MS0, $\overline{WR}$/MS1
   CMOS interface inputs: DM0–DM3, DOTE, PMOD0, PMOD1, A1/YL0–A3/YL2
2. TTL interface outputs: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, MA0–MA15, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$, RS/ADJ/A4
   CMOS interface outputs: $\overline{CU}$, $\overline{CD}$, R0/LU0–R3/LU3, G0/LD0–G3/LD3, B0–B3, M, FLM, CL1, CL2, CL3, CL4
3. I/O common pins: A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, RS/ADJ/A4
   Inputs other than I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, $\overline{CS}$/MS0, $\overline{WR}$/MS1, $\overline{RES}$, DOTE, DM0–DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

AC Characteristics (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = –20°C to +75°C)

Video Signal Interface 1 (V_{CC} = 5.0V ± 5%)

Item	Symbol	Min	Max	Unit	Reference
DOTCLK cycle time	t_{CYCD}	33	1000	ns	Figure 33
DOTCLK high-level pulse width	t_{WDH}	16.5	—	ns	
DOTCLK low-level pulse width	t_{WDL}	16.5	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
RGB setup time	t_{VDS}	10	—	ns	
RGB hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Figure 33 except for DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	

Video Signal Interface 2 (V_{CC} = 5.0V ± 10%)

Item	Symbol	Min	Max	Unit	Reference
DOTCLK cycle time	t_{CYCD}	40	1000	ns	Figure 33
DOTCLK high-level pulse width	t_{WDH}	20	—	ns	
DOTCLK low-level pulse width	t_{WDL}	20	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
RGB setup time	t_{VDS}	10	—	ns	
RGB hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Figure 33 except for DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	

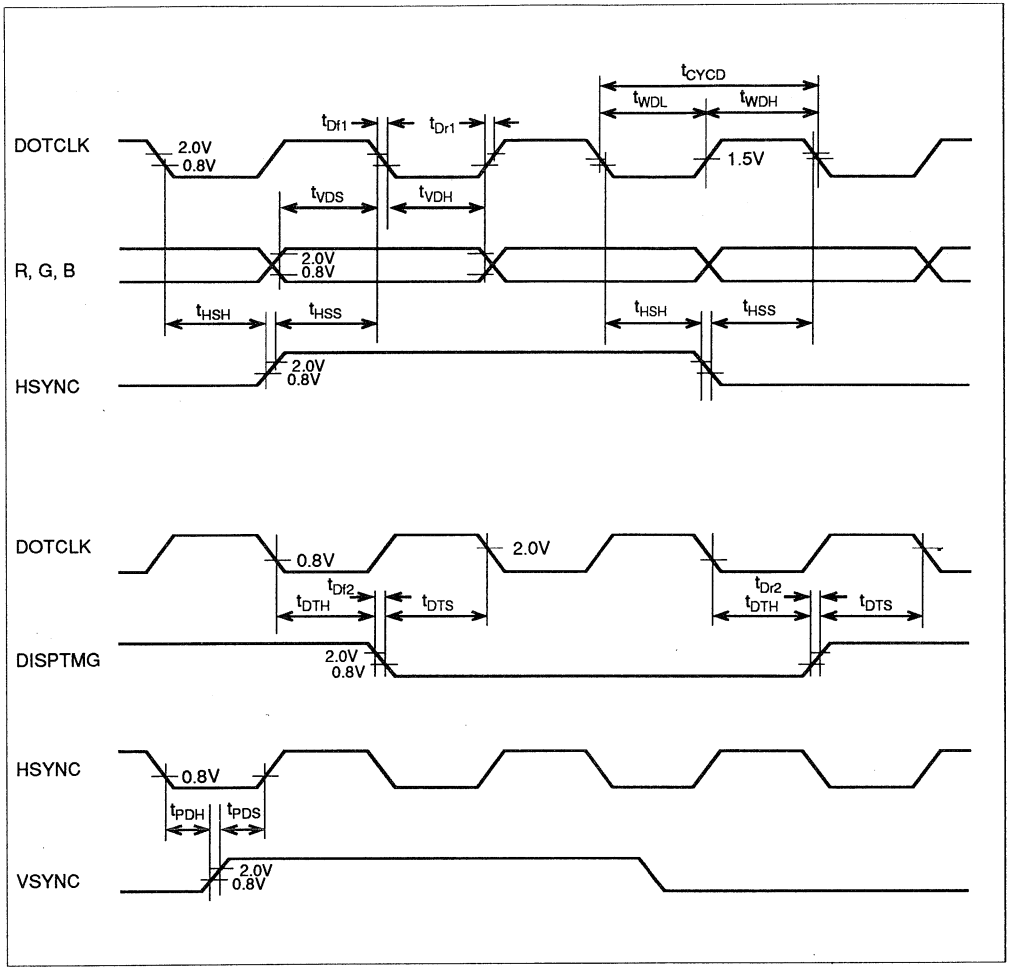


Figure 33 Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Unit	Reference
Read cycle time	t_{RC}	5 t_{CYCD} – 50	ns	Figures 34 and 35
RD0–RD7, GD0–GD7, BD0–BD7 data setup time	t_{SMD}	25	ns	
RD0–RD7, GD0–GD7, BD0–BD7 data hold time	t_{HMD}	0	ns	
Write cycle time	t_{WC}	6 t_{CYCD} – 50	ns	
Address setup time	t_{MAS}	t_{CYCD} – 30	ns	
Address hold time	t_{WR}	t_{CYCD} – 30	ns	
Chip select time	t_{CW}	4 t_{CYCD} – 40	ns	
Write pulse width	t_{WP}	4 t_{CYCD} – 40	ns	
RD0–RD7, GD0–GD7, BD0–BD7 output setup time	t_{SMDW}	2 t_{CYCD} – 25	ns	
RD0–RD7, GD0–GD7, BD0–BD7 output hold time	t_{HMDW}	0	ns	

Note: t_{CYCD} is the DOTCLK cycle time (min 40ns, max 1000ns).

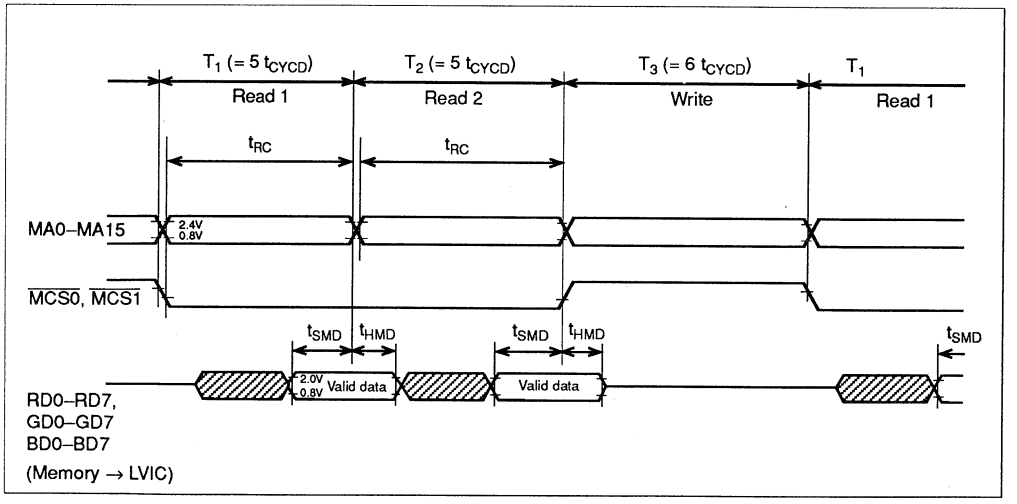


Figure 34 Buffer Memory Interface (RAM read timing)

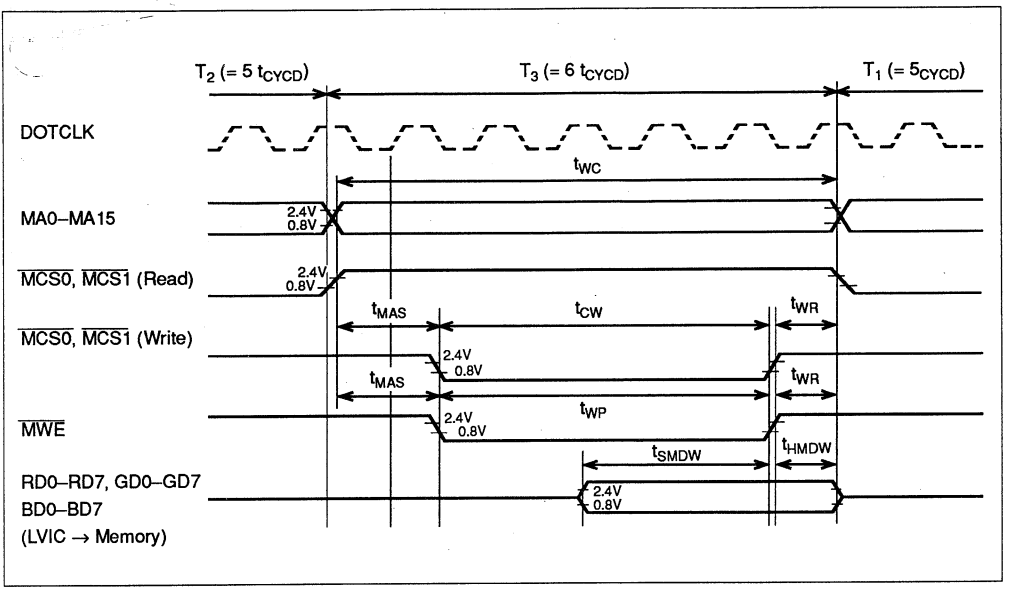


Figure 35 Buffer Memory Interface (RAM write timing)

LCD Driver Interface

TN-Type LCD Driver

Item	Symbol	Min	Max	Unit	Reference
CL2 cycle time	t_{WCL2}	166	—	ns	Figures 36 and 37
CL2 high-level pulse width	t_{WCL2H}	50	—	ns	
CL2 low-level pulse width	t_{WCL2L}	50	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level pulse width	t_{WCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
CL1 setup time	t_{SCL1}	500	—	ns	
CL1 hold time	t_{HCL1}	200	—	ns	
FLM hold time	t_{HF}	200	—	ns	
M output delay time	t_{DM}	—	300	ns	
Data delay time	t_{DD}	–20	20	ns	
LDOTCK cycle time	t_{WLDOT}	41	—	ns	

Note: All values are measured at f_{CL2} = 6MHz.

TFT-Type LCD Driver

Item	Symbol	Min	Max	Unit	Reference
CL2 cycle time (X-drivers on one side)	t_{TCL2S}	133	—	ns	Figures 38 and 39
CL2 high-level pulse width (X-drivers on one side)	t_{TCL2HS}	30	—	ns	
CL2 low-level pulse width (X-drivers on one side)	t_{TCL2LS}	30	—	ns	
CL2 cycle time (X-drivers on both sides)	t_{TCL2D}	266	—	ns	
CL2 high-level pulse width (X-drivers on both sides)	t_{TCL2HD}	80	—	ns	
CL2 low-level pulse width (X-drivers on both sides)	t_{TCL2LD}	80	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level pulse width	t_{TCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
Data delay time	t_{DD1}	–20	20	ns	
Data setup time	t_{LDS}	15	—	ns	
Data hold time	t_{LDH}	15	—	ns	
CL1 setup time	t_{TSCL1}	500	—	ns	
CL1 hold time	t_{THCL1}	200	—	ns	
CL3 delay time	t_{DCL3}	50	—	ns	
M output delay time	t_{DM}	—	300	ns	
FLM hold time	t_{TFH}	200	—	ns	
LDOTCK cycle time	t_{WLDOT}	33	—	ns	

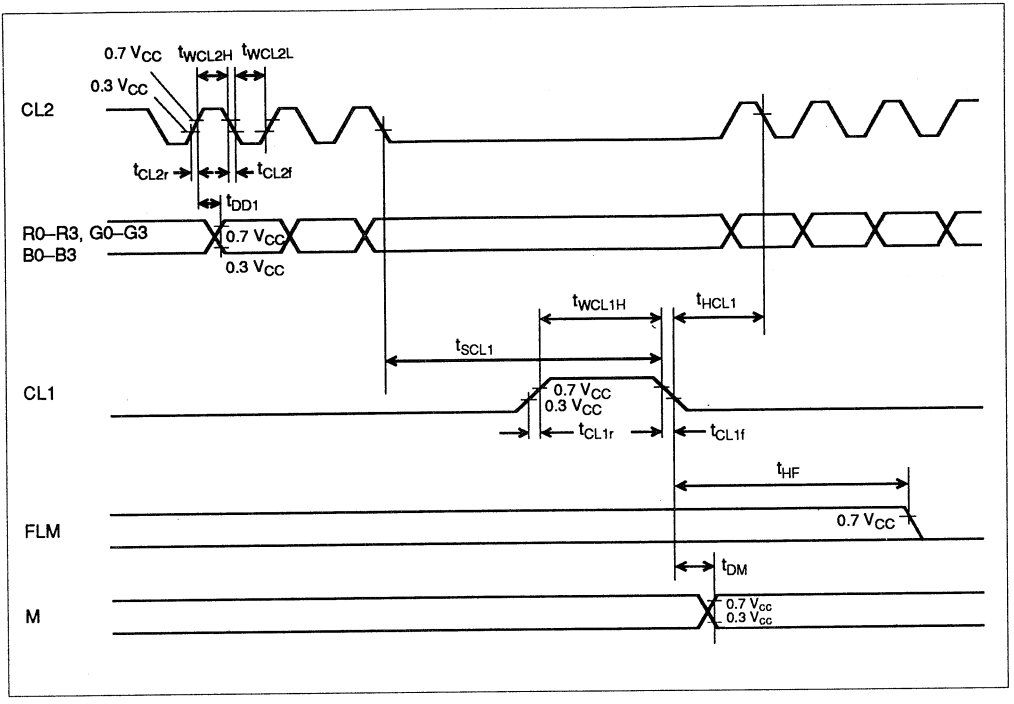


Figure 36 TN-Type LCD Driver Interface

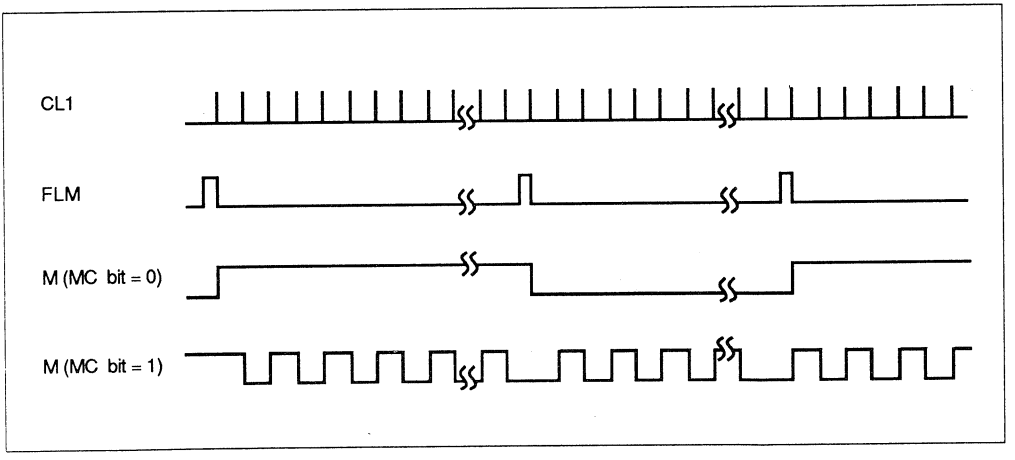


Figure 37 CL1, FLM, and M (expanded view of figure 36)

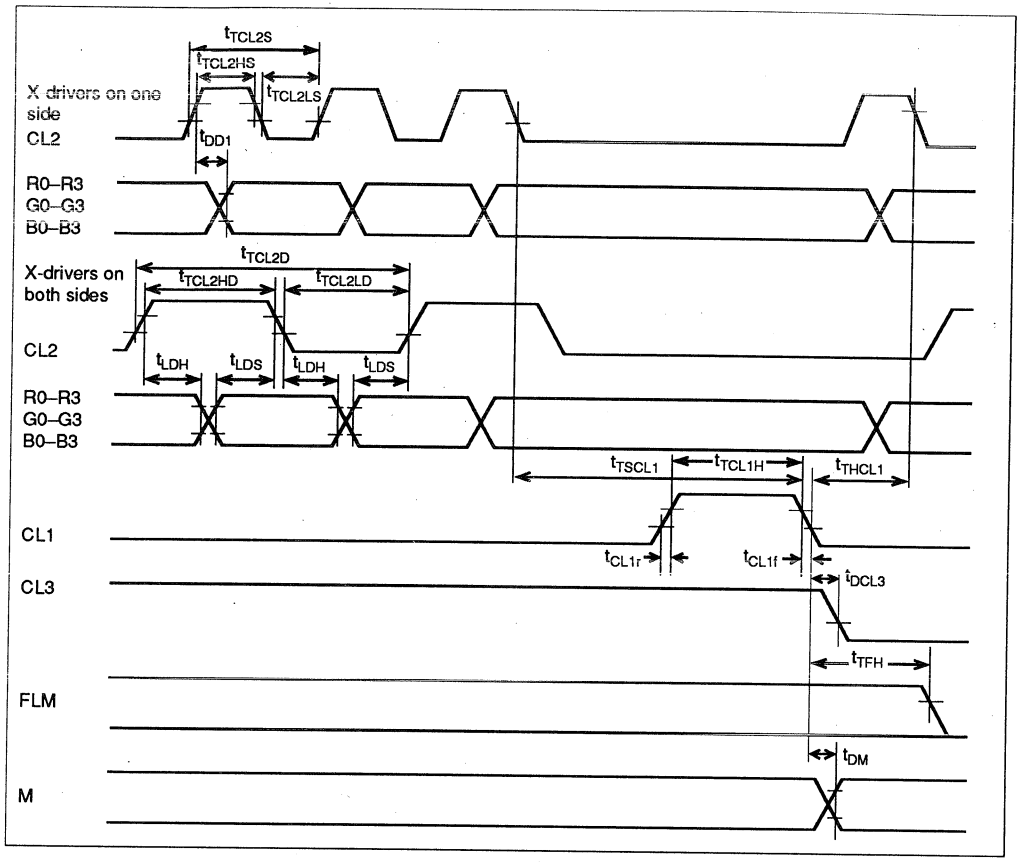


Figure 38 TFT-Type LCD Driver Interface

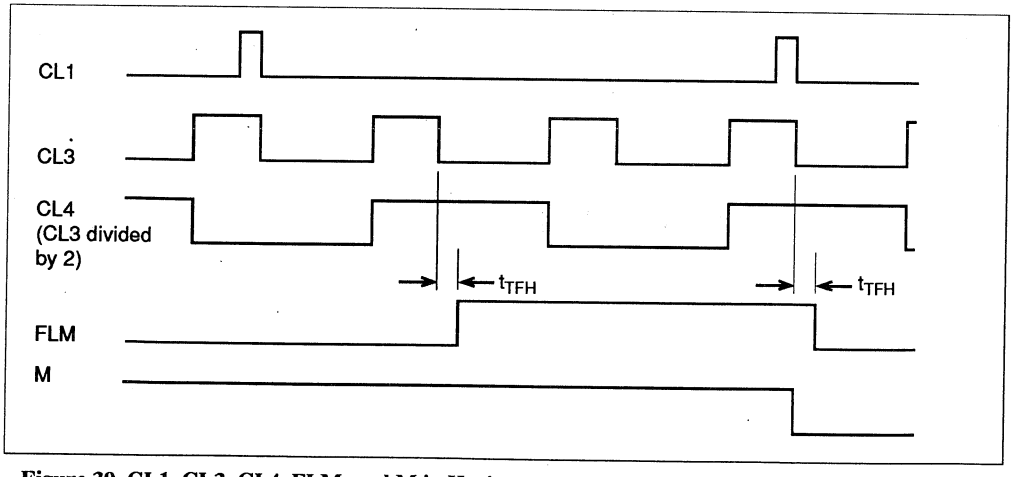


Figure 39 CL1, CL3, CL4, FLM, and M in Horizontal Stripe Modes (expanded detail of figure 38)

Register Programming

MPU Write

Item	Symbol	Min	Max	Unit	Reference
$\overline{RD}$ high-level pulse width	t_{WRDH}	190	—	ns	Figure 40
$\overline{RD}$ low-level pulse width	t_{WRDL}	190	—	ns	
$\overline{WR}$ high-level pulse width	t_{WWRH}	190	—	ns	
$\overline{WR}$ low-level pulse width	t_{WWRL}	190	—	ns	
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns	
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns	
D0–D3 setup time	t_{DSW}	100	—	ns	
D0–D3 hold time	t_{DHW}	0	—	ns	
D0–D3 output delay time	t_{DDR}	—	150	ns	
D0–D3 output hold time	t_{DHR}	10	—	ns	

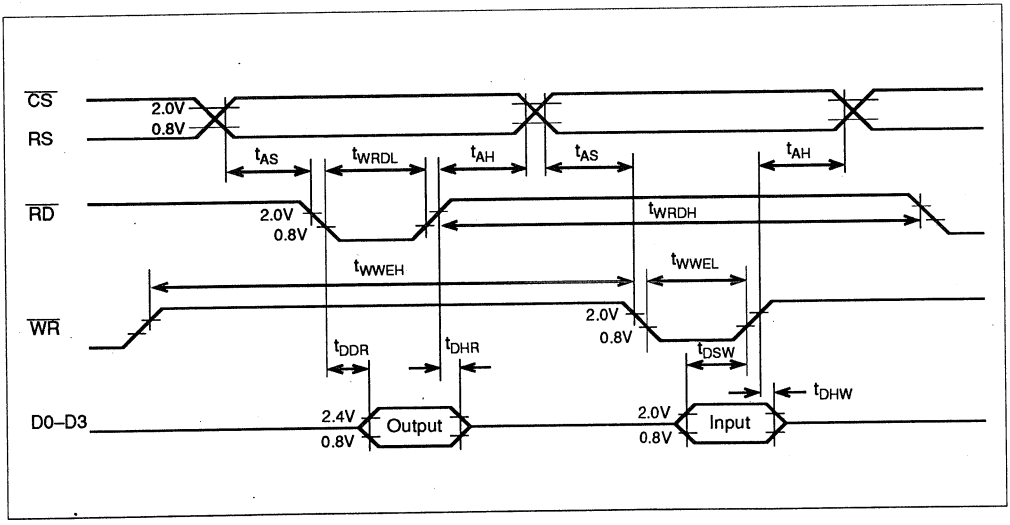


Figure 40 MPU Write Timing

ROM Write

Item	Symbol	Min	Max	Unit	Reference
A signal cycle time	t_{CYCA}	528	—	ns	Figure 41
A signal rise time	t_{Ar}	—	100	ns	
A signal fall time	t_{Af}	—	100	ns	
D signal ROM data setup time	t_{DSWD}	120	—	ns	
D signal ROM data hold time	t_{DHWD}	0	—	ns	

Note: $t_{CYCA} = 16\ t_{CYCD}$ (t_{CYCD}: DOTCLK cycle time)

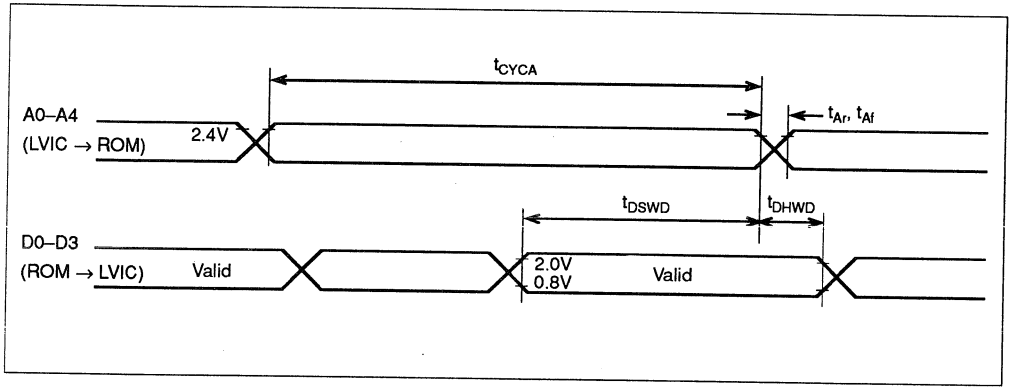


Figure 41 ROM Write Timing

PLL Interface

Item	Symbol	Min	Max	Unit	Reference
$\overline{CU}$ fall delay time	t_{Uf}	—	80	ns	Figure 42
$\overline{CU}$ rise delay time	t_{Ur}	—	80	ns	
$\overline{CD}$ fall delay time	t_{Df}	—	80	ns	
$\overline{CD}$ rise delay time	t_{Dr}	—	80	ns	

Reset Input

Item	Symbol	Min	Max	Unit	Reference
Reset input pulse width	$t_{\overline{RES}}$	1	—	µs	Figure 43

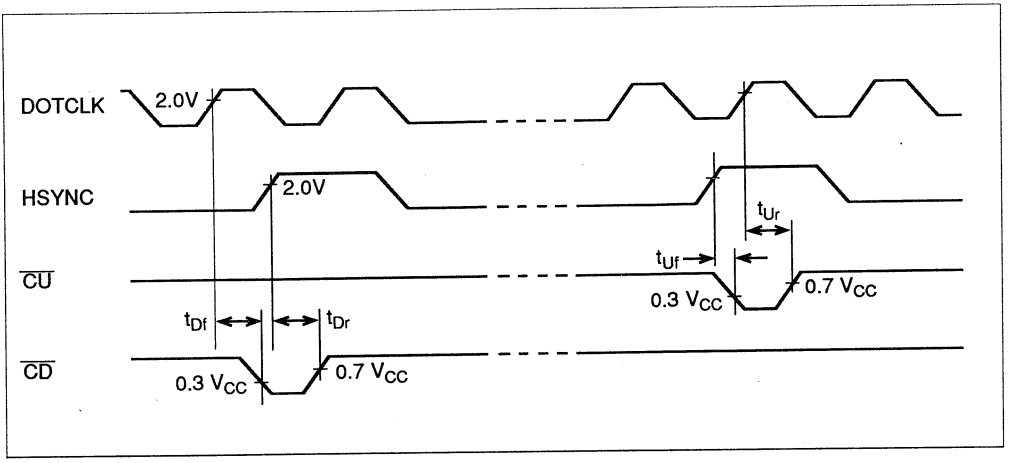


Figure 42 PLL Interface

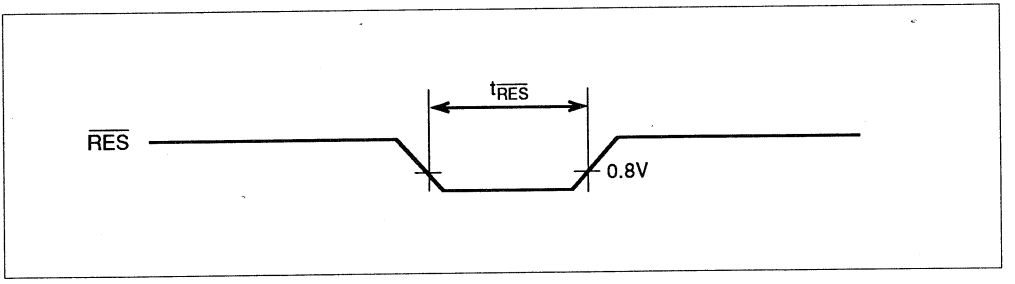


Figure 43 Reset Input

Load Circuits

TTL Load

Pins	R_L	R	C	Remarks
MA0–MA15, $\overline{MWE}$, $\overline{MCS0}$, $\overline{MCS1}$, BD0–BD7, GD0–GD7, RD0–RD7	2.4kΩ	11kΩ	40pF	tr, tf: Not specified
A0/$\overline{RD}$/XDOT, A1/YL0–A3/YL2, A4/RS/ADJ	2.4kΩ	11kΩ	40pF	tr, tf: Specified

Capacitive Load

Pins	C	Remarks
CL1, CL2	40pF	tr, tf: Specified
R0–R3, G0–G3, B0–B3, FLM, M, $\overline{CU}$, $\overline{CD}$, CL3, CL4	40pF	tr, tf: Not specified

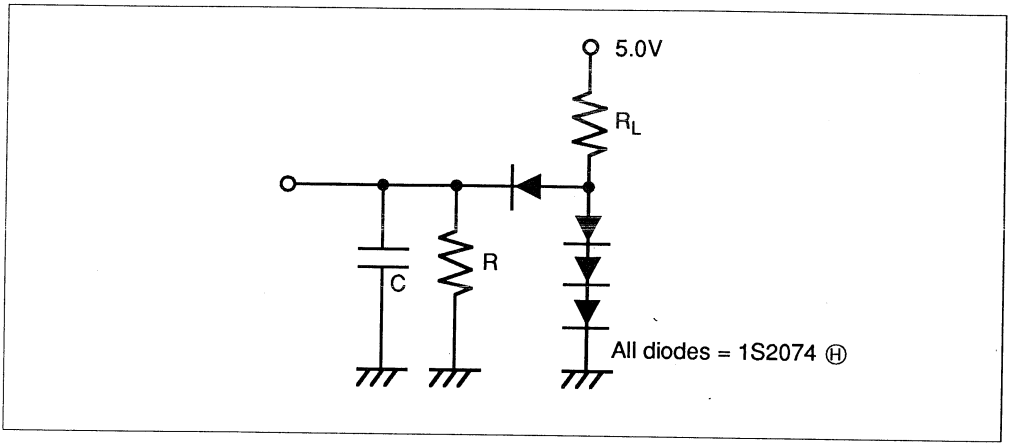


Figure 44 TTL Load Circuit

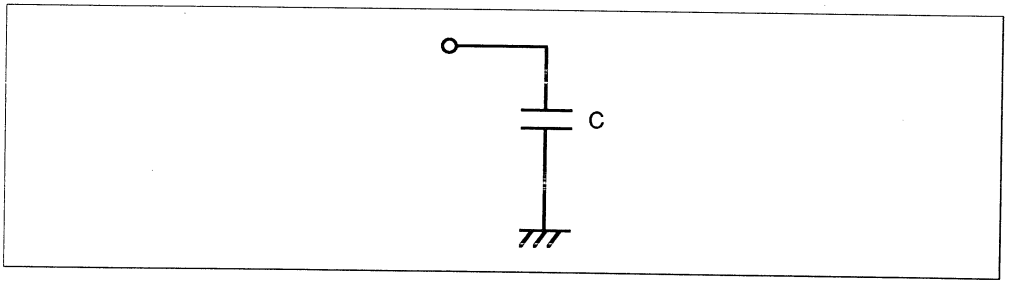


Figure 45 Capacitive Load Circuit

HD153108

Color Palette with Triple 4-bit DA Converters

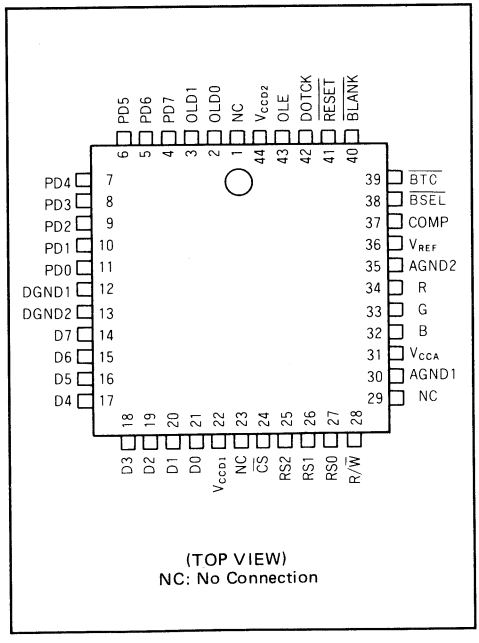
The HD153108 is a triple 4 bit video DAC with dual port RAM, designed specifically for high performance, high resolution color graphics. The HD153108 supports up to 256 simultaneous colors from a 4096 color palette and generates RS-343-A compatible red, green and blue video signals.
The HD153108 realizes high speed, high density and low power dissipation by implementing in Hi-BiCMOS.

Features

- Displays 256 colors simultaneously among total 4096 colors.
- Provides R-G-B 3 channels 4 bit D/A converter on a chip.
- Blanking input to control display.
- Overlay displaying applied for cursor or menu.
- Built in overlay color register to select any 4 colors among 4096 colors.
- Supporting TTL interface.
- Maximum Dotting Rate of 50MHz.
- Utilizing Hi-BiCMOS process of super high speed and low power dissipation.

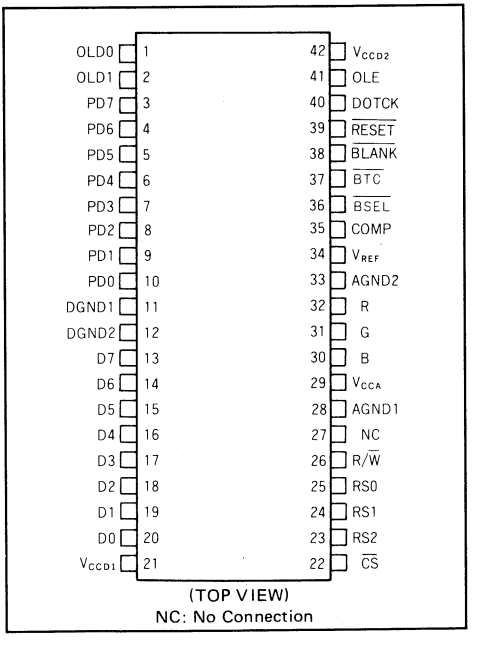
Pin Arrangement

- 44 pin PLCC (CP-44)



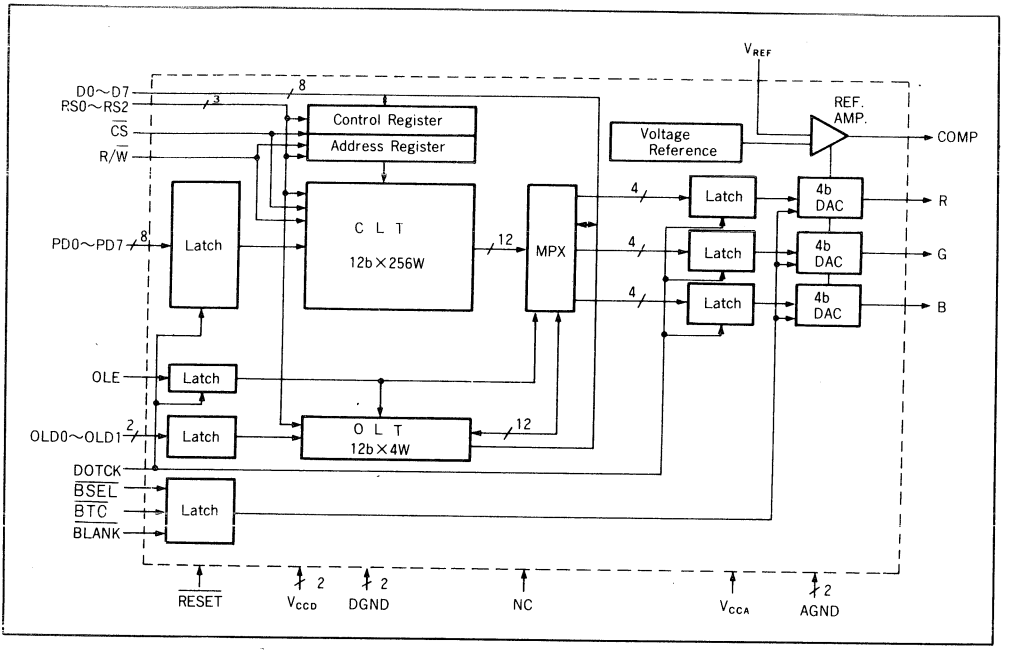
(TOP VIEW)
NC: No Connection

- 42 pin Shrink DIP (DP-42S)



(TOP VIEW)
NC: No Connection

Block Diagram



Pin Description

Pin Name	Pin Number (*)	Description
NC	1, 23, 29 (–, –, 27)	No Connection pin. Usual GNDed.
OLD0, OLD1	2, 3 (1, 2)	Overlay select inputs.
PD0–PD7	11, 10, 9, 8, 7, 6, 5, 4 (10, 9, 8, 7, 6, 5, 4, 3)	Pixel select inputs.
D0–D7	21, 20, 19, 18, 17, 16, 15, 14 (20, 19, 18, 17, 16, 15, 14, 13)	Data input/output terminal when writing/reading CLT. OLT and registers (Address Register, RGB Register, Read Mask Register, Blink Mask Register, Overlay Control Register, Blink Timing Register).
DGND1	12 (11)	Digital ground.
DGND2	13 (12)	Digital ground.
$\overline{CS}$	24 (22)	Chip select control input when writing/reading CLT, OLT.
RS0–RS2	27, 26, 25 (25, 24, 23)	Terminal to select CLT, OLT and registers. For selection, see register mapping in Table 1.1.

(to be continued)

Pin Name	Pin Number (*)	Description
R/$\overline{W}$	28 (26)	Terminal to switch write/read modes of CLT, OLT and registers. The R/$\overline{W}$ signal is activated at $\overline{CS}$="0", and R/$\overline{W}$="1" takes read mode and R/$\overline{W}$="0" takes write mode.
V_{CCD1}	22 (21)	Digital power.
V_{CCD2}	44 (42)	Digital power.
AGND1	30 (28)	Analog ground.
AGND2	35 (33)	Analog ground.
B	32 (30)	DAC(Blue) analog output.
G	33 (31)	DAC(Green) analog output.
R	34 (32)	DAC(Red) analog output.
V_{REF}	36 (34)	Terminal to connect a reference resistor. A reference resistor must be connected between this terminal and AGND1.
COMP	37 (35)	Terminal to connect a capacitor for phase-compensation. A 0.1μF capacitor and a 4.7μF capacitor must be connected between COMP and AGND1.
$\overline{BSEL}$	38 (36)	Input terminal to set BLANK level. At $\overline{BSEL}$ = "0", the BLANK level is set. At $\overline{BSEL}$ = "1", it's not set. When set, the BLANK level will be 7.5 IRE.
$\overline{BTC}$	39 (37)	Input terminal to provide reference clock when setting the blink timing. For the concrete setting method, refer to the section of blink timing register below. Normally, vertical synchronizing signal is provided.
$\overline{BLANK}$	40 (38)	Composite blank control input. When $\overline{BLANK}$="0". DAC output becomes blank level in any CLT and OLT.
$\overline{RESET}$	41 (39)	Reset signal input for all the F/F in digital part. At $\overline{RESET}$="0", they are reset and initialized.
DOTCK	42 (40)	Clock input to do operation of digital and analog parts. Operating speed is determined by the speed of this clock. When this clock rises, CLT and OLT addresses and each input data of $\overline{BSEL}$, $\overline{BTC}$ and $\overline{BLANK}$ are taken, and analog signals are output. And, it's also used as the reference clock on writing into CLT and OLT.
OLE	43 (41)	Signal input to switch CLT and OLT. OLT is selected at OLE="1" and at OLE="0" CLT is selected. However, when OLE="1", OLD0, OLD1="0" and b6 of overlay control register="1", CLT can be selected.
VCCA	31 (29)	Analog power.

(*) Pin numbers at the upper column indicate those of PLCC-44 and the figures in parentheses at the lower column indicate those of DILP-42 shrink.

Functional Description

1. Address Register

Address Register is selected by input signal at RS0–RS2 Pins. (Table 1.1) The less significant 2 bits of the register are used as R.G.B pointer, and the more significant 8 bits are used to select words of CLT (Color Lookup Table) and OLT (Overlay Table). (Table 2)

Table 1.1 Register Mapping

RS2	RS1	RS0	Register Contents
0	0	0	Address Register (A0–A9)
0	0	1	Color Lookup Table
0	1	0	Reserved
0	1	1	Overlay Table
1	0	0	Read Mask Register
1	0	1	Blink Mask Register
1	1	0	Overlay Control Register (See Table 1.2)
1	1	1	Blink Timing Register

Table 1.2 Overlay Control Register

Address of Register	Controls
b7	Reserved
b6	CLT Enable
b5	Reserved
b4	Reserved
b3	OLD1 Blink Mask
b2	OLD0 Blink Mask
b1	OLD1 Read Mask
b0	OLD0 Read Mask

Table 2 Address Register Function

Address Register	Value	RS1	Selected Block
A0–A1	00		Red
	01		Green
	10		Blue
A2–A9	$00–$FF	0	Color Lookup Table
	$00	1	Overlay Color 0
	$01	1	Overlay Color 1
	$02	1	Overlay Color 2
	$03	1	Overlay Color 3

2. Access to CLT/OLT

CLT/OLT are accessed by the unit of R, G or B set and the word is selected by address information in the address register. When addresses are written from D0–D7 to A2–A9, A0–A1 are initialized to select R.
Once, initialized, each access to select CLT/OLT increases A0–A1 to select in the order or R→G→B. Written data to R and G are latched internally until the data is written to B, write to R, G and B is taken simultaneously. After access to B, A2–A9 increase by 1 and A0–A1 select R. (Table 3)

During the OLE terminal is "Low". CLT output of the address defined by PD7–PD0 is selected to be displayed. During OLE "High", OLT output defined by OLD1–OLD0 is displayed. However, even if OLE is "High", OLE0, OLE1="0" and b6 of overlay control register is "High", CLT can be selected (Table 4.)

Table 3 Read/Write Operation Truth Table

	R/$\overline{W}$	RS2	RS1	RS0	A1	A0	Functions
CLT	0	0	0	0	–	–	Write to Address Register ; D0–D7→A2–A9, 00→A0–A1
	0	0	0	1	0	0	Write R(red) data ; +1 increment for A0–A9
	0	0	0	1	0	1	Write G(green) data ; +1 increment for A0–A9
	0	0	0	1	1	0	Write B(blue) data ; +2 increment for A0–A9
	1	0	0	0	–	–	Read from Address Register ; A2–A9→D0–D7, 00→A0–A1
	1	0	0	1	0	0	Read R(red) data ; +1 increment for A0–A9
	1	0	0	1	0	1	Read G(green) data ; +1 increment for A0–A9
	1	0	0	1	1	0	Read B(blue) data ; +2 increment for A0–A9
OLT	0	0	0	0	–	–	Write to Address Register ; D0–D1→A2–A3, 00→A0–A1
	0	0	1	1	0	0	Write R(red) data ; +1 increment for A0–A3
	0	0	1	1	0	1	Write G(green) data ; +1 increment for A0–A3
	0	0	1	1	1	0	Write B(blue) data ; +2 increment for A0–A3
	1	0	0	0	–	–	Read from Address Register ; A2–A3→D0–D1, 00→A0–A1
	1	0	1	1	0	0	Read R(red) data ; +1 increment for A0–A3
	1	0	1	1	0	1	Read G(green) data ; +1 increment for A0–A3
	1	0	1	1	1	0	Read B(blue) data ; +2 increment for A0–A3

Table 4 Pixel Selection & Overlay Control Truth Table

OLE	OLD1	OLD0	Overlay Control Register	PD7–PD0	Selected Block
0	X	X	X	$nn	Color Lookup Table ($nn)
1	0	0	0	X	Overlay color 0
1	0	1	0	X	Overlay color 1
1	1	0	0	X	Overlay color 2
1	1	1	0	X	Overlay color 3
1	0	0	1	$nn	Color Lookup Table ($nn)

3. Internal Registers

1. Read Mask Register
   Read Mask register is used to mask CLT address terminals (PD0–PD7). Read Mask register consists of 8 bits (bR0–bR7). The bR0 corresponds to PD0 and bR7 to PD7. When each bit of the register is "1", the corresponding address input terminal is masked. At "0", the mask is cancelled.
2. Blink Mask Register
   Blink Mask register is used to mask CLT address input terminals (PD0–PD7) being blink conditions. Blink Mask register of 8 bits (bB0–bB7). The bB0 corresponds to PD0 and bB7 to PD7. When each bit of the register is "1", the blink of the corresponding address input terminal is masked. At "0", the mask is cancelled.
   Accordingly, when blinking is not desired, it should normally be masked by setting all bits of the blink mask register to "1".
3. Overlay Control Register
   Overlay Control register is used for read mask of OLT address input terminals, blink mask, and switching OLT to CLT. Overlay Control register consists of 8 bits (b0–b7) (Table 1.2) and b0–b1 are used for read mask of OLD0–OLD1. b2–b3 are used for blink mask and b6 enables selection of CLT (Table 4).
4. Blink Timing Register
   Blink Timing register is used to set the blink on timing and blink off timing of CLT, OLT address input terminals. Blink Timing register consists of 8 bits (b_{T0}–b_{T7}). The least significant 4 bit bT0–bT3 set the blink on time and the most significant 4 bits bT4–bT7 set the blink off timing. Both of the blink on timing and blink off timing are set by the 4(n+1) magnifications of $\overline{BTC}$ signal cycle (Table 5.1, Table 5.2).

Table 5.1 Blink on Time

b_{T3}	b_{T2}	b_{T1}	b_{T0}	Blink On Time
0	0	0	0	4 x t_{BTC}
0	0	0	1	8 x t_{BTC}
0	0	1	0	12 x t_{BTC}
0	0	1	1	16 x t_{BTC}
0	1	0	0	20 x t_{BTC}
0	1	0	1	24 x t_{BTC}
0	1	1	0	28 x t_{BTC}
0	1	1	1	32 x t_{BTC}
1	0	0	0	36 x t_{BTC}
1	0	0	1	40 x t_{BTC}
1	0	1	0	44 x t_{BTC}
1	0	1	1	48 x t_{BTC}
1	1	0	0	52 x t_{BTC}
1	1	0	1	56 x t_{BTC}
1	1	1	0	60 x t_{BTC}
1	1	1	1	64 x t_{BTC}

Table 5.2 Blink off Time

b_{T7}	b_{T6}	b_{T5}	b_{T4}	Blink Off Time
0	0	0	0	4 x t_{BTC}
0	0	0	1	8 x t_{BTC}
0	0	1	0	12 x t_{BTC}
0	0	1	1	16 x t_{BTC}
0	1	0	0	20 x t_{BTC}
0	1	0	1	24 x t_{BTC}
0	1	1	0	28 x t_{BTC}
0	1	1	1	32 x t_{BTC}
1	0	0	0	36 x t_{BTC}
1	0	0	1	40 x t_{BTC}
1	0	1	0	44 x t_{BTC}
1	0	1	1	48 x t_{BTC}
1	1	0	0	52 x t_{BTC}
1	1	0	1	56 x t_{BTC}
1	1	1	0	60 x t_{BTC}
1	1	1	1	64 x t_{BTC}

t_{BTC}: $\overline{BTC}$ cycle time

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_{IN}	0 to V_{CC}	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{str}	–55 to +150	°C

Recommended Operating Conditions

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.75	5.00	5.25	V
Input "Low" Level Voltage	V_{IL}	0	–	0.8	V
Input "High" Level Voltage	V_{IH}	2.0	–	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

Electrical Characteristics

DAC Characteristics (V_{CC} = 5V, Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		4	4	4	bits	
Maximum Operating Frequency	f_{CLK}	–	–	50	MHz	
Analog Output Voltage (R_{VREF}=12kΩ)	V_A(Full)	–15	–	15	% of FSR	
	V_A(Zero)	– 2	–	2	% of FSR	
Differential Linearity	DLE	–1/2	–	+1/2	LSB	
Integral Linearity	ILE	–1/2	–	+1/2	LSB	
Output Rise Time (20%–80%)	tr	–	–	10	ns	C_L = 15pF
Output Fall Time (80%–20%)	tf	–	–	10	ns	C_L = 15pF
Settling Time	ts	–	–	30	ns	C_L = 15pF
Glitch Energy	E_G	–	90	–	PVS	

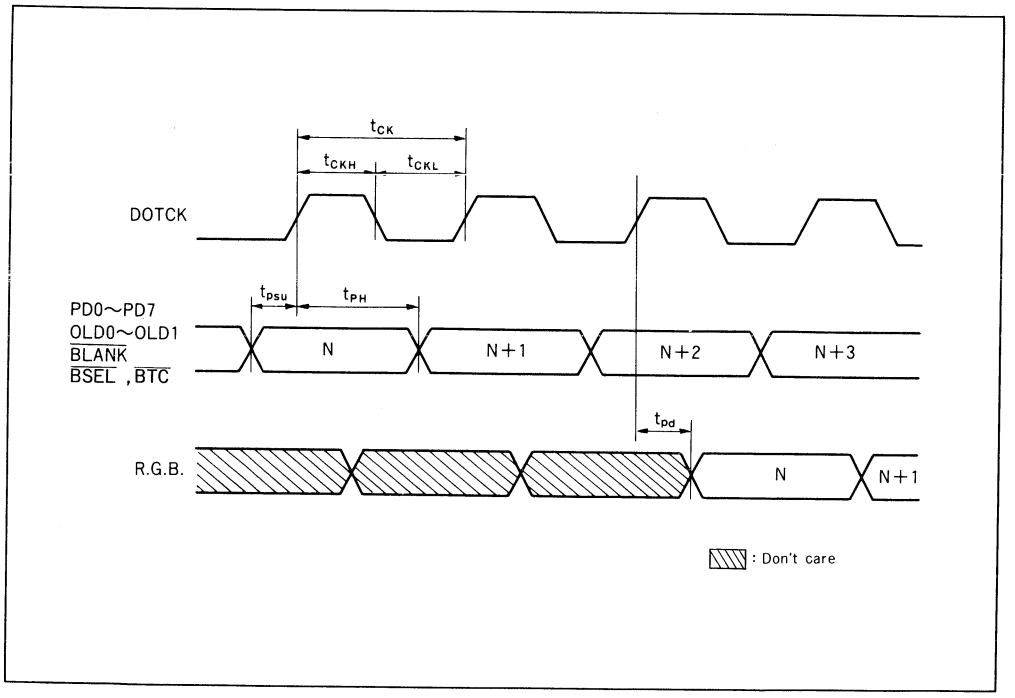
DC Characteristics (V_{CC}=5V±5%, Ta=0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input "High" Level Voltage	V_{IH}	2.0	–	V_{CC}	V	
Input "Low" Level Voltage	V_{IL}	–0.3	–	0.8	V	
Input Clamp Voltage	V_I	–	–	–1.5	V	V_{CC} = 4.75V I_{IN} = –18mA
Output "High" Level Voltage	V_{OH}	2.7	–	–	V	V_{CC} = 4.75V I_{OH} = –400μA
Output "Low" Level Voltage	V_{OL}	–	–	0.5	V	V_{CC} = 4.75V I_{OL} = 8mA
Input Current	I_I	–	–	1	mA	V_{CC} = 5.25V V_I = 5.5V
"High" Level Input Current	I_{IH}	–	–	20	μA	V_{CC} = 5.25V V_I = 2.7V
"Low" Level Input Current	I_{IL}	–	–	–400	μA	V_{CC} = 5.25V V_I = 0.4V

Switching Characteristics

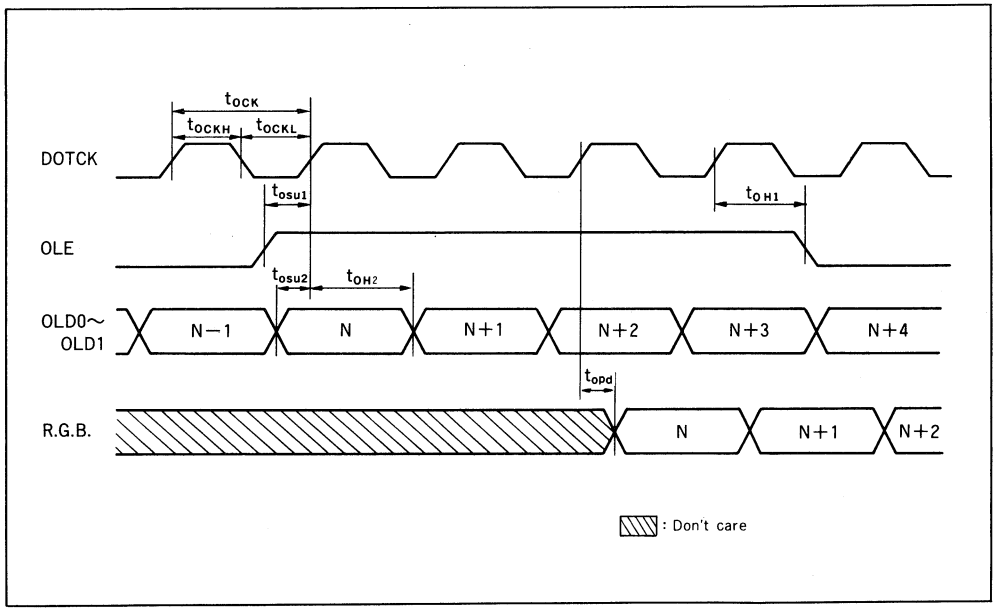
VIDEO Output (CLT) (V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
DOTCK Cycle Time	t_{CK}	20	—	ns	
DOTCK Width High	t_{CKH}	8	—	ns	
DOTCK Width Low	t_{CKL}	8	—	ns	
Data Setup Time	t_{PSU}	6	—	ns	
Data Hold Time	t_{PH}	6	—	ns	
Output Delay Time	t_{pd}	—	30	ns	C_L = 15pF



VIDEO Output (OLT) (V_{CC} = 5V, Ta = 25°C)

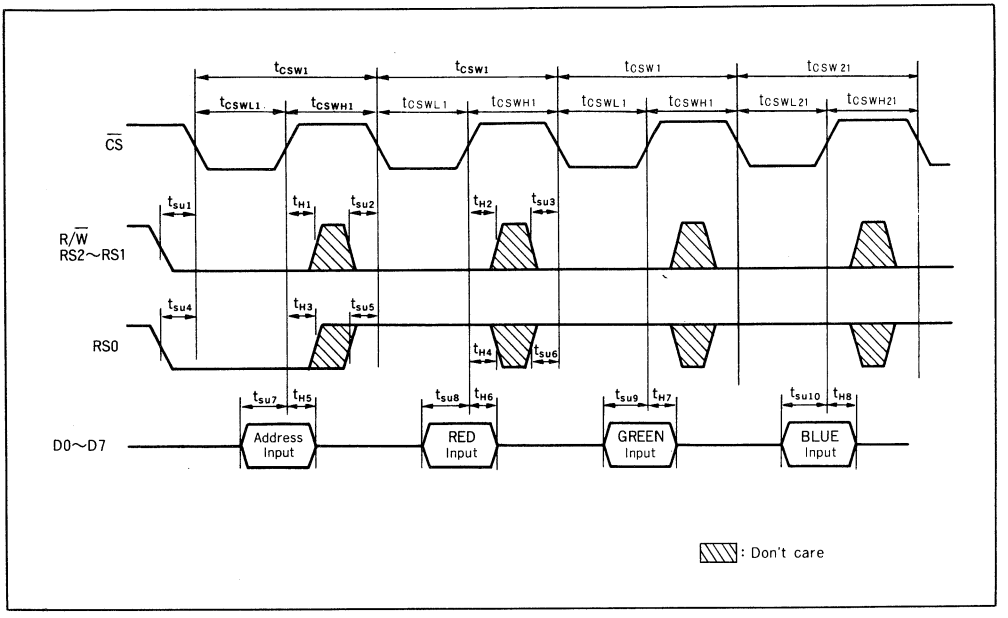
Item	Symbol	Min	Max.	Unit	Test Condition
DOTCK Cycle Time	t_{OCK}	20	–	ns	
DOTCK Width High	t_{OCKH}	8	–	ns	
DOTCK Width Low	t_{OCKL}	8	–	ns	
Data Setup Time	t_{OSU1}	6	–	ns	
Data Setup Time	t_{OSU2}	6	–	ns	
Data Hold Time	t_{OH1}	6	–	ns	
Data Hold Time	t_{OH2}	6	–	ns	
Output Delay Time	t_{Opd}	–	30	ns	C_L = 15pF



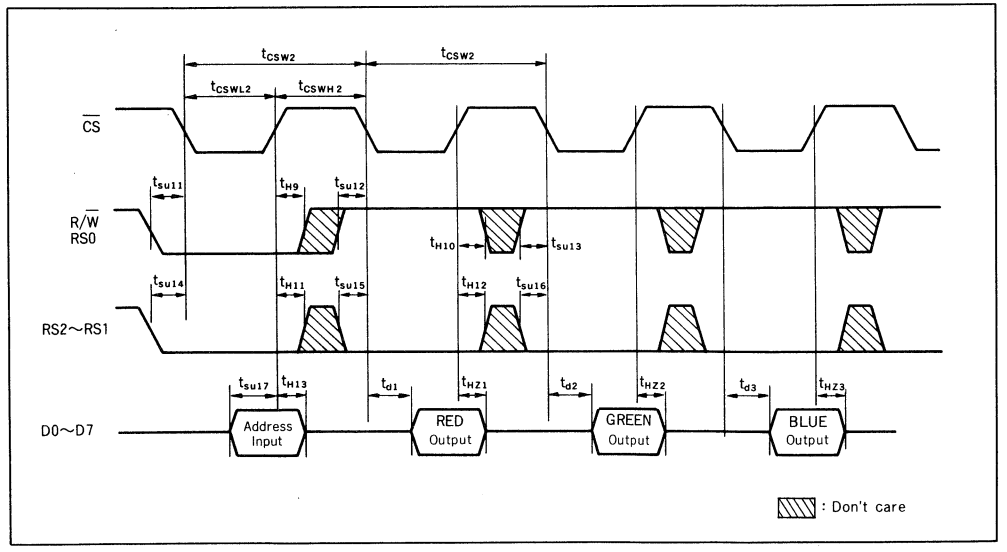
CLT Access (V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{CS}$ Cycle Time	t_{CSW1}	100	–	ns	
$\overline{CS}$ Width Low	t_{CSWL1}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH1}	50	–	ns	
R/$\overline{W}$, RS2, RS1 Setup Time	t_{SU1}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Setup Time	t_{SU2}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Setup Time	t_{SU3}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Hold Time	t_{H1}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Hold Time	t_{H2}	6	–	ns	
RS0 Setup Time	t_{SU4}	6	–	ns	
RS0 Setup Time	t_{SU5}	6	–	ns	
RS0 Setup Time	t_{SU6}	6	–	ns	
Address Data Setup Time	t_{SU7}	6	–	ns	
RED Data Setup Time	t_{SU8}	6	–	ns	
GREEN Data Setup Time	t_{SU9}	6	–	ns	
BLUE Data Setup Time	t_{SU10}	6	–	ns	
RS0 Hold Time	t_{H3}	6	–	ns	
RS0 Hold Time	t_{H4}	6	–	ns	
Address Data Hold Time	t_{H5}	6	–	ns	
RED Data Hold Time	t_{H6}	6	–	ns	
GREEN Data Hold Time	t_{H7}	6	–	ns	
BLUE Data Hold Time	t_{H8}	6	–	ns	
$\overline{CS}$ Cycle Time	t_{CSW2}	100	–	ns	
$\overline{CS}$ Width Low	t_{CSWL2}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH2}	50	–	ns	
R/$\overline{W}$, RS0 Setup Time	t_{SU11}	6	–	ns	
R/$\overline{W}$, RS0 Setup Time	t_{SU12}	6	–	ns	
R/$\overline{W}$, RS0 Setup Time	t_{SU13}	6	–	ns	
RS2, RS1 Setup Time	t_{SU14}	6	–	ns	
RS2, RS1 Setup Time	t_{SU15}	6	–	ns	
RS2, RS1 Setup Time	t_{SU16}	6	–	ns	
Address Data Setup Time	t_{SU17}	6	–	ns	
R/$\overline{W}$, RS0 Hold Time	t_{H9}	6	–	ns	
R/$\overline{W}$, RS0 Hold Time	t_{H10}	6	–	ns	
RS2, RS1 Hold Time	t_{H11}	6	–	ns	
RS2, RS1 Hold Time	t_{H12}	6	–	ns	
Address Data Hold Time	t_{H13}	6	–	ns	
RED Output Delay Time	t_{d1}	–	75	ns	C_L = 50pF
GREEN Output Delay Time	t_{d2}	–	75	ns	C_L = 50pF
BLUE Output Delay Time	t_{d3}	–	75	ns	C_L = 50pF
RED Output Hold Time	t_{HZ1}	5	–	ns	
GREEN Output Hold Time	t_{HZ2}	5	–	ns	
BLUE Output Hold Time	t_{HZ3}	5	–	ns	
$\overline{CS}$ Cycle Time	t_{CSW21}	50 + 3 x t_{CK}	–	ns	
$\overline{CS}$ Width Low	t_{CSWL21}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH21}	3 x t_{CK}	–	ns	

WRITE


tCSW1
tCSW1
tCSW1
tCSW21
tCSWL1
tCSWH1
tCSWL1
tCSWH1
tCSWL1
tCSWH1
tCSWL21
tCSWH21
CS
tsu1
tH1
tsu2
tH2
tsu3
R/W
RS2~RS1
tsu4
tH3
tsu5
RS0
tH4
tsu6
tsu7
tH5
tsu8
tH6
tsu9
tH7
tsu10
tH8
D0~D7
Address Input
RED Input
GREEN Input
BLUE Input
: Don't care

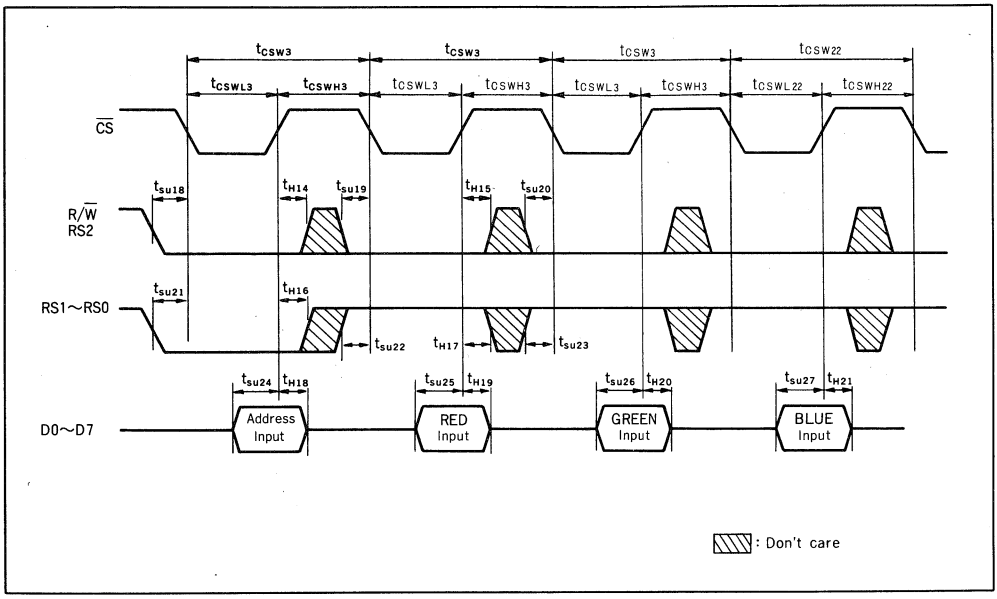
READ


tCSW2
tCSW2
tCSWL2
tCSWH2
CS
tsu11
tH9
tsu12
R/W
RS0
tH10
tsu13
tsu14
tH11
tsu15
tH12
tsu16
RS2~RS1
tsu17
tH13
td1
tHZ1
td2
tHZ2
td3
tHZ3
D0~D7
Address Input
RED Output
GREEN Output
BLUE Output
: Don't care

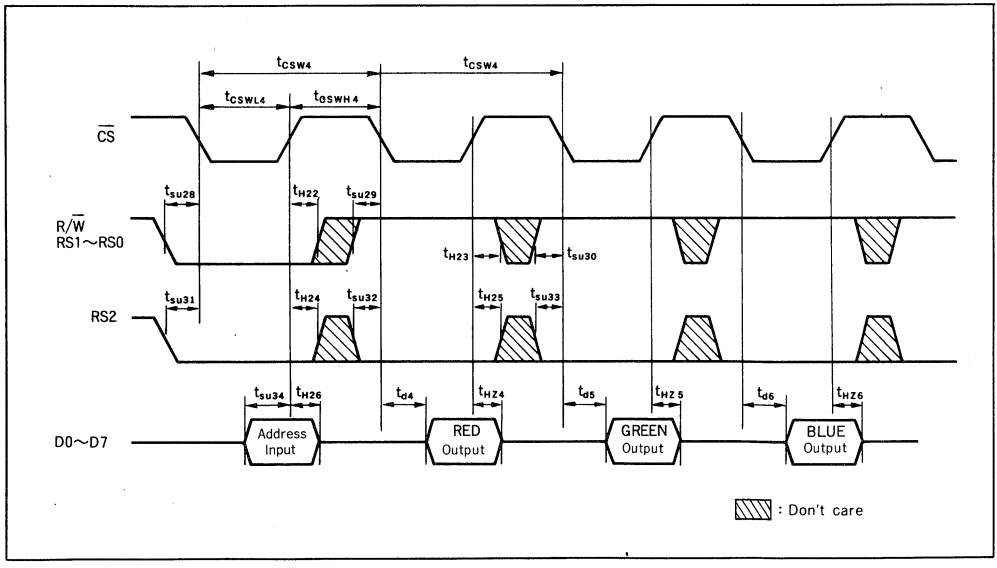
OLT Access (V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{CS}$ Cycle Time	t_{CSW3}	100	–	ns	
$\overline{CS}$ Width Low	t_{CSWL3}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH3}	50	–	ns	
R/$\overline{W}$, RS2 Setup Time	t_{SU18}	6	–	ns	
R/$\overline{W}$, RS2 Setup Time	t_{SU19}	6	–	ns	
R/$\overline{W}$, RS2 Setup Time	t_{SU20}	6	–	ns	
RS1, RS0 Setup Time	t_{SU21}	6	–	ns	
RS1, RS0 Setup Time	t_{SU22}	6	–	ns	
RS1, RS0 Setup Time	t_{SU23}	6	–	ns	
Address Data Setup Time	t_{SU24}	6	–	ns	
RED Data Setup Time	t_{SU25}	6	–	ns	
GREEN Data Setup Time	t_{SU26}	6	–	ns	
BLUE Data Setup Time	t_{SU27}	6	–	ns	
R/$\overline{W}$, RS2 Hold Time	t_{H14}	6	–	ns	
R/$\overline{W}$, RS2 Hold Time	t_{H15}	6	–	ns	
RS1, RS0 Hold Time	t_{H16}	6	–	ns	
RS1, RS0 Hold Time	t_{H17}	6	–	ns	
Address Data Hold Time	t_{H18}	6	–	ns	
RED Data Hold Time	t_{H19}	6	–	ns	
GREEN Data Hold Time	t_{H20}	6	–	ns	
BLUE Data Hold Time	t_{H21}	6	–	ns	
$\overline{CS}$ Cycle Time	t_{CSW4}	100	–	ns	
$\overline{CS}$ Width Low	t_{CSWL4}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH4}	50	–	ns	
R/$\overline{W}$, RS1, RS0 Setup Time	t_{SU28}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Setup Time	t_{SU29}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Setup Time	t_{SU30}	6	–	ns	
RS2 Setup Time	t_{SU31}	6	–	ns	
RS2 Setup Time	t_{SU32}	6	–	ns	
RS2 Setup Time	t_{SU33}	6	–	ns	
Address Data Setup Time	t_{SU34}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Hold Time	t_{H22}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Hold Time	t_{H23}	6	–	ns	
RS2 Hold Time	t_{H24}	6	–	ns	
RS2 Hold Time	t_{H25}	6	–	ns	
Address Data Hold Time	t_{H26}	6	–	ns	
RED Output Delay Time	t_{d4}	–	75	ns	C_L = 50pF
GREEN Output Delay Time	t_{d5}	–	75	ns	C_L = 50pF
BLUE Output Delay Time	t_{d6}	–	75	ns	C_L = 50pF
RED Output Hold Time	t_{HZ4}	5	–	ns	
GREEN Output Hold Time	t_{HZ5}	5	–	ns	
BLUE Output Hold Time	t_{HZ6}	5	–	ns	
$\overline{CS}$ Cycle Time	t_{CSW22}	50 + 3 x t_{OCK}	–	ns	
$\overline{CS}$ Width Low	t_{CSWL22}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH22}	3 x t_{OCK}	–	ns	

WRITE


tCSW3
tCSW3
tCSW3
tCSW22
tCSWL3
tCSWH3
tCSWL3
tCSWH3
tCSWL3
tCSWH3
tCSWL22
tCSWH22
CS
R/W
RS2
RS1~RS0
tsu18
tH14
tsu19
tH15
tsu20
tsu21
tH16
tsu22
tH17
tsu23
tsu24
tH18
tsu25
tH19
tsu26
tH20
tsu27
tH21
D0~D7
Address Input
RED Input
GREEN Input
BLUE Input
: Don't care

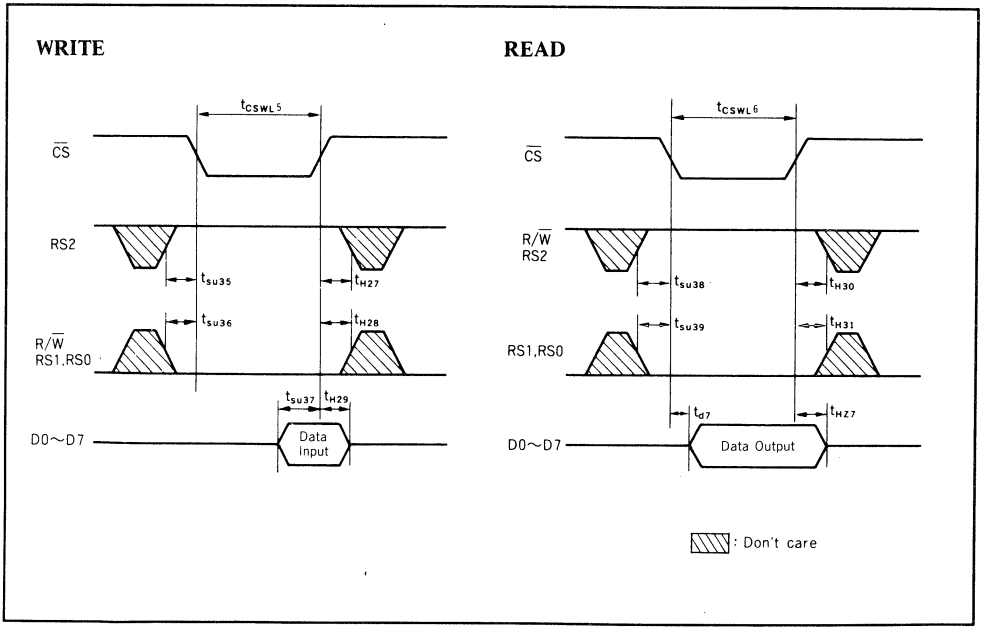
READ


tCSW4
tCSW4
tCSWL4
tCSWH4
CS
R/W
RS1~RS0
RS2
tsu28
tH22
tsu29
tH23
tsu30
tsu31
tH24
tsu32
tH25
tsu33
tsu34
tH26
td4
tHZ4
td5
tHZ5
td6
tHZ6
D0~D7
Address Input
RED Output
GREEN Output
BLUE Output
: Don't care

READ MASK Register Access

(V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
$\overline{CS}$ Width Low	t_{CSWL5}	50	–	ns	
RS2 Setup Time	t_{SU35}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Setup Time	t_{SU36}	6	–	ns	
Input Data Setup Time	t_{SU37}	6	–	ns	
RS2 Hold Time	t_{H27}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Hold Time	t_{H28}	6	–	ns	
Input Data Hold Time	t_{H29}	6	–	ns	
$\overline{CS}$ Width Low	t_{CSWL6}	50	–	ns	
R/$\overline{W}$, RS2 Setup Time	t_{SU38}	6	–	ns	
RS1, RS0 Setup Time	t_{SU39}	6	–	ns	
R/$\overline{W}$, RS2 Hold Time	t_{H30}	6	–	ns	
RS1, RS0 Hold Time	t_{H31}	6	–	ns	
READ MASK Register Output Delay	t_{d7}	–	75	ns	C_L = 50pF
READ MASK Register Output Hold Time	t_{HZ7}	5	–	ns	

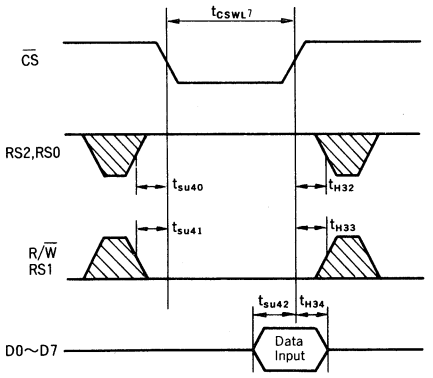


BLINK MASK Register Access

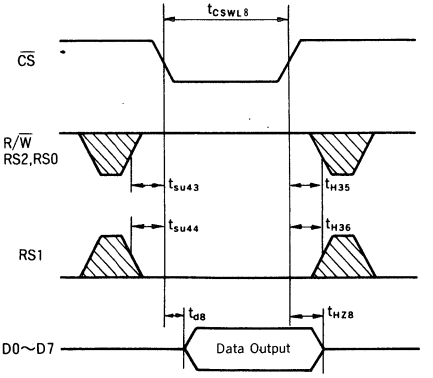
(V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
$\overline{CS}$ Width Low	t_{CSWL7}	50	–	ns	
RS2, RS0 Setup Time	t_{SU40}	6	–	ns	
R/$\overline{W}$, RS1 Setup Time	t_{SU41}	6	–	ns	
Input Data Setup Time	t_{SU42}	6	–	ns	
RS2, RS0 Hold Time	t_{H32}	6	–	ns	
R/$\overline{W}$, RS1 Hold Time	t_{H33}	6	–	ns	
Input Data Hold Time	t_{H34}	6	–	ns	
$\overline{CS}$ Width Low	t_{CSWL8}	50	–	ns	
R/$\overline{W}$, RS2, RS0 Setup Time	t_{SU43}	6	–	ns	
RS1 Setup Time	t_{SU44}	6	–	ns	
R/$\overline{W}$, RS2, RS0 Hold Time	t_{H35}	6	–	ns	
RS1 Hold Time	t_{H36}	6	–	ns	
BLINK MASK Register Output Delay	t_{d8}	–	75	ns	C_L = 50pF
BLINK MASK Register Output Hold Time	t_{HZ8}	5	–	ns	

WRITE



READ

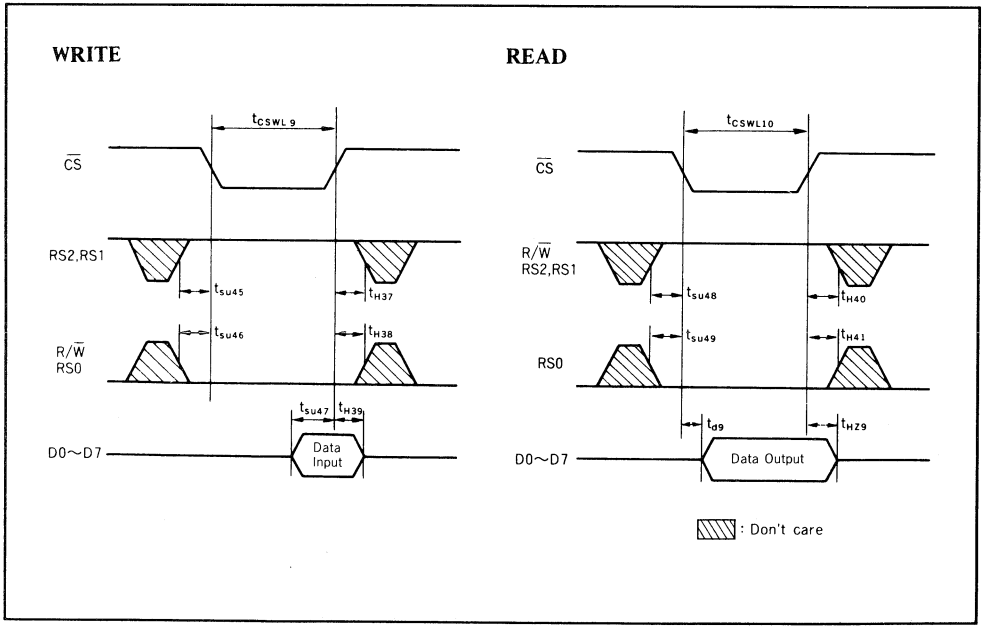


: Don't care

OVERLAY CONTROL Register Access

(V_{CC} = 5V, Ta = 25°C)

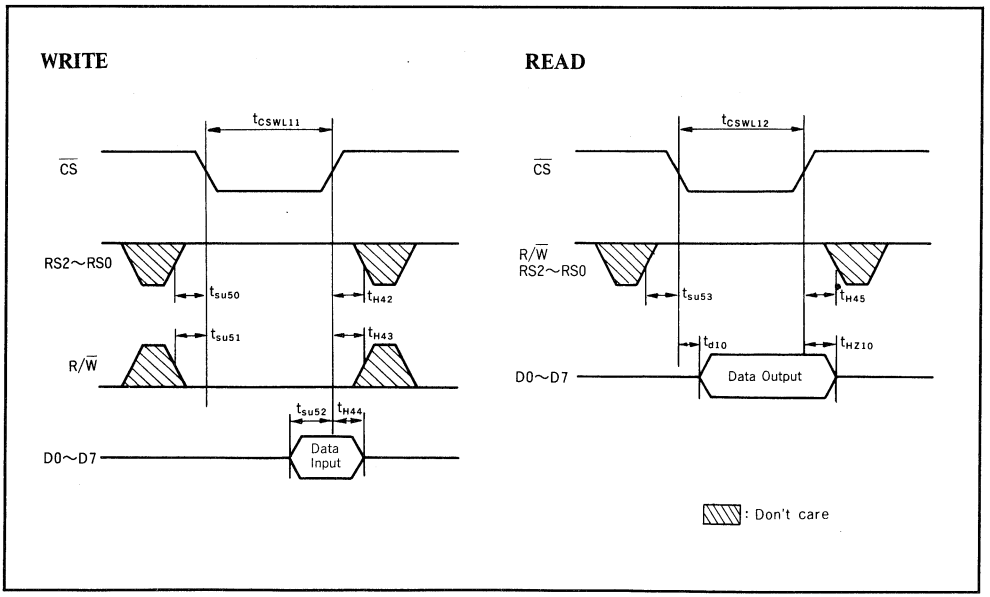
Item	Symbol	Min.	Max.	Unit	Test Condition
$\overline{CS}$ Width Low	t_{CSWL9}	50	–	ns	
RS2, RS1 Setup Time	t_{SU45}	6	–	ns	
R/$\overline{W}$, RS0 Setup Time	t_{SU46}	6	–	ns	
Input Data Setup Time	t_{SU47}	6	–	ns	
RS2, RS1 Hold Time	t_{H37}	6	–	ns	
R/$\overline{W}$, RS0 Hold Time	t_{H38}	6	–	ns	
Input Data Hold Time	t_{H39}	6	–	ns	
$\overline{CS}$ Width Low	t_{CSWL10}	50	–	ns	
R/$\overline{W}$, RS2, RS1 Setup Time	t_{SU48}	6	–	ns	
RS0 Setup Time	t_{SU49}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Hold Time	t_{H40}	6	–	ns	
RS0 Hold Time	t_{H41}	6	–	ns	
OVERLAY CONTROL Register Output Delay	t_{d9}	–	75	ns	C_L = 50pF
OVERLAY CONTROL Register Output Hold Time	t_{HZ9}	5	–	ns	



BLINK TIMING Register Access

(V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
$\overline{CS}$ Width Low	t_{CSWL11}	50	–	ns	
RS2, RS1, RS0 Setup Time	t_{SU50}	6	–	ns	
R/$\overline{W}$ Setup Time	t_{SU51}	6	–	ns	
Input Data Setup Time	t_{SU52}	6	–	ns	
RS2, RS1, RS0 Hold Time	t_{H42}	6	–	ns	
R/$\overline{W}$ Hold Time	t_{H43}	6	–	ns	
Input Data Hold Time	t_{H44}	6	–	ns	
$\overline{CS}$ Width Low	t_{CSWL12}	50	–	ns	
R/$\overline{W}$, RS2, RS1, RS0 Setup Time	t_{SU53}	6	–	ns	
R/$\overline{W}$, RS2, RS1, RS0 Hold Time	t_{H45}	6	–	ns	
BLINK TIMING Register Output Delay	t_{d10}	–	75	ns	C_L = 50pF
BLINK TIMING Register Output Hold Time	t_{HZ10}	5	–	ns	



CRT Monitor Interface

R, G and B output (analog) waveform will be like Fig. 2 (a), (b) under the load condition in Fig. 1.

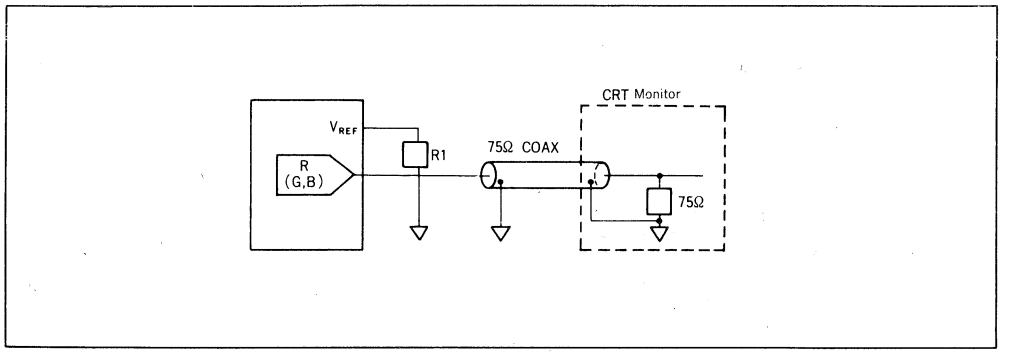


Fig. 1. CRT Monitor Interface

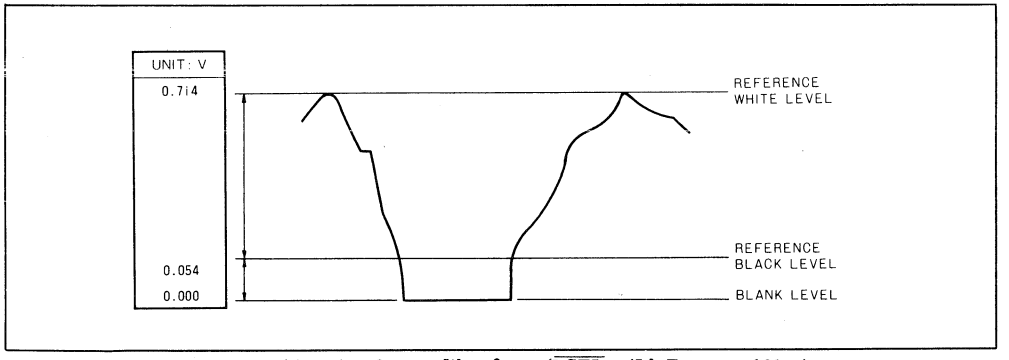


Fig. 2. (a) Video Output Waveform ($\overline{BSEL}$ = 'L', R_{REF} = 13kΩ)

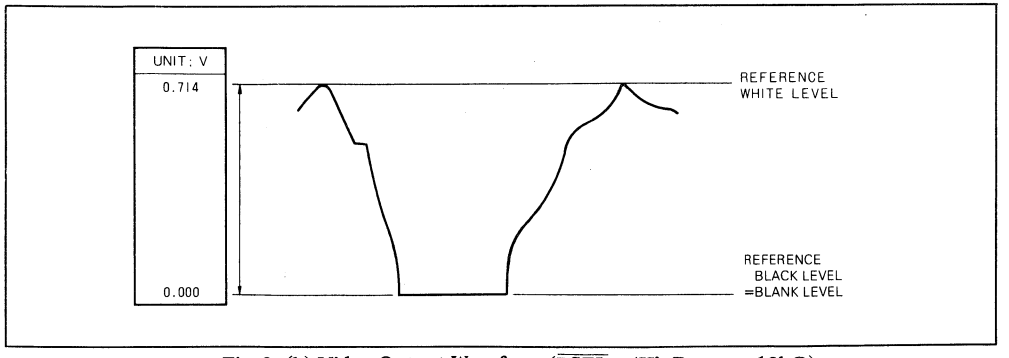
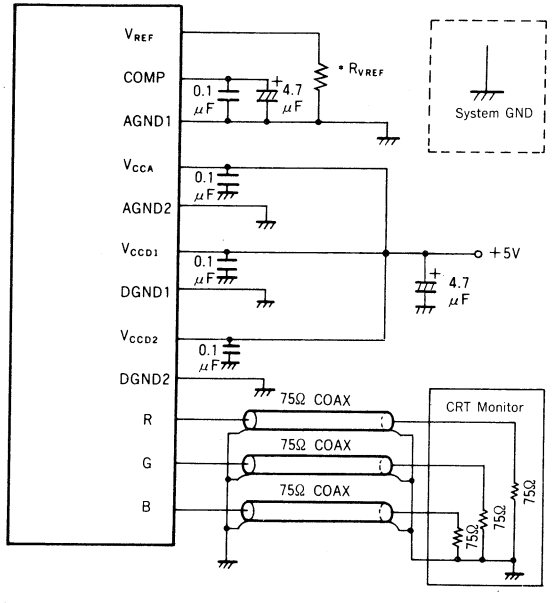


Fig. 2. (b) Video Output Waveform ($\overline{BSEL}$ = 'H', R_{REF} = 12kΩ)

Typical Connection Diagram



*R_{VREF} ··· typical···12kΩ

HD153109

Color Palette with Triple 6-bit DA Converter

The HD153109 is a triple 6-bit video DAC with color palette RAM, designed specifically for high performance high resolution color graphics. The HD153109 supports up to 256 simultaneous colors from a 262, 144 color palette and generates RS-343A/170A compatible red, green and blue video signals.
The HD153109 realizes high speed, high density and low power dissipation by implementing in Hi-Bi CMOS process.

Features

- Displays 256 colors simultaneously among total 262, 144 colors
- Provides R-G-B 3 channels 6-bit DA converter on a chip
- Pixel word mask to control display
- Personal system/2™ compatible
- Extractable G (green) digital outputs from the CLT. (color look up table) enables application to lap top computers (Selectable of DAC outputs and digital outputs)
- DAC's outputs level can be set by 1 registor
- Programmable pedestral (0 or 7.5 IRE)
- DA converter consists of 3 channels, all of which can composite $\overline{\text{SYNC}}$ signal
- Selectable of $\overline{\text{SYNC}}$ signal composite and $\overline{\text{SYNC}}$ signal non-composite (HD153109FS only)
- At digital output, unrequired signals can be cut off. (HD153109FS and HD153109MA only)
- Maximum dotting rate of 50/65 MHz
- Low power dissipation of 650 mW typical
- Supporting TTL interface
- Less external parts

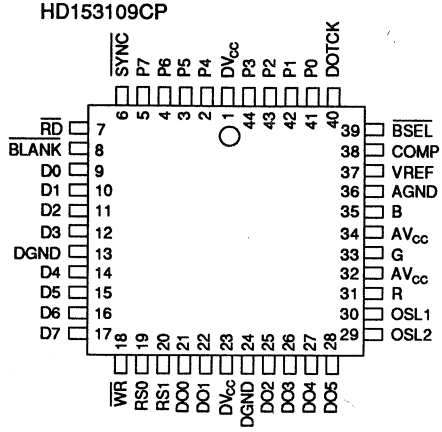
The "Personal System/2" is a registered trademark of IBM Corp.

Ordering Information

Type No.	Maximum operating frequency	Package
HD153109CP	50 MHz	44 pin PLCC (CP-44)
HD153109CP-65	65 MHz	
HD153109FS	50 MHz	64 pin QFP (FP-64B)
HD153109FS-65	65 MHz	
HD153109MA	50 MHz	44 pin shrink MSP (MP-44S)
HD153109FS-65	65 MHz	

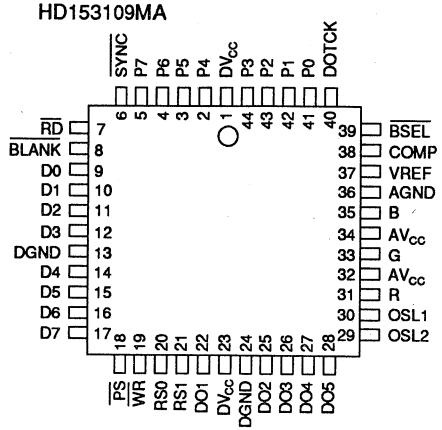
Pin Arrangement

HD153109CP



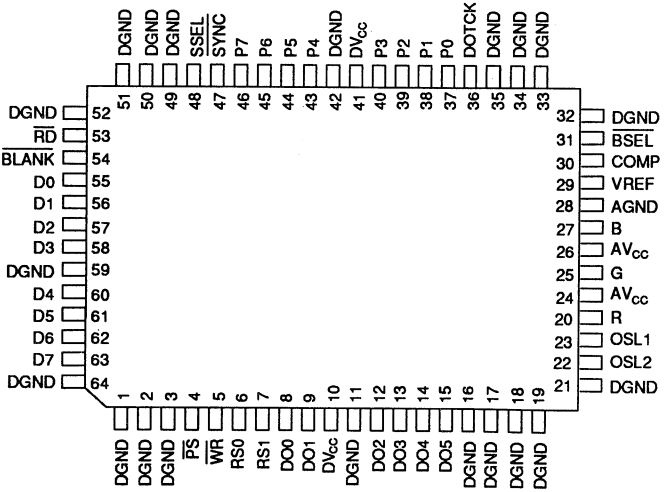
(CP-44)

HD153109MA



(MP-44S)

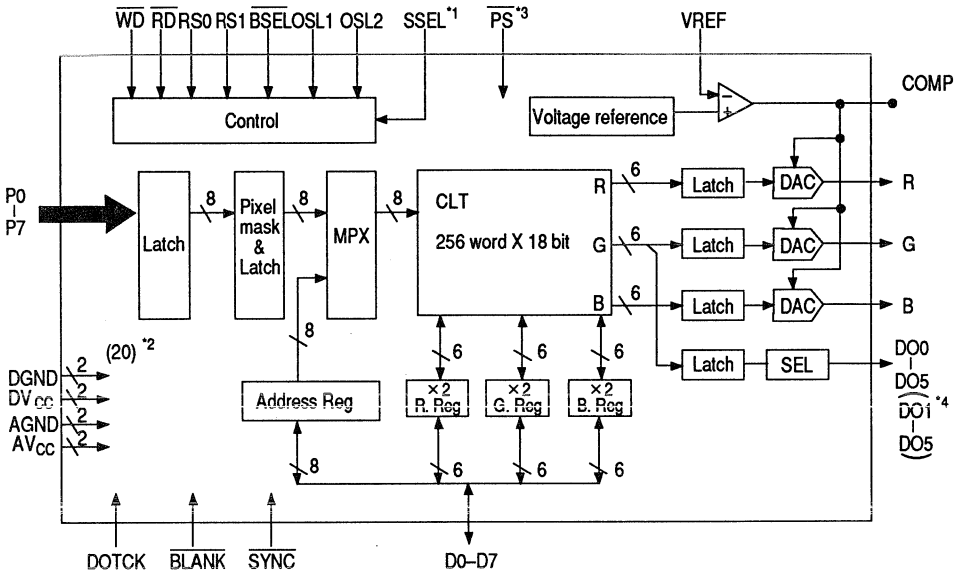
HD153109FS



(FP-64B)

(Top View)

Block Diagrams



Notes:
1. SSEL is only provided on the HD153109FS. It is not provided on the HD153109CP or HD153109MA.
2. The figure in parentheses is for the HD153109FS.
3. $\overline{PS}$ is only provided on the HD153109FS and HD153109MA. It is not provided on the HD153109CP.
4. The HD153109MA is not provided with the DO0 output.

Figure 2 Block Diagrams

Table 1 Pin Description

Pin name	Pin number HD153109CP	HD153109FS	HD153109MA	Description
P0 to P7	41, 42, 43, 44, 2, 3, 4, 5	37, 38, 39, 40, 43, 44, 45, 46	41, 42, 43, 44, 2, 3, 4, 5	Pixel select inputs. P7 is MSB and P0 is LSB.
D0 to D7	9, 10, 11, 12, 14, 15, 16, 17	55, 56, 57, 58, 60, 61, 62, 63	9, 10, 11, 12, 14, 15, 16, 17	Data input/output terminal when writing/reading CLT and registers (address register, pixel mask register and R, G, B register) D7 is MSB and D0 is LSB.
$\overline{RD}$	7	53	7	Clock terminal when reading CLT and registers (address register, pixel mask register and R, G, B register)
$\overline{WR}$	18	5	19	Clock terminal when writing CLT and registers (address register, pixel mask register and R, G, B register)
RS0, RS1	19, 20	6, 7	20, 21	Terminal to select CLT, address register and pixel mask register
DO0 to DO5 (DO1 to DO5)*	21, 22, 25, 26 27, 28	8, 9, 12, 13, 14, 15	22, 25, 26, 27, 28	Terminal to extract green digital signal from the palette DO5 is MSB and DO0 is LSB. Since the HD153109MA is not provided with a DO0 output, DO5 is MSB and DO1 is LSB.
VREF	37	29	37	Terminal to connect a reference resistor to determine the output level of DAC analog signal (R_{VREF} = 12 kΩ typ.)
COMP	38	30	38	Terminal to connect a capacitor for phase-compensation
OSL1, OSL2	30, 29	22, 21	30, 29	Terminal to select an output of digital signals
R, G, B	31, 33, 35	23, 25, 27	31, 33, 35	DAC analog outputs
$\overline{BLANK}$	8	54	8	Terminal to set the DAC analog signal on BLANK level
$\overline{BSEL}$	39	31	39	Terminal to set pedestral (0 or 7.5 IRE)
DOTCK	40	36	40	Clock input to do operation of digital and analog parts. When this clock rises, CLT and input data of $\overline{BLANK}$ is taken and analog signals are output.
SSEL	—	48	—	Terminal to select SYNC level (0 or 40 IRE)

* The HD153109MA is not provided with the DO0 output.

Pin Description (cont)

Pin name	Pin number HD153109CP	HD153109FS	HD153109MA	Description
$\overline{SYNC}$	6	47	6	• HD153109FS Terminal to set the analog signal of DAC on SYNC level. when SSEL = 'H', DAC output level will be SYNC level. • HD153109CP CRT synchronous signal inputs
$\overline{PS}$	—	4	18	When only digital output is used and DAC is not used, unrequired signal to DAC and RAM red and blue cells (total 12 bits) can be cut off by setting this terminal 'L'.
DV_{CC}	1, 23	10, 41	1, 23	Digital power
DGND	13, 24	1, 2, 3, 11, 16, 17, 18, 19, 20, 32, 33, 34, 35, 42, 49, 50, 51, 52, 59, 64	13, 24	Digital GND
AV_{CC}	32, 34	24, 26	32, 34	Analog power
AGND	36	28	36	Analog GND

Functions

Access to CLT and registers

RS0 and RS1 select the CLT or a register. (See table 2)

Address register: The address register is a register which is set with the address of CLT from D0 to D7 when a data write/read operation is performed to/from CLT. Write/read is performed to/from this register with D0 as the LSB and D7 as the MSB.
When data is to be written to CLT, the address register is selected by RS0 = '0' and RS1 = '0', and then the write address is set to the address register from D0 to D7 (see figure 7).
When data is to be read from CLT, the address register is selected by RS0 = '1' and RS1 = '1', and then the read address is set to the address register from D0 to D7 (see figure 8). Also, the address register contents are read out as shown in figures 10 and 11.

Pixel mask register: The pixel mask can change the displayed color without changing the contents of the video memory or CLT. To use the pixel mask, select the pixel mask register by RS0 = '0' and RS1 = '1' and then set the pixel mask data from D0 (LSB) to D7 (MSB) (see figures 13 and 14). The color palette LSI inputs the logical product (AND) of the address data from P0 (LSB) to P7 (MSB) and the value set in the pixel mask register for use as the CLT address. As a result, the address data is masked when the value in the pixel mask register is '0' and is canceled when the value in the pixel mask register is '1'.
An example of how the value set in the pixel mask register determines the CLT address value from the address data input value is shown below in table 3.

RGB register: There are two types of RGB register -- a register for holding color data to be written to CLT and a register for holding color data read from CLT. Each register is comprised of 18 bits.
When data is to be written to or read from CLT, the RGB register is selected by RS0 ='1' and RS1 = '0', and then the data is read from or written to D0 (LSB) to D5 (MSB). At this time, values D6 and D7 can be either '0' or '1'. Data is written or read in the RGB sequence (see figures 7 and 8).

Table 2 Register Selection

RS1	RS0	Selection
0	0	Address register (write mode)
1	1	Address register (read mode)
0	1	CLT
1	0	Pixel mask register

Table 3 Pixel Mask Example

Pixel mask register	1	0	1	0	1	1	0	1
Address input (P7 to P0)	Pd7	Pd6	Pd5	Pd4	Pd3	Pd2	Pd1	Pd0
CLT address value	Pd7	0	Pd5	0	Pd3	Pd2	0	Pd0

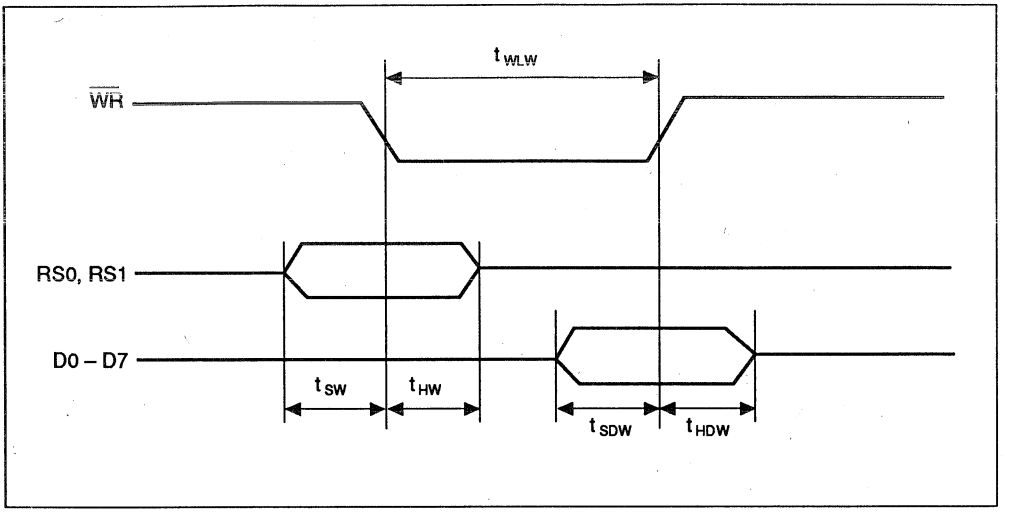


Figure 3 Data Write Timing

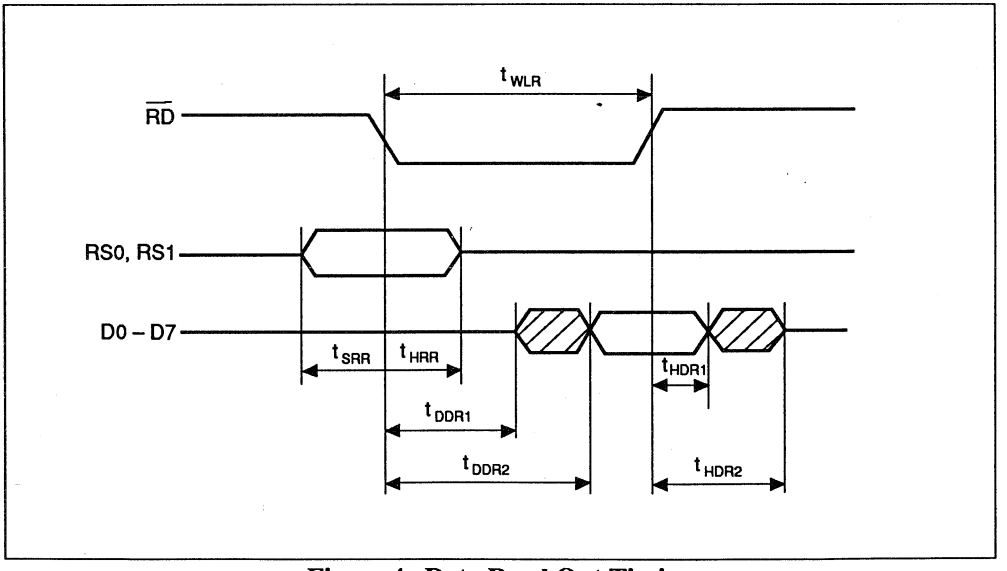


Figure 4 Data Read Out Timing

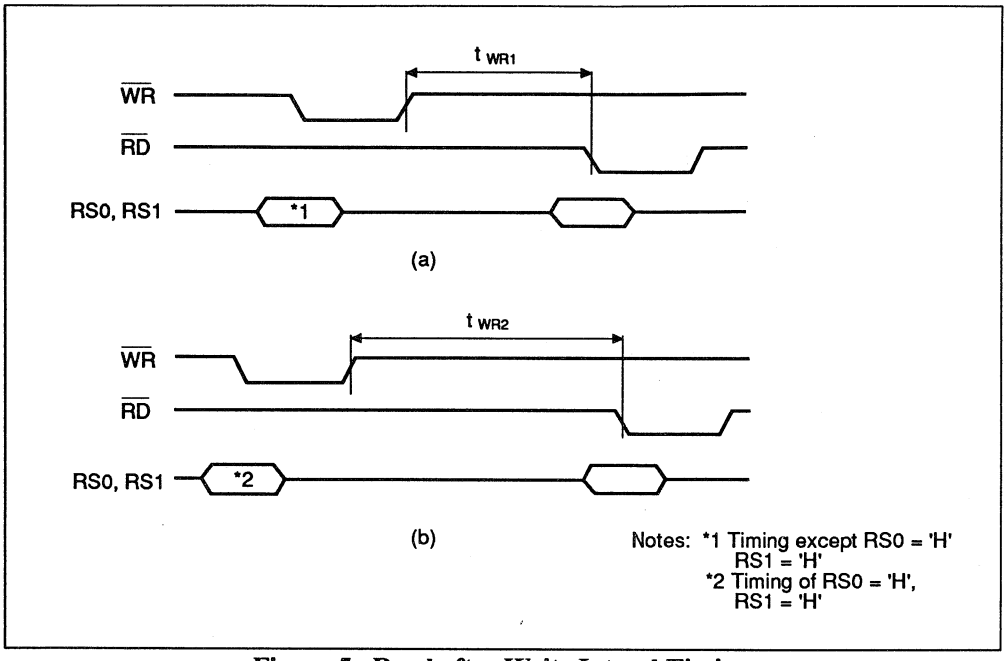


Figure 5 Read after Write Inteval Timing

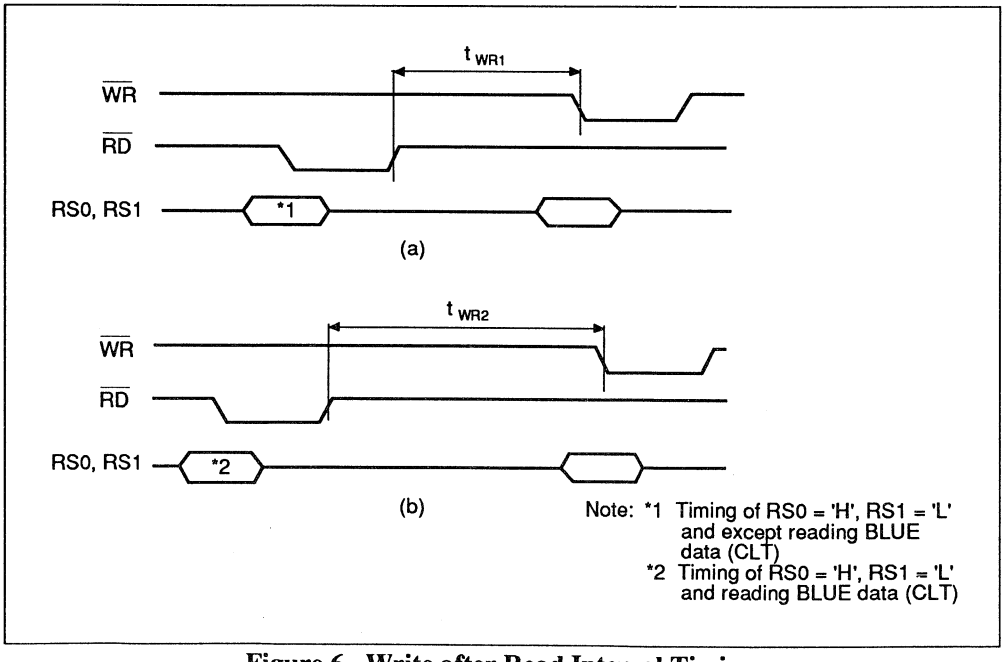
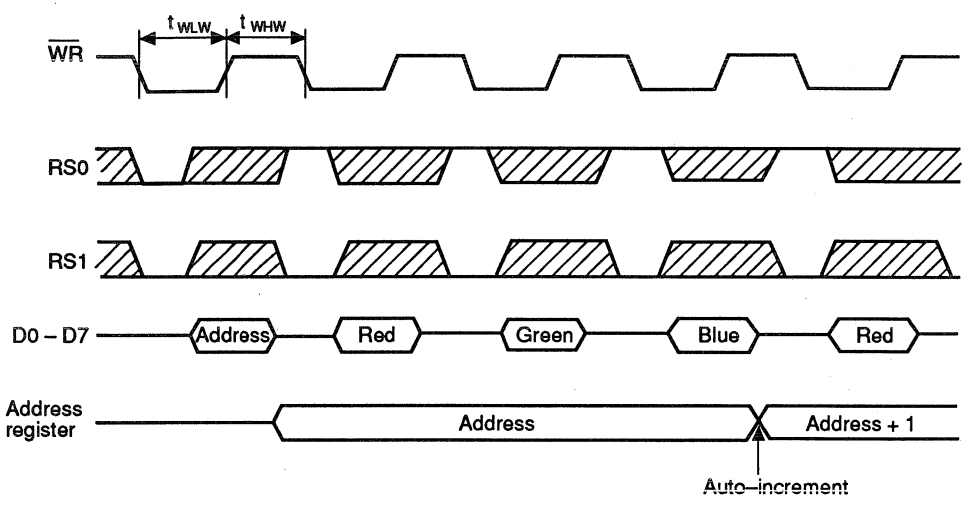
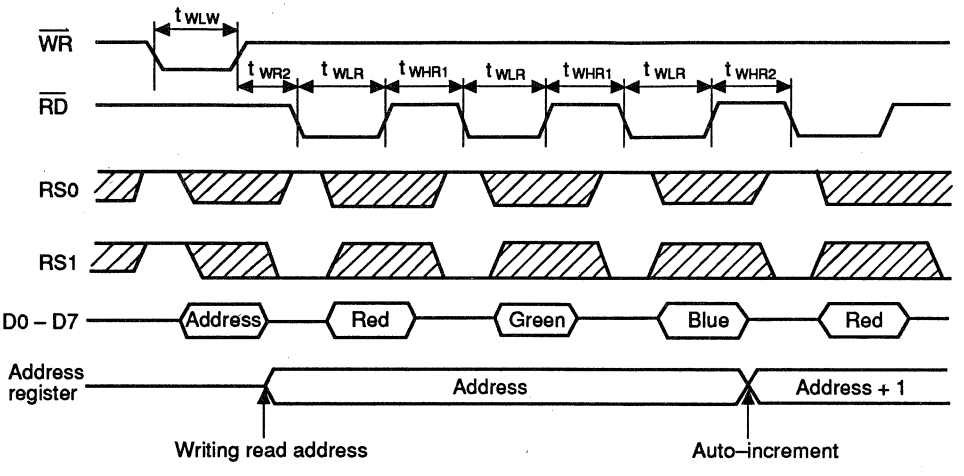


Figure 6 Write after Read Interval Timing



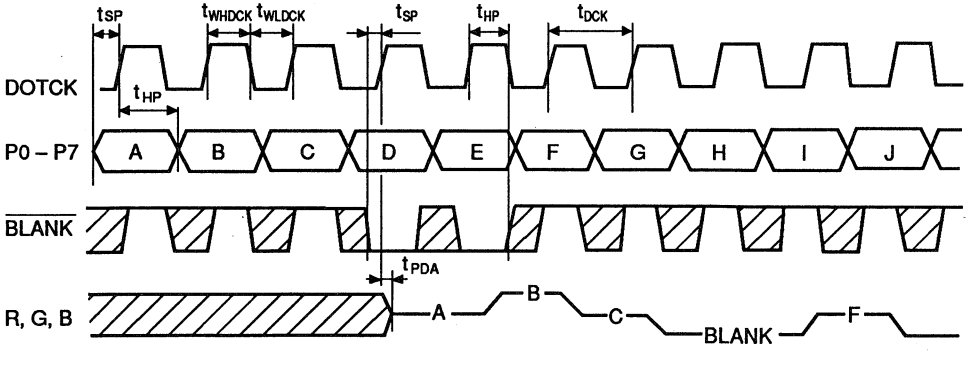
1. Write address information into the address register.
2. Apply each NRZ data at D0 to D5 inputs in the order of red, green and blue. Total 18 bits of R, G, B data are written into CLT, simultaneously.
3. When data write is completed, the address information increases by 1. Continuously, the next data is applied in the order of R, G and B to be written.

Figure 7 Data Write to CLT



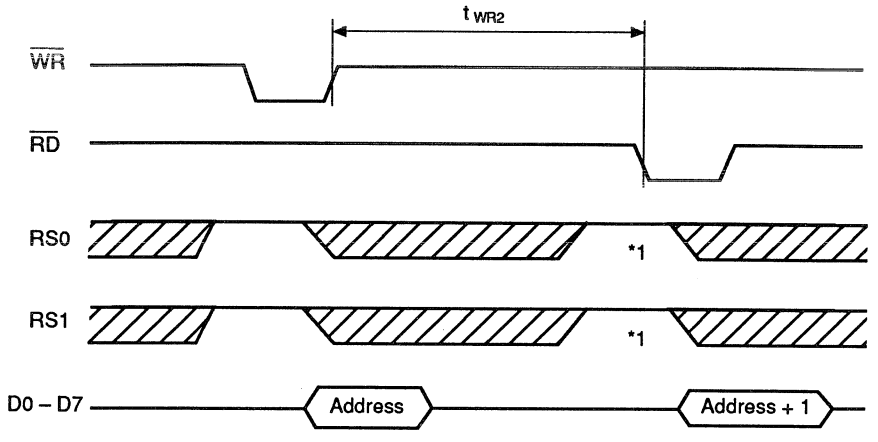
1. Read address is written into the address register.
2. By RD, the contents of CLT is read out from D0 to D5 in the order of R, G and B.
3. When the data is read out until blue, the address increases by 1. Then the next address can be read out in the order of R, G and B.

Figure 8 Read Out from CLT



Video output provides data at the address indicated by address data P0 – P7, as analog signal outputs. Then, the video signal output delays by 3 clocks from the clock of the address taken into by DOTCK.

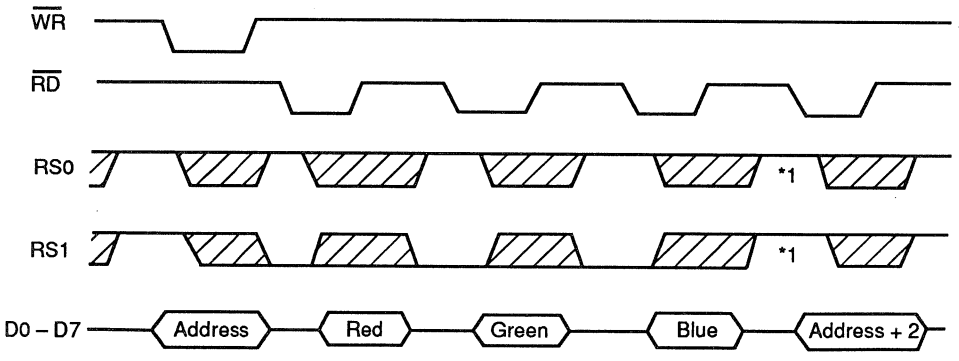
Figure 9 Video Output



1. By $\overline{WR}$, the read address is written.
2. By $\overline{RD}$, the information of an address register is read out. Then, the address information read out is +1 increased one.

Note: 1. Address register can be read out even when RS0 and RS1 are 'L' and 'L'.

Figure 10 Read Out of Address Register (1)



1. By $\overline{WR}$, the read address is written.
2. By $\overline{WR}$, CLT contents are read out in the order of red, green and blue.
3. By $\overline{RD}$, address register informations are read out. Then, the address information to be read out is +2 increased one, corresponding to the count up of reading red, green and blue.

Note: 1. Address register can be read out even when RS0 and RS1 are 'L' and 'L'.

Figure 11 Read Out of Address Register (2)

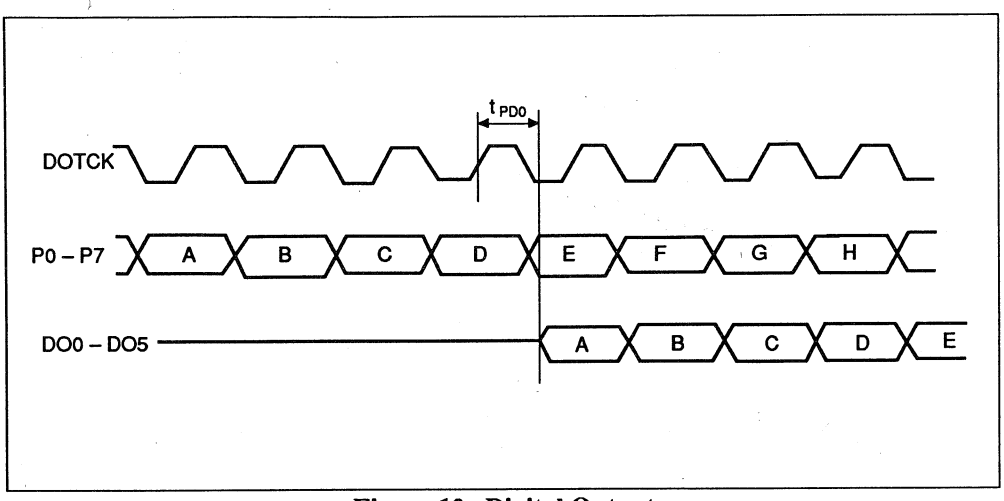


Figure 12 Digital Output

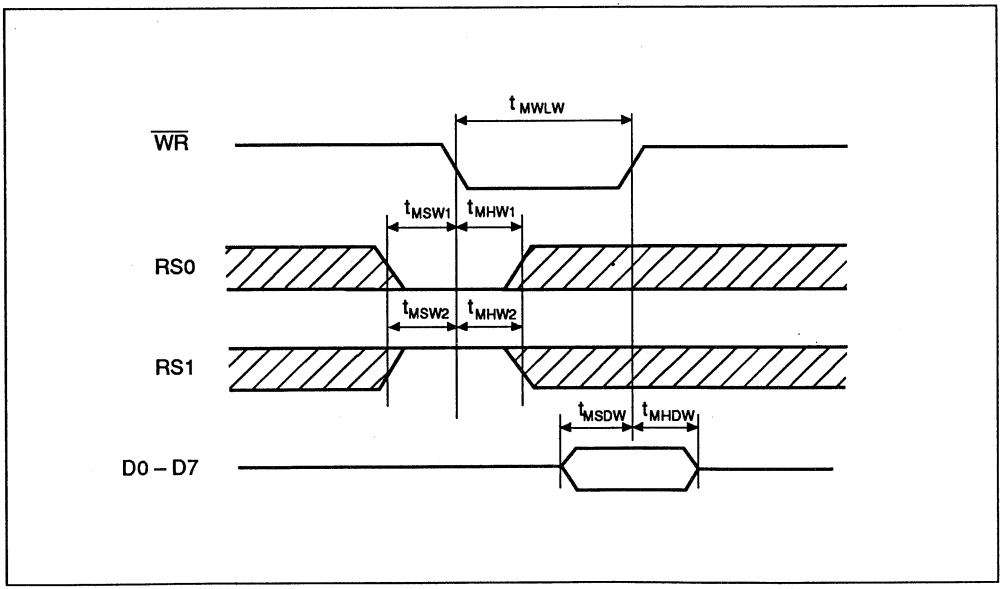


Figure 13 Data Write to Pixel Mask Register

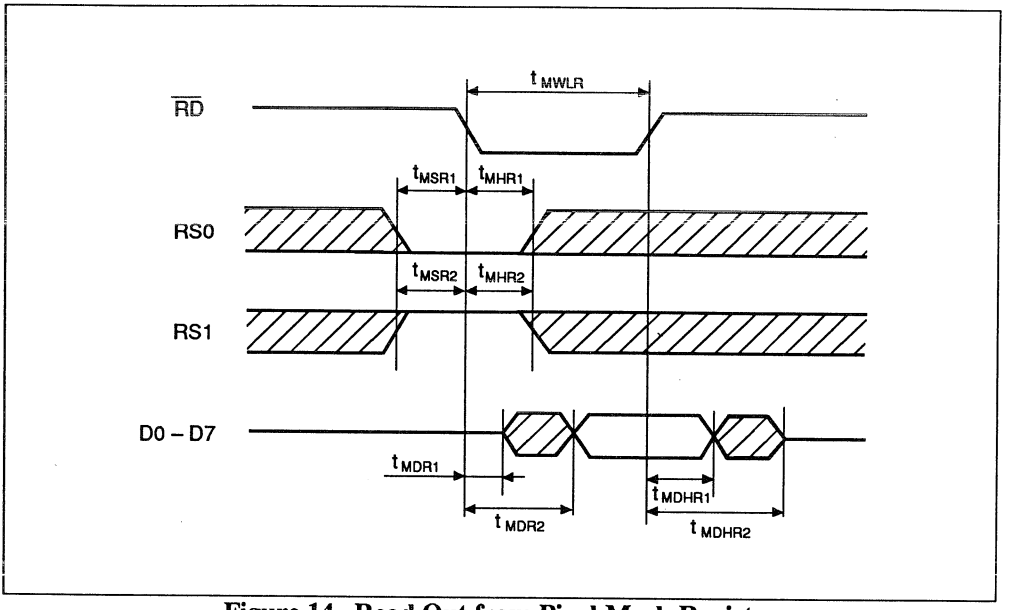


Figure 14 Read Out from Pixel Mask Register

The following two levels are selectable for the video output by fixing BSEL 'L' or 'H'.
Please select according to the CRT spec.

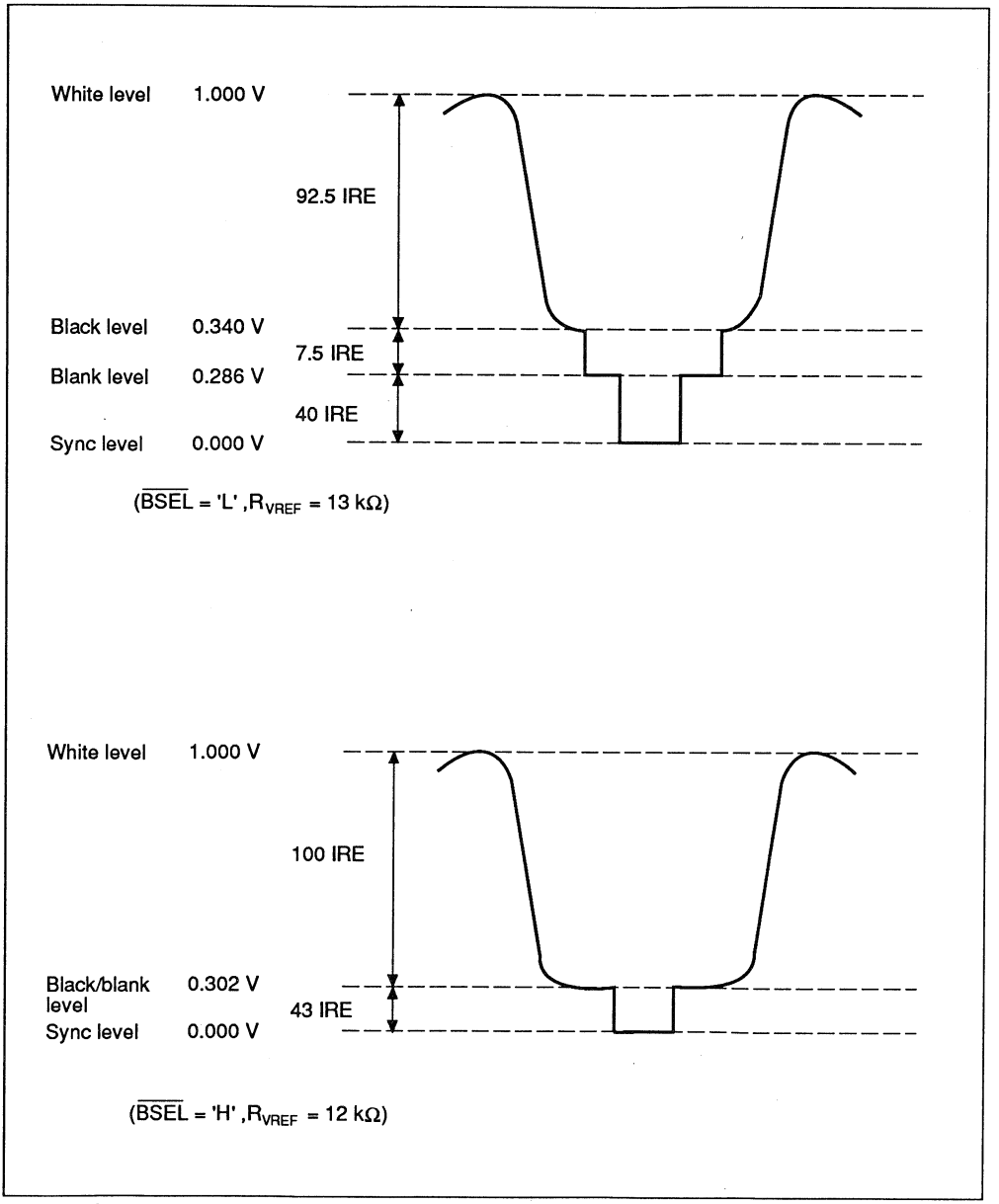


Figure 15 HD153109CP and HD153109MA VIDEO Output Waveform (In case of $\overline{SYNC}$ signal composite)

When SYNC signals are not composed, the output waveforms will be like;

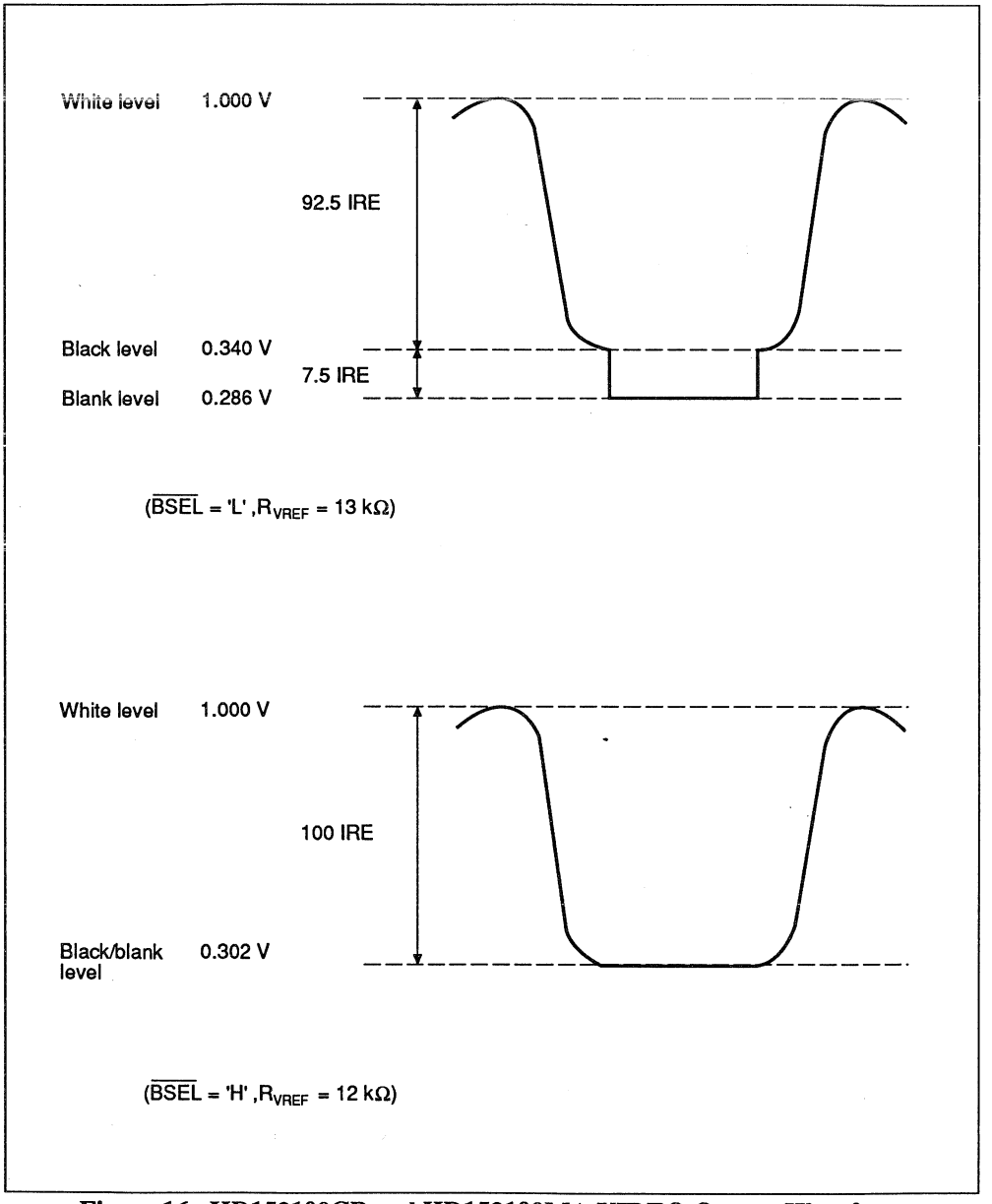
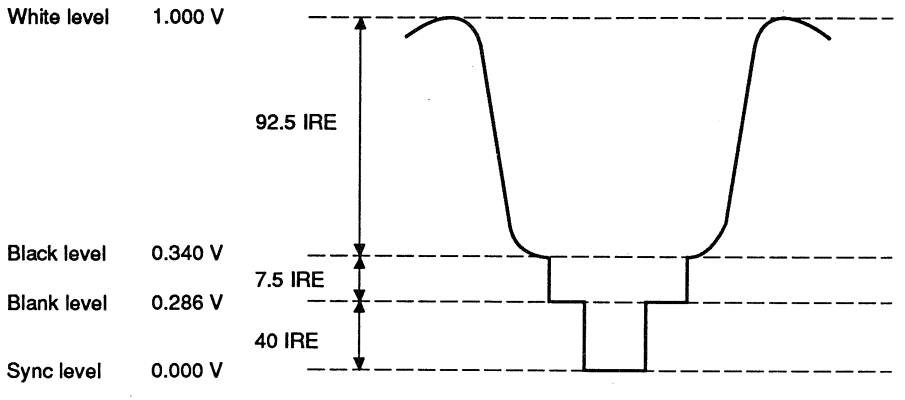
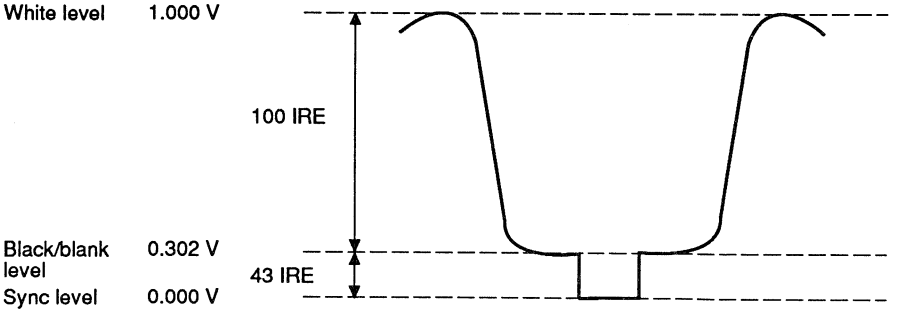


Figure 16 HD153109CP and HD153109MA VIDEO Output Waveform (In case of $\overline{\text{SYNC}}$ signal non-composite)

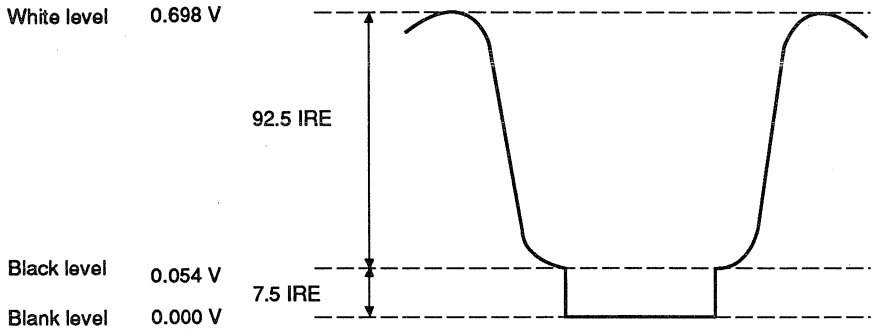


(SSEL = 'H', $\overline{BSEL}$ = 'L', R_{VREF} = 13 kΩ)

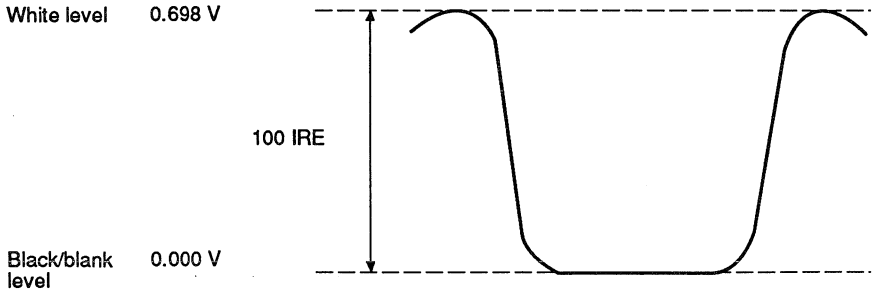


(SSEL = 'H', $\overline{BSEL}$ = 'H', R_{VREF} = 12 kΩ)

Figure 17 HD153109FS VIDEO Output Waveform (In case of $\overline{SYNC}$ signal composite)



(SSEL = 'L', $\overline{BSEL}$ = 'L' ,R_{VREF} = 13 kΩ)



(SSEL = 'L', $\overline{BSEL}$ = 'H' ,R_{VREF} = 12 kΩ)

Figure 18 HD153109FS VIDEO Output Waveform (Incase of $\overline{SYNC}$ signal non-composite)

Switch of DAC outputs and Digital Output: OSL1 and OSL2 are used to switch the DAC output and digital output. (See table 4)

Table 4

OSL1	OSL2	Output
0	0	DAC output
1	1	DAC output and digital output (green)
0	1	Prohibited
1	0	Prohibited

Correspondance of CLT with Each Register

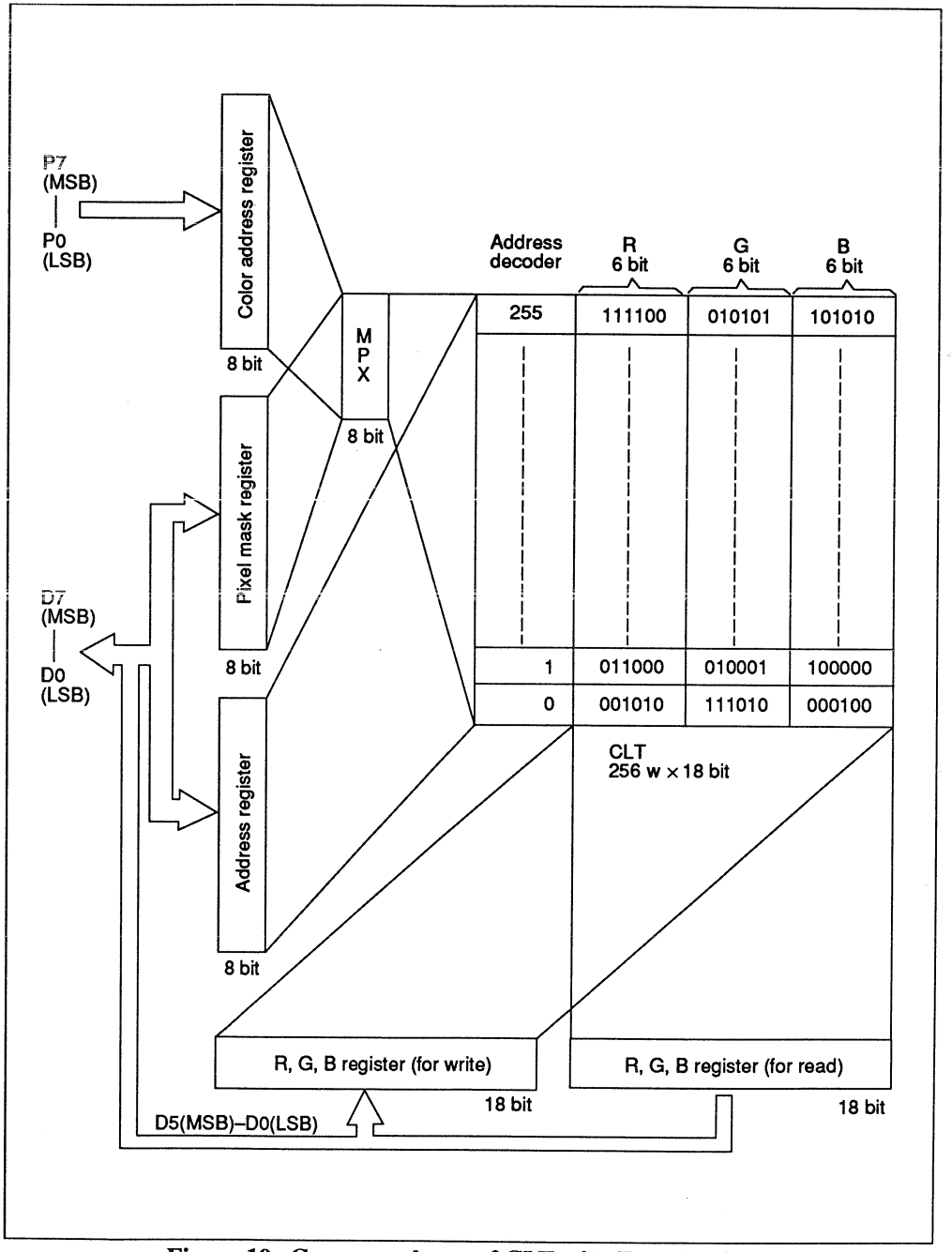


Figure 19 Correspondance of CLT with Each Register

Example Construction of a Standard System

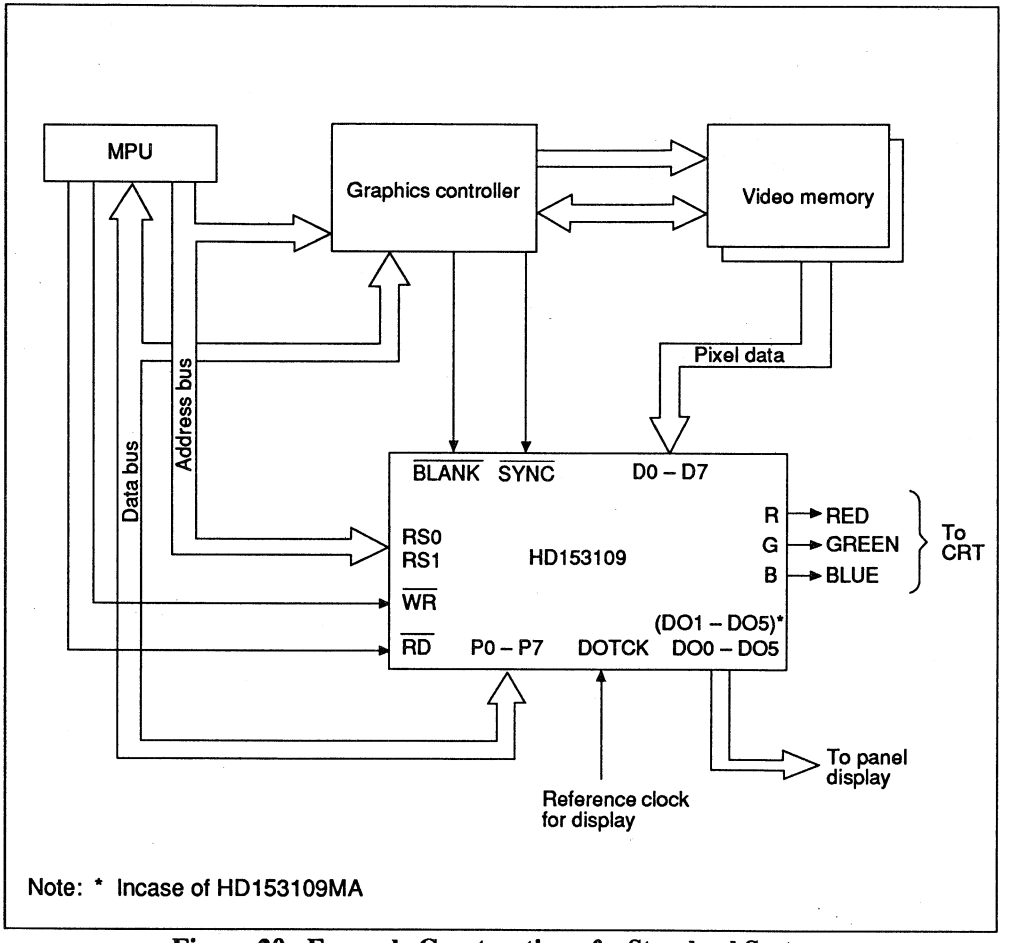


Figure 20 Example Construction of a Standard System

Table 5 Absolute Maximum Ratings (Ta = 25 °C)

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	0 to V_{CC}	V
Operating temperature	T_{opr}	0 to +70 (+60)*	°C
Storage temperature	T_{str}	–55 to +150	°C

Note: * HD153109MA only

Electrical Characteristics

Table 6 DAC Characteristics (V_{CC} = 5 V, Ta = 25 °C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		6	6	6	bits	
Max. operating frequency	f_{CLK}	—	—	50/65	MHz	
Analog output voltage (R_{VREF} = 12 kΩ)	V_A(Full)	–15	—	15	% of FSR	
	V_A(Zero)	–2	—	2	% of FSR	
Differential linearity	DLE	–1	—	+1	LSB	
Integral linearity	ILE	–1	—	+1	LSB	
Output rise time (20 % to 80 %)	tr	—	—	10	ns	C_L = 15 pF
Output fall time (80 % to 20 %)	tf	—	—	10	ns	C_L = 15 pF
Setting time	ts	—	—	30	ns	C_L = 15 pF
Glitch energy	E_G	—	90	—	PVS	

Table 7 DC Characteristics

(Unless otherwise specified, V_{CC} = 5 V + 5 %, Ta = 0 to +70 °C, (Ta = 0 to +60 °C)*1)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input "High" level voltage	V_{IH}	2.0	—	V_{CC}	V	
Input "Low" level voltage	V_{IL}	–0.3	—	0.8	V	
Input clamp voltage	V_I	—	—	–1.5	V	V_{CC} = 4.7 V I_{IN} = –18 mA
Output "High" level voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V I_{OH} = –400 µA

DC Characteristics
(Unless otherwise specified, V_{CC} = 5 V + 5 %, Ta = 0 to +70 °C, (Ta = 0 to +60 °C)*1) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Output "Low" level voltage	V_{OL}	—	—	0.5	V	V_{CC} = 4.75 V I_{OL} = 8 mA
Input current	I_I	—	—	1	mA	V_{CC} = 5.25 V V_I = 5.5 V
"High" level input current	I_{IH}	_	—	20	µA	V_{CC} = 5.25 V V_I = 2.7 V
"Low" level input current	I_{IL}	—	—	–400	µA	V_{CC} = 5.25 V V_I = 0.4 v
Supply current (HD153109FS) (1)*2	I_{CC}	—	130	190	mA	V_{CC} = 5.25 V
Supply current (HD153109FS) (2)*3	I_{CC}	—	80	130	mA	V_{CC} = 5.25 V
Supply current (HD153109CP) (3)*4	I_{CC}	_	130	190	mA	V_{CC} = 5.25 V

Notes: 1. HD153109MA only
2. PS = 'H', OSL1 = 'L', OSL2 = 'L'
3. PS = 'L', OSL1 = 'H', OSL2 = 'H'
4. OSL1 = 'L', OSL2 = 'L'

Table 8 Digital Parts AC Characteristics (V_{CC} = 5 V, Ta = 25 °C)

		50 MHz		65 MHz			Test	Reference
Item	Symbol	Min	Max	Min	Max	Unit	conditions	figure
DOTCK cycle time	t_{DCK}	20	—	15.3	—	ns		9
DOTCK L level time	t_{WLDCK}	8	—	6	—	ns		9
DOTCK H level time	t_{WHDCK}	8	—	6	—	ns		9
Data setup time	t_{sp}	6	—	5	—	ns		9
Data hold time	t_{HP}	6	—	5	—	ns		9
Data output delay time	t_{PDA}	—	30	—	30	ns	C_L = 15 pF	9
$\overline{WR}$ L level time	t_{WLW}	50	—	50	—	ns		3, 7, 9
$\overline{WR}$ H level time	t_{WHW}	4×t_{DCK}	—	4×t_{DCK}	—	ns		7
$\overline{RD}$ L level time	t_{WLR}	50	—	50	—	ns		8
$\overline{RD}$ H level time (1)	t_{WHR1}	4×t_{DCK}	—	4×t_{DCK}	—	ns		8

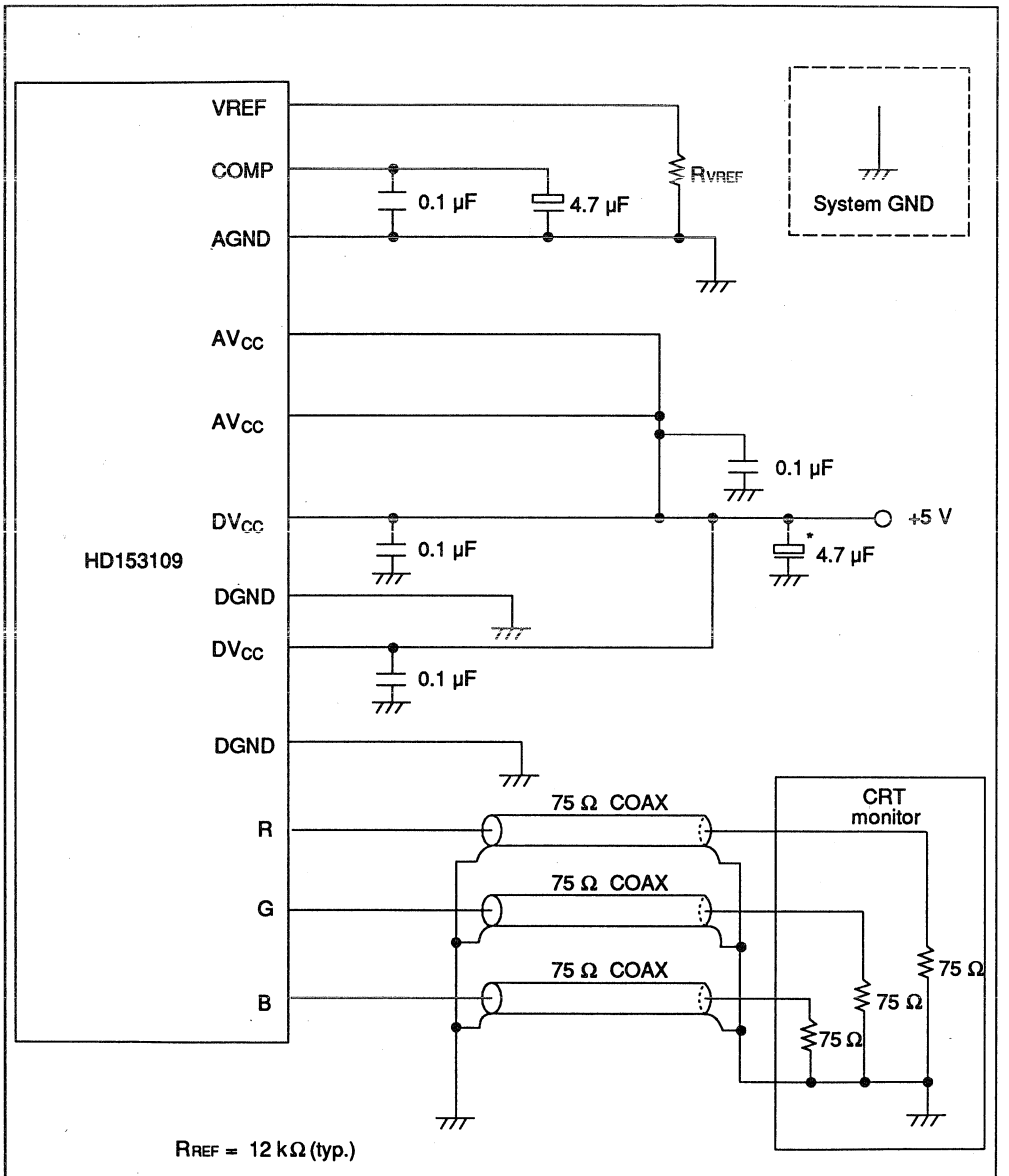
Digital Parts AC Characteristics (V_{CC} = 5 V, Ta = 25 °C) (cont)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Test conditions	Reference figure
$\overline{RD}$ H level time (2)	t_{WHR2}	$7 \times t_{DCK}$	—	$7 \times t_{DCK}$	—	ns		8
$\overline{WR}$/$\overline{RD}$ interval time (1)	t_{WR1}	$4 \times t_{DCK}$	—	$4 \times t_{DCK}$	—	ns		5, 6
$\overline{WR}$/$\overline{RD}$ interval time (2)	t_{WR2}	$7 \times t_{DCK}$	—	$7 \times t_{DCK}$	—	ns		5, 6, 8, 9
$\overline{WR}$/RS0, RS1 setup time	t_{SW}	10	—	10	—	ns		3
$\overline{WR}$/RS0, RS1 hold time	t_{HW}	10	—	10	—	ns		3
$\overline{RD}$/RS0, RS1 setup time	t_{SRR}	10	—	10	—	ns		4
$\overline{RD}$/RS0, RS1 hold time	t_{HRR}	10	—	10	—	ns		4
$\overline{WR}$ data setup time	t_{SDW}	10	—	10	—	ns		3
$\overline{WR}$ data hold time	t_{HDW}	10	—	10	—	ns		3
$\overline{RD}$ data output delay time (1)	t_{DDR1}	5	—	5	—	ns	C_L = 15 pF	4
$\overline{RD}$ data output delay time (2)	t_{DDR2}	—	40	—	40	ns	C_L = 15 pF	4
$\overline{RD}$ data output hold time (1)	t_{HDR1}	5	—	5	—	ns	C_L = 15 pF	4
$\overline{RD}$ data output hold time (2)	t_{HDR2}	—	20	—	20	ns	C_L = 15 pF	4
Digital output delay time	t_{PDO}	—	19	—	19	ns	C_L = 15 pF	12
$\overline{WR}$ L level time	t_{MWLW}	50	—	50	—	ns		13
$\overline{RD}$ L level time	t_{MWLR}	50	—	50	—	ns		14
$\overline{WR}$/RS0, RS1 setup time	t_{MSW1}	10	—	10	—	ns		13
	t_{MSW2}	10	—	10	—	ns		13
$\overline{WR}$/RS0, RS1 hold time	t_{MHW1}	10	—	10	—	ns		13
	t_{MHW2}	10	—	10	—	ns		13
$\overline{RD}$/RS0, RS1 setup time	t_{MSR1}	10	—	10	—	ns		14
	t_{MSR2}	10	—	10	—	ns		14
$\overline{RD}$/RS0, Rs1 hold time	t_{MHR1}	10	—	10	—	ns		14
	t_{MHR2}	10	—	10	—	ns		14
$\overline{WR}$ data setup time	t_{MSDW}	10	—	10	—	ns		13

Digital Parts AC Characteristics (V_{CC} = 5 V, Ta = 25 °C) (cont)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Test conditions	Reference figure
$\overline{WR}$ data hold time	t_{MHDW}	10	—	10	—	ns		13
$\overline{RD}$ data output delay time (1)	t_{MDR1}	5	—	5	—	ns	C_L = 15 pF	14
$\overline{RD}$ data output delay time (2)	t_{MDR2}	—	40	—	40	ns	C_L = 15 pF	14
$\overline{RD}$ data output hold time (1)	t_{MDHR1}	5	—	5	—	ns	C_L = 15 pF	14
$\overline{RD}$ data output hold time (2)	t_{MDHR2}	—	20	—	20	ns	C_L = 15 pF	14

Example of External Parts



*: Not necessary if an electrolytic capacitor is installed on the system side.

Figure 21 Example of External Parts

HD153110

Preliminary

Color Palette with Triple 8-bit DA Converter

The HD153110FS is a color palette with built-in triple 8-bit DA converter. Manufactured with Hitachi's Hi-BiCMOS process, this LSI realizes high speed, high density, low power consumption and minimizes the need for externally connected parts. Also, in addition to applications for existing CRTs, the provision of digital R, G and B outputs for color LCD ensure that the HD153110FS can easily accomodate future systems using full-color LCD. With color palette, advanced functions, small size and low cost, the HD153110FS is an essential component for advanced graphics systems.

Ordering Information

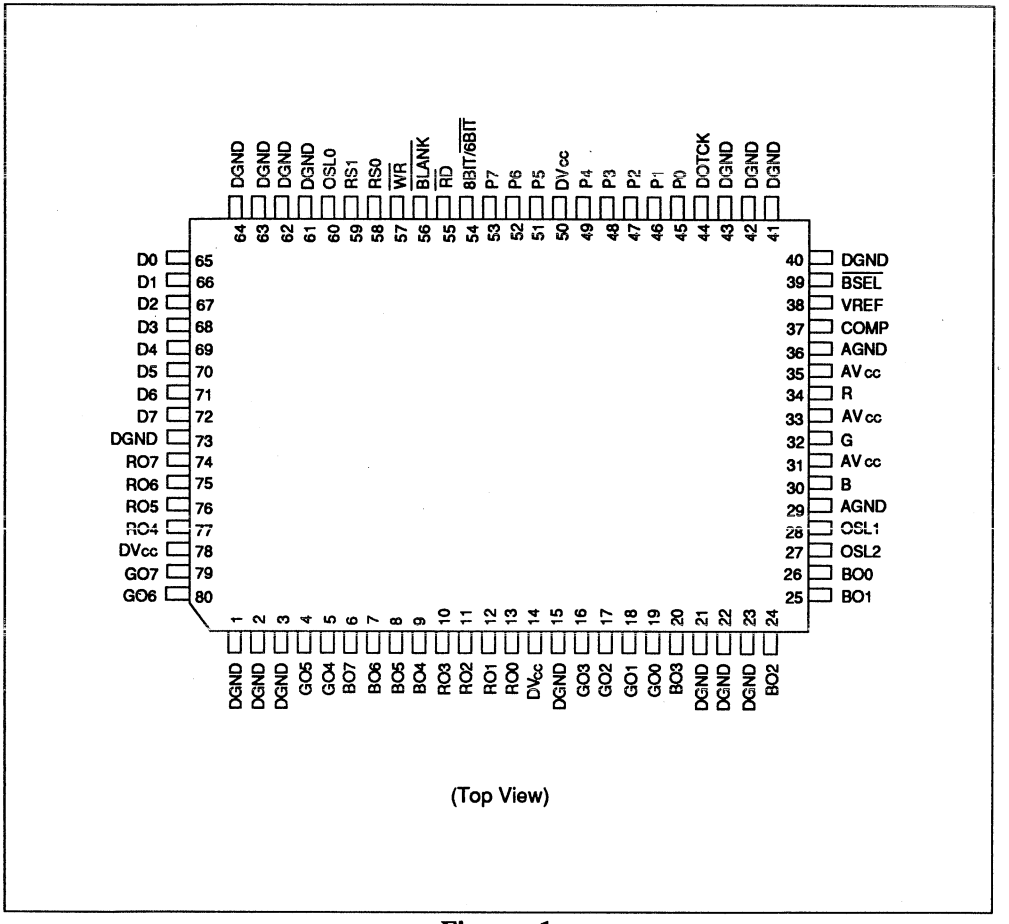
Type No.	Max. Operating Freq.	Package
HD153110FS	50 MHz	80 pin plastic QFP (FP-80B)
HD153110FS-65	65 MHz	

Features

- Displays 256 colors simultaneously from a total of 16,777,216 possible colors.
- Three 8-bit DA converters for RGB video ouput on a single chip
- Read mask function for display control
- Compatible with VGA* graphics standard
- For each pixel, dynamic switching between 16,777,216-color simultaneous display mode and normal mode
- In addition to existing CRT applications, direct digital RGB outputs from the color lookup table (CLT) are provided for color LCD applications.
- Variable BLACK level (0 or 7.5 IRE)
- Switchable between 8-bit/6-bit mode; supports both 8-bit and 6-bit software.
- Dot rate maximum of 50/65 MHz
- TTL compatible I/O levels
- 28-pin DIP package

Note: VGA is a registered trademark of IBM.

Pin Arrangement



(Top View)

Figure 1

Block Diagram

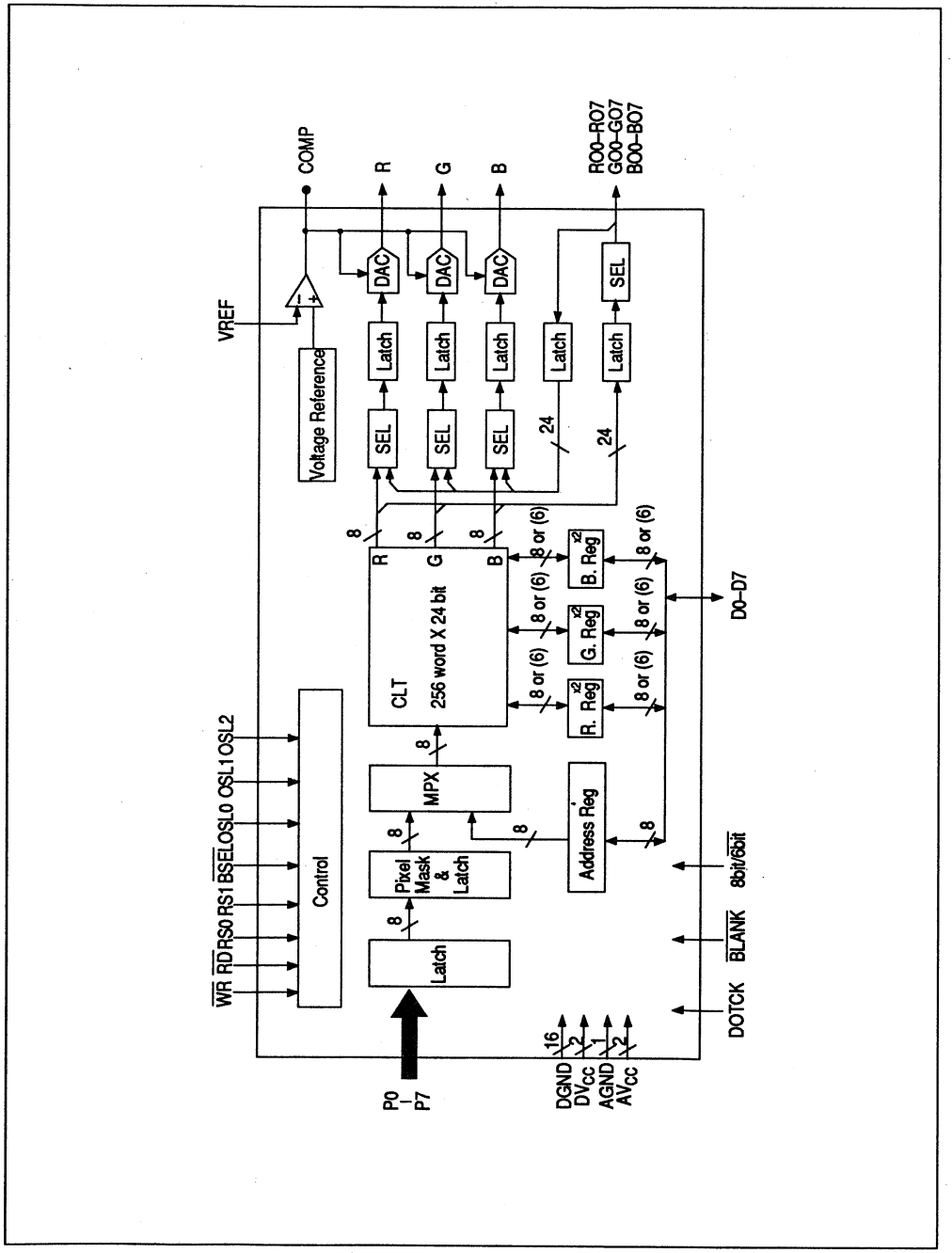


Figure 2 Block Diagram

Table 1 Pin Description

Pin Name	Pin Number	Description
P0 to P7	45 to 49, 51 to 53	CLT address inputs. P7 is MSB, P0 is LSB.
D0 to D7	65 to 72	Data port for reading\writing CLT or address, pixel mask, R, G and B registers. D7 is MSB, D0 is LSB.
$\overline{RD}$	55	Read clock input. Strobes data from CLT or address, pixel mask, R, G or B registers during read operation.
$\overline{WR}$	57	Write clock input. Strobes data to CLT or address, pixel mask, R, G or B registers during write operation.
RS0, RS1	58, 59	Select inputs for CLT, address register or pixel mask register
RO0 to RO7 GO0 to BO0 to BO7	13 to 10, 77 to 74 19 to 16, 3, 4 26 to 24, 20 9 to 6	Palette (CLT) digital signal outputs. RO7, GO7 and BO7 are the MSBs and RO0, GO0, and BO0 are the LSBs.
VREF	38	Terminal for connecting reference resistor to set DAC analog output level
COMP	37	Terminal for connecting a phase-compensation capacitor
OSL0, OSL1, OSL2	60, 28, 27	Select inputs for digital signal outputs
R, G, B	34, 32, 30	DAC analog signal outputs
BLANK	56	Video blank input for activating blank signal levels at DAC analog outputs
8BIT/$\overline{6BIT}$	54	Inputs for setting color palette resolution. 'H' for an 8-bit palette, 'L' for a 6-bit palette
BSEL	39	Input for selecting DAC BLANK level (0 or 7.5 IRE)
DOTCK	44	Reference clock input for digital and analog sections. On the rise of this signal, CLT and BLANK operations are processed and analog signal outputs become active.
DVCC	14, 50, 78	Digital power supply
DGND	1 to 3, 15, 21 to 23, 40 to 43, 61 to 64, 73	Digital GND
AV_{CC}	31, 33, 35	Analog power supply
AGND	29, 36	Analog GND

Functions

Accessing the CLT and Registers

The CLT and registers are selected with inputs RS0 and RS1 (see Table 2).

Registers

Address Register: To perform read/write operations on the CLT, the CLT address must be set in the address register through D7 to D0 (D7 is the MSB and D0 is the LSB).
For a CLT write operation, write the CLT address via D7 to D0 with RS0 = '0' and RS1 = '0' (in order to select the address register, write mode).
To set up the address register for a CLT read operation, write the CLT address via D7 to D0 with RS0 = '1' and RS1 = '1' (in order to select the address register, read mode).
Also, the address register contents can be read as shown in figure 10 and figure 11.

Pixel Mask Register: The pixel mask register is used when displayed colors to be modified by altering the value input from video memory and the contents of the CLT. The pixel mask register is set by writing a pixel mask value to D7 (MSB) to D0(LSB) with RS0 = '0' and RS1 = '1' (in order to select the pixel mask register for a data write) as shown in figure 13. During color palette operations, the value input from video memory at P7 (MSB) to P0(LSB) is ANDed with the pixel mask register value, and the resulting value is applied as an address to the CLT. Consequently, pixel mask '0' bits will cancel corresponding video memory value '1' bits. The following table shows the CLT address that is generated for a particular pixel mask register value and video memory value.

RGB Registers: There are two RGB register types: one for writing color information to the CLT and one for reading color information from the CLT. Each register type is organized as an 24-bit word.
To read or write data to the CLT, set RS0 = '1' and RS1 = '0' to select the appropriate RGB register while performing the read or write via data port D7 (MSB) to D0 (LSB). Write or read the data in the order of R, G, B as shown in figure 7 and figure 8.

Table 2 Register Selection

RS1	RS0	Selection
0	0	Address register (write mode)
1	1	Address register (read mode)
0	1	CLT
1	0	Pixel mask register

Table 3 Pixel Mask Example

	MSB							LSB
Pixel mask register	1	0	1	0	1	1	0	1
Address input (P7 to P0)	Pd7	Pd6	Pd5	Pd4	Pd3	Pd2	Pd1	Pd0
CLT address value	Pd7	0	Pd5	0	Pd3	Pd2	0	Pd0

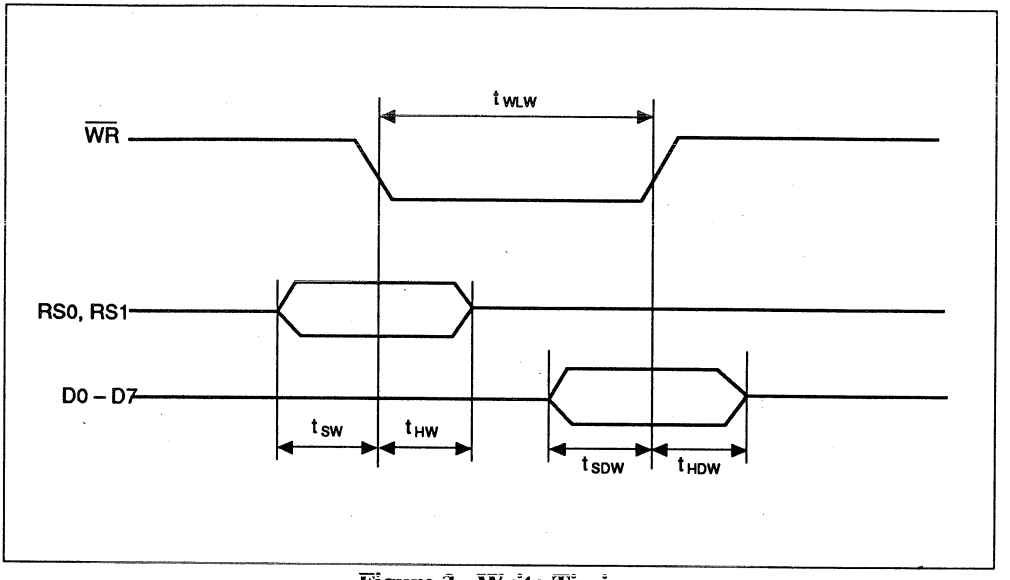


Figure 3 Write Timing

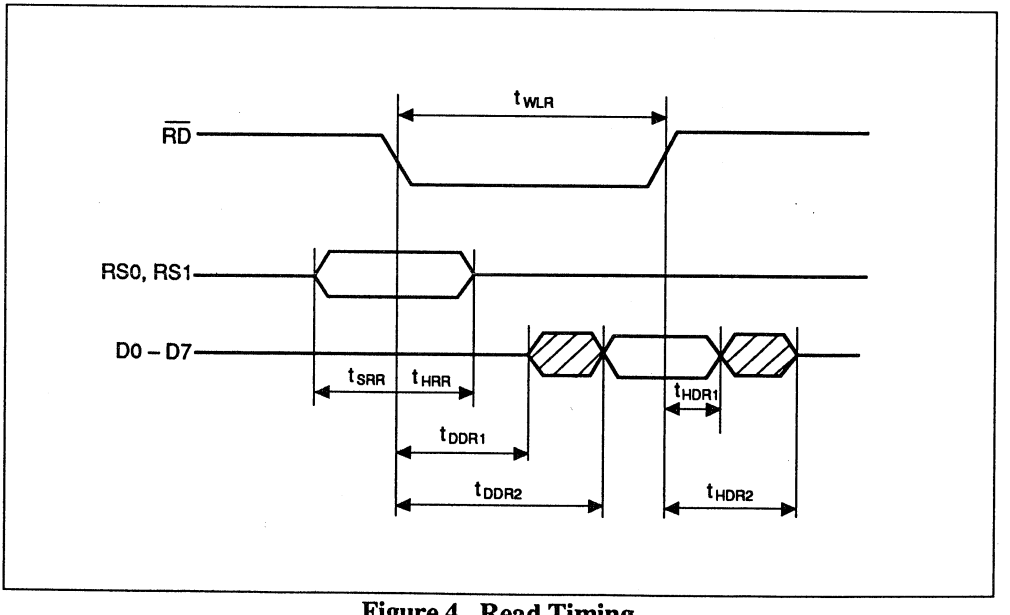
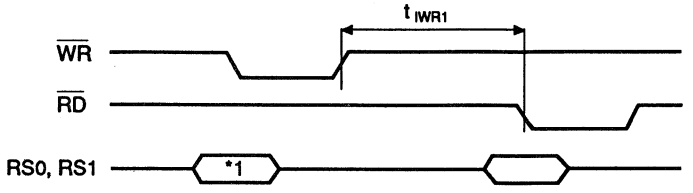


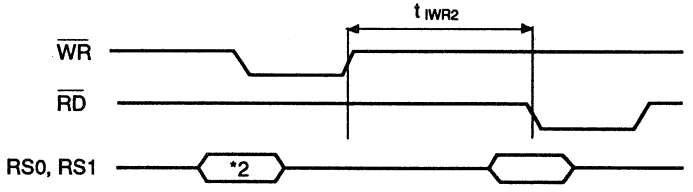
Figure 4 Read Timing

(a) Applies to all read-after-write operations except when the write operation is placing a read address in the address register.



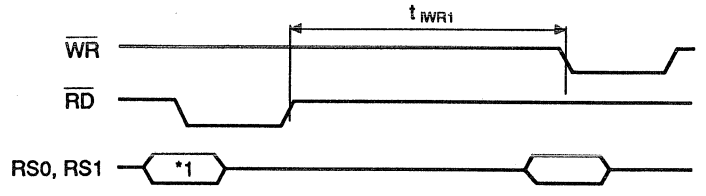
Note 1: This timing not valid when RS0 = 'H' and RS1 = 'H'

(b) Applies to the case when the write operation is placing a read address in the address register.



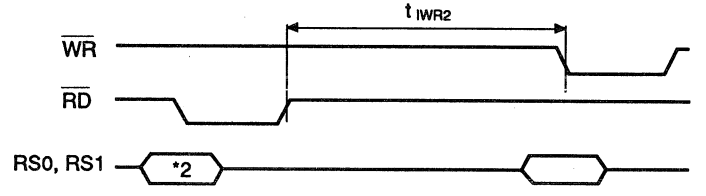
Note 2: This timing is valid when RS0 = 'H' and RS1 = 'H'

Figure 5 Read after Write



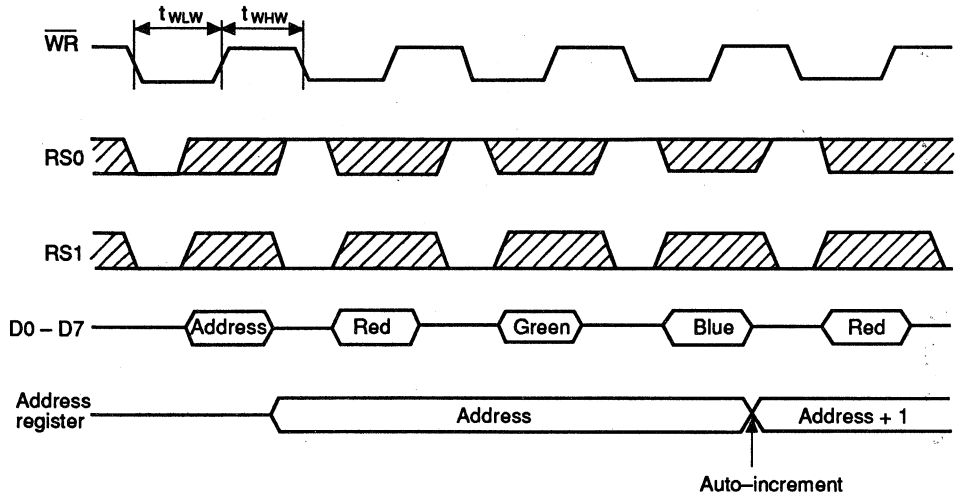
Note 1: This timing not valid for reading CLT Blue data or when RS0 = 'H' and RS1 = 'L'.

(b) Applies to the case where the read operation is for CLT Blue data.



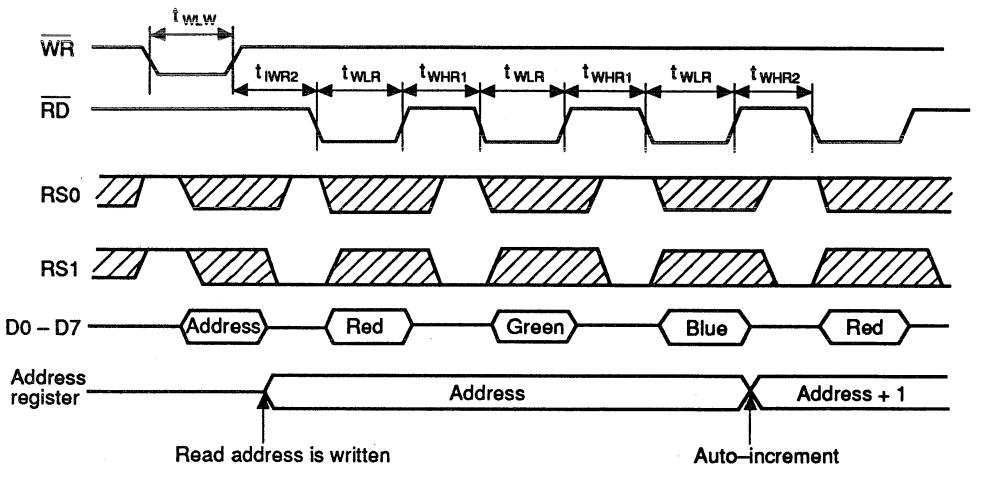
Note 2: This timing is valid for reading CLT Blue data or when RS0 = 'H' and RS1 = 'L'.

Figure 6 Write after Read



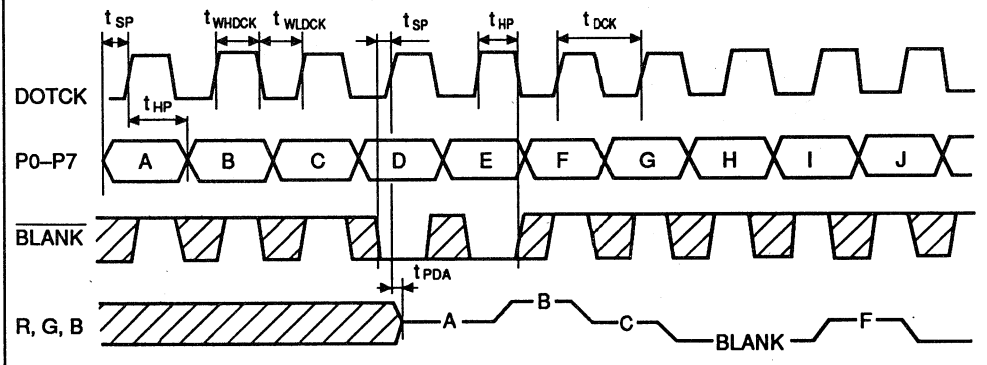
1. Write the CLT address to the address register.
2. Write the data (NRZ format) in the order red, green, then blue to D0-D7. This R, G, and B data forms an 18-bit word that is written to the CLT.
3. When the R, G and B data writes are completed, the address is automatically incremented by 1 and the next data set can be applied again in RGB order. All subsequent CLT data writes should continue in this manner.

Figure 7 CLT Write



1. Write CLT address to the Address Register.
2. With each strobe of the $\overline{RD}$ line, CLT data can be read in the order Red, Green and Blue at D0-D7.
3. When the Blue data read is completed, the address is automatically incremented and the CLT data for that address can then be read in the order of R, G and B.

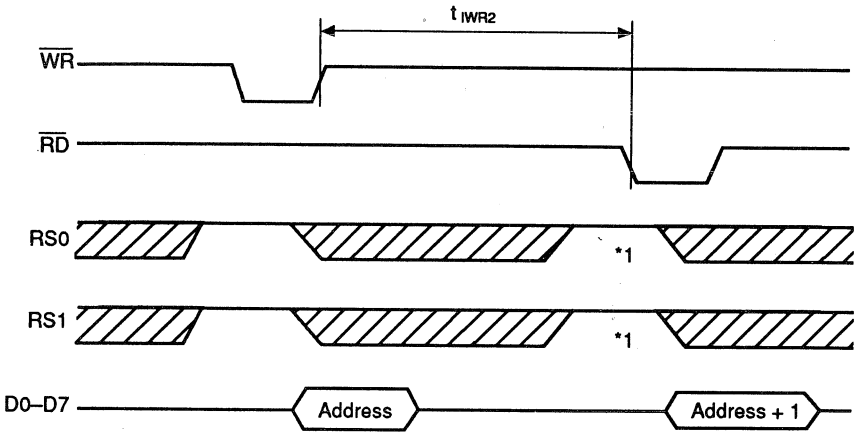
Figure 8 CLT Read



Video output is generated when a CLT data location is selected by the address input at P7-P0 and subsequently output as analog R, G, and B signals. The video output lags behind the PCLK strobe of its corresponding address at P7-P0 by three PCLK clock periods.

Note: Digital and Video signals are output in unison. During a blanking period, all outputs go to the 'L' level.

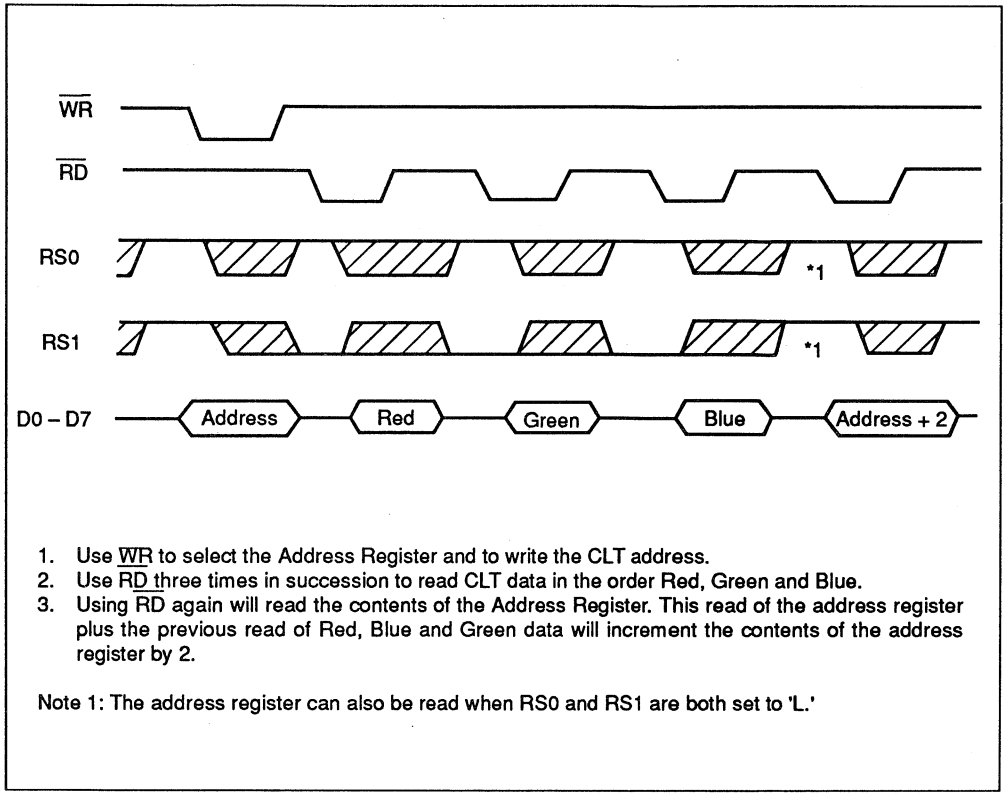
Figure 9 Video Output



1. Use WR to select the Address Register and to write the CLT read address.
2. Use RD to read the contents of the Address Register. At this time, the Address Register is incremented by 1.

Note 1: The address register can also be read when RS0 and RS1 are both set to 'L.'

Figure 10 Address Register Read (1)



1. Use WR to select the Address Register and to write the CLT address.
2. Use RD three times in succession to read CLT data in the order Red, Green and Blue.
3. Using RD again will read the contents of the Address Register. This read of the address register plus the previous read of Red, Blue and Green data will increment the contents of the address register by 2.

Note 1: The address register can also be read when RS0 and RS1 are both set to 'L.'

Figure 11 Address Register Read (2)

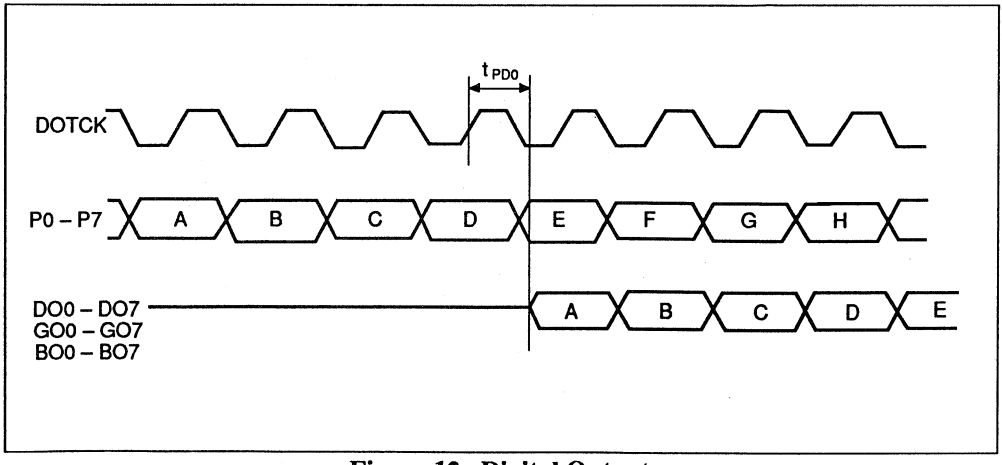


Figure 12 Digital Output

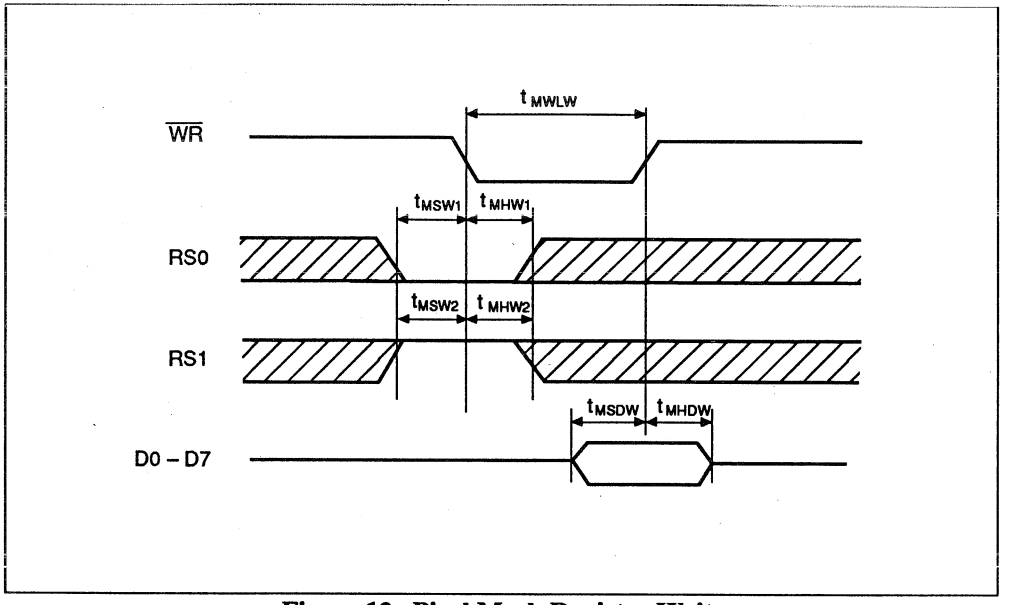


Figure 13 Pixel Mask Register Write

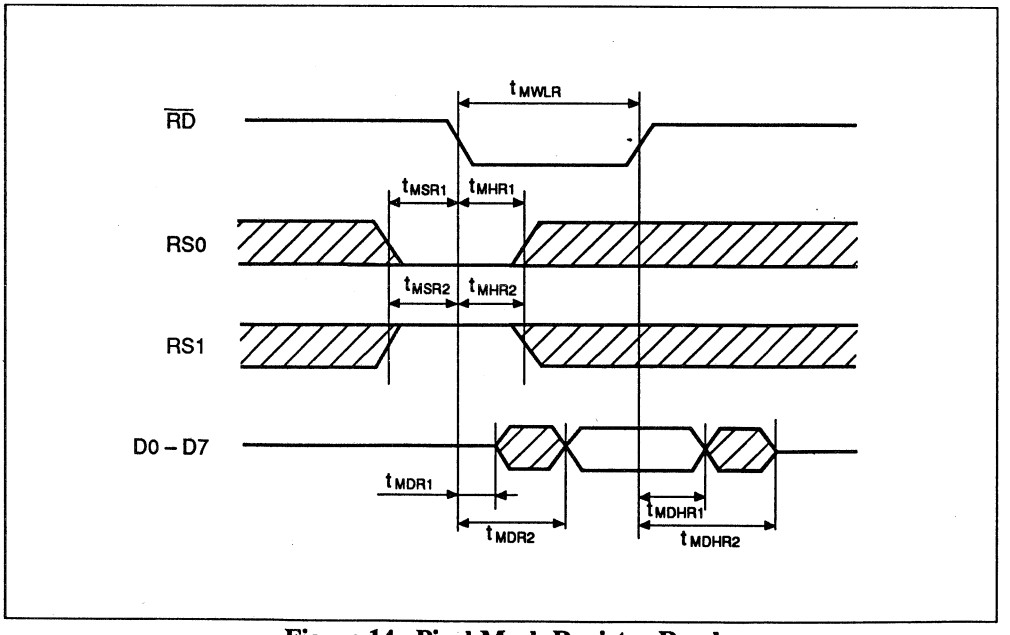


Figure 14 Pixel Mask Register Read

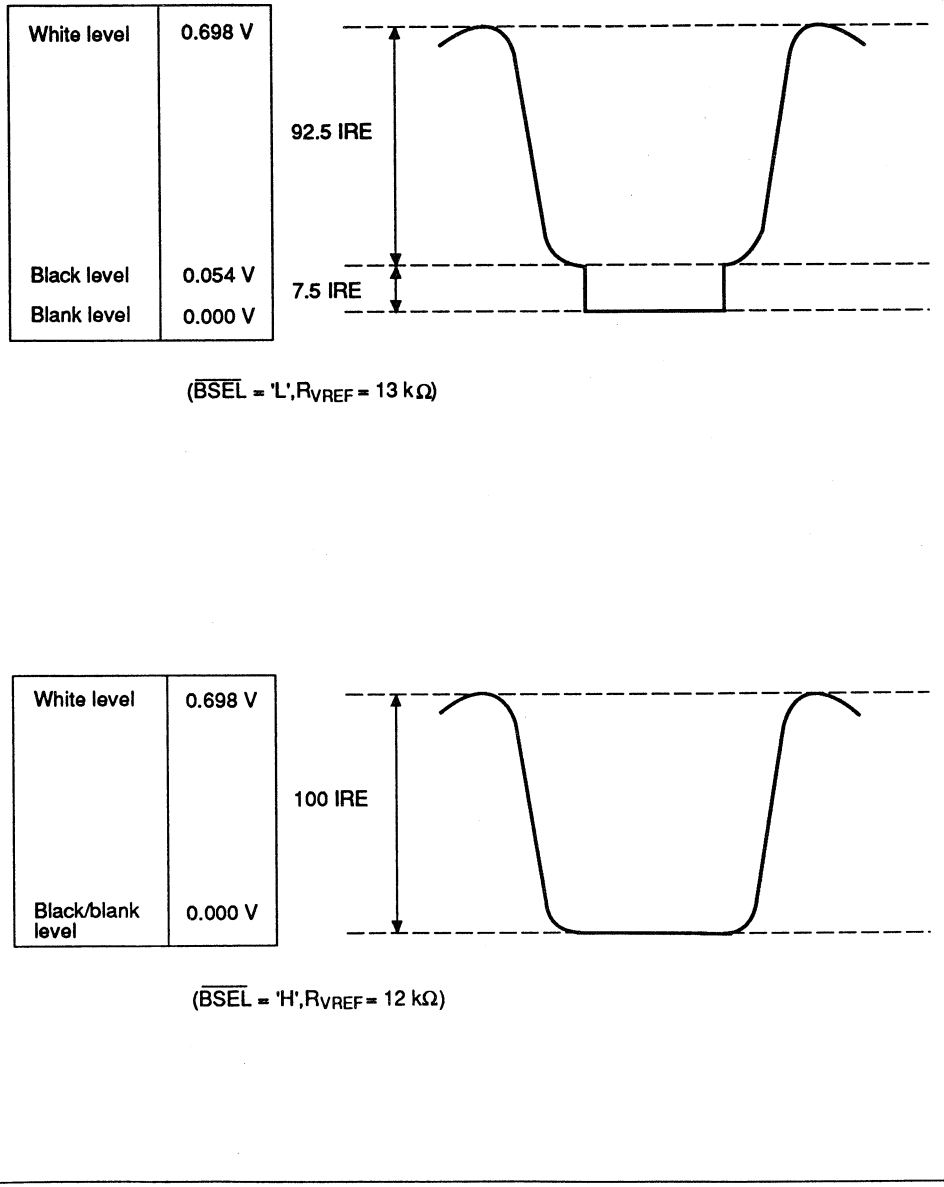


Figure 15 Video Output Waveforms

Mode Switching

HD153110 operating mode is switched as shown below. (8 bit/6bit='H')
When the 8 bit/6bit terminal is 'L' a 6-bit color palette can be used; when in 24-bit digital output mode, the digital outputs will be on the upper six bits of each 8-bit word and the lower two bits will be set 'L.'

Table 4 Mode Switching

OSL2	OSL1	OSL0	Operating Mode	Notes
L	L	L	DAC output mode	1
L	L	H	DAC direct Input (16,777,216-color simultaneous display mode)	1
L	H	L	Digital output 12-bit mode (R, G and B are output on upper 4 bits)	2
L	H	H	Prohibited (Digital output 24-bit mode)	3
H	L	L	Digital output 6-bit mode (Green output only)	2
H	L	H	Prohibited	
H	H	L	Digital output 24-bit mode	2
H	H	H	Prohibited	

Notes: 1. Digital output is Hi-Z.
2. DAC outputs are off.
3. Both Digital and DAC outputs are active.

Register Correspondence with CLT

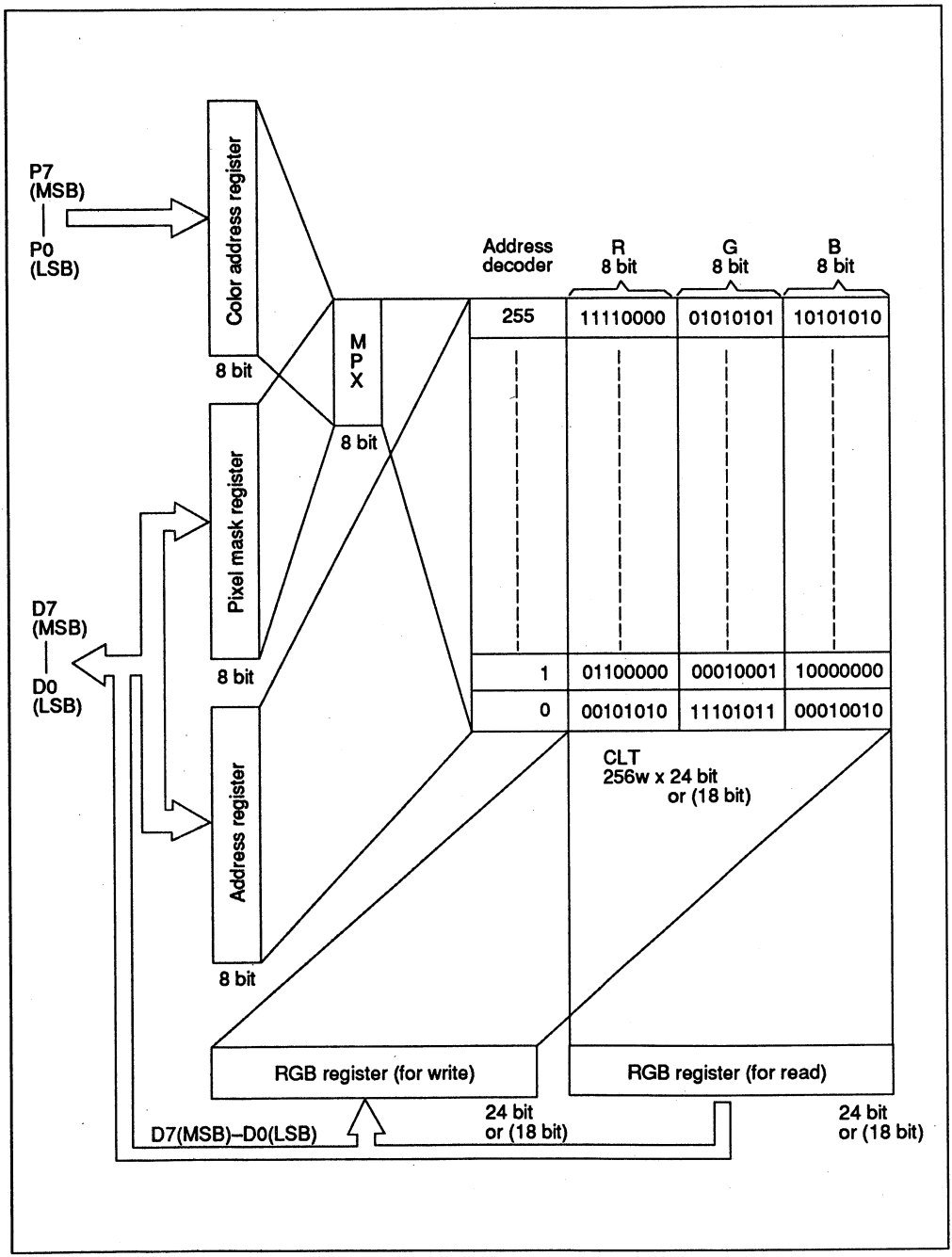


Figure 16 Register Correspondence with CLT

System Configuration Example

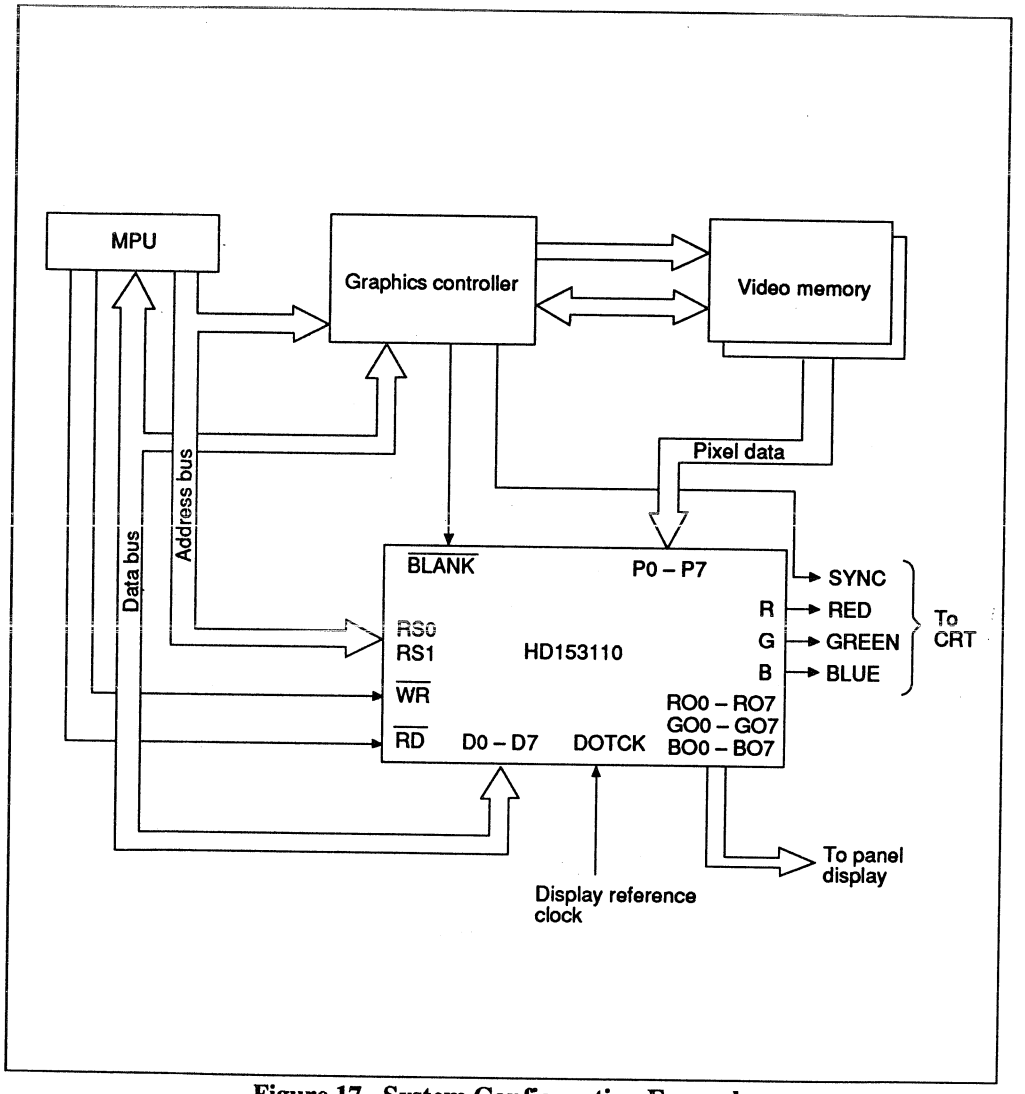


Figure 17 System Configuration Example

Table 5 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	0 to VCC	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	– 55 to +150	°C

Electrical Characteristics

Table 6 DAC Section Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Resolution		8 (6)	8 (6)	8 (6)	bits	
Maximum operating frequency	f_{CLK}	—	—	50/65	MHz	
Analog output voltage	V_A (Full)	–15	—	15	% of FSR	
(R_{VREF} = 12 kΩ)	V_A (Zero)	–2	—	2	% of FSR	
Differential linearity	DLE	–1	—	+1	LSB	
Integral linearity	ILE	–1	—	+1	LSB	
Output rise time (20 – 80%)	t_r	—	—	10	ns	C_L = 15 pF
Output fall time (80 – 20%)	t_f	—	—	10	ns	C_L = 15 pF
Settling time	t_s	—	—	30	ns	C_L = 15 pF
Glitch energy	E_G	—	90	—	PVS	

( ) indicates 6-bit mode.

Table 7 Digital Section DC Characteristics (unless otherwise specified V_{CC} = 5 V ±5 %: Ta = 0 to +70 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input "High" level voltage	V_{IH}	2.0	—	V_{CC}	V		
Input "Low" level voltage	V_{IL}	–0.3	—	0.8	V		
Input clamp voltage	V_I	—	—	–1.5	V	V_{CC} = 4.75 V I_{IN} = –18 mA	

Digital Section DC Characteristics
(unless otherwise specified V_{CC} = 5 V ±5 %: Ta = 0 to +70 °C) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Output "High" level voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V I_{OH} = –400 µA	
Output "Low" level voltage	V_{OL}	—	—	0.5	V	V_{CC} = 4.75 V I_{OL} = 8 mA	
Input current	I_I	—	—	1	mA	V_{CC} = 5.25 V V_I = 5.5 V	
"High" level input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V V_I = 2.7 V	
"Low" level input current	I_{IL}	—	—	–400	µA	V_{CC} = 5.25 V V_I = 0.4 V	
Supply current (1)	I_{CC} (1)	—	130	190	mA	V_{CC} = 5.25 V	1
Supply current (2)	I_{CC} (2)	—	110	160	mA	V_{CC} = 5.25	2

Notes: 1. OSL0 = 'L', OSL1 ='L', OSL2 ='L'
2. OSL0 ='L', OSL1 = 'H', OSL2 = 'H'

Table 8 Digital Section AC Characteristics (V_{CC} = 5 V, Ta = 25 °C)

		50 MHz		65 MHz				Reference
Item	Symbol	Min	Max	Min	Max	Unit	Remarks	Figure
DOTCK cycle time	t_{DCK}	20	—	15.3	—	ns		9
DOTCK low level time	t_{WLDCK}	8	—	6	—	ns		9
DOTCK high level time	t_{WHDCK}	8	—	6	—	ns		9
Data setup time	t_{SP}	6	—	5	—	ns		9
Data hold time	t_{HP}	6	—	5	—	ns		9
Data output delay time	t_{PDA}	—	30	—	30	ns	C_L =15 pF	9
$\overline{WR}$ low level time	t_{WLW}	50	—	50	—	ns		3, 7, 8
$\overline{WR}$ high level time	t_{WHW}	3×t_{DCK}	—	3×t_{DCK}	—	ns		7
$\overline{RD}$ low level time	t_{WLR}	50	—	50	—	ns		8
$\overline{RD}$ high level time (1)	t_{WHR1}	3×t_{DCK}	—	3×t_{DCK}	—	ns		8
$\overline{RD}$ high level time (2)	t_{WHR2}	6×t_{DCK}	—	6×t_{DCK}	—	ns		8
$\overline{WR}$/$\overline{RD}$ interval time (1)	t_{IWR1}	3×t_{DCK}	—	3×t_{DCK}	—	ns		5, 6
$\overline{WR}$/$\overline{RD}$ interval time (2)	t_{IWR2}	6×t_{DCK}	—	6×t_{DCK}	—	ns		5, 6, 8, 9

Digital Section AC Characteristics (V_{CC} = 5 V, Ta = 25 °C) (cont)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Remarks	Reference Figure
$\overline{WR}$/RS0, RS1 setup time	t_{SW}	10	—	10	—	ns		3
$\overline{WR}$/RS0, RS1 hold time	t_{HW}	10	—	10	—	ns		3
$\overline{RD}$/RS0, RS1 setup time	t_{SRR}	10	—	10	—	ns		4
$\overline{RD}$/RS0, RS1 hold time	t_{HRR}	10	—	10	—	ns		4
$\overline{WR}$ data setup time	t_{SDW}	10	—	10	—	ns		3
$\overline{WR}$ data hold time	t_{HDW}	10	—	10	—	ns		3
$\overline{RD}$ data output delay time (1)	t_{DDR1}	5	—	5	—	ns	C_L = 15 pF	4
$\overline{RD}$ data output delay time (2)	t_{DDR2}	—	40	—	40	ns	C_L =15 pF	4
$\overline{RD}$ data output hold time (1)	t_{HDR1}	5	—	5	—	ns	C_L =15 pF	4
$\overline{RD}$ data output hold time (2)	t_{HDR2}	—	20	—	20	ns	C_L =15 pF	4
Digital output delay time	t_{PDO}	—	19	—	19	ns	C_L = 15 pF	12
$\overline{WR}$ low level time	t_{MWLW}	50	—	50	—	ns		13
$\overline{RD}$ low level time	t_{MWLR}	50	—	50	—	ns		14
$\overline{WR}$/RS0, RS1 setup time	t_{MSW1}	10	—	10	—	ns		13
	t_{MSW2}	10	—	10	—	ns		13
$\overline{WR}$/RS0, RS1 hold time	t_{MHW1}	10	—	10	—	ns		13
	t_{MHW2}	10	—	10	—	ns		13
$\overline{RD}$/RS0, RS1 setup time	t_{MSR1}	10	—	10	—	ns		14
	t_{MSR2}	10	—	10	—	ns		14
$\overline{RD}$/RS0, RS1 hold time	t_{MHR1}	10	—	10	—	ns		14
	t_{MHR2}	10	—	10	—	ns		14
$\overline{WR}$ data setup time	t_{MSDW}	10	—	10	—	ns		13
$\overline{WR}$ data hold time	t_{MHDW}	10	—	10	—	ns		13

Digital Section AC Characteristics (V_{CC} = 5 V, Ta = 25 °C) (cont)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Remarks	Reference Figure
RD data output delay time	t_{MDR1}	5	—	5	—	ns	C_L = 15 pF	14
	t_{MDR2}	—	40	—	40	ns	C_L = 15 pF	14
RD data output hold time	t_{MDHR1}	5	—	5	—	ns	C_L = 15 pF	14
	t_{MDHR2}	—	20	—	20	ns	C_L = 15 pF	14

Connection Example

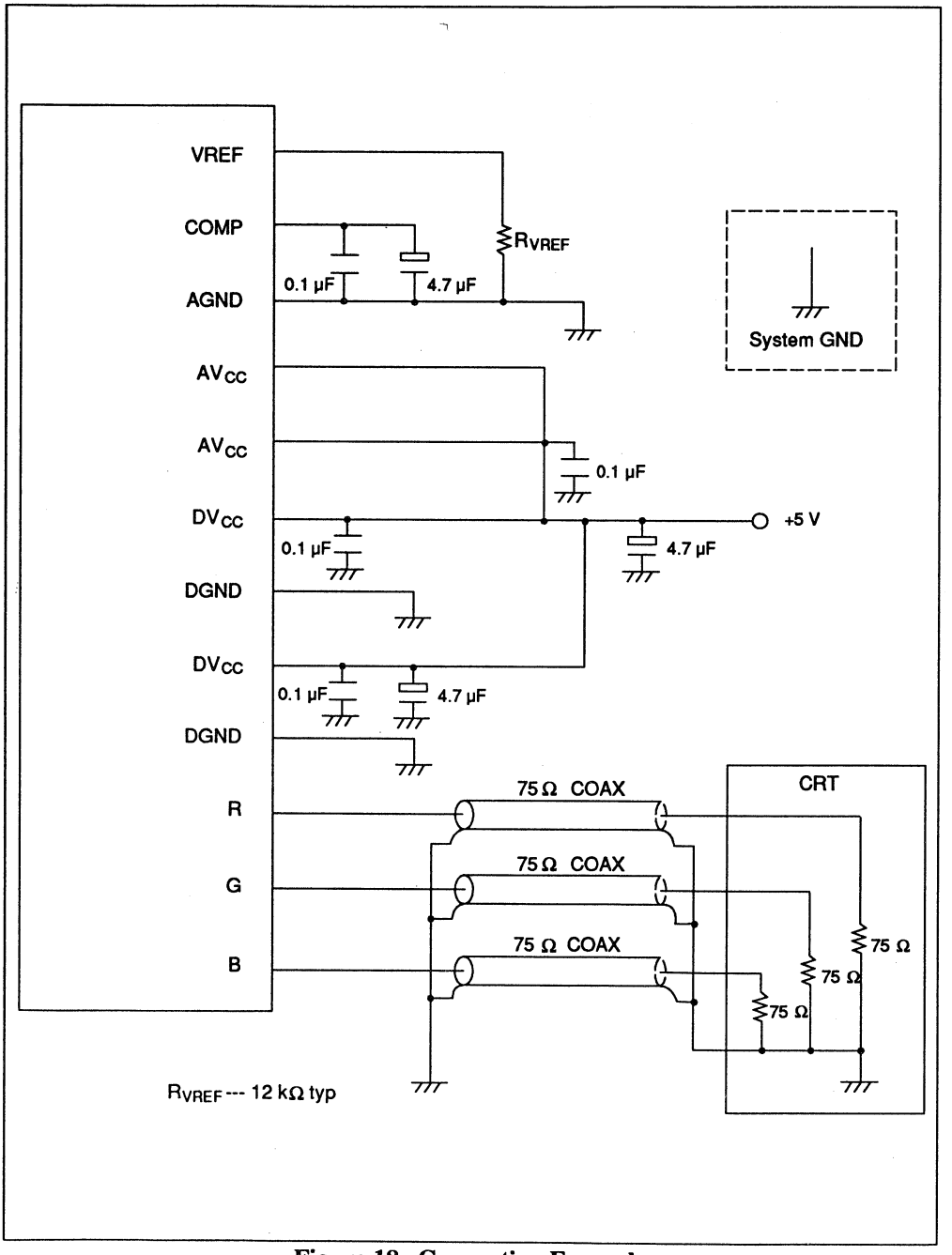


Figure 18 Connection Example

HD153119

Color Palette with Triple 6-bit DA Converter

The HD153119FS/CP is a color palette with triple 6-bit DA converter. Manufactured with Hitachi's Hi-BiCMOS process, this LSI realizes high speed, high density, low power consumption and minimizes the need for externally connected parts. Also, in addition to applications for existing CRTs, the provision of digital R, G and B outputs for color LCD ensure that the HD153119 can easily accomodate future systems using full-color LCD. With color palette, advanced functions, small size and low cost, the HD153119 is an essential component for advanced graphics systems.

Features

- Displays 256 colors simultaneously from a total of 262,144 possible colors
- Three 6-bit DA converters for RGB video output on a single chip
- Pixel mask function for display control
- Compatible with personal system/2*
- For each pixel, dynamic switching between 262,144-color simultaneous display mode and normal mode.
- In addition to existing CRT applications, direct digital RGB outputs from the color lookup table(CLT) are provided for color LCD applications.
- Variable BLACK level (0 or 7.5 IRE)
- Selectable composite or non-composite SYNC signal (composite is RGB three-channel)
- Dot rate maximum of 50/65 MHz
- Synchronous timing for pipeline control selectable between rise or fall of DOTCK.
- TTL compatible I/O levels

Note: Personal System/2 is a registered trademark of IBM corporation.

Ordering Information

Type No.	Max. Operating Freq.	Package
HD153119FS	50 MHz	80 pin plastic QFP (FP-80B)
HD153119FS-65	65 MHz	
HD153119CP	50 MHz	68 pin plastic QFJ (CP-68)
HD153119CP-65	65 MHz	

Pin Arrangement

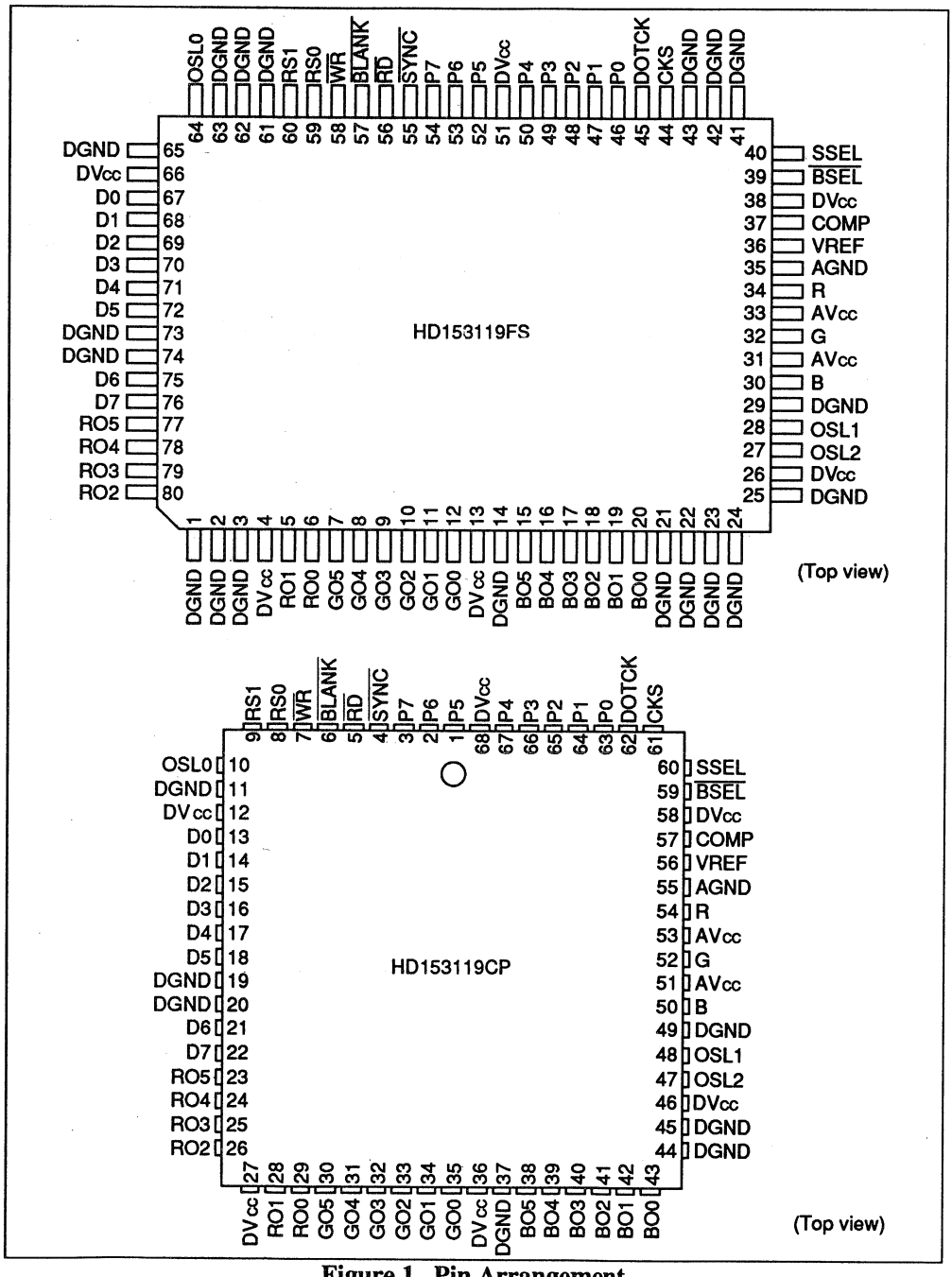
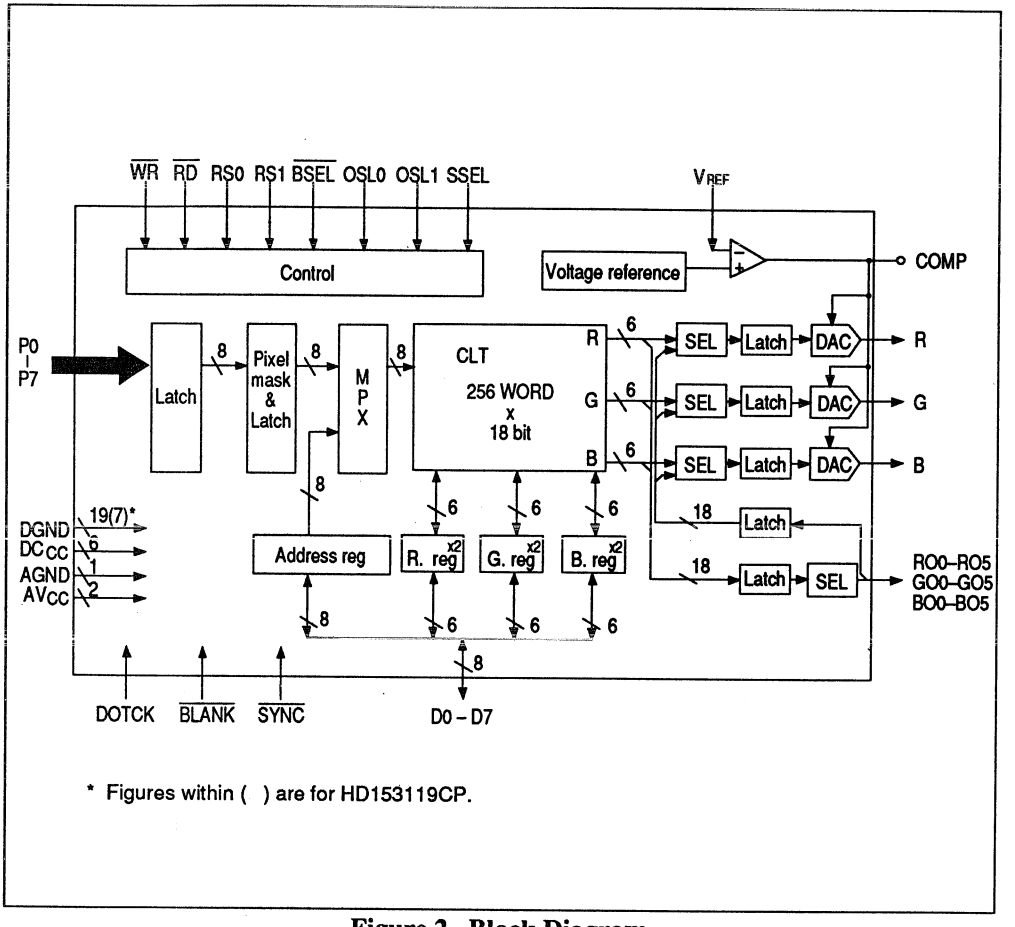


Figure 1 Pin Arrangement

Block Diagram



* Figures within ( ) are for HD153119CP.

Figure 2 Block Diagram

Table 1 Pin Description

Pin name	Pin number *	Description
P0 – P7	46 – 50 52 – 54 (63 – 67, 1 – 3)	CLT address inputs. P7 is MSB. P0 is LSB.
D0 – D7	67 – 72, 75, 76 (13 – 18, 21, 22)	Data port for reading/writing CLT or address, pixel mask, R, G and B registers. D7 is MSB, D0 is LSB.
$\overline{RD}$	56 (5)	Read clock input. Strobes data from CLT or address, pixel mask, R, G or B registers during read operation.
$\overline{WR}$	58 (7)	Write clock input. Strobes data to CLT or address, pixel mask, R, G or B registers during write operation.
RS0, RS1	59, 60 (8, 9)	Select input for CLT, address register or pixel mask register.
RO0 – RO5 GO0 – GO5 BO0 – BO5	6, 5, 80 – 77 (29, 28, 26 – 23) 12 – 7 (35 – 30) 20 – 15 (43 – 38)	Palette (CLT) digital signal outputs. RO5, GO5 and BO5 are the MSBs and RO0, GO0, and BO0 are the LSBs.
VREF	36 (56)	Terminal for connecting reference resistor to set DAC analog output level.
COMP	37 (57)	Terminal for connecting a phase-compensation capacitor
OSL0, OSL1, OSL2	64, 28, 27 (10, 48, 47)	Select inputs for digital signal outputs.
R, G, B	34, 32, 30 (54, 52, 50)	DAC analog signal outputs.
$\overline{BLANK}$	57 (6)	Video blank input for activating blank signal levels at DAC analog outputs.
$\overline{BSEL}$	39 (59)	Input for selecting DAC BLANK level (0 or 7.5 IRE)
DOTCK	45 (62)	Reference clock input for digital and analog sections. On the rise of this signal, CLT, BLANK and SYNC operations are processed and analog signal outputs become active.
CKS	44 (61)	Input for selecting active polarity of DOTCK. When CKS = 'L' operations occur on DOTCK rise. When CKS = 'H' operations occur on DOTCK fall.

* Upper pin numbers are for HD153119FS. Lower pin numbers within ( ) are for HD153119CP.

Pin Description (cont)

Pin name	Pin number *	Description
SSEL	40 (60)	Input for selecting composite or non-composite SYNC signal. Composite when SSEL = 'H' and non-composite when SSEL = 'L'. For composite, the SYNC level is 0 IRE, blank level is 40 IRE and the WHITE level is 140 IRE.
DVCC	4, 13, 26, 38, 51, 66 (12, 27, 36, 46, 58, 68)	Digital power supply
DGND	1 – 3, 14, 21 – 25 29, 41 – 43, 61 – 63, 65, 73, 74 (11, 19, 20, 37, 44, 45, 49)	Digital GND
AV_{CC}	31, 33 (51, 53)	Analog power supply
AGND	35 (55)	Analog GND

* Upper pin numbers are for HD153119FS. Lower pin numbers within ( ) are for HD153119CP.

Functions

Accessing the CLT and Registers

The CLT and registers are selected with inputs RS0 and RS1 (see table 2).

Table 2 Register Selection

RS1	RS0	Selection
0	0	Address register (write mode)
1	1	Address register (read mode)
0	1	CLT
1	0	Pixel mask register

Registers

Address register: To set up the address register for a CLT write operation, write the CLT address via D7 – D0 with RS0 = '0' and RS1 = '0' (in order to select the address register, write mode). For a CLT read operation, write the CLT address via D7 – D0 with RS0 = '1' and RS1 = '1' (in order to select the address register, read mode). Also, the address register contents can be read as shown in figure 10 and figure 11.

Pixel mask register: The pixel mask register is used when displayed colors to be modified (by altering the value input from video memory and the contents of the CLT). The pixel mask register is set by writing a pixel mask value to D7 (MSB) – D0 (LSB) with RS0 = '0' and RS1 = '1' (in order to select the pixel mask register for a data write) as shown in figure 13. During color palette operations, the value input from video memory at P7 (MSB) – P0 (LSB) is ANDed with the pixel mask register value, and the resulting value is applied as an address to the CLT. Consequently, pixel mask '0' bits will cancel corresponding video memory value '1' bits. Table 3 shows the CLT address that is generated for a particular pixel mask register value and video memory value.

Table 3 Pixel Mask Example

Pixel mask register	1	0	1	0	1	1	0	1
Address input	Pd7	Pd6	Pd5	Pd4	Pd3	Pd2	Pd1	Pd0
CLT address value	Pd7	0	Pd5	0	Pd3	Pd2	0	Pd0

RGB Registers: There are two RGB register types: one for writing color information to the CLT and one for reading color information from the CLT. Each register type is organized as an 18-bit word. To read or write data to the CLT, set RS0 = '1' and RS1 = '0' to select the appropriate RGB register while performing the read or write via data port D0 (LSB) – D5 (MSB). Bits D6 and D7 may be either '0' or '1' at this time. Write or read the data in the order of R, G, B as shown in figure 7 and figure 8.

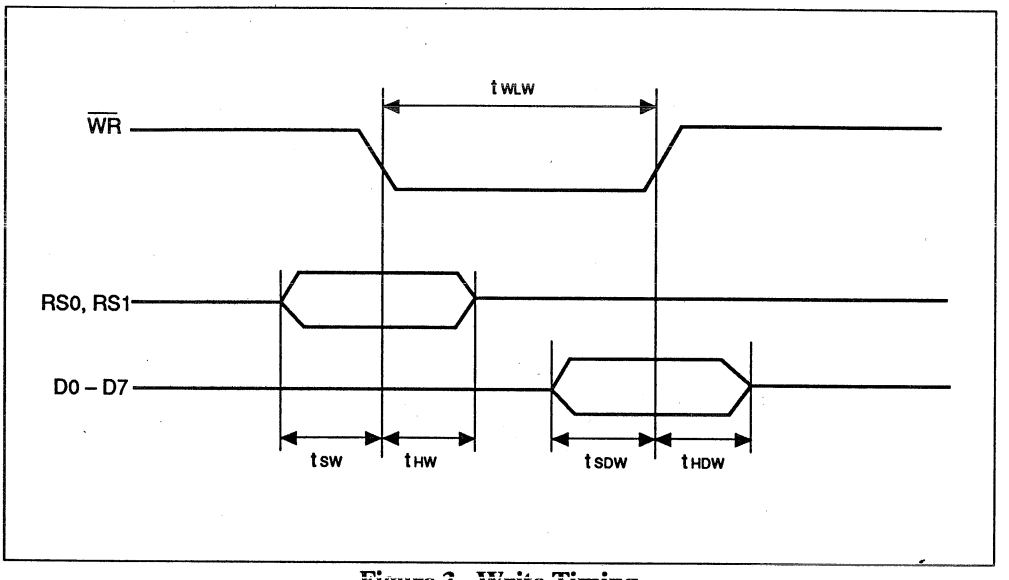


Figure 3 Write Timing

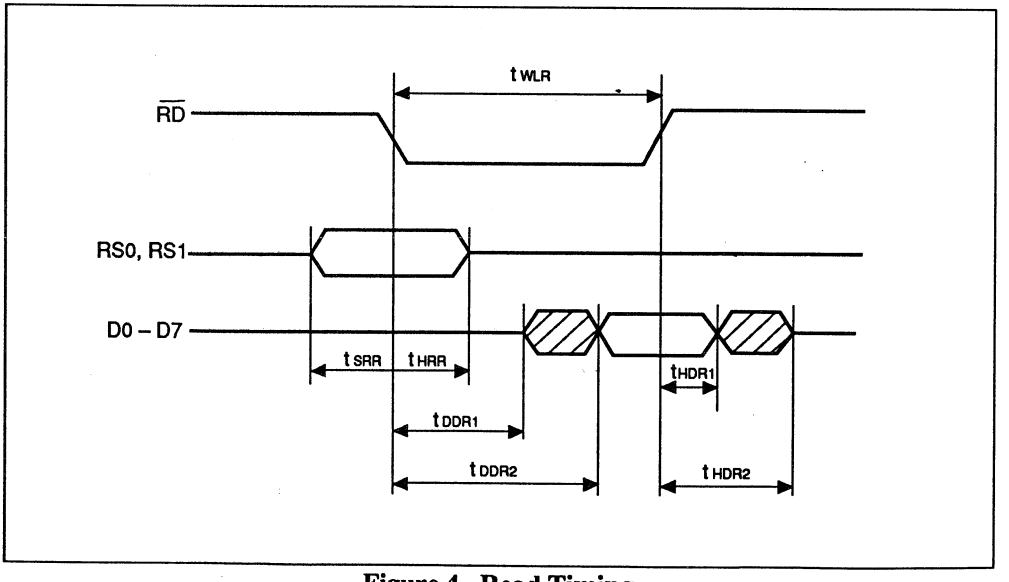
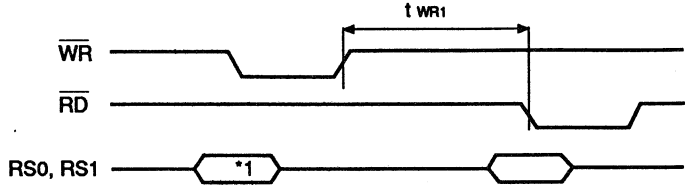


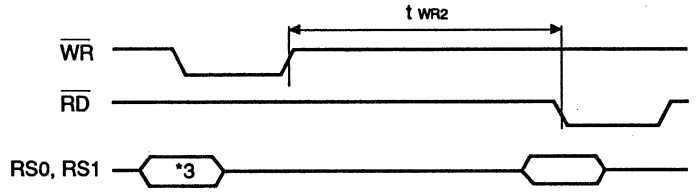
Figure 4 Read Timing

Applies to all read-after-write operations except when the write operation is placing a read address in the address register.



*1:
This timing not valid when RS0 = 'H' and RS1 = 'H'.

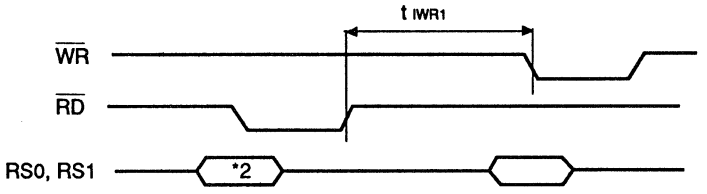
Applies to the case when the write operation is placing a read address in the address register.



*3:
This timing is valid when RS0 = 'H' and RS1 = 'H'.

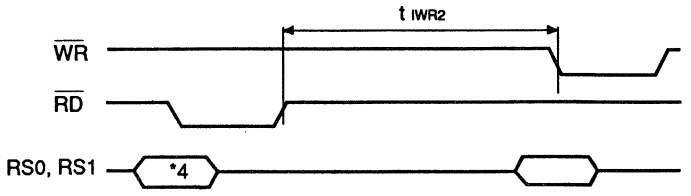
Figure 5 Read after Write

Applies to all cases except when the read operation is for CLT blue data.



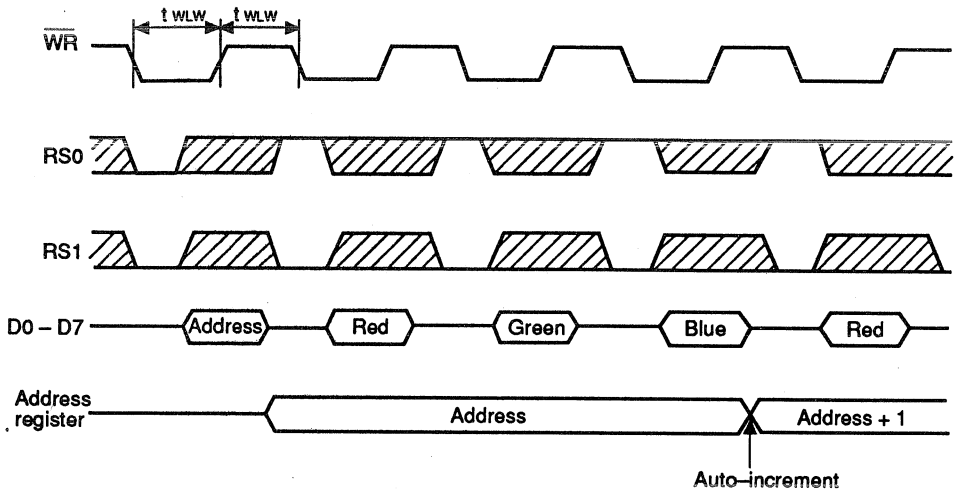
*2:
This timing not valid for reading CLT blue data or when RS0 = 'H' and RS1 = 'L'.

Applies to the case where the read operation is for CLT blue data.



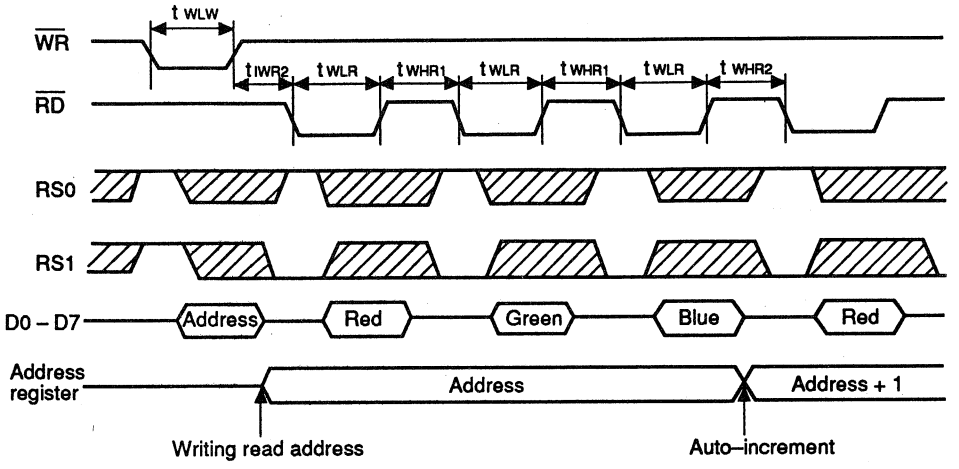
*4:
This timing is valid for reading CLT blue data or when RS0 = 'H' and RS1 = 'L'.

Figure 6 Write after Read



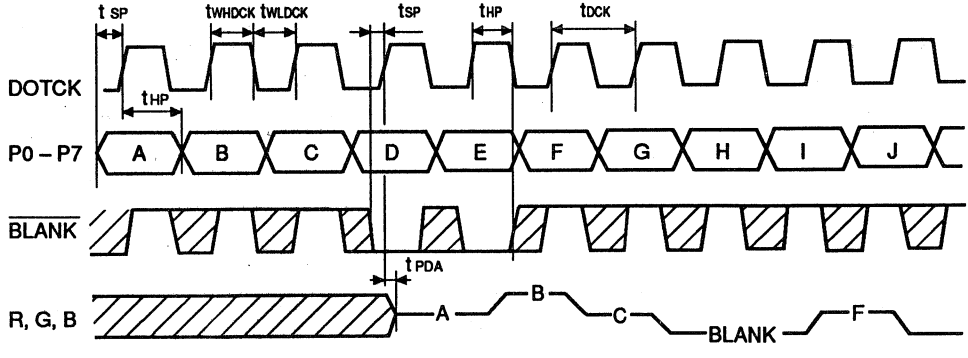
1. Write the CLT address to the address register.
2. Write the data (NRZ format) in the order red, green, then blue to D0 – D5. This R, G, and B data forms an 18-bit word that is written to the CLT.
3. When the R, G and B data writes are completed, the address is automatically incremented by +1 and the next data set can be applied again in RGB order. All subsequent CLT data writes should continue in this manner.

Figure 7 CLT Write



1. Write CLT address to the address register.
2. With each strobe of the $\overline{RD}$ line, CLT data can be read in the order red, green and blue at D0 – D5.
3. When the blue data read is completed, the address is automatically incremented and the CLT data for that address can then be read in the order of R, G and B.

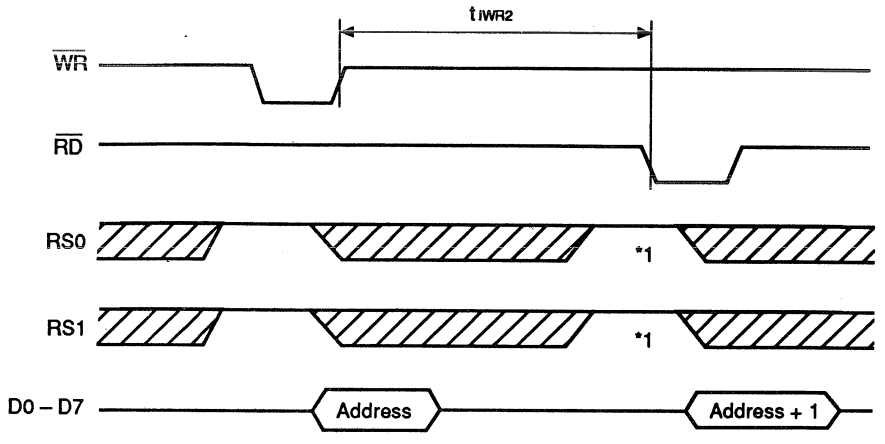
Figure 8 CLT Read



Video output is generated when a CLT adta location is selected by the address input at P7 – P0 and subsequently output as analog R, G, and B signals. The video output lags behind the PCLK strobe of its corresponding address at P7 – P0 by three PCLK clock periods.

Note: Digital and video signals are output in unison. During a blanking period, all outputs go to the 'L' level.

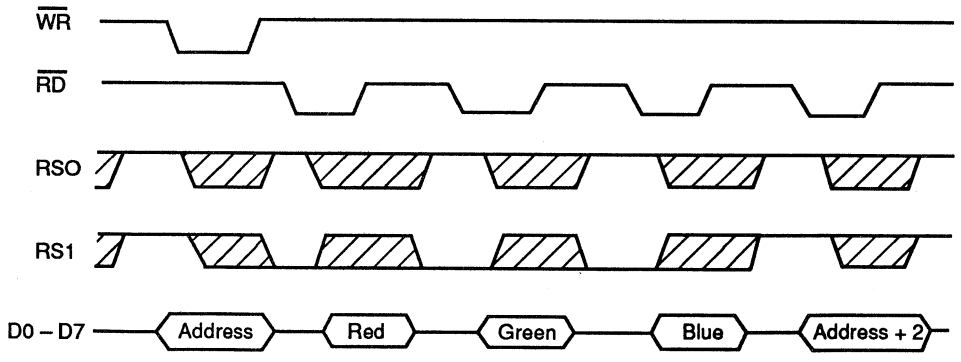
Figure 9 Video Output



1. Use $\overline{WR}$ to select the address register and to write the CLT read address.
2. Use $\overline{RD}$ to read the contents of the address register. At this time, the contents of the address register is incremented by +1.

*1: The address register can also be read when RS0 and Rs1 are both set to 'L'.

Figure 10 Address Register Read (1)



1. Use $\overline{WR}$ to select the address register and to write the CLT write address.
2. Use $\overline{RD}$ three times in succesion to read CLT data in the order red, green and blue.
3. Using $\overline{RD}$ again will read the contents of the address register. This read of the address register plus the previous read of red, blue and green data will increment the contents of the address register by +2.

*1: The address register can also be read when Rs0 and RS1 are both set to 'L'.

Figure 11 Address Register Read (2)

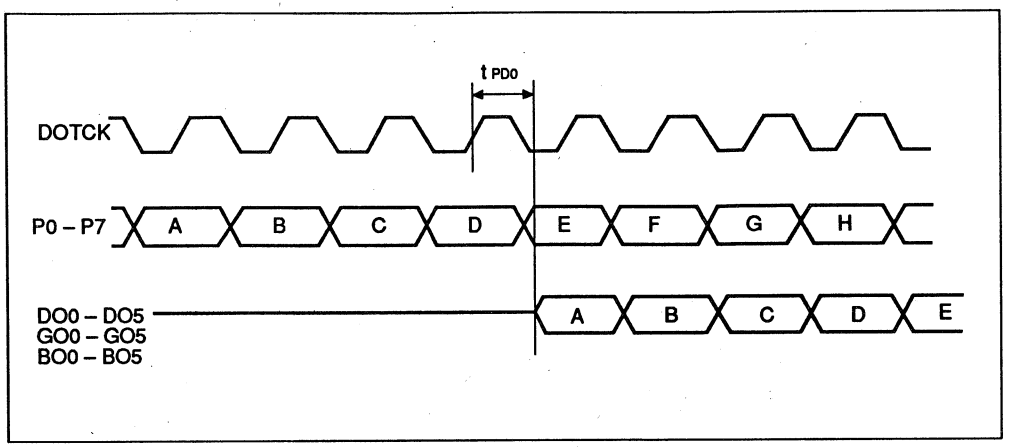


Figure 12 Digital Output

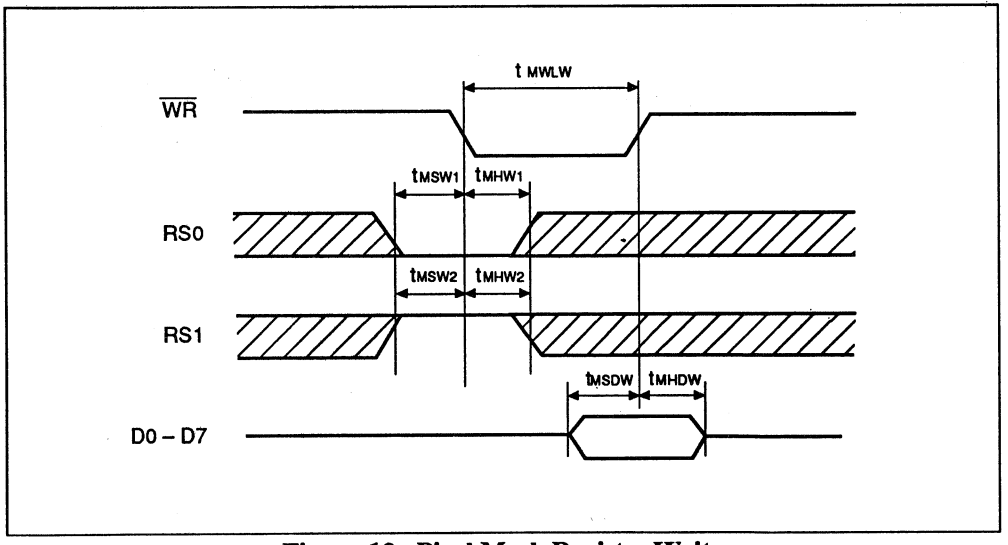


Figure 13 Pixel Mask Register Write

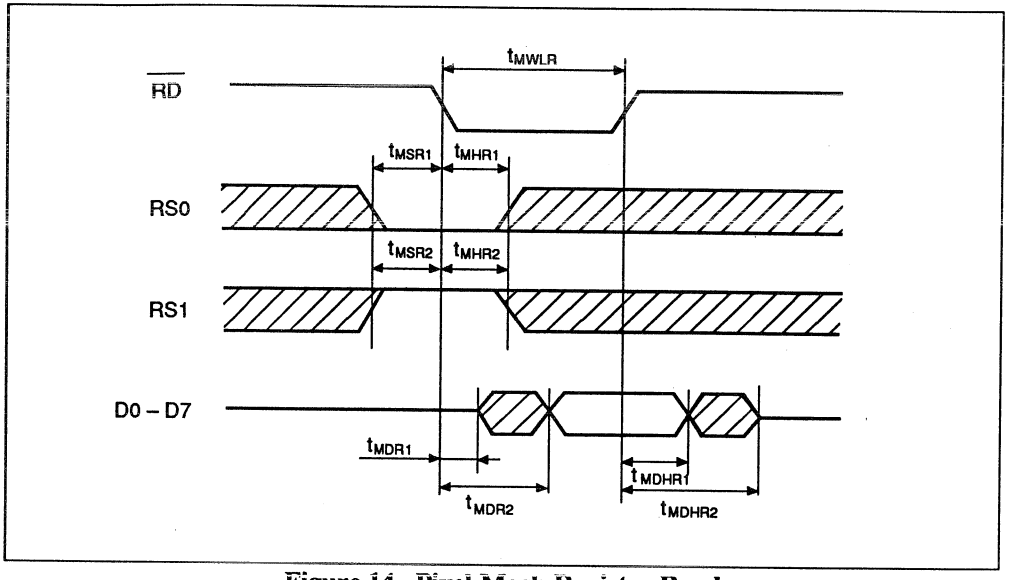
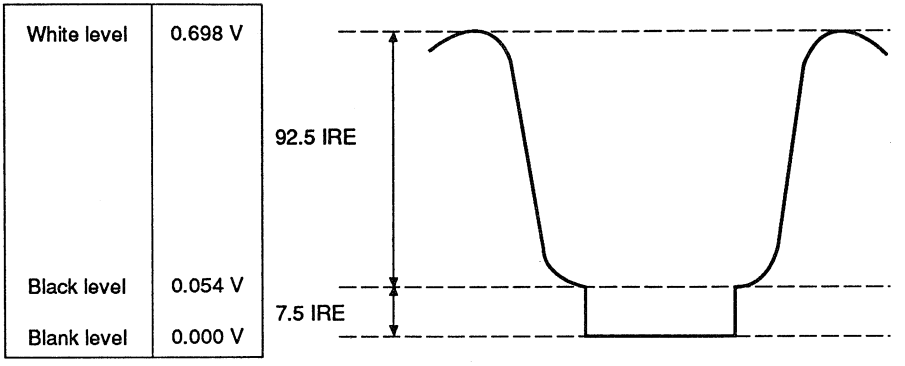
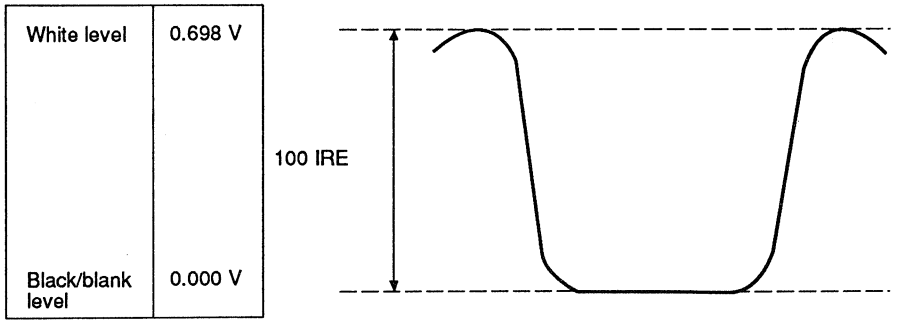


Figure 14 Pixel Mask Register Read

Video Output Waveforms



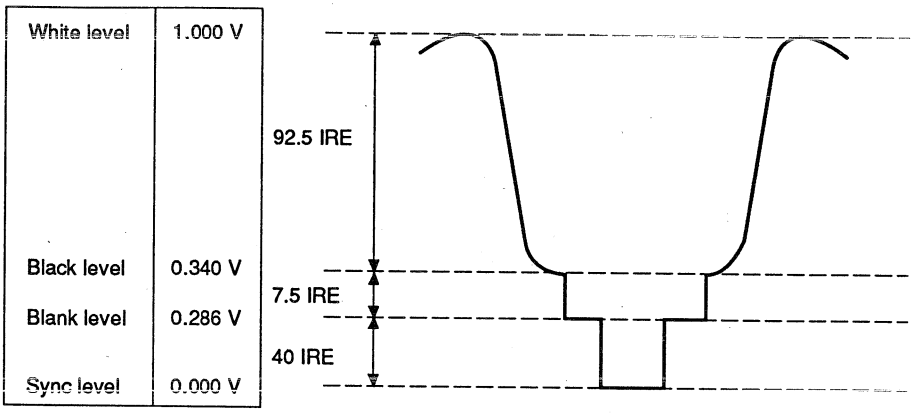
(SSEL = 'L', $\overline{BSEL}$ = 'L', R_{VREF} = 13 kΩ)



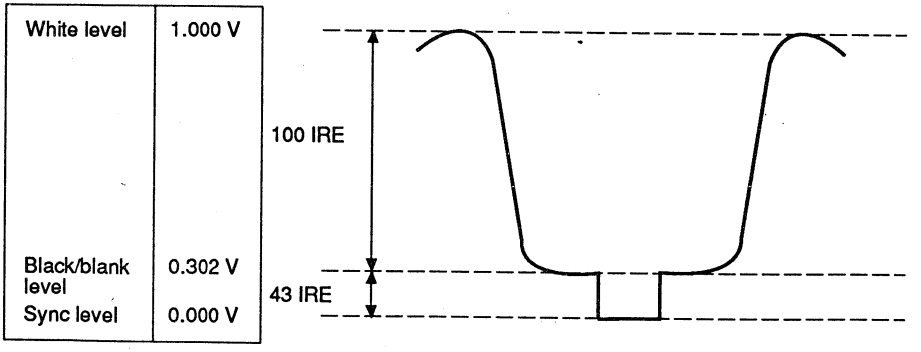
(SSEL = 'L', $\overline{BSEL}$ = 'H', R_{VREF} = 12 kΩ)

Figure 15 Video Output Waveforms

Video Output Waveforms (for composite $\overline{\text{SYNC}}$ signal)



(SSEL = 'H', $\overline{\text{BSEL}}$ = 'L', R_{VREF} = 13 kΩ)



(SSEL = 'H', $\overline{\text{BSEL}}$ = 'H', R_{VREF} = 12 kΩ)

Figure 16 Video Output Waveforms (for composite SYNC signal)

Mode Switching

HD153110 operating mode is switched as shown table 3.

Table 3 Mode Switching

OSL2	OSL1	OSL0	Operating mode	Note
L	L	L	DAC output mode	1
L	L	H	DAC direct input (262,144-color simultaneous display mode)	1
L	H	L	Digital output 12-bit mode (R, G and B are output on upper 4 bits)	2
L	H	H	Prohibited (Digital output 18-bit mode)	3
H	L	L	Digital output 6-bit mode (Green output only)	2
H	L	H	Prohibited	
H	H	L	Digital output 18-bit mode	2
H	H	h	Prohibited	

Notes: 1. Digital output is Hi-Z.
2. DAC outputs are off.
3. Both digital and DAC outputs are active.

Resister Correspondence with CLT

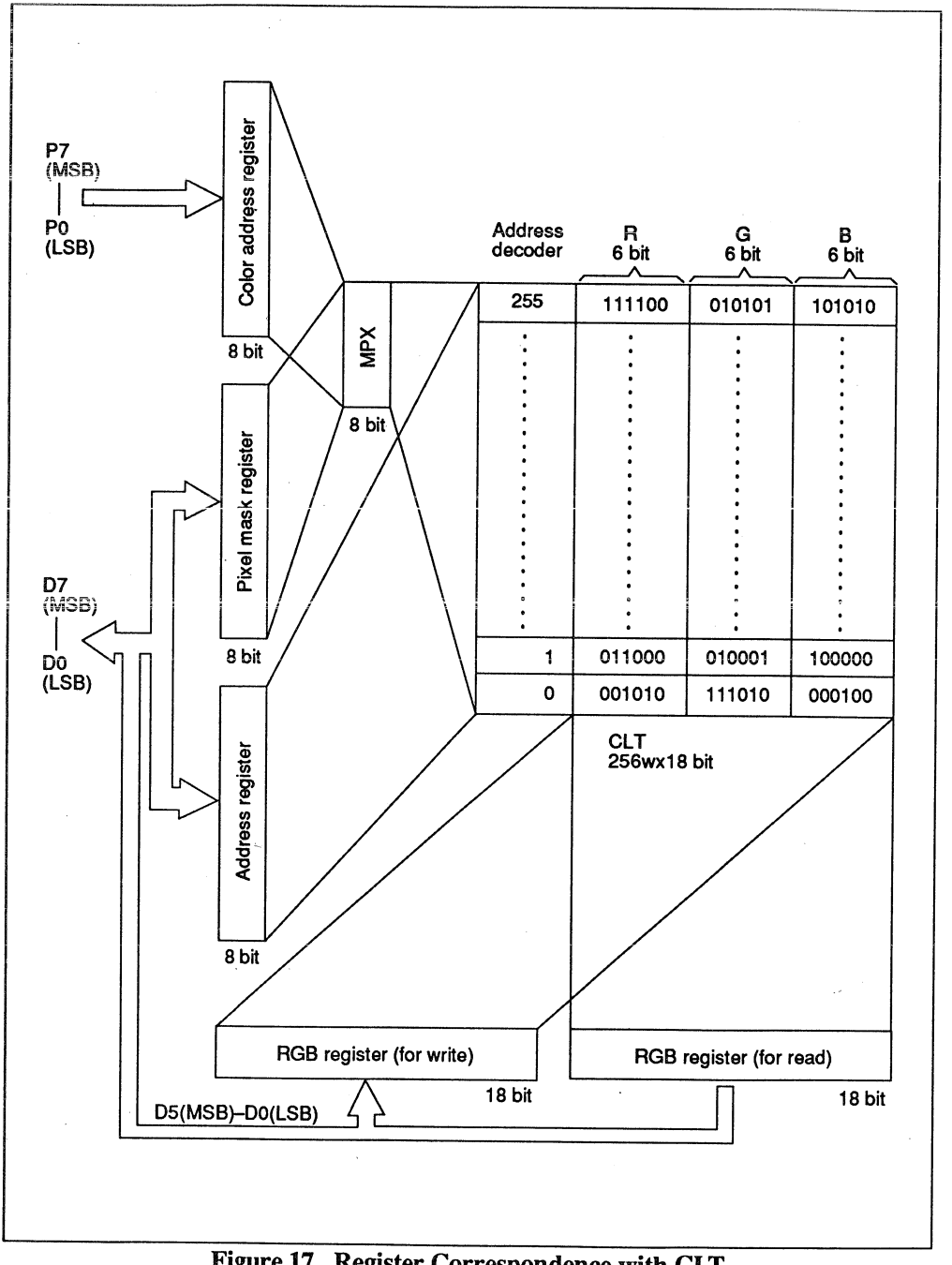


Figure 17 Register Correspondence with CLT

System Configuration Example

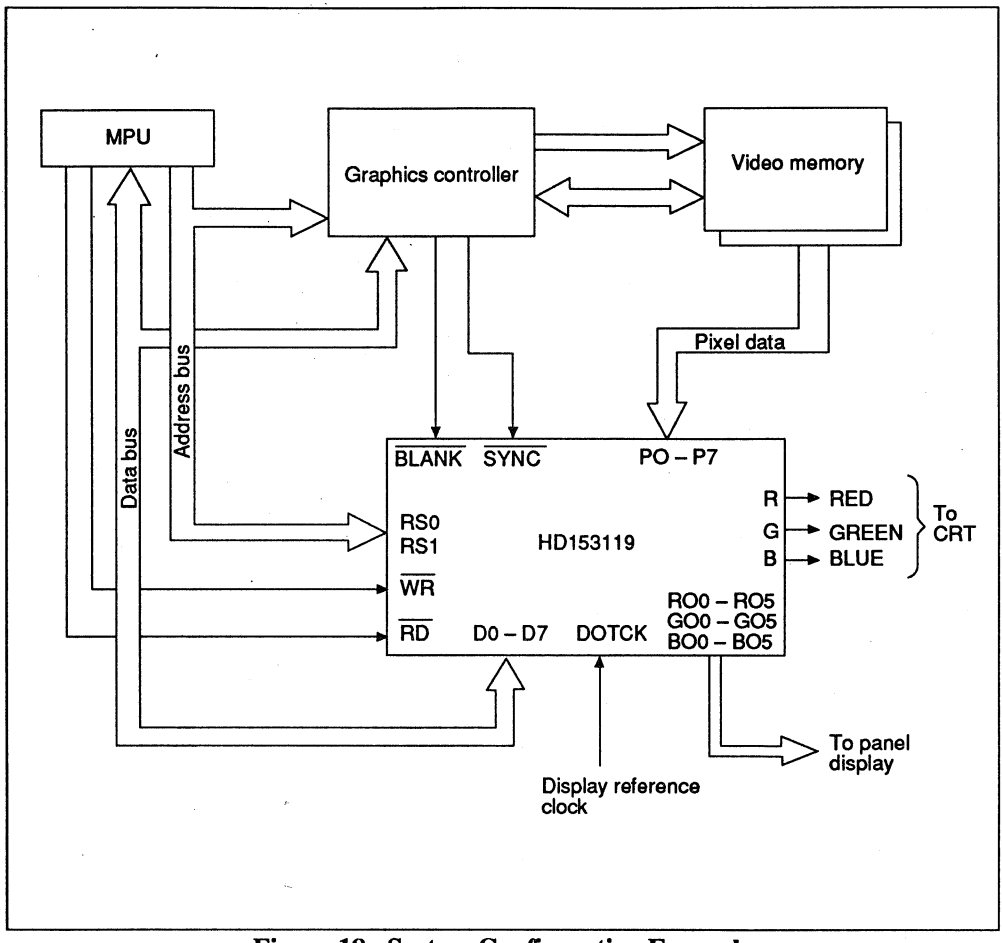


Figure 18 System Configuration Example

Table 4 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	7.0	V
Input voltage	V_{in}	0 to VCC	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +150	°C

Electrical Characteristics

Table 5 DAC Section Electrical Characteristics (V_{CC} = 5 V, Ta = 25 °C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		6	6	6	bits	
Maximum operating frequency	f_{CLK}	—	—	50/65	MHz	
Analog output voltage	V_A (Full)	–15	—	15	% of FSR	
(R_{VREF} = 12 kΩ)	V_A (Zero)	–2	—	2	% of FSR	
Differential linearity	DLE	–1	—	+1	LSB	
Integral linearity	ILE	–1	—	+1	LSB	
Output rise time (20 to 80 %)	tr	—	—	10	ns	C_L = 15 pF
Output fall time (80 to 20 %)	tf	—	—	10	ns	C_L = 15 pF
Settling time	ts	—	—	30	ns	C_L = 15 pF
Glitch energy	E_G	—	90	—	PVS	

Table 6 Digital section DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input "High" level voltage	V_{IH}	2.0	—	V_{CC}	V	
Input "Low" level voltage	V_{IL}	–0.3	—	0.8	V	
Input clamp voltage	V_I	—	—	–1.5	V	V_{CC} = 4.75 V I_{IN} = –18 mA
Output "High" level voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V I_{OH} = –400 µA
Output "Low" level voltage	V_{OL}	—	—	0.5	V	V_{CC} = 4.75 V I_{OL} = 8 mA
Input current	I_I	—	—	1	mA	V_{CC} = 5.25 V V_I = 5.5 V
"High" level input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V V_I = 2.7 V
"Low" level input current	I_{IL}	—	—	–400	µA	V_{CC} = 5.25 V V_I = 0.4 V
Supply current (1) *1	I_{CC} (1)	—	130	190	mA	V_{CC} = 5.25 V
Supply current (2) *2	I_{CC} (2)	—	110	160	mA	V_{CC} = 5.25 V

Notes: 1. OSL0 = 'L', OSL1 = 'L', OSL2 = 'L'
2. OSL0 = 'L', OSL1 = 'H', OSL2 = 'H'

Table 7 Digital Section AC Characteristics (V_{CC} = 5 V, Ta = 25 °C)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Test conditions	Reference figure
DOTCK cycle time	t_{DCK}	20	—	15.3	—	ns		9
DOTCK low level time	t_{WLDCK}	8	—	6	—	ns		9
DOTCK high level time	t_{WHDCK}	8	—	6	—	ns		9
Data setup time	t_{SP}	6	—	5	—	ns		9
Data hold time	t_{HP}	6	—	5	—	ns		9
Data output delay time	t_{PDA}	—	30	—	30	ns	C_L = 15 pF	9
$\overline{WR}$ low level time	t_{WLW}	50	—	50	—	ns		3, 7, 8
$\overline{WR}$ high level time	t_{WHW}	3 × t_{DCK}	—	3 × t_{DCK}	—	ns		4, 8
$\overline{RD}$ low level time	t_{WLR}	50	—	50	—	ns		8
$\overline{RD}$ high level time (1)	t_{WHR1}	3 × t_{DCK}	—	3 × t_{DCK}	—	ns		8
$\overline{RD}$ high level time (2)	t_{WHR2}	6 × t_{DCK}	—	6 × t_{DCK}	—	ns		8
$\overline{WR}$/$\overline{RD}$ interval time (1)	t_{IWR1}	3 × t_{DCK}	—	3 × t_{DCK}	—	ns		5, 6
$\overline{WR}$/$\overline{RD}$ interval time (2)	t_{IWR2}	6 × t_{DCK}	—	6 × t_{DCK}	—	ns		5, 6, 8, 9
$\overline{WR}$/RS0, RS1 setup time	t_{SW}	10	—	10	—	ns		3
$\overline{WR}$/RS0, RS1 hold time	t_{HW}	10	—	10	—	ns		3
$\overline{RD}$/RS0, RS1 setup time	t_{SRR}	10	—	10	—	ns		4
$\overline{RD}$/RS0, RS1 hold time	t_{HRR}	10	—	10	—	ns		4
$\overline{WR}$ data setup time	t_{SDW}	10	—	10	—	ns		3
$\overline{WR}$ data hold time	t_{HDW}	10	—	10	—	ns		3
$\overline{RD}$ data output delay time (1)	t_{DDR1}	5	—	5	—	ns	C_L = 15 pF	4
$\overline{RD}$ data output delay time (2)	t_{DDR2}	—	40	—	40	ns	C_L = 15 pF	4
$\overline{RD}$ data output hold time (1)	t_{HDR1}	5	—	5	—	ns	C_L = 15 pF	4
$\overline{RD}$ data output hold time (2)	t_{HDR2}	—	20	—	20	ns	C_L = 15 pF	4
Digital output delay time	t_{PDO}	—	19	—	19	ns	C_L = 15 pF	12
$\overline{WR}$ low level time	t_{MWLW}	50	—	50	—	ns		13
$\overline{RD}$ low level time	t_{MWLR}	50	—	50	—	ns		14

Digital Section AC Characteristics (V_{CC} = 5 V, Ta = 25 °C) (cont)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Test conditions	Reference figure
$\overline{WR}$/RS0, RS1 setup time	t_{MSW1}	10	—	10	—	ns		13
	t_{MSW2}	10	—	10	—	ns		13
$\overline{WR}$/RS0, RS1 hold time	t_{MHW1}	10	—	10	—	ns		13
	t_{MHW2}	10	—	10	—	ns		13
$\overline{RD}$/RS0, RS1 setup time	t_{MSR1}	10	—	10	—	ns		14
	t_{MSR2}	10	—	10	—	ns		14
$\overline{RD}$/RS0, RS1 hold time	t_{MHR1}	10	—	10	—	ns		14
	t_{MHR2}	10	—	10	—	ns		14
$\overline{WR}$ data setup time	t_{MSDW}	10	—	10	—	ns		13
$\overline{WR}$ data hold time	t_{MHDW}	10	—	10	—	ns		13
$\overline{RD}$ data output delay time	t_{MDR1}	5	—	5	—	ns	C_L = 15 pF	14
	t_{MDR2}	—	40	—	40	ns	C_L = 15 pF	14
$\overline{RD}$ data output hold time	t_{MDHR1}	5	—	5	—	ns	C_L = 15 pF	14
	t_{MDHR2}	—	20	—	20	ns	C_L = 15 pF	14

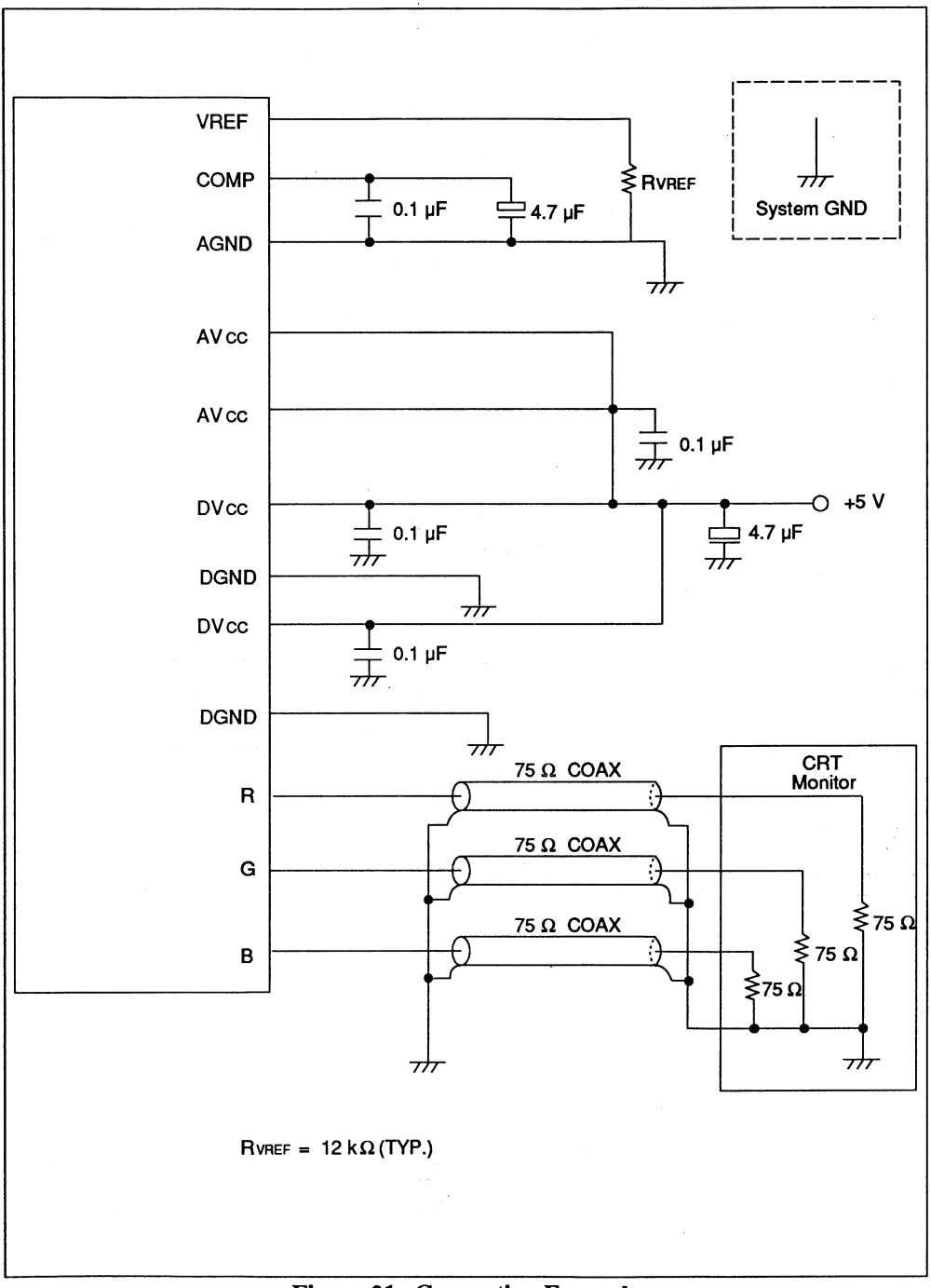


Figure 21 Connection Example

Preliminary

HD153129

Color Palette with Triple 6-bit DA Converter

The HD153129P is a high-speed, high-density, low-power color palette with triple 6-bit DA converter.

Manufactured using a Hi-BiCMOS process, it realizes advanced DA conversion, high-speed SRAM and high-speed logic all on a single LSI chip with its color palette, advanced functions, small size and low cost, the HD153129P is an essential component for advanced graphics systems.

Features

- Displays 256 colors simultaneously from a total of 262,144 possible colors.
- Three 6-bit DA converters for RGB video output on a single chip
- Pixel mask function for display control
- Compatible with personal system/2
- Dot rate maximum of 50/65 MHz
- TTL compatible I/O levels
- 28-pin plastic DIP

Ordering Information

Type No.	Max. Operating Freq.	Package
HD153129P	50 MHz	600 mil 28 pin plastic DIP (DP-28)
HD153129P-65	65 MHz	

Note: Personal system/2 is a registered trademark of IBM.

Pin Arrangement

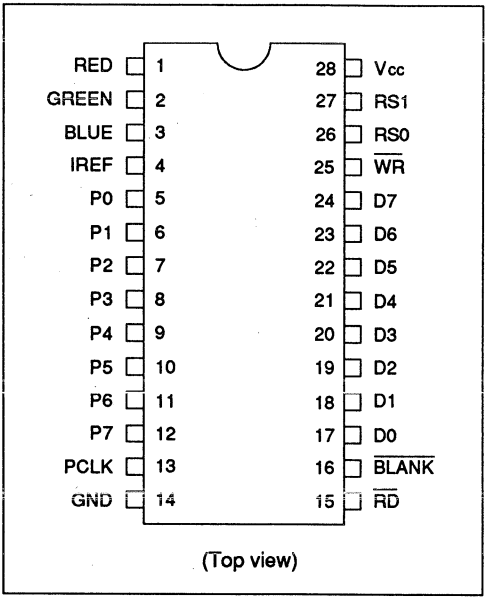


Figure 1 Pin Arrangement

Block Diagram

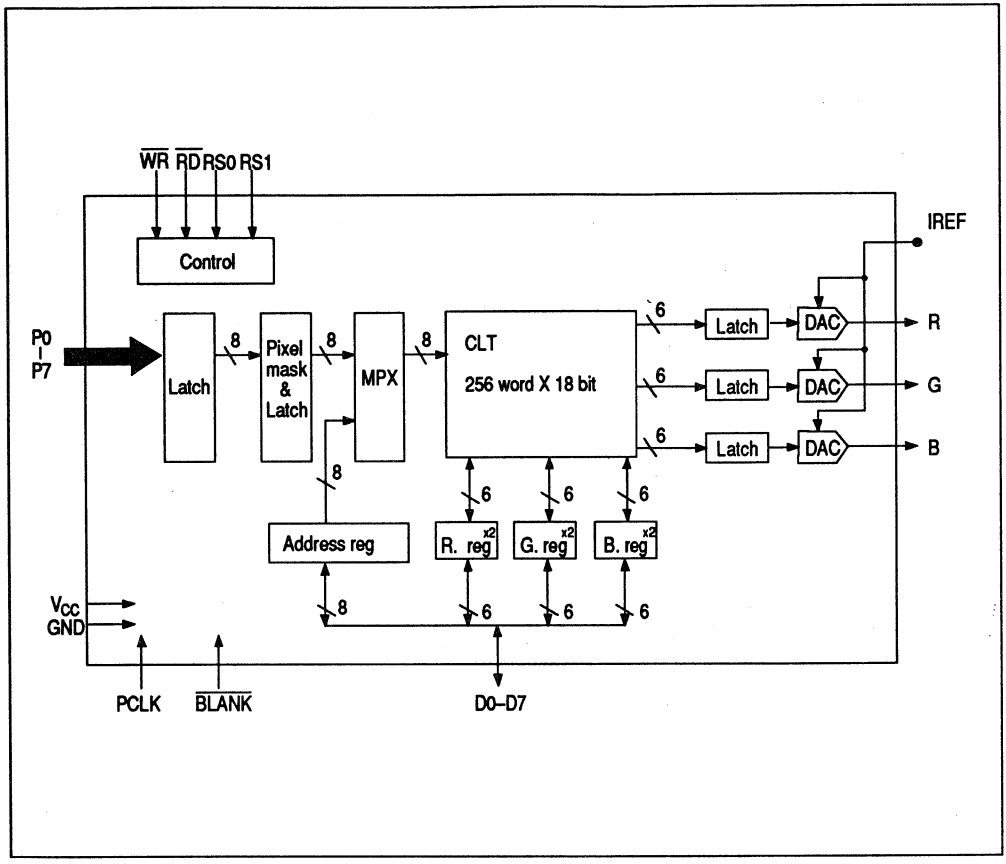


Figure 2 Block Diagram

Table 1 Pin Description

Pin name	Pin number	Description
P0 – P7	5, 6, 7, 8, 9, 10, 11, 12	CLT address inputs. P7 is MSB, P0 is LSB.
D0 – D7	17, 18, 19, 20, 21, 22, 23, 24	Data port for reading/writing CLT or address, pixel mask, R, G and B registers. D7 is MSB, D0 is LSB.
$\overline{RD}$	15	Read clock input. Strobes data from CLT or address, pixel mask, R, G or B registers during read operation.
$\overline{WR}$	25	Write clock input. Strobes data to CLT or address, pixel mask, R, G or B registers during write operation.
RS0, RS1	26, 27	Select inputs for CLT, address register or pixel mask register.
IREF	4	Terminal for connecting reference resistor to set DAC analog output level
RED, GREEN BLUE	1, 2, 3	DAC analog output signals
$\overline{BLANK}$	16	Video blank input for activating blank signal levels at DAC analog outputs.
PCLK	13	Reference clock input for digital and analog sections. On the rise of this signal, CLT and $\overline{BLANK}$ operations are processed and analog signal outputs become active.
V_{CC}	28	Power supply
GND	14	Ground

Functions

Accessing the CLT and Registers

The CLT and registers are selected with inputs RS0 and RS1 (see table 2).

Table 2 Register Selection

RS1	RS0	Selection
0	0	Address register (write mode)
1	1	Address register (read mode)
0	1	CLT
1	0	Pixel mask register

Address register: To perform read/write operations on the CLT, the CLT address must be set in the address register through D7 to D0 (D7 is the MSB and D0 is the LSB).
For a CLT write operation, write the CLT address via D7 to D0 with RS0 = "0" and RS1 = "0" (in order to select the address register, write mode).
To set up the address register for a CLT read operation, write the CLT address via D7 to D0 with RS0 = "1" and RS1 = "1" (in order to select the address register, read mode).
Also, the address register contents can be read as shown in figure 10 and figure 11.

Pixel mask register: The pixel mask register allows displayed colors to be modified by altering the value input from video memory and the contents of the CLT. The pixel mask register is set by writing a pixel mask value to D7 (MSB) to D0 (LSB) with RS0 "0" and RS1 = "1" (in order to select the pixel mask register for a data write) as shown in figure 13. During color palette operations, the value input from video memory at P7 (MSB) to P0 (LSB) is ANDed with the pixel mask register value, and the resulting value is applied as an address to the CLT. Consequently, pixel mask "0" bits will cancel corresponding video memory value "1" bits. The following table shows the CLT address that results for a particular pixel mask register value and video memory value.

Table 3 Pixel Mask Example

Pixel mask register	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**1**
Address input (P7 – P0)	Pd_7	Pd_6	Pd_5	Pd_4	Pd_3	Pd_2	Pd_1	Pd_0
CTL address value	Pd_7	0	Pd_5	0	Pd_3	Pd_2	0	Pd_0

RGB registers: There are two RGB register types: one for writing color information to the CLT and one for reading color information from the CLT. Each register type is organized as an 18-bit word.
To read or write data to the CLT, set RS0 = '0' to select the appropriate RGB register wrile performing the read or write via data port D5 (MSB) to D0 (LSB). Bits D6 and D7 may be either '0' or '1' at this time. Write or read the data in the order of R, G, B as shown in figure 7 and figure 8.

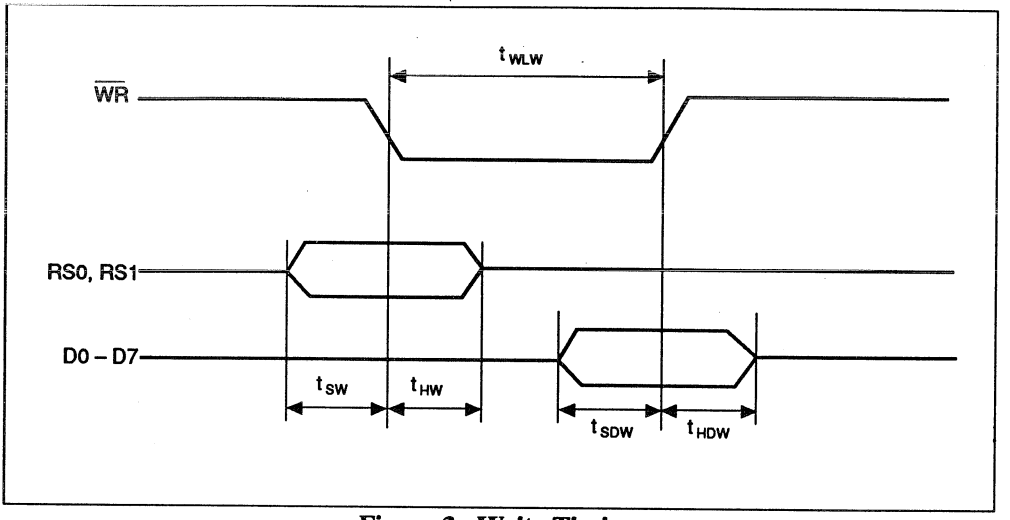


Figure 3 Write Timing

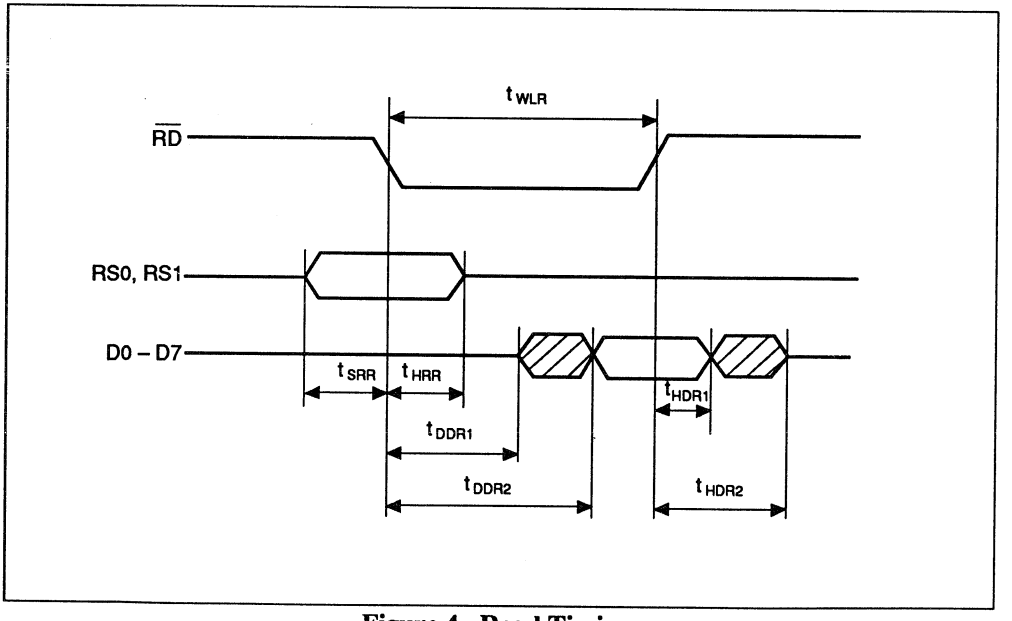


Figure 4 Read Timing

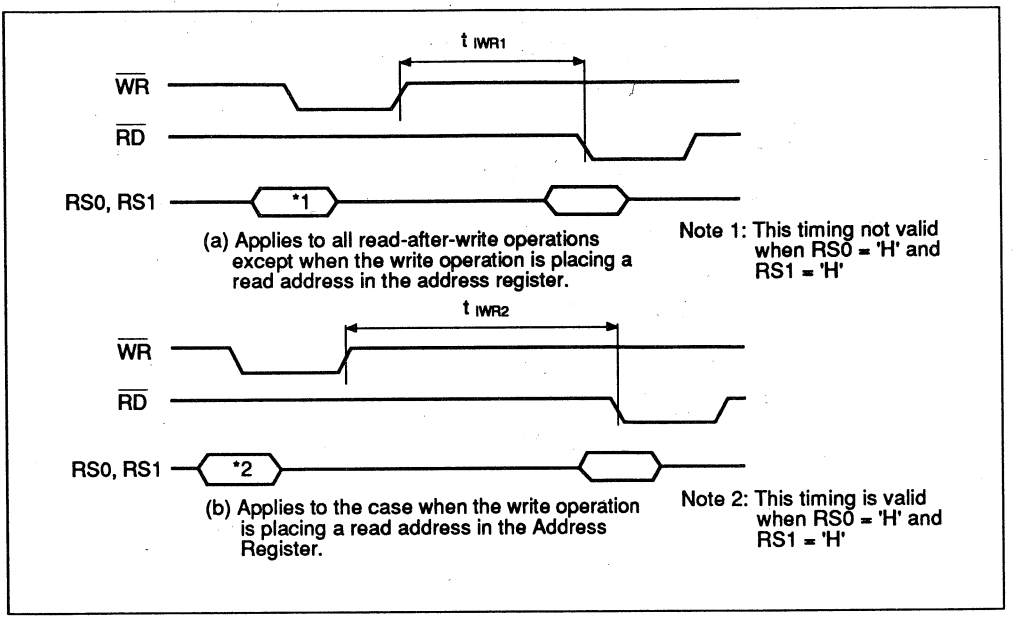


Figure 5 Read after Write

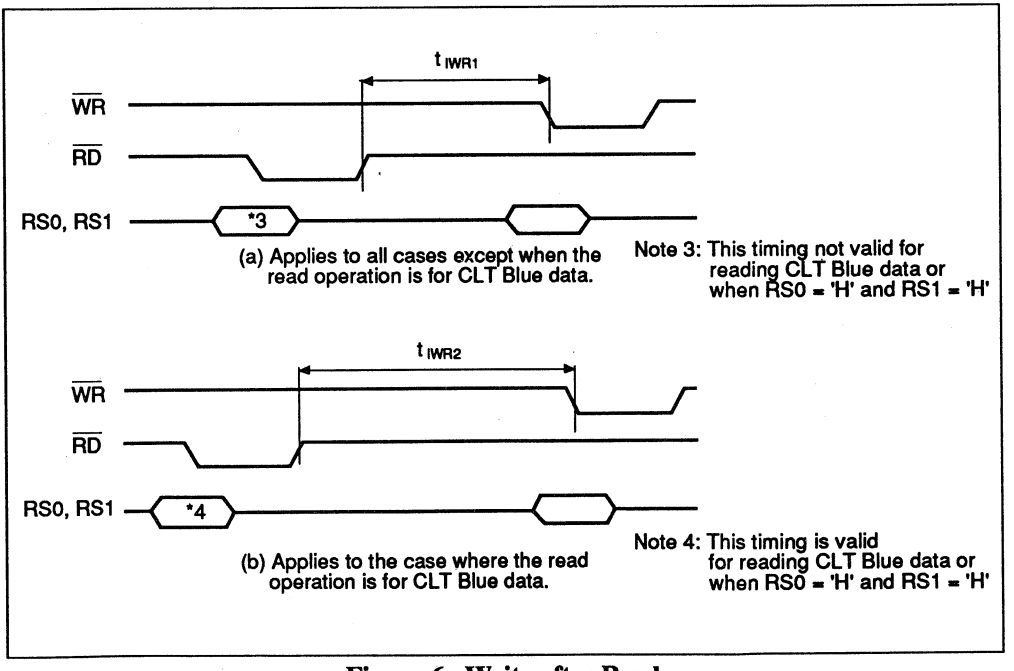
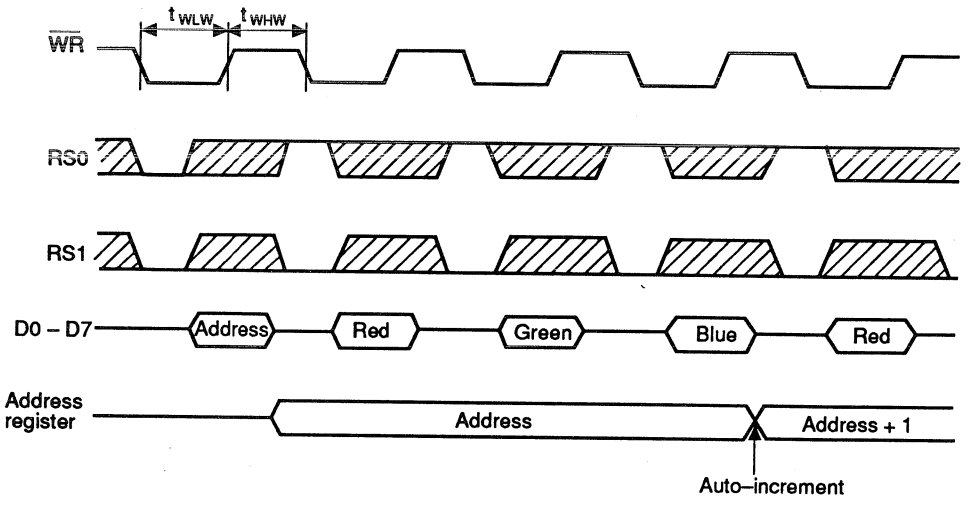
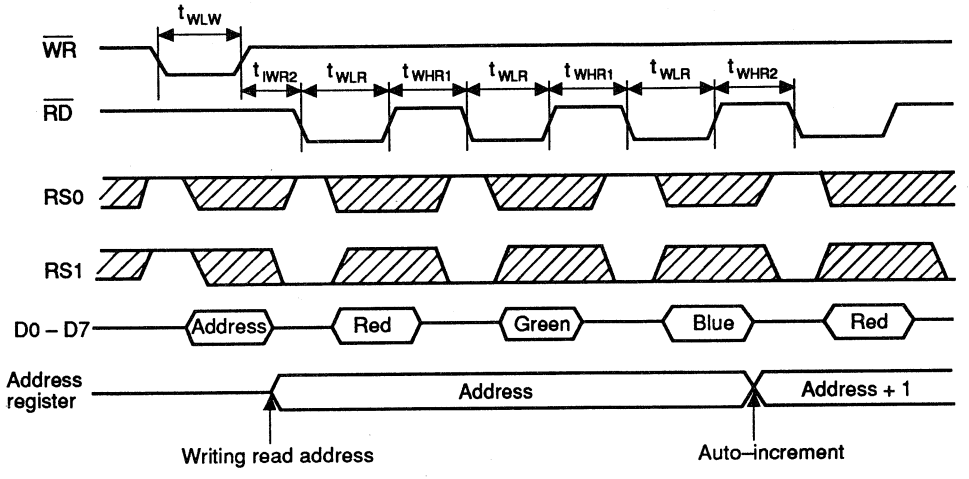


Figure 6 Write after Read



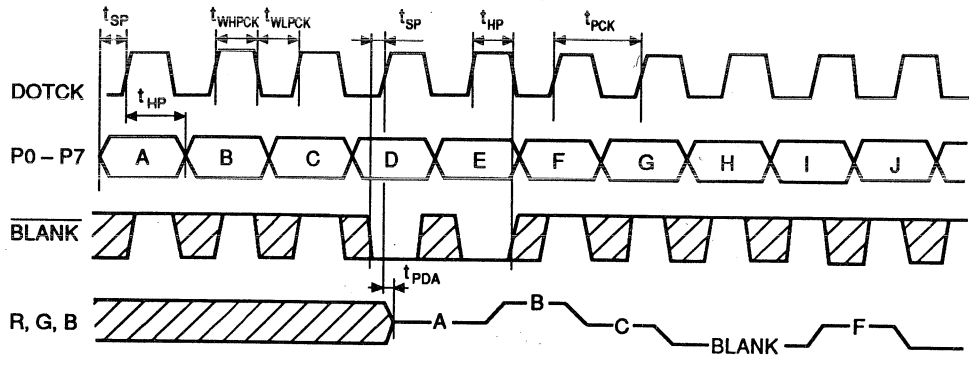
1. Write the CLT address to the address register.
2. Write the data (NRZ format) in the order red, green, then blue to D0 to D5. This R, G, and B data forms an 18-bit word that is written to the CLT.
3. When the R, G and B data writes are completed, the address is automatically incremented by 1 and the next data set can be applied again in RGB order. All subsequent CLT data writes should continue in this manner.

Figure 7 CLT Write



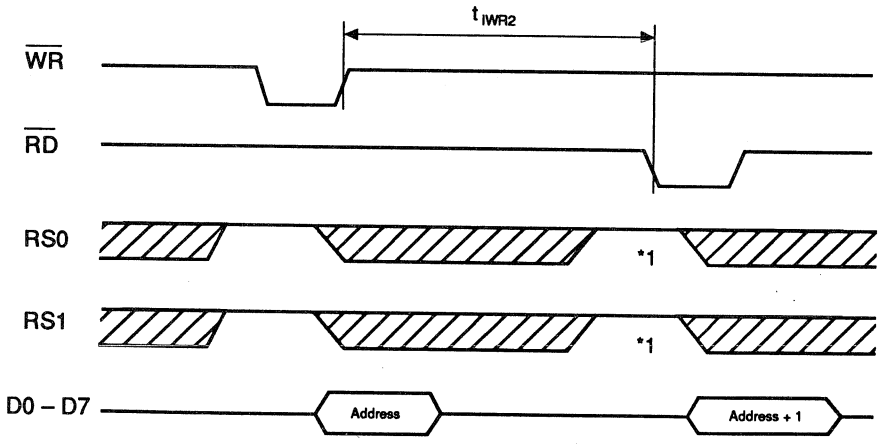
1. Write CLT address to the address register.
2. With each strobe of the RD line, CLT data can be read in the order red, green and blue at D0 to D5.
3. When the blue data read is completed, the address is automatically incremented and the CLT data for that address can then be read in the order of R, G and B.

Figure 8 CLT Read



Video output is generated when a CLT data location is selected by the address input at P7 to P0 and subsequently output as analog RGB signals. The video output lags behind the PCLK strobe of its corresponding address at P7 to P0 by three PCLK clock periods.

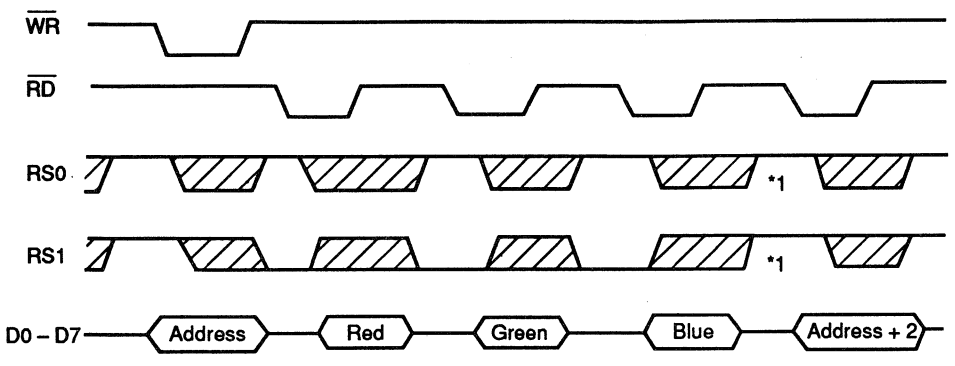
Figure 9 Video Output



1. Use $\overline{WR}$ to select the address register and to write the CLT read address.
2. Use RD to read the contents of the address register. At this time, the contents of the address register is incremented by 1.

Note *1: The address register can also be read when RS0 and RS1 are both set to 'L'.

Figure 10 Address Register Read (1)



1. Use $\overline{WR}$ to select the address register and to write the CLT address.
2. Use $\overline{RD}$ three times in succession to read CLT data in the order red, green and blue.
3. Using $\overline{RD}$ again will read the contents of the address register. This read of the address register plus the previous read of red, blue and green data will increment the contents of the address register by 2.

Note *1: The address register can also be read when RS0 and RS1 are both set to 'L'.

Figure 11 Address Register Read (2)

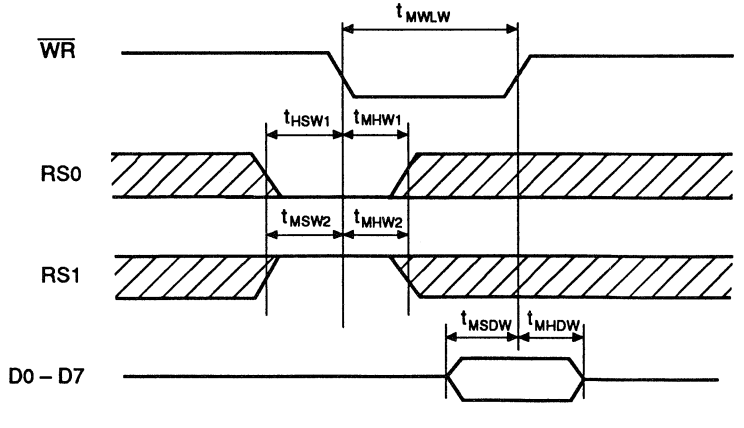


Figure 12 Pixel Mask Register Write

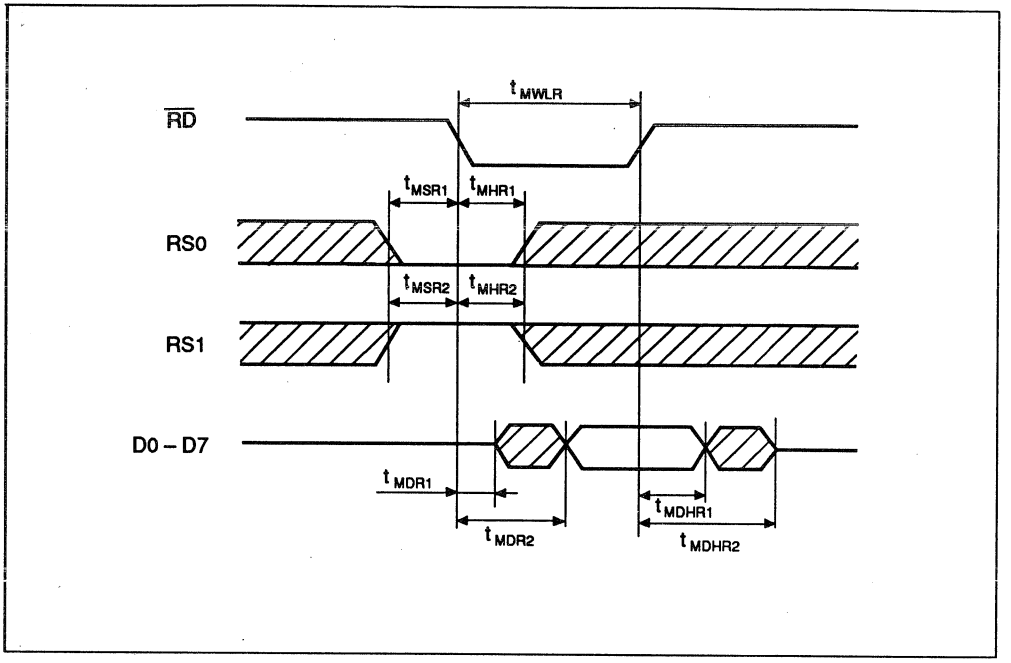


Figure 13 Pixel Mask Register Read

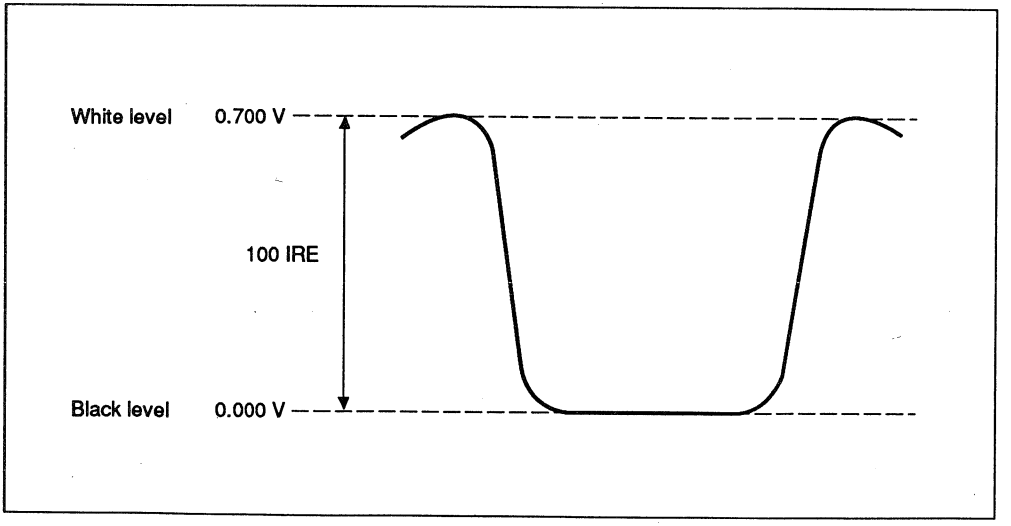


Figure 14 Video Output Waveform

Registers Correspondence with the CLT

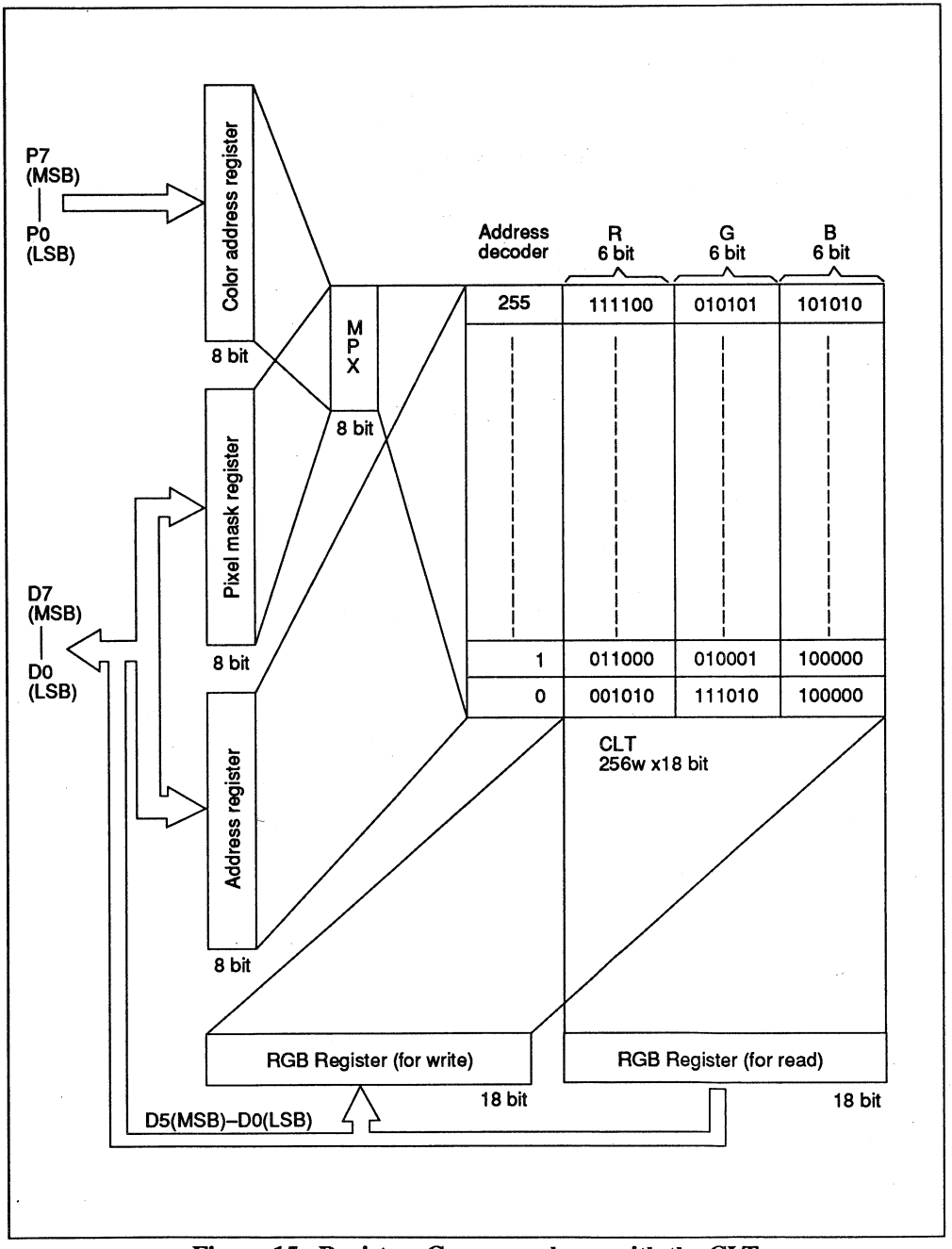


Figure 15 Registers Correspondence with the CLT

System Configuration Example

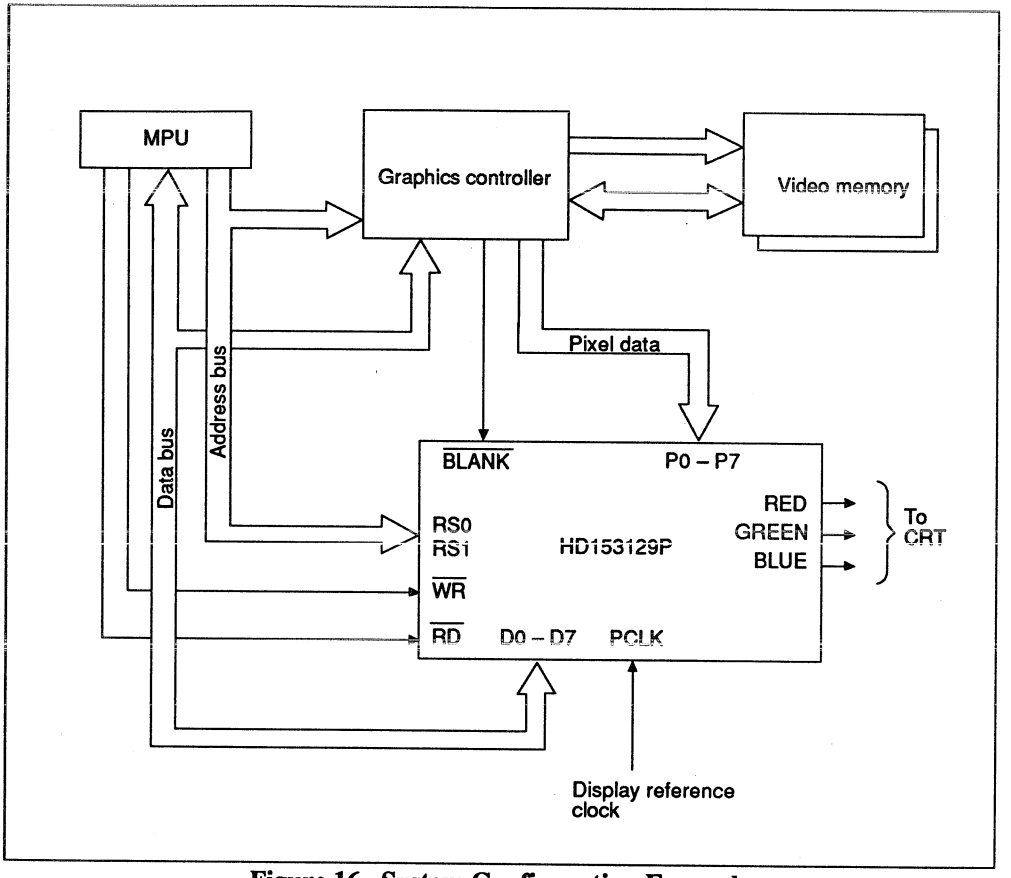


Figure 16 System Configuration Example

Table 4 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	0 to V_{CC}	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +150	°C

Electrical Characteristics

Table 5 DAC Section Electrical Characteristics (V_{CC} = 5 V, Ta = 25 °C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		6	6	6	bits	
Maximum operating frequency	f_{CLK}	—	—	50/65	MHz	
Analog output voltage	V_A (Full)	–5	—	5	% of FSR	
I_{REF} = –4.44 mA	V_A (Zero)	–2	—	2	% of FSR	
Differential linearity	DLE	–1	—	+1	LSB	
Integral linearity	ILE	–1	—	+1	LSB	
Output rise time (20 – 80 %)	tr	—	—	10	ns	C_L = 15 pF
Output fall time (80 – 20 %)	tf	—	—	10	ns	C_L = 15 pF
Settling time	ts	—	—	30	ns	C_L = 15 pF
Glitch energy	E_G	—	90	—	PVS	

Table 6 Digital Section DC Characteristics
(unless otherwise specified V_{CC} = 5 V ± 5 %, Ta = 0 to +70 °C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input "High" level voltage	V_{IH}	2.2	—	V_{CC}	V	
Input "Low" level voltage	V_{IL}	–0.3	—	0.8	V	
Input clamp voltage	V_I	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA
Output "High" level voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, I_{OH} = –400 µA
Output "Low" level voltage	V_{OL}	—	—	0.5	V	V_{CC} = 4.75 V, I_{OL} = 8 mA
Input current	I_I	—	—	1	mA	V_{CC} = 5.25 V, V_I = 5.5 V
"High" level input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
"Low" level input current	I_{IL}	—	—	–400	µA	V_{CC} = 5.25 V, V_I = 0.4 V
Supply current	I_{CC}	—	110	170	mA	V_{CC} = 5.25 V, I_{REF} = –4.44 mA

Table 7 Digital Section AC Characteristics (V_{CC} = 5 V, Ta = 25 °C)

		50 MHz		65 MHz				Reference
Item	Symbol	Min	Max	Min	Max	Unit	Test conditions	figure
PCLK cycle time	t_{PCK}	20	—	15.3	—	ns		9
PCLK low level time	t_{WLPCK}	8	—	6	—	ns		9
PCLK high level time	t_{WHPCK}	8	—	6	—	ns		9
Data setup time	t_{SP}	6	—	5	—	ns		9
Data hold time	t_{HP}	6	—	5	—	ns		9
Data output delay time	t_{PDA}	—	30	—	30	ns	C_L = 15 pF	9
$\overline{WR}$ low level time	t_{WLW}	50	—	50	—	ns		3, 7, 8
$\overline{WR}$ high level time	t_{WHW}	3 x t_{DCK}	—	3 x t_{DCK}	—	ns		7
$\overline{RD}$ low level time	t_{WLR}	50	—	50	—	ns		4, 8
$\overline{RD}$ high level time	t_{WHR1}	3 x t_{DCK}	—	3 x t_{DCK}	—	ns		8
	t_{WHR2}	6 x t_{DCK}	—	6 x t_{DCK}	—	ns		8

Unit mm (inch)

Digital Section AC Characteristics (V_{CC} = 5 V, Ta = 25 °C) (cont)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Test conditions	Reference figure
$\overline{WR}/\overline{RD}$ interval time	t_{IWR1}	3 x t_{DCK}	—	3 x t_{DCK}	—	ns		5, 6
	t_{IWR2}	6 x t_{DCK}	—	6 x t_{DCK}	—	ns		5, 6, 8, 9
$\overline{WR}$/RS0, RS1 setup time	t_{SW}	10	—	10	—	ns		3
$\overline{WR}$/RS0, RS1 hold time	t_{HW}	10	—	10	—	ns		3
$\overline{RD}$/RS0, RS1 setup time	t_{SRR}	10	—	10	—	ns		4
$\overline{RD}$/RS0, RS1 hold time	t_{HRR}	10	—	10	—	ns		4
$\overline{WR}$ data setup time	t_{SDW}	10	—	10	—	ns		3
$\overline{WR}$ data hold time	t_{HDW}	10	—	10	—	ns		3
$\overline{RD}$ data output delay time	t_{DDR1}	5	—	5	—	ns	C_L = 15 pF	4
	t_{DDR2}	—	40	—	40	ns	C_L = 15 pF	4
$\overline{RD}$ data output hold time	t_{HDR1}	5	—	5	—	ns	C_L = 15 pF	4
	t_{HDR2}	—	20	—	20	ns	C_L = 15 pF	4
$\overline{WR}$ low level time	t_{MWLW}	50	—	50	—	ns		12
$\overline{RD}$ low level time	t_{MWLR}	50	—	50	—	ns		13
$\overline{WR}$/RS0, RS1 setup time	t_{MSW1}	10	—	10	—	ns		12
	t_{MSW2}	10	—	10	—	ns		12
$\overline{WR}$/RS0, RS1 hold time	t_{MHW1}	10	—	10	—	ns		12
	t_{MHW2}	10	—	10	—	ns		12
$\overline{RD}$/RS0, RS1 setup time	t_{MSR1}	10	—	10	—	ns		13
	t_{MSR2}	10	—	10	—	ns		13
$\overline{RD}$/RS0, RS1 hold time	t_{MHR1}	10	—	10	—	ns		13
	t_{MHR2}	10	—	10	—	ns		13
$\overline{WR}$ data setup time	t_{MSDW}	10	—	10	—	ns		12
$\overline{WR}$ data hold time	t_{MHDW}	10	—	10	—	ns		12
$\overline{RD}$ data output delay time	t_{MDR1}	5	—	5	—	ns	C_L = 15 pF	13
	t_{MDR2}	—	40	—	40	ns	C_L = 15 pF	13
$\overline{RD}$ data output hold time	t_{MDHR1}	5	—	5	—	ns	C_L = 15 pF	13
	t_{MDHR2}	—	20	—	20	ns	C_L = 15 pF	13

Connection Example

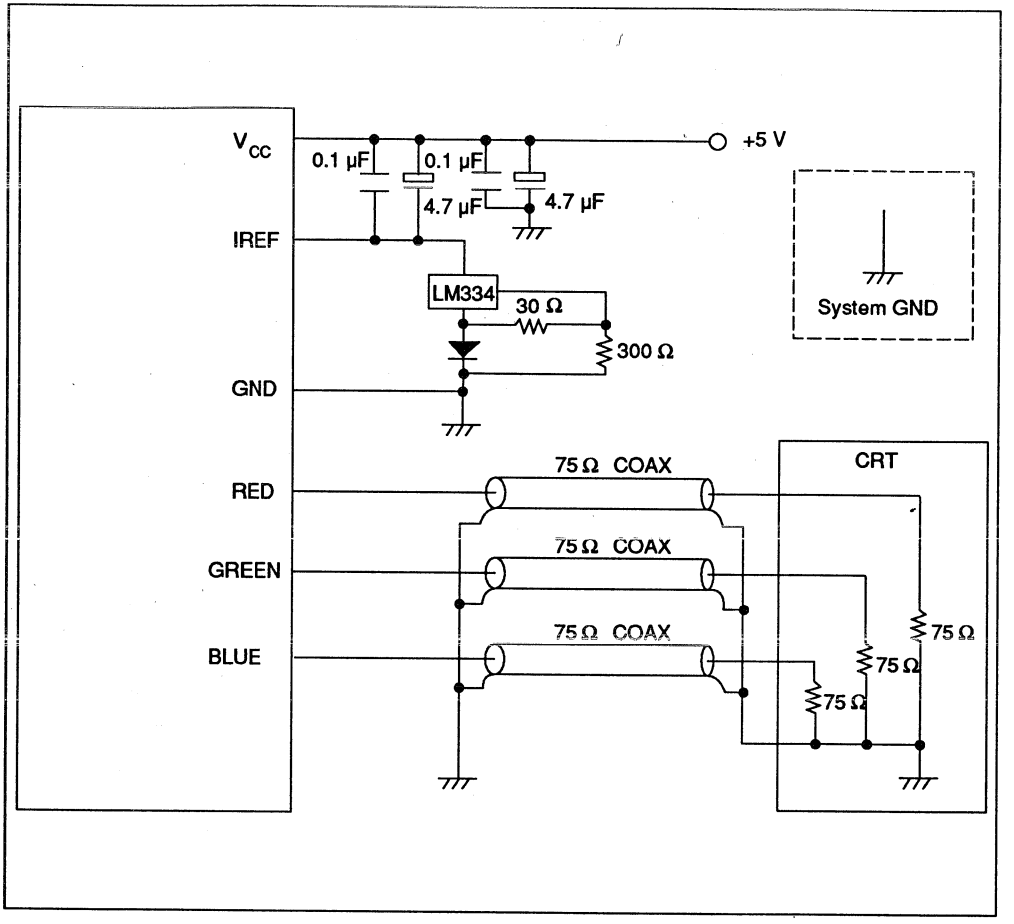


Figure 17 Connection Example

Document Image Processor

HD63084

Document Image Pre Processor (DIPP)

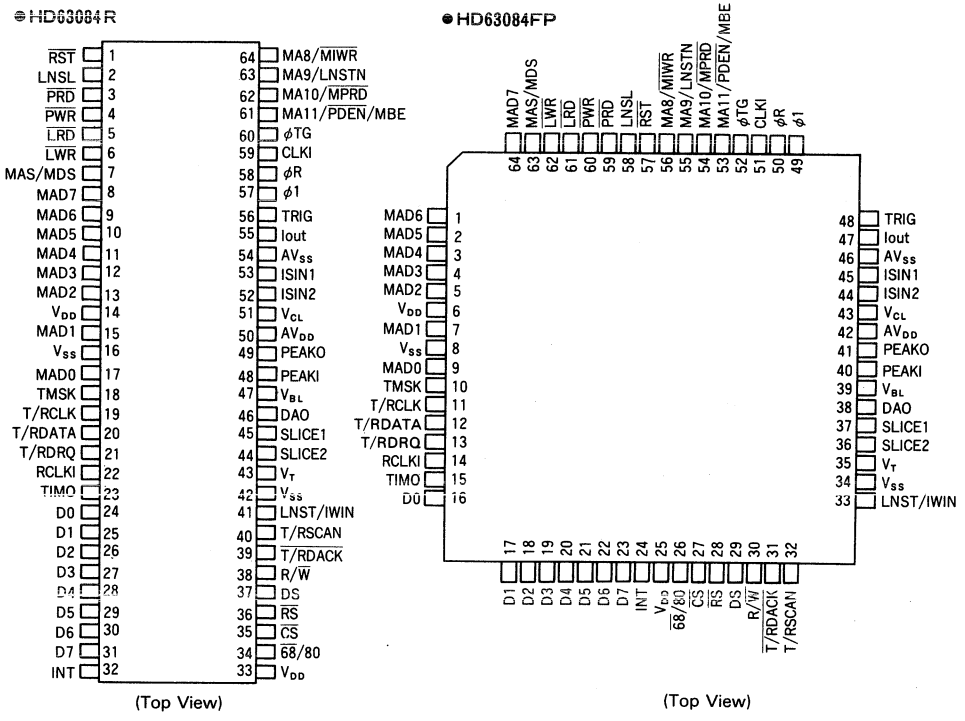
DIPP can read image signals coming from the line sensor of a facsimile apparatus or an image scanner at 5 M pels*/second, and after correcting for shading distortion, converts them into digital signals. Pel correction is to within a highly precise ±1%. While 4-bit coded data output, dithered data output and binary data output, which are set arbitrarily, it can be applied to very high speed, high precision systems.

* :The term 'picture element' is abbreviated to 'pel' in this document.

Features

- High speed reading of image signals
  The DIPP can read image signals with a speed of up to 5 M pels per second (when the input clock frequency is 10 MHz). This speed is 5 times faster than that of the VPP.
- Highly accurate processing of image signal
  —The peak to peak voltage of input image signals ranges from 0.1 V to 2 V. The highest permissible voltage of the input image signal is VDD, which is, however, clamped to 2 V in the internal sample and hold circuit.
  —The DIPP includes a peak value detection circuit with resolution of 8 bits, 7-bit successive approximation A/D and D/A converters, a 4-bit flash A/D converter, a 4-bit D/A converter and a shading wave RAM to perform highly accurate correction of distortion.
  —The DIPP can perform distortion correction for each pel with a resolution of 1% using an external pel correction RAM.
- Various digitization modes
  The DIPP has three modes to digitize read image data: binary coding, dithered coding and 4-bit coding.
  Binary coding: Converts the read signal to 1 or 0 by using a slice level selected by the user.
  Dithered coding: Generates 16 gradations of dummy halftones by using a 4 × 4 dither pattern specififed by the user.
  4-bit coding: Generates 16 gradations of real halftones in the format of 4 bits per pel.
- Wide range of programmable reduction of magnification ratios
  The DIPP can reduce image data in read (T) mode. The reduction ratio is programmable in about 1000 increments from 0.125 to 1.
  The DIPP can magnify image data in receive (R) mode. The magnification ratio is programmable in about 1000 increments from 1 to 8.
- Automatic determination of vertical resolution
  The DIPP counts the amount of changing pels along a scan line or between two scan lines. The result of the counting appears in a flag bit of the internal status register. In response to the status of this flag bit, the user can have the DIPP perform vertical resolution conversion, which allows shortening of the data transmit time.
- Burst DMA transfer of image data
  By using the line memory, the DIPP can transfer a line of digitized data at a stretch in burst DMA mode. This function allows the DIPP to be used in ultra high speed systems.
- Internal sensor interface
  The DIPP incorporates a sample and hold circuit which is directly connected to the sensor via coupling capacitor. This LSI also incorporates the sensor timing generator which generates control signals for the sensors.
- Package
  —64 pin plastic shrink DIP (DP-64S)
  —64 pin plastic QFP (FP-64A)

Pin Arrangement



1. 44 to 55: These are analog pins.
2. No lines should be connected to pin 43.

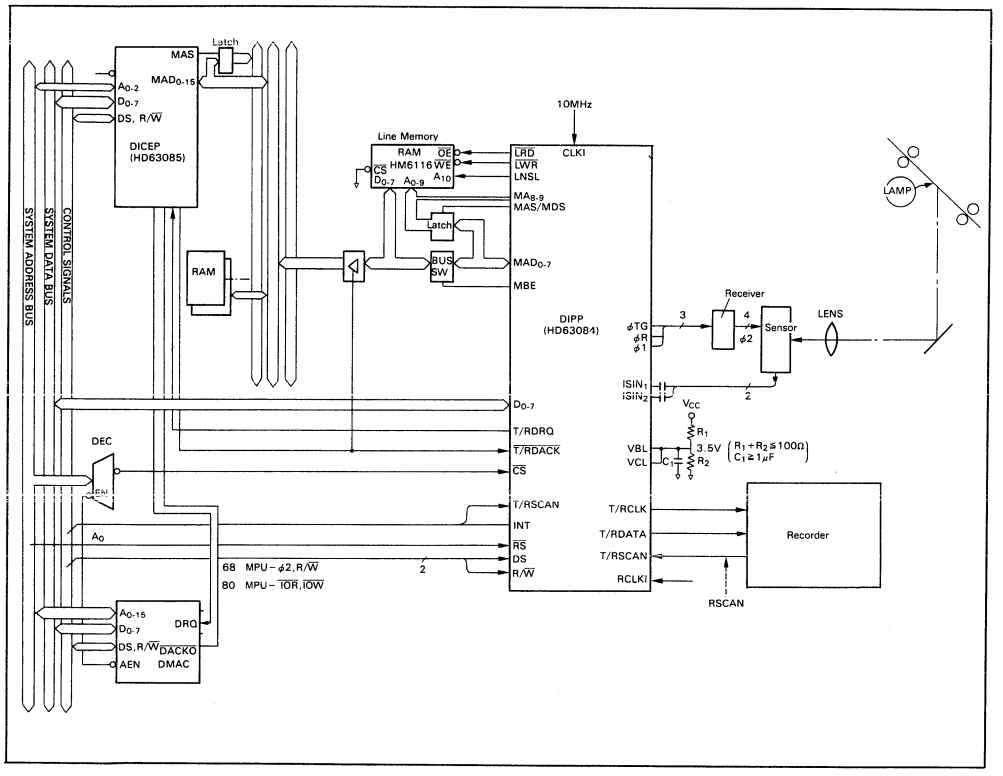
1. 36 to 47: These are analog pins.
2. No lines should be connected to pin 35.

Specifications

Item		Specifications
Input Clock frequency		1 MHz to 10 MHz
Image signal reading frequency (Operating frequency)		500 kHz to 5 MHz
Input image signal Vp-p		0.1 to 2.0 V
Shading distortion correcting range		70% of signal peak
Scan line length		64 to 5,280 pels
Sensor driving cycle		8,125 clocks per image signal clock
Half tone		16 gradations
Dithered pattern		4 × 4 dithered matrix
Horizontal resolution conversion (reduction & magnification)		0.125 to 8.00 times
Maximum DMA data transfer speed		System bus ..... 0.625 M Byte/sec Memory bus ..... 5 M Byte/sec
Serial data transfer speed		5 M-bit/sec
Interruption of MPU		· At completion of writing the shading waveform detection period · At completion of reading a scan line of image data to the external line memory
Supply voltage		5 V ± 5%
Power consumption		300 mW (Max)
Package	HD63084R	DP-64S
	HD63084FP	FP-64A

System Configuration

The following paragraphs provide a description of the pin functions.



Power Supply Pins

Table summarizes power supply pins.

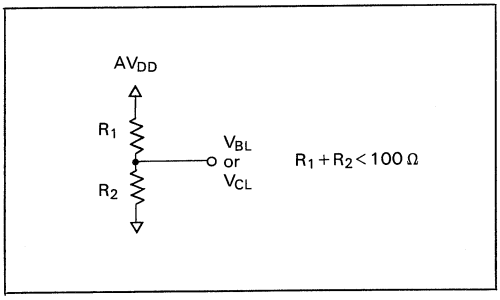
V_{DD}, V_{SS}
Power is supplied to all internal logic circuits using these two pins.
V_{DD} is power (+5 V ±5%) and V_{SS} is ground (V_{SS} = 0 V).

AV_{DD}, AV_{SS}
Power is supplied to all internal analog circuits using these two pins.
AV_{DD} is power (+5 V ±5%) and AV_{SS} is ground (AV_{SS} = 0 V).

V_{BL}, V_{CL}
These pins are used to supply external voltage references (black level) of video signals for the DIPP ISIN1 and ISIN2 inputs.
V_{BL} input is the voltage of the absolutely black level of the sensor output signals. Its recommended value is 3.5 V. (The allowable range is 2.0 V ≤ V_{BL} ≤ AV_{DD}.)
V_{CL} input is the voltage to which the sensor output signals are clamped in the sample and hold circuit.

V_T
No line should be connected to this pin.

				Pin Number	
Mnemonic	**Input/Output**	**Active State**	**Three State**	**DP-64S**	**FP-64A**
V_{DD}	Power Supply	—	—	14, 33	6, 25
V_{SS}	Power Supply	—	—	16, 42	8, 34
AV_{DD}	Power Supply	—	—	50	42
AV_{SS}	Power Supply	—	—	54	46
V_{BL}	Power Supply	—	—	47	39
V_{CL}	Power Supply	—	—	51	43
V_T	Open	—	—	43	35



MPU Interface Pins

Table Summarizes the MPU inteface pins

D0-D7 (input/output)
Data bus pins. These pins are connected to the system data bus to provide bidirectional data transfer between the MPU system and the DIPP.

$\overline{68}$/80 (input)
MPU select pin. When the $\overline{68}$/80 input is low, a 68 type MPU can be interfaced with the DIPP.

$\overline{CS}$ (input)
Chip select pin. A low level on the $\overline{CS}$ input indicates that the MPU can access a DIPP internal register. The $\overline{CS}$ input and the $\overline{T/RDACK}$ input must not be pulled low together.

$\overline{RS}$ (input)
Register select pin. This pin is used for selecting the register to be accessed by the MPU.

DS (input)
Data strobe pin. The function of this pin depends on the status of the $\overline{68}$/80 input.

R/$\overline{W}$ (input)
Read/Write pin. The function of this pin depends on the status of the $\overline{68}$/80 input.

$\overline{RST}$ (input)
Reset pin. When the $\overline{RST}$ input is driven low, the DIPP internal circuits are placed in the following states.

INT (output)
Interrupt request pin. The DIPP drives the INT output high to send an interrupt request to the MPU.

T/RSCAN (input)
Read (T) mode or receive (R) mode operation start pin. T/RSCAN input causes the DIPP to begin read (T) mode or receive (R) mode operations.

					Pin Number	
Pin Name	**Mnemonic**	**Input/Output**	**Active State**	**Three State**	**DP-64S**	**FP-64A**
Data Bus	D0-D7	Input/Output	High	Yes	24 to 31	16 to 23
MPU Select	$\overline{68}$/80	Input	A - Low, B - High	No	34	26
Chip Select	$\overline{CS}$	Input	Low	No	35	27
Register Select	$\overline{RS}$	Input	Low	No	36	28
Data Strobe	DS	Input	A - High, B - Low	No	37	29
Read/Write	R/$\overline{W}$	Input	A - read-High, write-Low, B - Low	No	38	30
Reset	$\overline{RST}$	Input	Low	No	1	57
Interrupt Request	INT	Output	High	No	32	24
Read (T) Mode/Receive (R) Mode Operation Start	T/RSCAN	Input	Read — High, Receive — Low	No	40	32

A ..... 68 type LSI
B ..... 80 type LSI
Read ..... Read mode
Receive ..... Receive mode

DMAC Interface Pins

Table summarizes DMAC interface pins.

T/RDRQ (output)
DMA request pin. By driving T/RDRQ output high, the DIPP can request the DMA controller (DMAC) to perform a DMA transfer of data.
The function of the T/RDRQ output depends on the status of T/R bit in the R00 register and BST bit in the R01 register.

$\overline{\text{T/RDACK}}$ (input)
DMA acknowledge input pin. This input is a response to T/RDRQ output. When a 68 type MPU is used, the DIPP recognizes the status of R/W input reversely while the $\overline{\text{T/RDACK}}$ input is low.

Clock Input Pins

Table summarizes clock input pins.

CLKI (input)
Clock input pin. This CLKI input acts as a fundamental clock in read (T) mode. Input clock frequency should be in the range from 1 MHz to 10 MHz with a duty cycle of 50%.

RCLKI (input)
Receive mode clock input pin. This RCLKI input acts as a fundamental clock in receive (R) mode. The DIPP extracts clocks required for a serial transfer to the recorder from the RCLKI inputs, and outputs the extracted clocks as RCLK via the T/RCLK pin. Input clock frequency should be in the range from 500 kHz to 5 MHz with a duty cycle of 50%.

					Pin Number	
Pin Name	**Mnemonic**	**Input/Output**	**Active State**	**Three State**	**DP-64S**	**FP-64A**
DMA Request	T/RDRQ	Output	High	No	21	13
DMA Acknowledge Input	$\overline{\text{T/RDACK}}$	Input	Low	No	39	31

					Pin Number		
Pin Name	**Mnemonic**	**Input/Output**	**Active State**	**Three State**	**DP-64S**	**FP-64A**	**When not used**
Clock Input	CLKI	Input	High	No	59	51	—
Receive Mode Clock Input	RCLKI	Input	High	No	22	14	*

* No lines should be connected to this pin.

CCD Image Sensor Interface Pins

Table summarizes the CCD image sensor interface pins.

ϕTG (output)
Transfer gate pulse output pin. When the ϕTG output is high, the transfer gate of the CCD image sensor is open.

ϕ1 (output)
CCD driving clock output pin. This pin outputs the clock which drives the CCD image sensor.

ϕR (output)
Sensor output reset clock output pin. This pin outputs the clock which resets the output of the CCD image sensor.

ISIN1 (input)
Image signal input pin 1. This pin acts as input of the CCD image sensor analog output signal.

ISIN2 (input)
Image signal input pin 2. The CCD image sensor analog output signals are input to both the ISIN1 and ISIN2 pins when the DIPP uses two sensor output channels.

IOUT (output)
Image signal output pin. This pin outputs the analog signal which is obtained by smoothing ISIN1 or ISIN2 inputs in the sample and hold circuit.

Pin Name	Mnemonic	Input/ Output	Active State	Three State	Pin Number DP-64S	Pin Number FP-64A	When not used
Transfer Gate Pulse	ϕTG	Output	High	No	60	52	—
CCD Driving Clock Output	ϕ1	Output	High	No	57	49	—
Output Amplifier Reset Clock Output	ϕR	Output	High	No	58	50	—
Image Signal Input 1	ISIN1	Input	High	No	53	45	—
Image Signal Input 2	ISIN2	Input	High	No	52	44	*
Image Signal Output	IOUT	Output	High	No	55	47	*

* No lines should be connected to this pin.

A/D Conversion Pins

Table summarizes the A/D conversion pins.

PEAKO (output)
Peak value output pin. This pin outputs the peak value of image signal referenced to V_{BL}.

PEAKI (input)
Peak value input pin. This pin is used to external input the peak value of image signal which will be input to the 7-bit A/D and D/A converters.

DAO (output)
Shading waveform output pin. This pin outputs a shading waveform regenerated by the 7-bit D/A converter. This pin provides an internal unity gain amplifier, which allows for a very low output impedance.

SLICE1 (input)
Slice level reference input pin for edge emphasis 1.

SLICE2 (input)
Slice level reference input pin for edge emphasis 2.

Internal Timer Pins

Table summarizes the internal timer pins.

TRIG (input)
Timer trigger input pin. ϕTRIG input is used to extend the duration of the internal timer counting or to drive the internal timer synchronously with an external timer.

TIMO (output)
Timer output pin. This pin outputs the counting value of the internal timer.

TMSK (output)
Transfer mask gate pin. This pin is used to advise the MPU of the DIPP internal state.

LNST/IWIN (output)
LNST/IWIN output pin. This pin is used to advise the MPU of the DIPP internal state.

Pin Name	Mnemonic	Input/ Output	Active State	Three State	Pin Number DP-64S	Pin Number FP-64A	When not used
Peak Value Output	PEAKO	Output	High	No	49	41	—
Peak Value Input	PEAKI	Input	High	No	48	40	*
Shading Waveform Output	DAO	Output	High	No	46	38	—
Slice Level Reference Input for Edge Emphasis 1	SLICE1	Input	High	No	45	37	*
Slice Level Reference Input for Edge Emphasis 2	SLICE2	Input	High	No	44	36	*

* No lines should be connected to this pin.

Pin Name	Mnemonic	Input/Output	Active State	Three State	Pin Number DP-64S	Pin Number FP-64A
Timer Trigger Input	TRIG	Input	High	No	56	48
Timer Output	TIMO	Output	High	No	23	15
Transfer Mask Gate	TMSK	Output	High	No	18	10
LNST/IWIN Output	LNST/IWIN	Output	High	No	41	33

Serial Interface Pins

Table summarizes the serial interface pins.

T/RDATA (output)
Serial data output pin. This pin outputs data which is serially transferred to the recorder (e.g. printers).

T/RCLK (output)
Serial clock output pin. This pin outputs a clock signal used to latch serial data output from the T/RDATA pin.

Memory Bus Interface Pins

Table summarizes the memory bus interface pins.

MAD0 TO MDA7 (I/O)
Memory address/data bus pins. These pins are interfaced with the 8-bit memory bus to provide bidirectional communication between the DIPP and the external RAM (pel correction RAM or line memory).

MAS/MDS (output)
Memory address strobe and memory data strobe output pin. The negative edge of MAS/MDS is used to latch the address or data which is output from MAD0 through MAD7 pins.

$\overline{\text{LWR}}$ (output)
Line memory write enable pin. The positive edge of $\overline{\text{LWR}}$ output is used to enable writing of data into the line memory.

Pin Name	Mnemonic	Input/ Output	Active State	Three State	Pin Number DP-64S	Pin Number FP-64A	When not used
Serial Data Output	T/RDATA	Output	High	No	20	12	*
Serial Clock Output	T/RCLK	Output	High	No	19	11	*

* No lines should be connected to this pin.

Pin Name	Mnemonic	Input/ Output	Active State	Three State	Pin Number DP-64S	Pin Number FP-64A	When not used
Memory Address/Data Bus	MAD0 to MAD7	Input/ Output	High	Yes	17, 15, 13, 12, 11, 10, 9, 8	9, 7, 5, 4, 3, 2, 1, 64	*
Memory Address Strobe and Memory Data Strobe Output	MAS/MDS	Output	High	No	7	63	*
Line Memory Write Enable	$\overline{\text{LWR}}$	Output	Low	No	6	62	*
Line Memory Read Enable	$\overline{\text{LRD}}$	Output	Low	No	5	61	*
Scan Line Select	LNSL	Output	—	No	2	58	*
Pel Correction RAM Write Enable	$\overline{\text{PWR}}$	Output	Low	No	4	60	*
Pel Correction RAM Read Enable	$\overline{\text{PRD}}$	Output	Low	No	3	59	*
Memory Address 8/4-bit Coded Data Write Enable	MA8/$\overline{\text{MIWR}}$	Output	MA8-High, $\overline{\text{MIWR}}$-Low	No	64	56	*
Memory Address 9/Line Start Notification	MA9/LNSTN	Output	High	No	63	55	*
Memory Address 10/pel Correction Data Read	MA10/$\overline{\text{MPRD}}$	Output	MA10-High, $\overline{\text{MPRD}}$-Low	No	62	54	*
Memory Address 11/Pel Data Enable/Memory Bus Enable	MA11/$\overline{\text{PDEN}}$/ MBE	Output	MA11-High, $\overline{\text{PDEN}}$-Low, MBE-High	No	61	53	*

* No lines should be connected to this pin.

$\overline{\text{LRD}}$ (output)
Line memory read enable pin. When the $\overline{\text{LRD}}$ output is low, either the horizontal-resolution-converted data or 4-bit coded data can be read from the line memory.

LNSL (output)
Scan line select pin. The LNSL output is a control signal which selects the address area of the line memory to read or write horizontal-resolution-converted data or 4-bit coded data.

$\overline{\text{PWR}}$ (output)
Pel correction RAM write enable pin. A positive edge of the $\overline{\text{PWR}}$ output enables the pel correction data to be written to the pel correction RAM.

$\overline{\text{PRD}}$ (output)
Pel correcton RAM read enable pin. A positive edge of the $\overline{\text{PRD}}$ output enables pel correction data to be read from the pel correction RAM.

MA8/$\overline{\text{MIWR}}$ (output)
Memory address 8/4-bit coded data write enable pin. The function of this output depends on the memory bus interface mode selected.

MA9/LNSTN (output)
Memory address 9/Line Start Notification pin.
The function of this pin depends on the memory bus interface mode selected.

MA10/$\overline{\text{MPRD}}$ (output)
Memory address 10/pel correction data read pin.
The function of this pin depends on the memory bus interface mode selected.

MA11/$\overline{\text{PDEN}}$/MBE (output)
Memory address 11/pel data enable/memory bus enable pin.
The function of this pin depends on the memory bus interface mode selected.

Registers

The DIPP contains an address register (AR), status register (SR), control registers (R01 to R1D) and DMA registers. All of these registers except for the DMA registers can be accessed by the MPU. The DIPP operates depending on the contents of these registers.

Reg. No.	$\overline{CS}$	$\overline{RS}$	Address Register 4	3	2	1	0	Name	R/W
—	0	0	—	—	—	—	—	Address Register	W
R00	0	1	0	0	0	0	0	Mode Select Register	R/W
R01	0	1	0	0	0	0	1	Work Enable Register	R/W
R02	0	1	0	0	0	1	0	SENS Starting Register	W
R03	0	1	0	0	0	1	1	SENS Ending Register	W
R04	0	1	0	0	1	0	0	IWIN Starting Register (H)	W
R05	0	1	0	0	1	0	1	IWIN Starting Register (L)	W
R06	0	1	0	0	1	1	0	PAPW Starting Register	W
R07	0	1	0	0	1	1	1	PAPW Ending Register	W
R08	0	1	0	1	0	0	0	Resolution Determination Register	W
R09	0	1	0	1	0	0	1	Resolution Determination/Sensor Type Register	W
R0A	0	1	0	1	0	1	0	Peak Value Limit Register	W
R0B	0	1	0	1	0	1	1	Slice Level Setting Register	W
R0C	0	1	0	1	1	0	0	γCorrection Resolution Register	W
R0D	0	1	0	1	1	0	1	m and k Parameter Register	W
R0E	0	1	0	1	1	1	0	l-Parameter Register (1)	W
R0F	0	1	0	1	1	1	1	l-Parameter Register (2)	W
R10	0	1	1	0	0	0	0	Dither Register (1)	R/W
R11	0	1	1	0	0	0	1	Dither Register (2)	R/W
R12	0	1	1	0	0	1	0	Dither Register (3)	R/W
R13	0	1	1	0	0	1	1	Dither Register (4)	R/W
R14	0	1	1	0	1	0	0	Dither Register (5)	R/W
R15	0	1	1	0	1	0	1	Dither Register (6)	R/W
R16	0	1	1	0	1	1	0	Dither Register (7)	R/W
R17	0	1	1	0	1	1	1	Dither Register (8)	R/W
R18	0	1	1	1	0	0	0	Horizontal Resolution Conversion Logic Register	W
R19	0	1	1	1	0	0	1	IWIN Ending Register (H)	W
R1A	0	1	1	1	0	1	0	IWIN Ending Register (L)	W
R1B	0	1	1	1	0	1	1	Peak Value Register	R/W
R1C	0	1	1	1	1	0	0	Initial Value Register	R
R1D	0	1	1	1	1	0	1	Shading Waveform Register	R/W
—	0	0	—	—	—	—	—	Status Register	R
—	1	—	—	—	—	—	—	DMA Read Register	*1
—	1	—	—	—	—	—	—	DMA Write Register	*1

*1: These registers are accessed by DMAC in cycle stealing DMA mode.

Block Diagram

Figure 1 shows the block diagram of the DIPP.

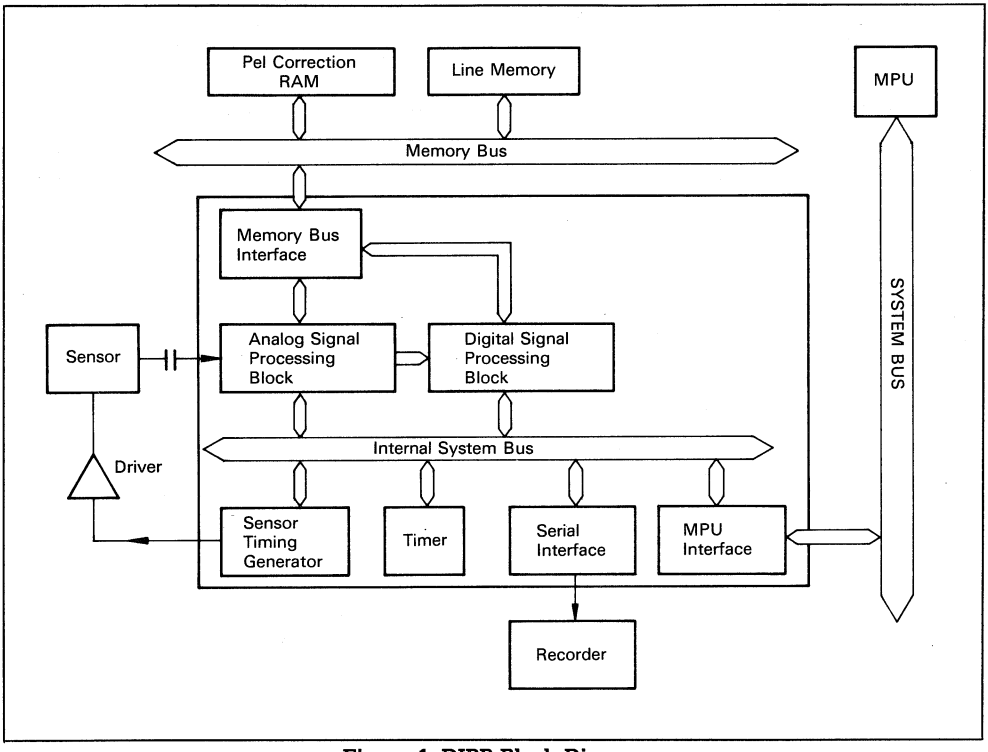


Figure 1 DIPP Block Diagram

Analog Signal Processing Block

Correction of distortion included in the image data coming from the sensor, and digitization of the corrected data.

Digital Signal Processing Block

1. Horizontal resolution conversion of digitized image data,
2. Automatic judgement of vertical resolution, and
3. Vertical resolution conversion of digitized image data.

The DIPP can reduce and magnify digitized data using horizontal resolution conversion or vertical resolution conversion.

Reduction is performed only in read (T) mode. The DIPP reduces the digitized data and transfers it to the MPU system, which allows the time required for transmitting the data to be shortened.

Magnification is performed in receive (R) mode. The DIPP can magnify the reduced data which has been transmitted via the internal system bus and transfers it to the recorder.

MPU Interface

The MPU interface allows the DIPP to be interfaceable with either a Motorola MPU or an Intel MPU. This block includes registers which can be directly accessed by the MPU.

Memory Bus Interface

The memory bus interface provides an interface between the DIPP and the memory bus.

Sensor Timing Generator

This block generates ϕTG, ϕ1 and ϕR signals which are used to drive the CCD image sensor.

Serial Interface

This block provides an interface between the DIPP and the recorder.

Timer

The DIPP internal timer is a programmable counter which is used to set the sensor drive cycles, that is, the ϕTG output cycle.

Function of DIPP

CCD image sensor or other optical sensing devices used in the image reading block of facsimiles generate shading distortion of data. The DIPP is used to solve this problem.

During reading of image data (that is, in read (T) mode), this LSI takes analog image data via a sensing device, corrects distortion included in the data, digitizes the corrected data, and then transfers the digitized data to the MPU system. The digitized data can be reduced before transferring the data to the MPU system.

When receiving image data via MODEM (that is, in receive (R) mode), the DIPP can also perform transfer of data from the MPU system to the recorder. The data can be magnified before being transferred.

The DIPP performs the above functions in response to the user's program.

Figure 2 shows the functions of the DIPP.

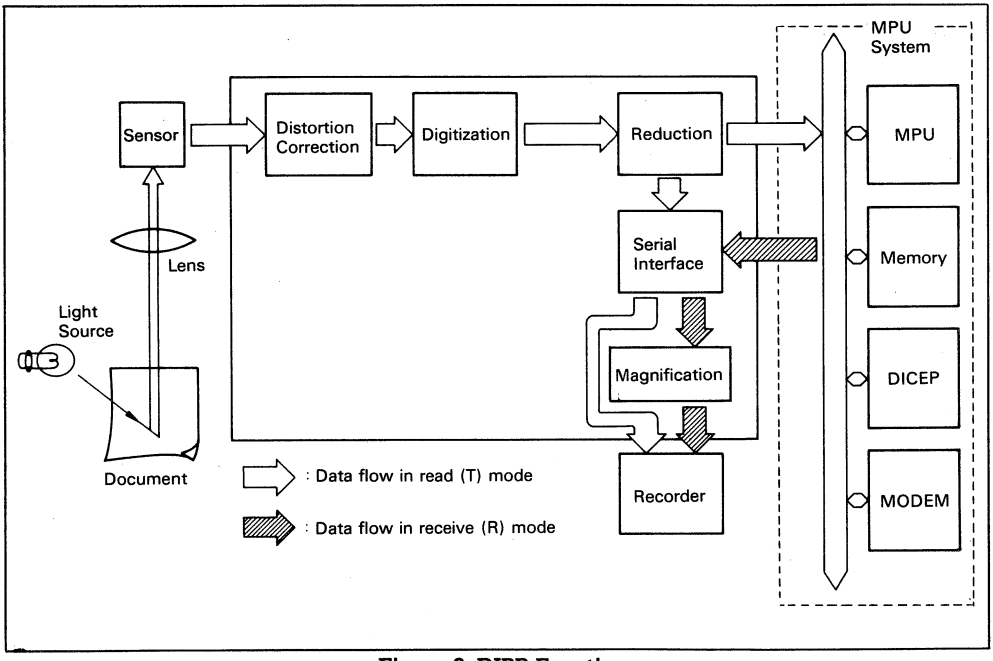


Figure 2 DIPP Function

Analog Signal Processing Block

The functions of this block are:

- Correction of distortion included in the image data coming from the sensor, and
- Digitization of the corrected data.

Figure 3 shows the configuration of the analog signal processing block.

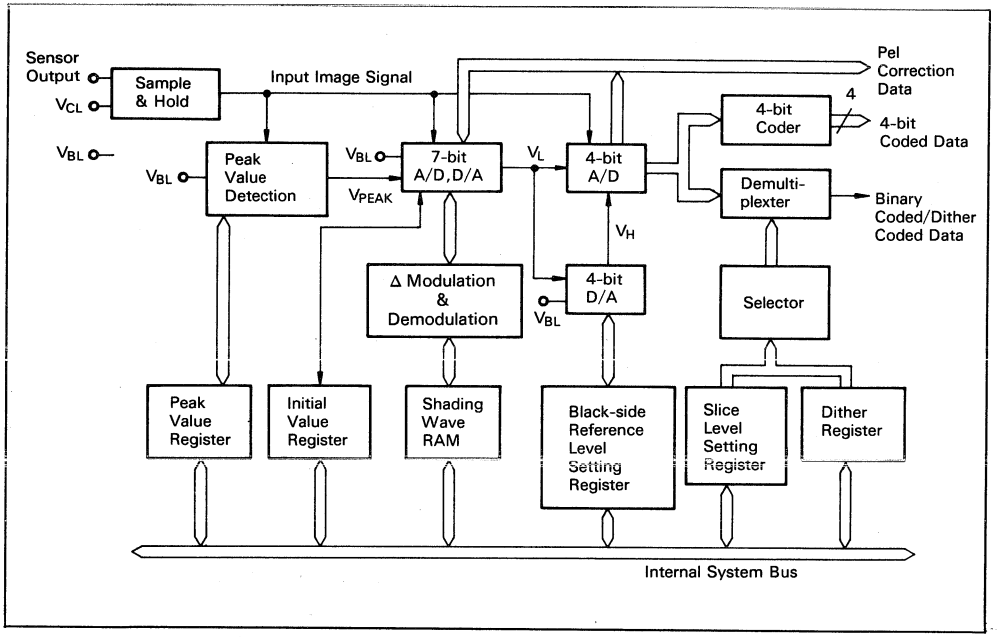


Figure 3 Analog Signal Processing Block Configuration

Sample and Hold Circuit

The sample and hold circuit clamps the black level (voltage of black pel) to V_{CL} and smoothes the waveform of the image signal coming from the sensor.

If image data representing white pels are input, this circuit generates a waveform shown in figure 4. V_{CL} is the clamp level and V_{BL} is the black level. In the DIPP, however, V_{CL} equals V_{BL}. When the DIPP is interfaced with a CCD sensor incorporating a sample and hold circuit, V_{CL} and V_{BL} of the DIPP must be equal to those of the CCD sensor.

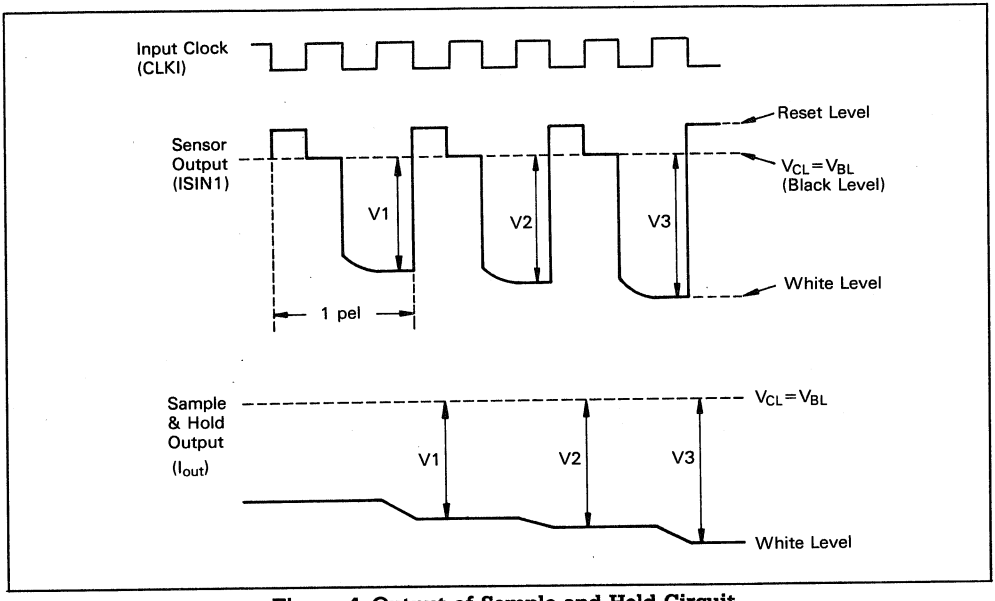


Figure 4 Output of Sample and Hold Circuit

Peak Value Detection Circuit

The image signals smoothed in the sample and hold circuit are input to the peak value detection circuit. This circuit detects and holds the peak value of the image signal. The voltage of the peak value is V_{PEAK}, which is used as the reference voltage for detecting and regenerating the shading waveform of the white image data.

The peak value is detected with 8-bit resolution (that is, in 256 increments) between V_{BL} and $V_{BL}-2.0$ V as shown in figure 5.

Figure 6 shows variation of the peak value (V_{PEAK}). The peak value detection circuit detects peak values while PAPW signal is high. When this signal is low, the peak value is shifted by 1 increment in the direction of the black level (V_{BL}) at every TG assertion. If the voltage of the sensor output signal becomes lower than V_{PEAK} when PAPW is high, V_{PEAK} follows the sensor output signal.

The MPU can obtain the peak value by reading the Peak Value register. In addition, the MPU can specify the peak value by writing to the Peak Value register.

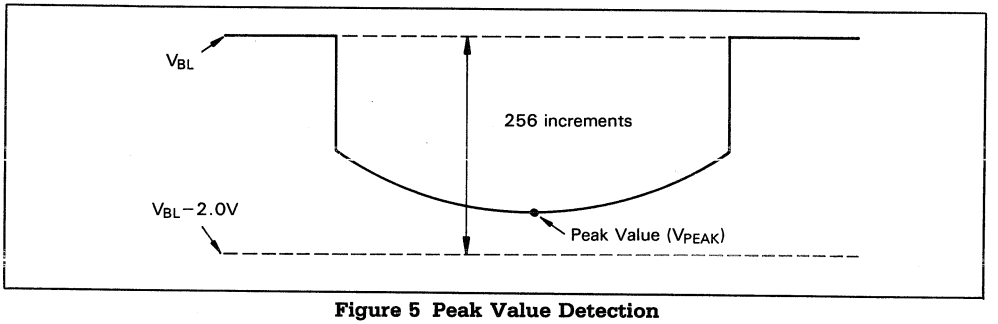


Figure 5 Peak Value Detection

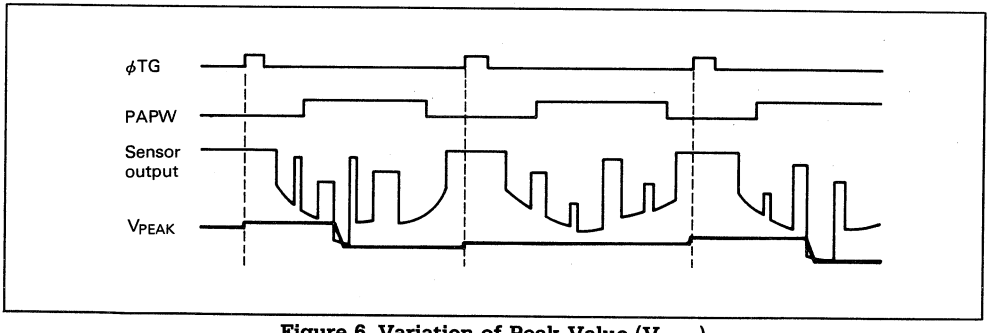


Figure 6 Variation of Peak Value (V_{PEAK})

7-bit A/D & D/A Converters

These converters detect and regenerate shading waveform of the white image data in the following order.

1. The initial value of the image data is detected by converting 70% of the difference between V_{BL} and the peak value to digital form with a resolution of 7 bits (that is, in 128 increments).
   The 1st cycle of the initial value detection period is initial value reset cycle, when the initial register is cleared to 0. At this time, the voltage at DAO (output of the 7-bit D/A converter) is equal to V_{PEAK}.
   From the 2nd cycle to the 23rd cycle, the voltage at DAO gradually nears the voltage of the initial value. Once the initial value is detected, the voltage at DAO is fixed as the voltage of the initial value.
2. The initial value is written into the Initial Value Register.
3. Referencing the initial value, these converters encode the changing volume per 16 pels or 32 pels to 4 bits via the Δ modulator (The least significant bit of the coded data which corresponds to the changing amount per 32 pels is masked).
4. A sign bit is added to the coded data and writes it to the shading wave RAM (5 bits 168 words). When the sign bit is 0, the shading waveform goes in the direction of black level. If 1, the shading waveform goes in the direction of white level. The sign bit plus the coded changing volume is called 'difference data'. (See figure 8.)
   The number of pels along a scan line is limited by the capacity of the shading wave RAM. If the changing amount per 16 pels is used, it is 2688 pels maximum.
5. The contents of the shading wave RAM is linearly approximated and converted to

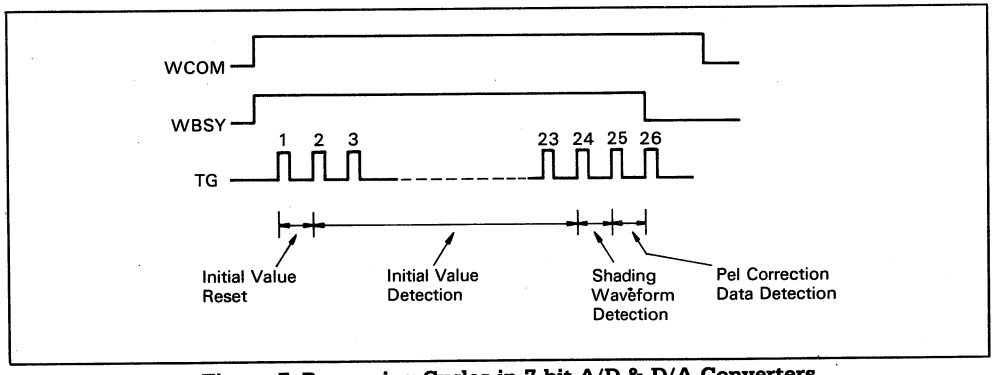


Figure 7 Processing Cycles in 7-bit A/D & D/A Converters

serial data via the Δ demodulator.

6. The output of Δ demodulator is converted to analog form to regenerate the shading waveform.

When performing pel correction, the DIPP takes the contents of the pel correction RAM and adds this data to the 7-bit A/D & D/A converters. (See figure 9)

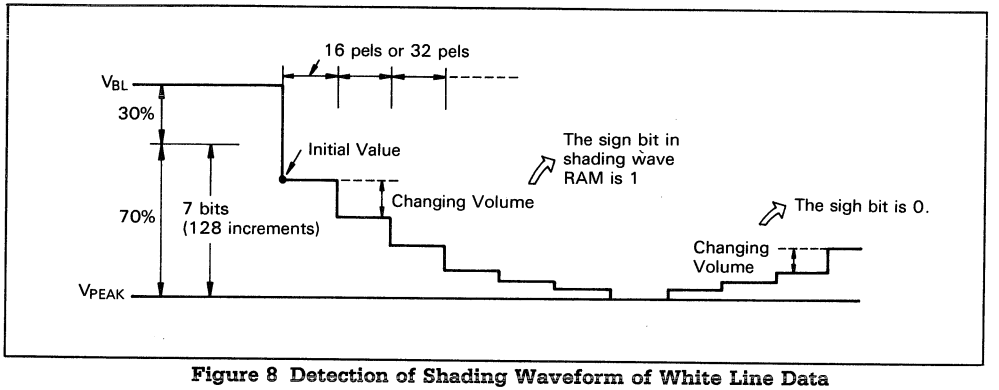


Figure 8 Detection of Shading Waveform of White Line Data

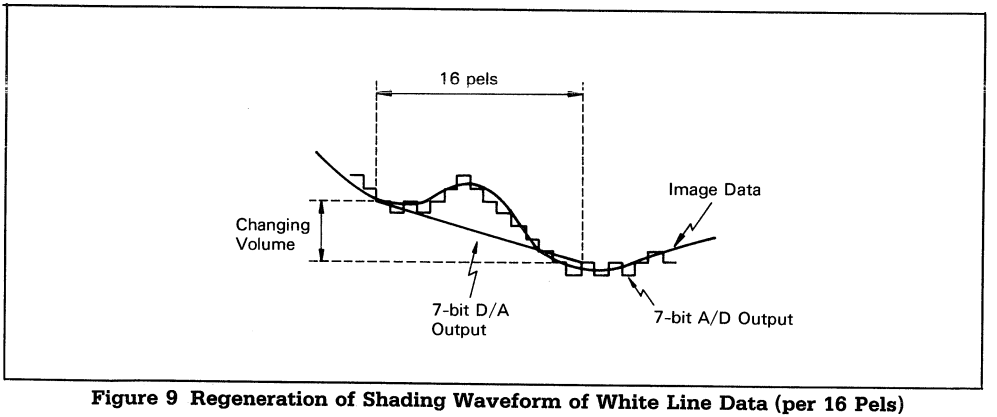


Figure 9 Regeneration of Shading Waveform of White Line Data (per 16 Pels)

4-bit A/D Converter

The 4-bit A/D converter generates 16 gradations of slice levels by dividing the voltage of the shading waveform of the white image data (V_L) which has been regenerated by the 7-bit A/D & D/A converters. It then converts these slice levels to digital form via internal 16 parallel comparators (ACMP0 to ACMP15). As a result, this circuit generates 16 outputs. (See figure 10).

When the DIPP performs pel correction, the 4-bit A/D converter detects the pel correction data.

The interval between outputs of this circuit is programmable by the γCONT0 and γCONT1 bits in the R0C register.

4-bit D/A Converter

The 4-bit D/A converter generates the black-side reference level (V_H) which will be used in the 4-bit A/D conversion. The V_H level can be selected out of 16 levels by the VH0 to VH3 bits in the R0B register.

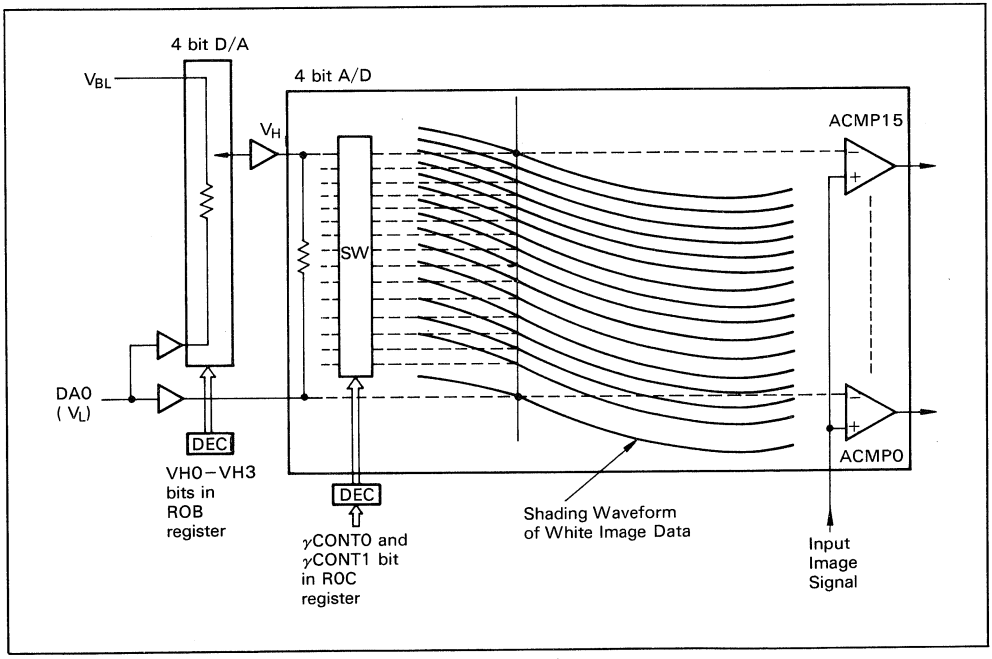


Figure 10 4-bit A/D Converter

4-bit Coder

When the DIPP performs 4-bit coding of the image signal, the outputs of the 4-bit A/D converter are input to the 4-bit coder.

The 4-bit coder digitizes the input data (except for the output of ACMP0) to a 4-bit code as shown in figure 11.

The 4-bit coder generates 16 gradations of half tones from $0000_{(2)}$ to $1111_{(2)}$. $0000_{(2)}$ represents white pel and $1111_{(2)}$ represents black pel. $0001_{(2)}$ to $1110_{(2)}$ represent half tones.

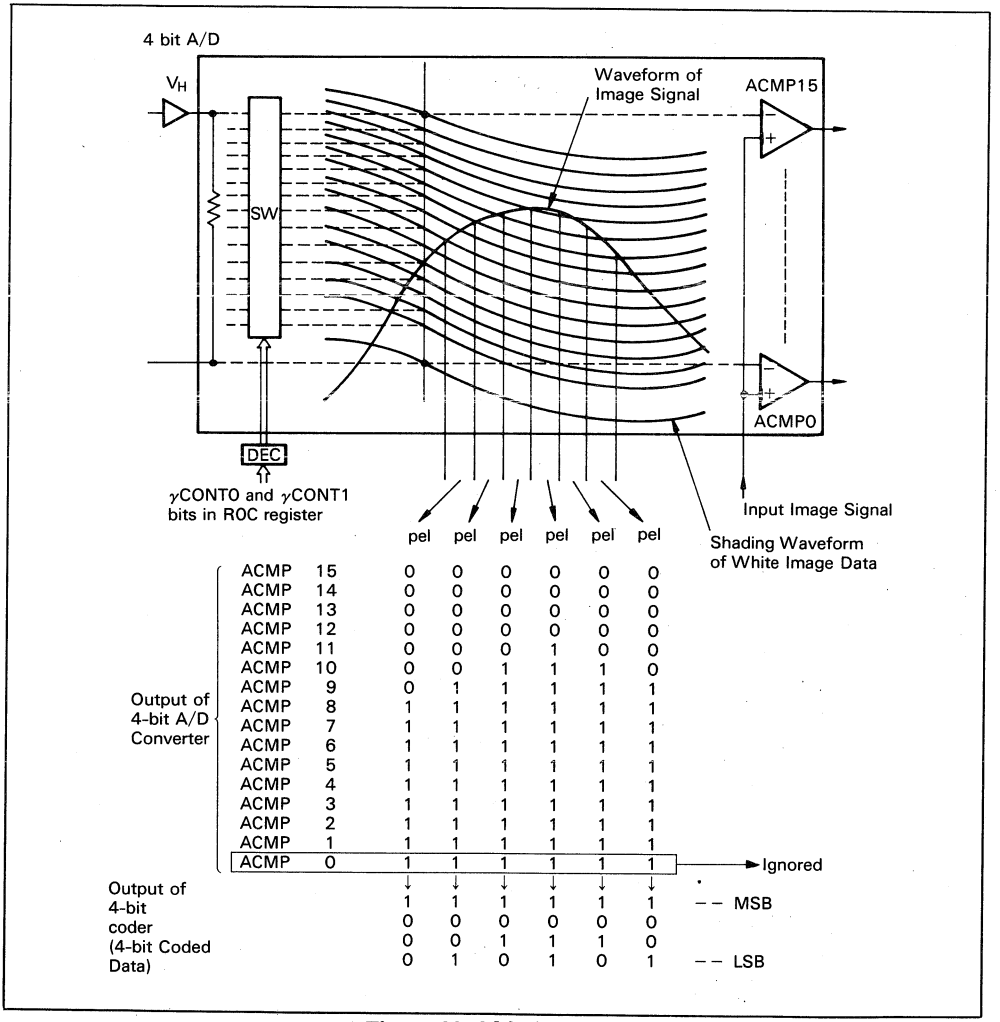
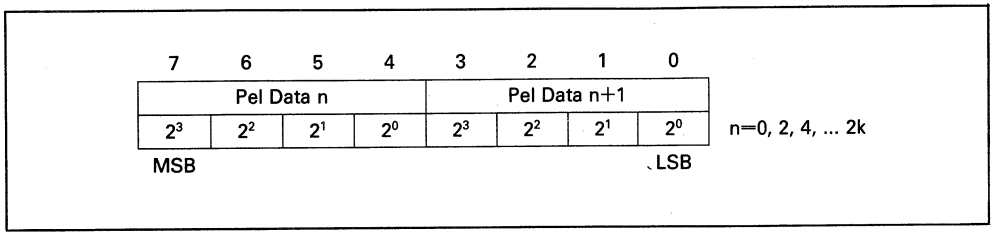


Figure 11 4-bit Coding

4 bits of 4-bit coded data represent a pel. Therefore, the 4-bit coded data are transfered to the memory bus in the following form.

Pel correction data are also transferred in this form.



Demultiplexer

When the DIPP performs binary coding or dithered coding of the image signal, the output of the 4-bit A/D converter (that is, the 16 analog comparators) enters the demultiplexer.

The demultiplexer encodes the 16 inputs to a 1 or 0.

1. Binary Coding

The demultiplexer performs binary coding as shown in figure 12. It selects one of 16 analog comparator outputs (ACMP0 to ACMP15) and outputs it.

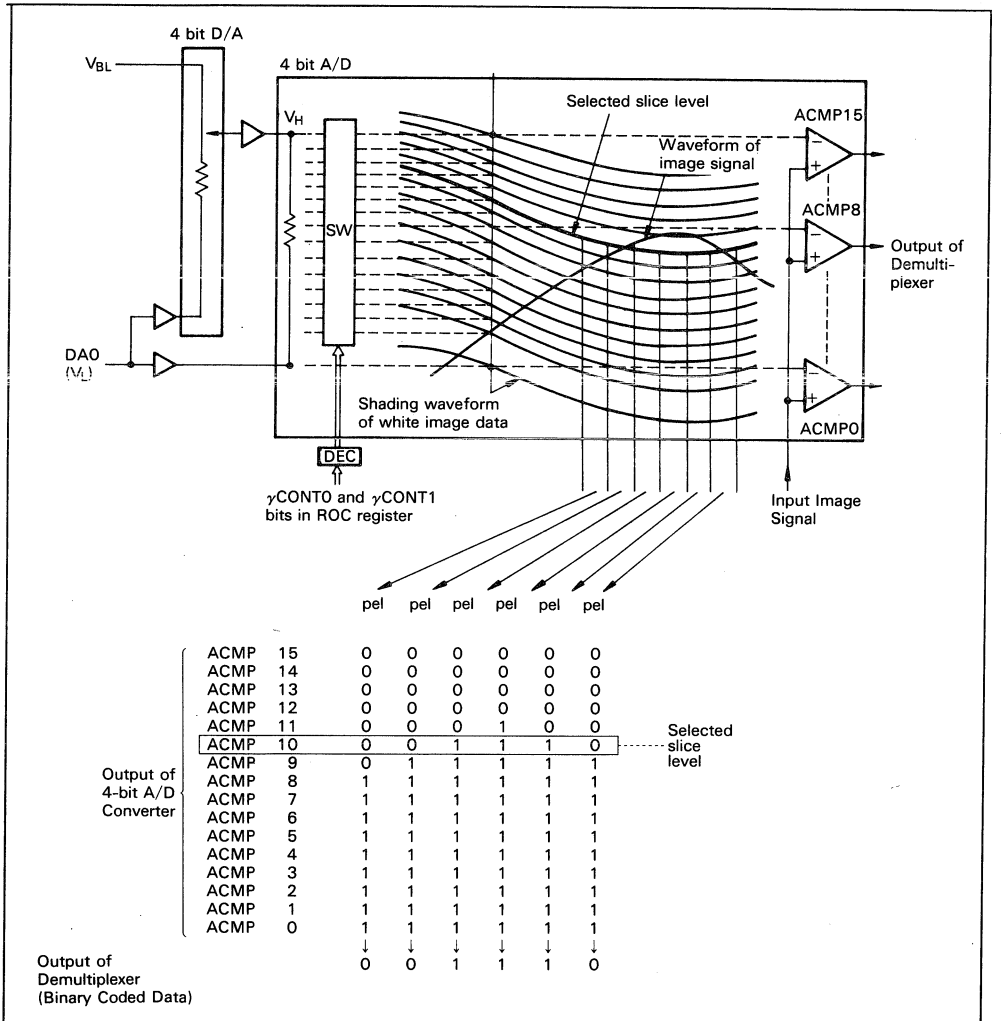


Figure 12 Binary Coding

Selecting an analog comparator output means selecting a slice level.

The selection of comparator output is programmable using SLICE0 to SLICE3 bits of the ROB register.

2. Dithered Coding

Dithered coding means digitizing a line of image data by changing slice levels in a cycle of 4 pels.

Practically, the demultiplexer selects one of 16 analog comparators in the 4-bit A/D converter similarly to the 4-bit coding. In the 4-bit coding, only one comparator output is used for digitization of a line of image data. In dithered coding, however, the user can change the comparator output for every 4 pels.

Which analog comparator output is selected (that is, which slice level is used) is detemined by the dither registers (R10 to R17 registers). The dither registers specify dither patterns as shown in figure 13.

Using the Bayer dither pattern, the demultiplexer performs dithered coding as shown in figure 14.

A bit of binary coded data or dither coded data represents 1 pel. These data are transferred to the internal system bus or memory bus in the following form. When the status of a bit is 0, it represents a white pel; a 1 represents a black pel.

0	8	2	10
12	4	14	6
3	11	1	9
15	7	13	5

(a) Bayer's Dither Pattern

4	10	5	11
15	0	2	6
9	3	1	12
14	8	13	7

(b) Scroll Pattern

Figure 13 Examples of Dither Patterns

7	6	5	4	3	2	1	0
Pel Data n	Pel Data n+1	Pel Data n+2	Pel Data n+3	Pel Data n+4	Pel Data n+5	Pel Data n+6	Pel Data n+7

MSB LSB

n=0, 8, 16, ... 8k

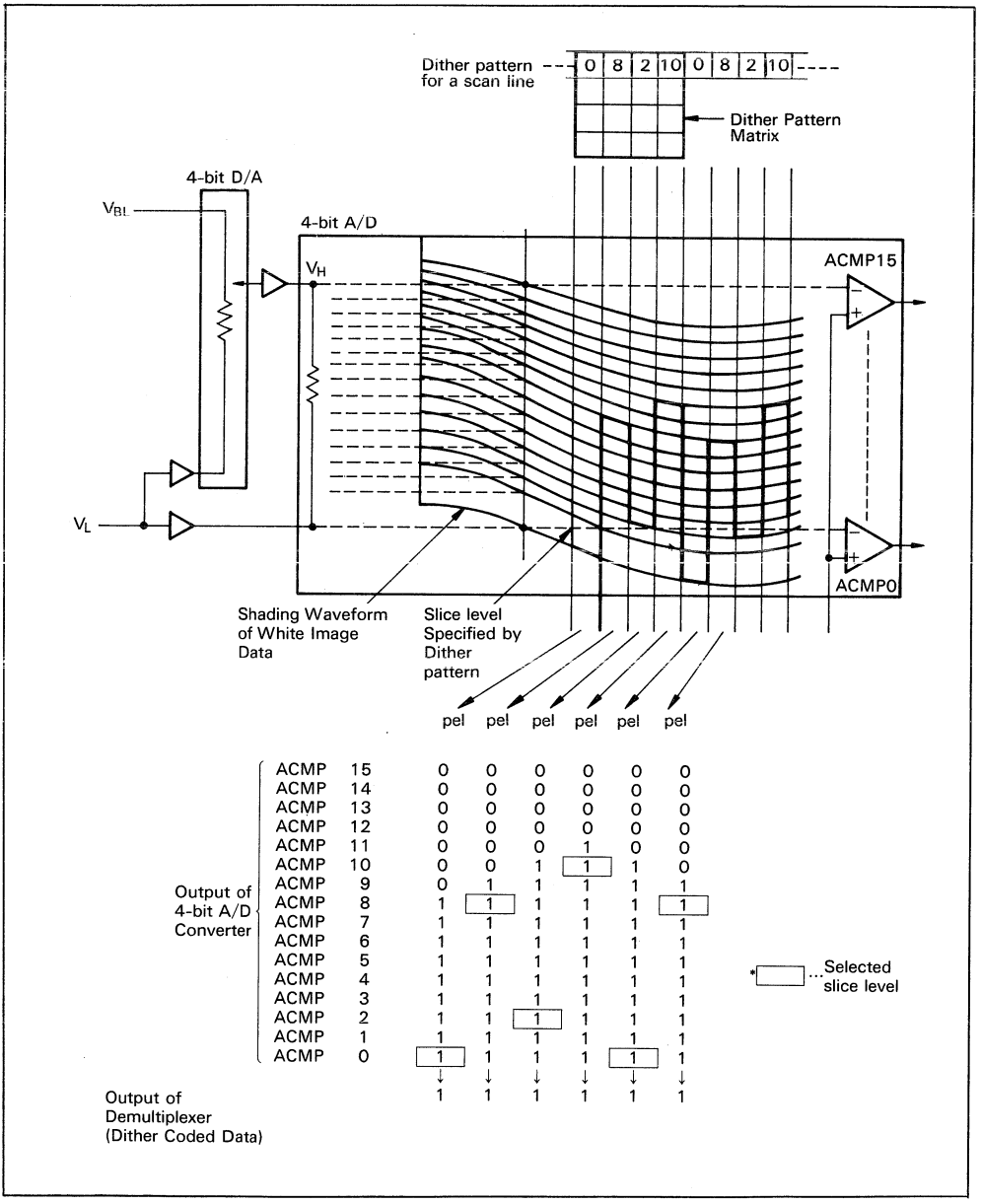


Figure 14 Dithered Coding

Digital Signal Processing Block

The functions of this block are:

- Horizontal resolution conversion of digitized image data,
- Automatic judgement of vertical resolution, and
- Vertical resolution conversion of digitized image data.

The DIPP can reduce and magnify digitized data using horizontal resolution conversion or vertical resolution conversion.

Reduction is performed only in read (T) mode. The DIPP reduces the digitized data and transfers it to the MPU system, which allows the time required for transmitting the data to be shortened.

Magnificaton is performed in receive (R) mode. The DIPP can magnify the reduced data which has been transmitted via the internal system bus and transfers it to the recorder.

Figure 15 shows the configuration of the digital signal processing block.

The functions of this block will be described in the following paragraphs.

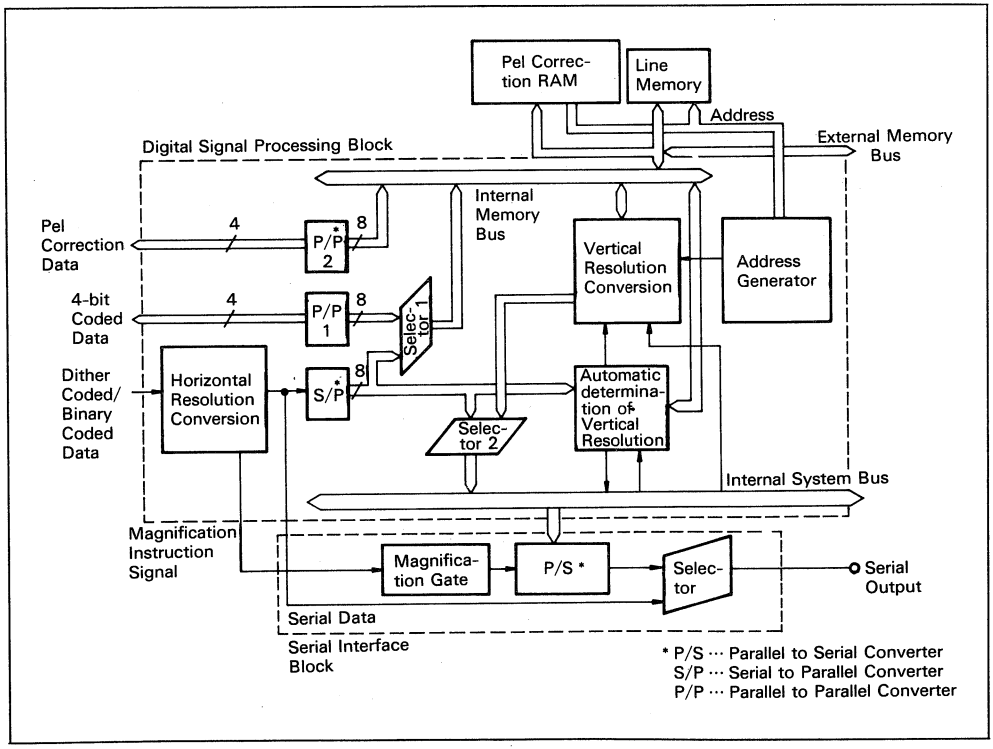


Figure 15 Configuration of Digital Signal Processing Block and Serial Interface Block

Horizontal Resolution Conversion

Horizontal reduction conversion means reduction or magnification of digital data along a scan line.

For reduction, the user must specify the horizontal reduction conversion logic and reduction ratio using R18 register, R0D register, R0E register and R0F register.

For magnification, the user must specify the magnification ratio using R0D register, R0E register and R0F register. The user can specify a magnification and reduction ratio from 0.125 to 8.

Figure 16 shows an example of horizontal resolution conversion.

The DIPP can perform horizontal resolution conversion on binary coded data and dither coded data, but not on 4-bit coded data.

Vertical Resolution Conversion

Vertical resolution conversion means execution of logical operations on data in the line before the previous line, data in the previous line, and data in the current scan line. Vertical resolution conversion requires an external line memory which stores data in the line before the previous line and data in the previous line.

Logical operations A+B, A+B · $\overline{C}$, $\overline{A}$ · B+B · C and null can be selected using VRCNT0 and VRCNT1 bits in the R00 register.

The DIPP transfers all of the vertical-resolution-converted data (including unnecessary data) to the MPU system. The MPU must select necessary data according to the horizontal resolution conversion ratio.

When the DIPP performs a DMA transfer of digitized data to the MPU system in read (T) mode, both horizontal resolution conversion (reduction) and vertical resolution conversion (reduction) are possible. When the DIPP performs serial output of digitized data to the recorder, however, only horizontal resolution conversion (reduction) is possible.

In receive (R) mode, only horizontal resolution conversion (magnification) is possible. In this case, the DIPP can increase the amount of data which have been transferred from the MPU system to the P/S circuit before outputting them via T/RDATA pin.

Automatic Determination of Vertical Resolution

Automatic determination of vertical resolution means counting the number of changing pels between adjacent data along the current scan line or between the current scan line and the previous scan line.

This function compares the counted value with the value specified by the R09 register. Result of the comparison appears in the REJ flag bit of the status register.

In response to the status of the REJ bit, the MPU can have the DIPP perform vertical resolution conversion using VRCNT0 and VRCNT1 bits in the R00 register.

The DIPP has 4 patterns of changing pels detection. The user can select a pattern through the CD0 and CD1 bits in he R08 register. In matrix modes, a changing pel is detected by using information of 4 pels.

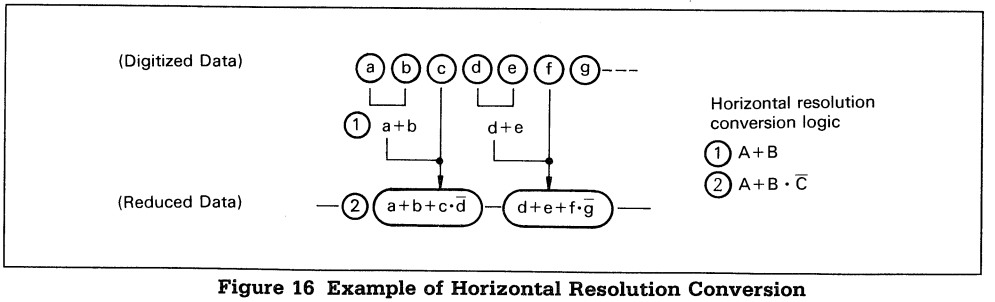


Figure 16 Example of Horizontal Resolution Conversion (Reduction Ratio ..... 1/3)

DMA Transfer

In read mode, the DIPP can perform a DMA transfer of digitized data from the DIPP to the MPU system. The DIPP has two DMA transfer modes: cycle stealing DMA mode and burst DMA mode.

1. Cycle Stealing DMA Transfer in Read (T) Mode
   The DIPP can transfer binary coded data and dither coded data via the internal system bus in the cycle stealing DMA mode. Figure 17 shows the timing diagram for stealing DMA transfer of the digitized data (The DIPP cannot perform cycle stealing DMA transfer of 4-bit coded data).
2. Burst DMA Transfer in Read (T) Mode
   When the external line memory is interfaced, the DIPP can transfer a line of binary coded data, dither coded data or 4-bit coded data in the burst DMA mode. Figure 18 shows the timing diagram for burst DMA transfer of the digitized data. The burst DMA transfer speed depends on the operating frequency of the DMAC.

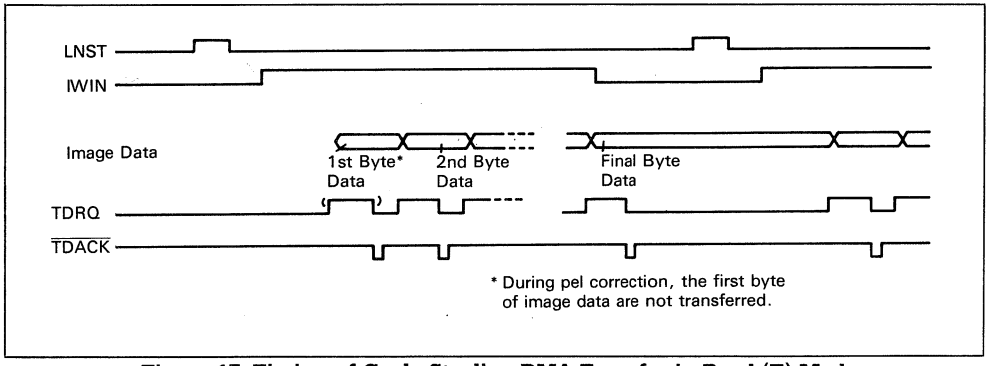


Figure 17 Timing of Cycle Stealing DMA Transfer in Read (T) Mode

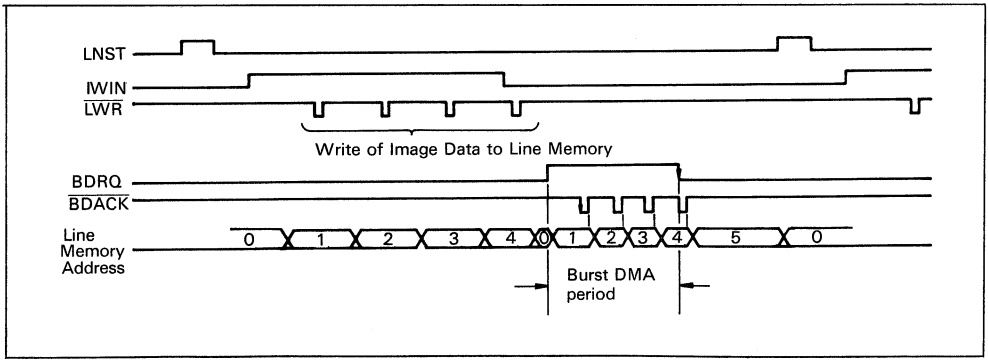


Figure 18 Timing of Burst DMA Transfer in Read (T) Mode

3. Cycle Stealing DMA Transfer in Receive (R) Mode
   In addition, the DIPP can perform cycle stealing DMA transfer of image data from the MPU system to the DIPP in receive (R) mode (Image data coming from the MPU system are transferred to the recorder via the serial interface block). The timing diagram for cycle stealing DMA transfer of image data from the MPU system to the DIPP is shown in figure 19.

   These DMA transfers depend on the $\overline{T}/R$ bit in the R00 register and the BST bit and DMAE bit in the R01 register.

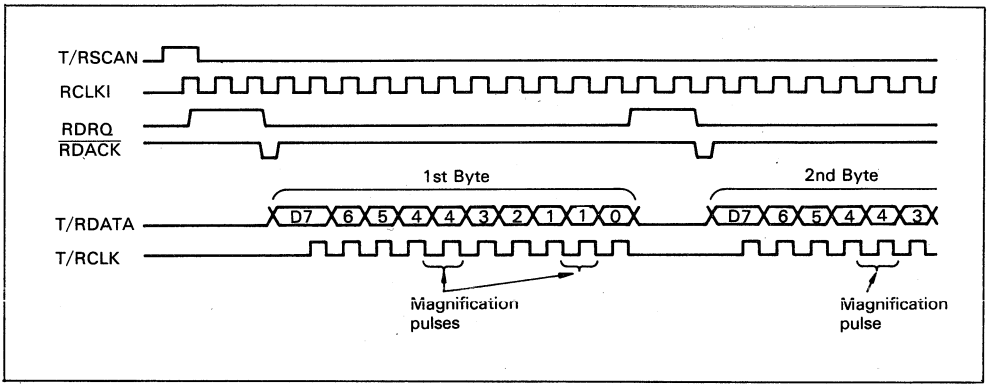


Figure 19 Timing of Cycle Stealing DMA Transfer and Serial Output in Receive (R) Mode

Table 1 Summary of DMA Transfers in Read Mode

	Distortion Correction	Shading Distortion Correction		Pel Correction	
	Data	Binary/Dither Coded Data	4-bit Coded Data	Binary/Dither Coded Data	4-bit Coded Data
Bus	Internal System Bus → System Bus* (Cycle Stealing DMA)	0.625M bytes per second	No Performed	0.3125M bytes per second	Not Performed
	Internal Memory Bus → Memory Bus (Burst DMA)	5M bytes per second	5M bytes per second	5M bytes per second	5M bytes per second
Memory Bus Interface Mode		A Mode	B Mode	C Mode / D Mode	

(*) In this case, 'System Bus' includes the system bus and the document image bus.

Edge Emphasis

The DIPP can generate a sharp outline of graphics by differentiating input image signal. (This function is called 'edge emphasis' in this document.)

When the DIPP uses binary coding, edge emphasis is performed in the following order.

1. An integrating circuit is placed between the IOUT pin (image signal output) and the DAO pin (output of shading waveform regenerated in 7-bit A/D & D/A converters), and the output of this circuit is then interfaced with the SLICE1 pin (input of the reference voltage for slice levels). See figure 20.
2. The DIPP generates a waveform which is used as the reference for slice levels. (See figure 21).
3. Using this waveform as a reference, the DIPP generates slice levels following input image signals.

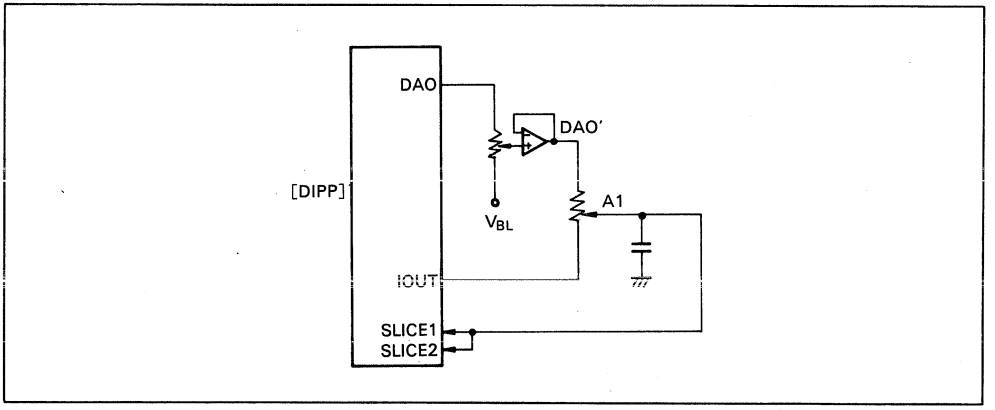


Figure 20 Edge Emphasis Circuit

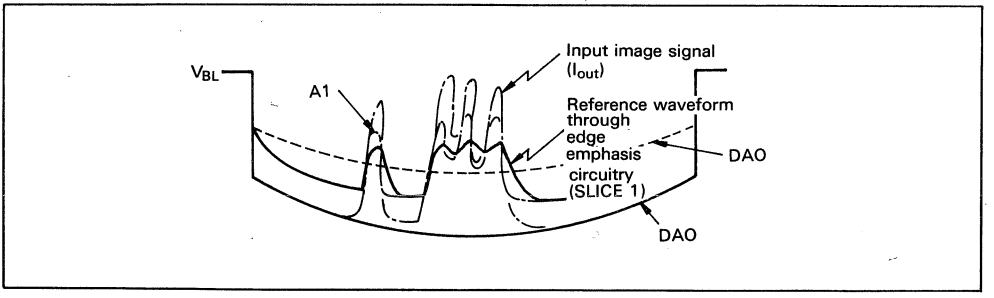


Figure 21 Edge-Emphasized Wave

Memory Bus Interface Operation

Memory Bus Interface

The operation of the memory bus interface in four memory bus interface modes is explained in the following paragraphs.

Memory Bus Interface in A Mode

The DIPP is interfaced with the line memory as shown in figure 22. Memory bus interface timing is shown in figure 23 and figure 24.

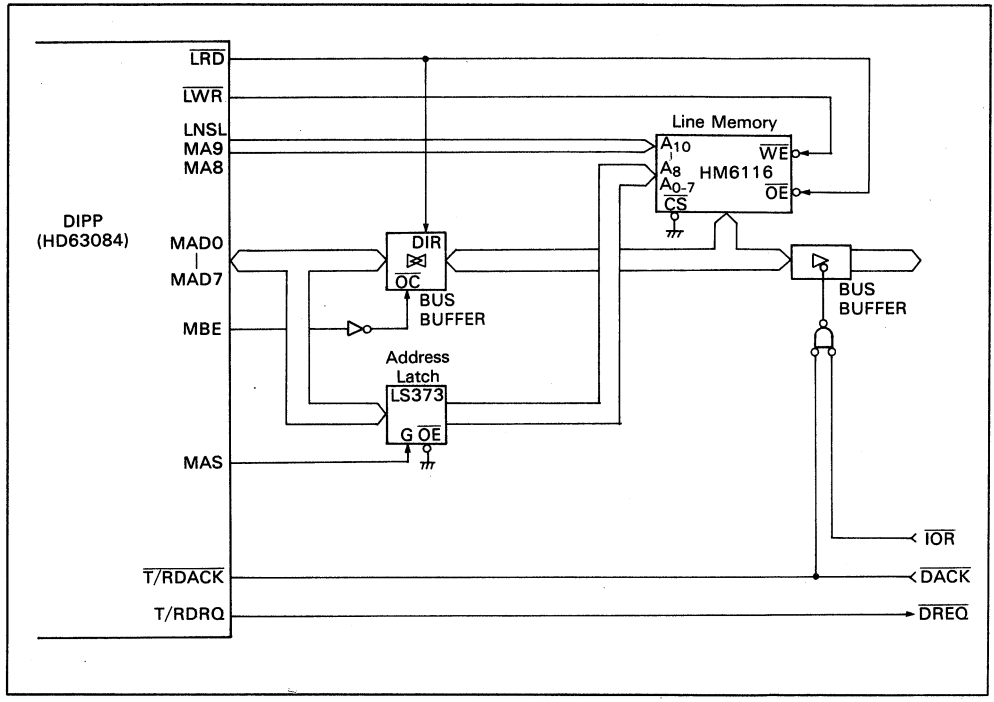


Figure 22 Memory Bus Interface in A Mode

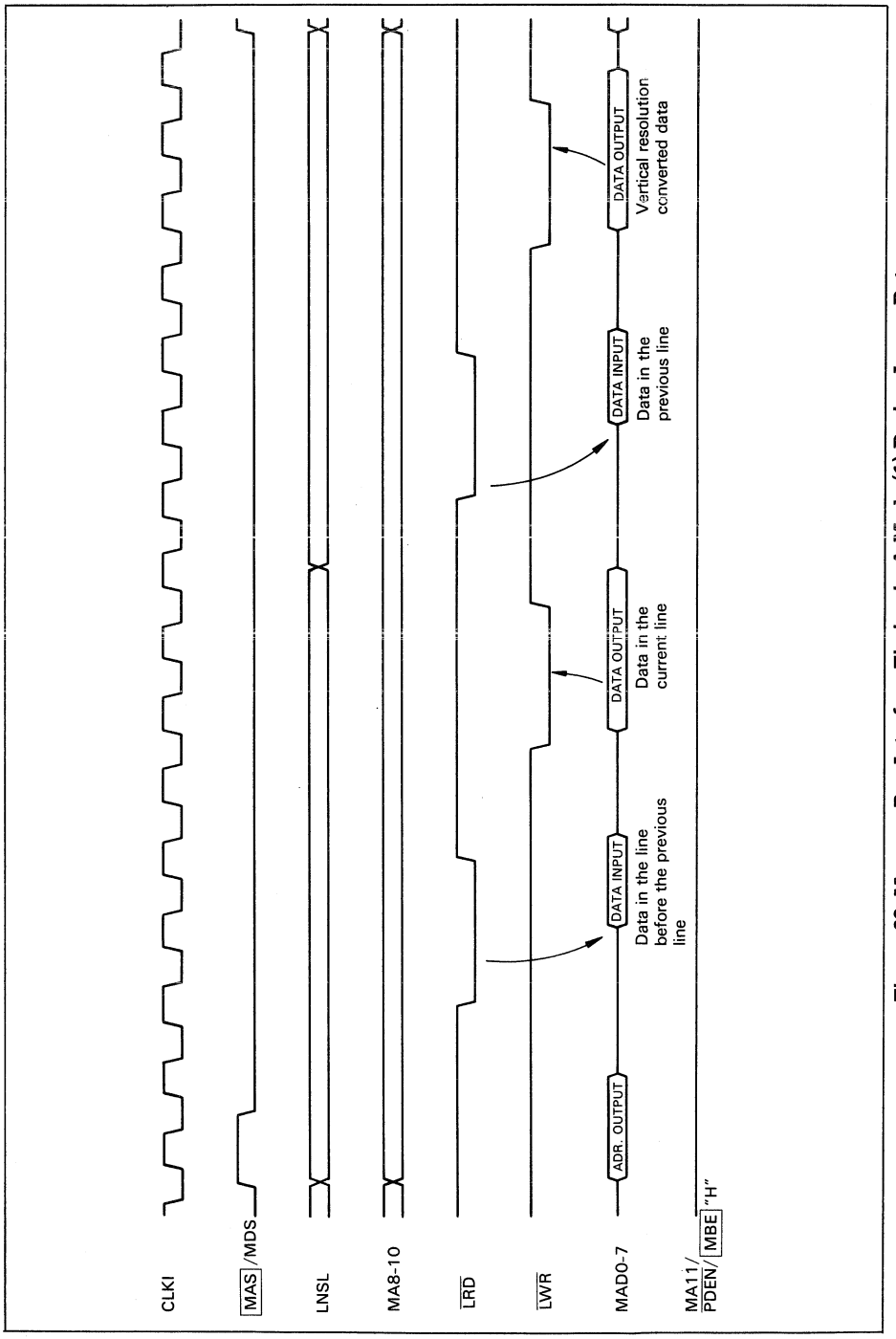


Figure 23 Memory Bus Interface Timing in A Mode (1) During Image Data Processing

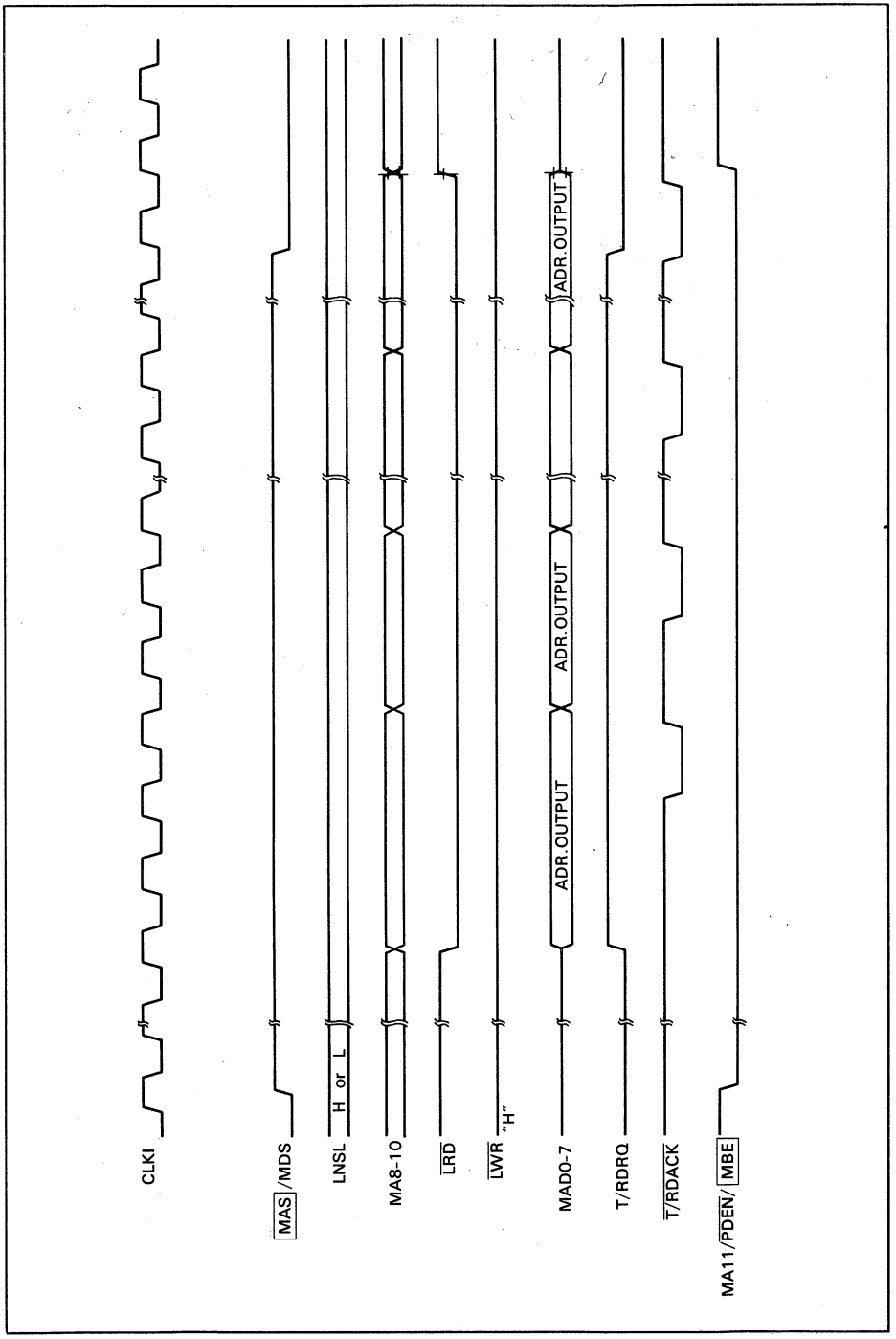


Figure 24 Memory Bus Interface Timing in A Mode (2) During Burst DMA Transfer

Memory Bus Inteface in B Mode

The DIPP is interfaced with the pel correction RAM and the line memory as shown in figure 25. Memory bus interface timing is shown in figure 26, figure 27 and figure 28.

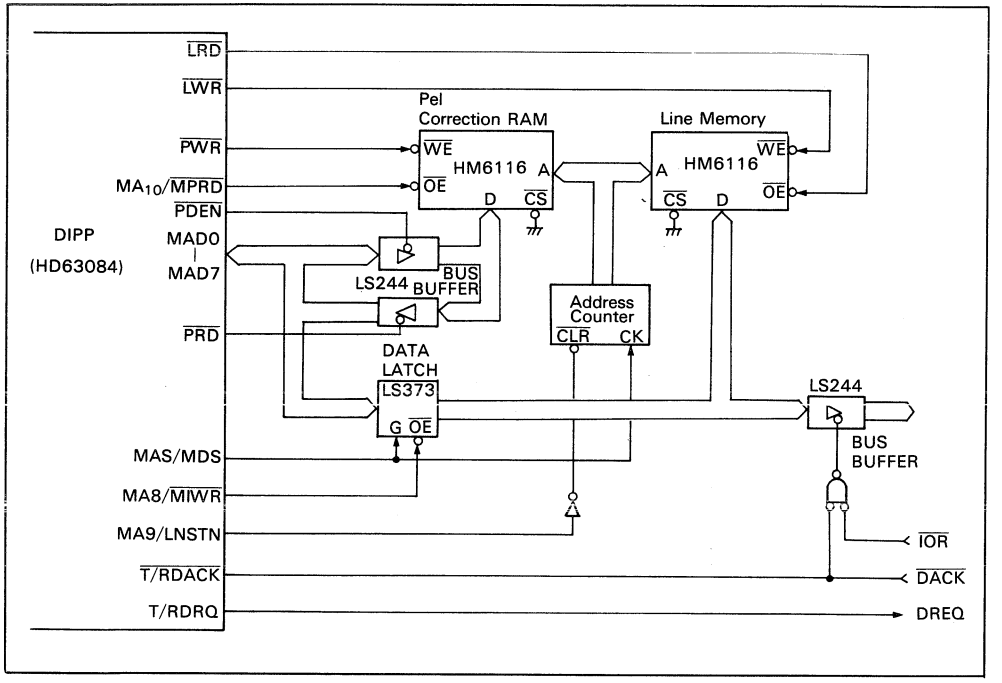


Figure 25 Memory Bus Interface in B Mode

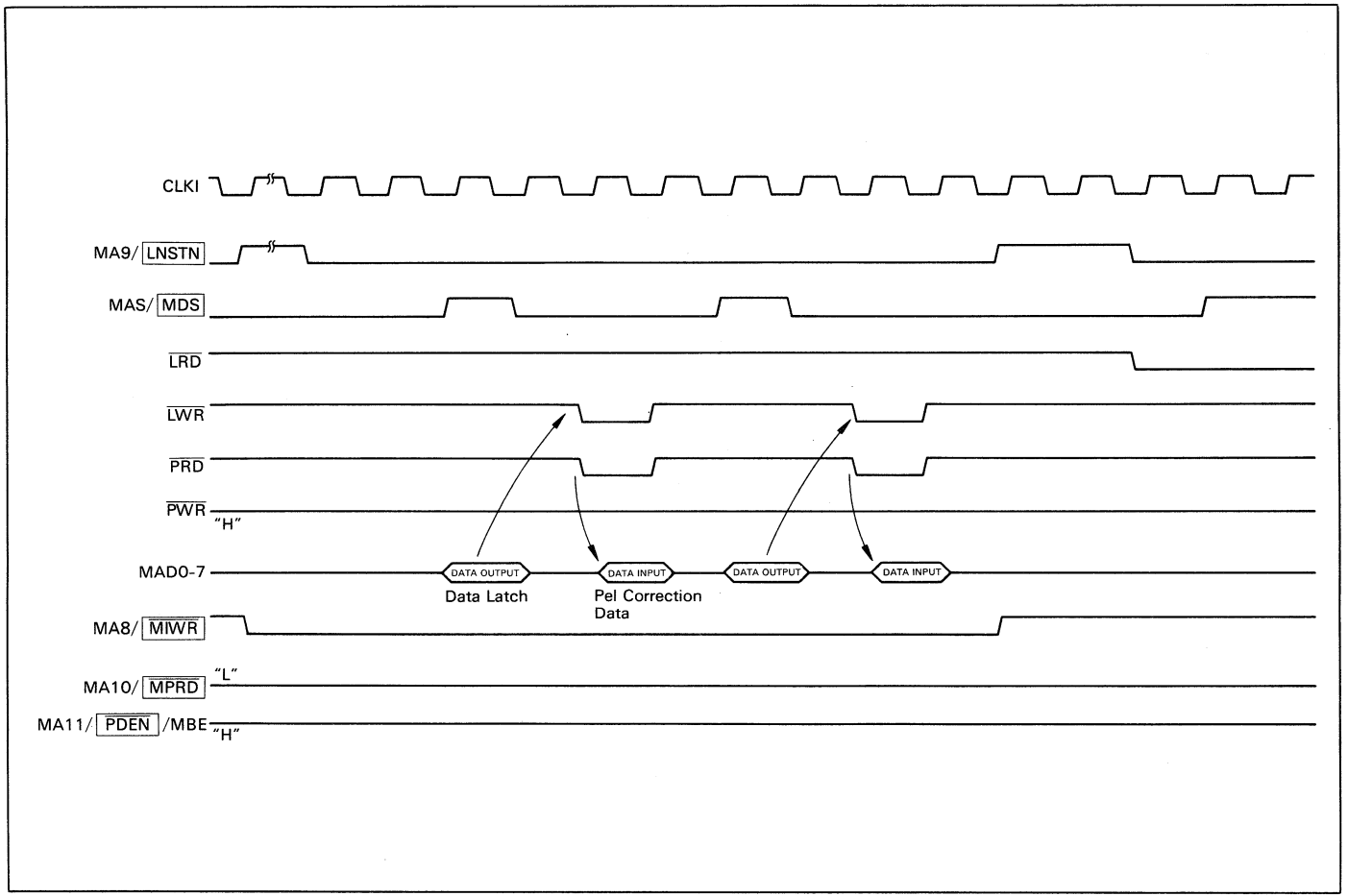


Figure 26 Memory Bus Interface Timing in B Mode (1) During 4-bit Coded Data Output

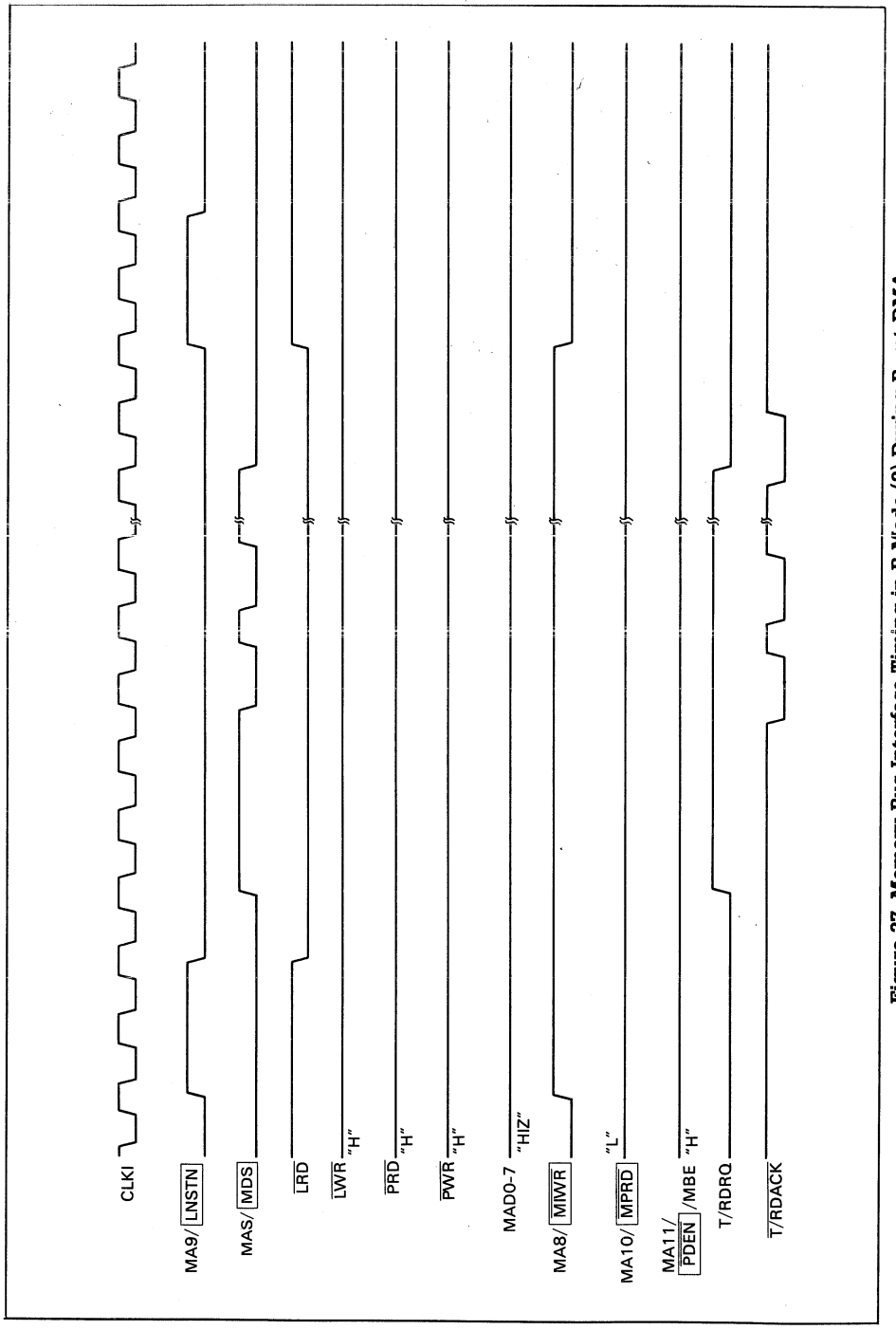


Figure 27 Memory Bus Interface Timing in B Mode (2) During Burst DMA Transfer

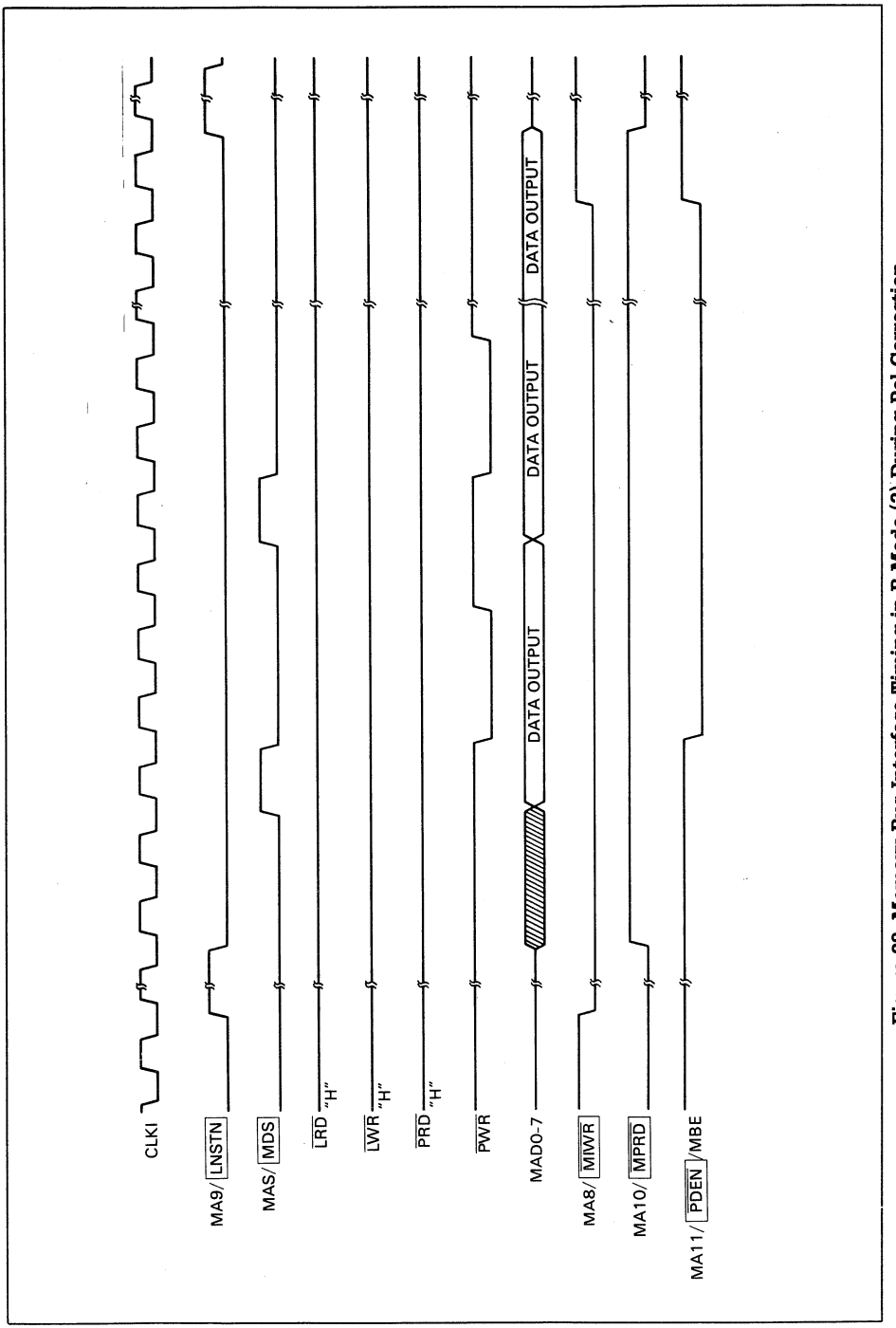


Figure 28 Memory Bus Interface Timing in B Mode (3) During Pel Correction Data Detection

Memory Bus Interface in C or D Mode

The DIPP is interfaced with the pel correction RAM and line memory as shown in figure 29. Memory bus interface timing is shown in figure 30 and figure 31.

If no external RAMs can be connected with the memory bus (that is, if the RAMLESS bit in the R00 register is 1), MAD0 to MAD7 pins are placed in the high impedance state and other memory bus interface pins function in the same way as in C and D modes.

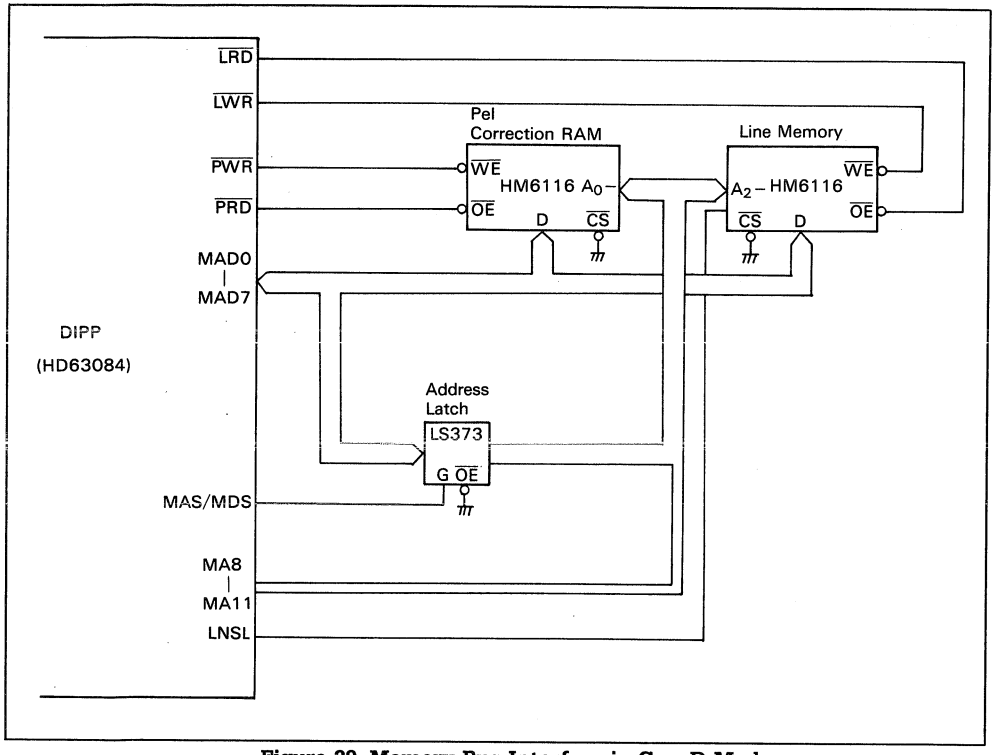


Figure 29 Memory Bus Interface in C or D Mode

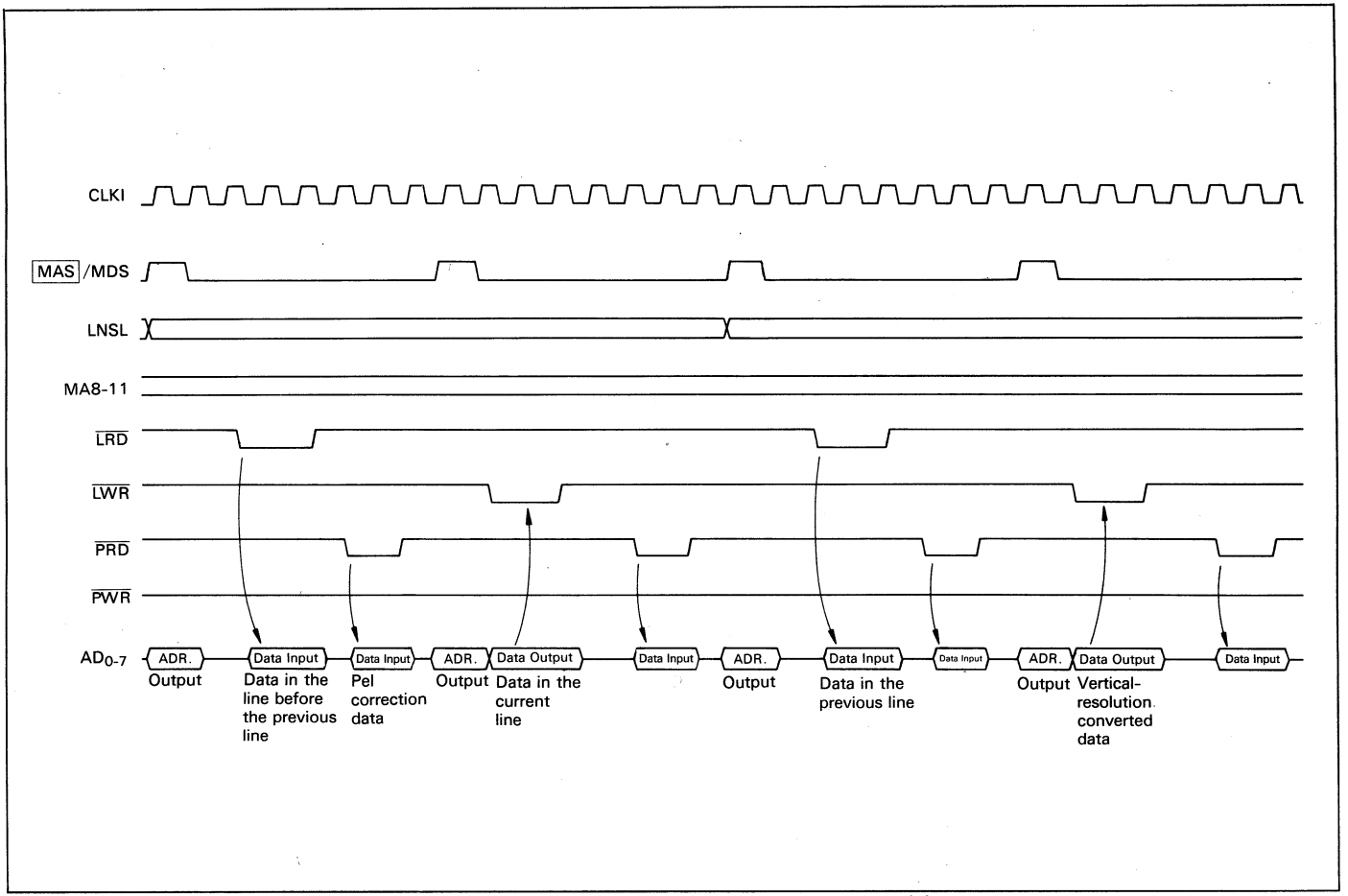


Figure 30 Memory Bus Interface Timing in C or D Mode (1) During Image Data Processing

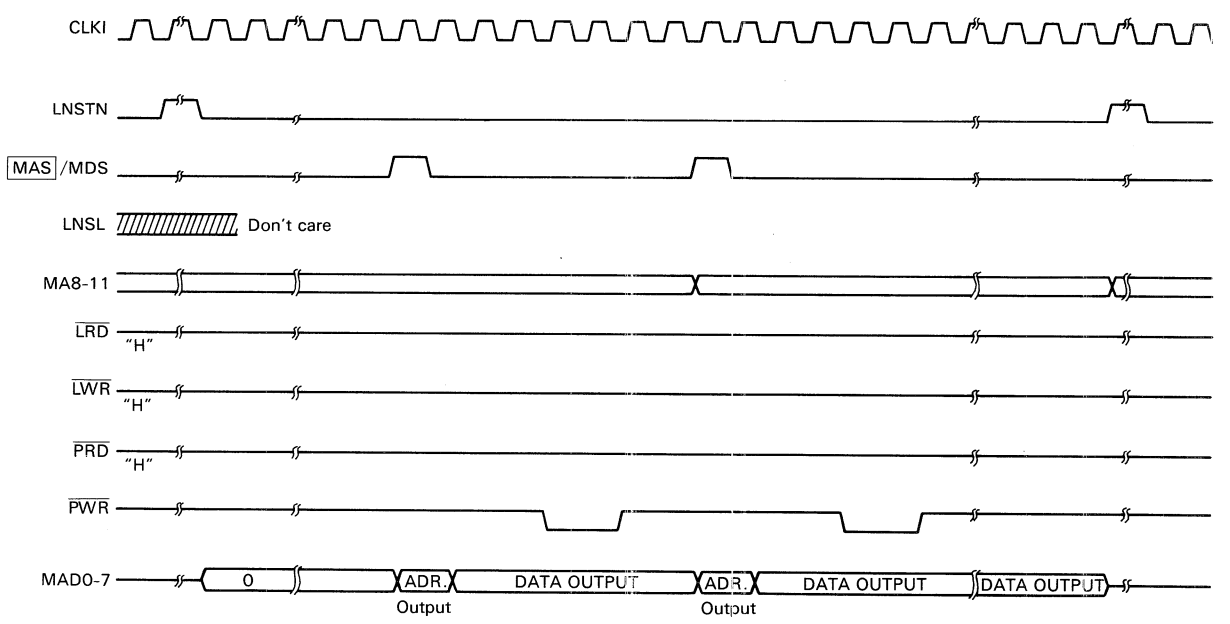


Figure 31 Memory Bus Interface Timing in C or D Mode (2) During Pel Correction Data Detection

Absolute Maximum Rating

Internal Digital Circuits (Voltages referenced to V_{SS} = 0 V. Ta = 25°C)

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage (Digital Input Pins)	V_I	−0.3 to V_{DD}+0.3	V
Input Voltage (Digital I/O Pins)	V_{IT}	−0.3 to V_{DD}+0.3	V

Internal Analog Circuits (Voltages referenced to AV_{SS} = 0 V. Ta = 25°C)

Item	Symbol	Value	Unit
Supply Voltage	AV_{DD}	−0.3 to +7.0	V
Reference Voltage	$V_{2.5}$ V_{CL} V_{BL}	−0.3 to AV_{DD}+0.3	V
Input Voltage (Analog Input Pins)	V_{IA}	−0.3 to AV_{DD}+0.3	V

Common Characteristics between Digital and Analog Circuits

Item	Symbol	Value	Unit
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Power Consumption *1	Pc	500	mW

*1) Ta = 25°C

Precaution in Using the DIPP

- Applying overvoltage more than the maximum rating to the input terminals due to overshooting or under shooting may cause latch-up, electro-static breakdown, etc.
- Precaution is needed in noise protection and shield for the analog terminals.

Electrical Characteristics

Internal Digital Circuits

DC Characteristics (V_{DD} = 5.0 V±5%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Condition
Input High Voltage	V_{IH}	2.0	—	V_{DD}+0.3	V	V_{DD}=5.25 V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V	V_{DD}=4.75 V
Output High Voltage	V_{OH}	3.0	—	—	V	V_{DD}=4.75 V I_{OH}=−400 µA V_{IH}=2.0 V V_{IL}=0.8 V
Output Low Voltage	V_{OL}	—	—	0.4	V	V_{DD}=4.75 V V_{IH}=2.0 V V_{IL}=0.8 V Other output pins: Low I_{OL}=1.6 mA
Input Leakage Voltage	I_{IN}	−10*1	—	10	µA	V_{DD}=5.25 V V_I=0 to V_{DD}
Three-State (Off State) Leakage Current	I_{OZH}	−10	—	10	µA	V_{DD}=5.25 V V_0=V_{DD}
	I_{OZL}	−10	—	10	µA	V_{DD}=5.25 V V_0=V_{SS}

*1) The minimum leakage current at pin 34 ($\overline{68}$/80) is −100µA because it has an internal pull-up resistor.

AC Characteristics (V_{DD} = 5.0 V±5%, V_{SS} = 0 V, Ta = 0 to +70°C)

68 Type MPU Interface Timing

Item	Symbol	min	typ	max	Unit	Test Condition	Applicable Pin
DS Pulse Width	t_{WDS6}	320	—	—	ns	Figure 34	DS
DS to R/$\overline{W}$ Setup Time	t_{SRW6}	140	—	—	ns		R/$\overline{W}$
DS to R/$\overline{W}$ Hold Time	t_{HRW6}	10	—	—	ns		
DS to $\overline{CS}$ Setup Time	t_{SCS6}	140	—	—	ns		$\overline{CS}$
DS to $\overline{CS}$ Hold Time	t_{HCS6}	10	—	—	ns		
DS to $\overline{RS}$ Setup Time	t_{SRS6}	140	—	—	ns		$\overline{RS}$
DS to $\overline{RS}$ Hold Time	t_{HRS6}	50	—	—	ns		
Read Data Access Time	t_{RAC6}	—	—	290	ns		D0 to D7
Read Data Hold Time	t_{RH6}	10	—	—	ns		
Write Data Setup Time	t_{WS6}	190	—	—	ns		
Write Data Hold Time	t_{WH6}	20	—	—	ns		
DS to $\overline{T}$/RDACK Setup Time	t_{SDK6}	140	—	—	ns	Figure 35	$\overline{T}$/RDACK
DS to $\overline{T}$/RDACK Hold Time	t_{HDK6}	10	—	—	ns		

80 Type MPU Interface Timing

Item	Symbol	min	typ	max	Unit	Test Condition	Applicable Pin
DS ($\overline{RD}$) Pulse Width	t_{WDS8}	250	—	—	ns	Figure 36	DS
R/$\overline{W}$ ($\overline{WR}$) Pulse Width	t_{WRW8}	200	—	—	ns		R/$\overline{W}$
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{SRC8}	0	—	—	ns		$\overline{CS}$
$\overline{RD}$ to $\overline{CS}$ Hold Time	t_{HRC8}	0	—	—	ns		
$\overline{WR}$ to $\overline{CS}$ Setup Time	t_{SWC8}	0	—	—	ns		
$\overline{WR}$ to $\overline{CS}$ Hold Time	t_{HWC8}	0	—	—	ns		
$\overline{RD}$ to $\overline{RS}$ Setup Time	t_{SRR8}	50	—	—	ns		$\overline{RS}$
$\overline{RD}$ to $\overline{RS}$ Hold Time	t_{HRR8}	50	—	—	ns		
$\overline{WR}$ to $\overline{RS}$ Setup Time	t_{SWR8}	50	—	—	ns		
$\overline{WR}$ to $\overline{RS}$ Hold Time	t_{HWR8}	50	—	—	ns		
Read Data Access Time	t_{RAC8}	—	—	250	ns		D0 to D7
Read Data Hold Time	t_{RH8}	20	—	—	ns		
Write Data Setup Time	t_{WS8}	150	—	—	ns		
Write Data Hold Time	t_{WH8}	50	—	—	ns		
$\overline{RD}$ to T/$\overline{RDACK}$ Setup Time	t_{SDK8}	0	—	—	ns	Figure 37	T/$\overline{RDACK}$
$\overline{RD}$ to T/$\overline{RDACK}$ Hold Time	t_{HDK6}	0	—	—	ns		
$\overline{WR}$ to T/$\overline{RDACK}$ Setup Time	t_{SRK8}	0	—	—	ns		
$\overline{WR}$ to T/$\overline{RDACK}$ Hold Time	t_{HRK8}	0	—	—	ns		

MPU Interface Timing (common to 68 Type MPU and 80 Type MPU)

Item	Symbol	min	typ	max	Unit	Test Condition	Applicable Pin
T/RDRQ Positive Edge Delay	t_{DRQH}	—	—	180	ns	Figure 38	T/RDRQ
T/RDRQ Negative Edge Delay	t_{DRQL}	—	—	180	ns		
INT Positive Edge Delay	t_{INTH}	—	—	230	ns	Figure 39	INT
T/RSCAN Input to INT Negative Edge Delay	t_{INTL}	—	—	100	ns		
DS Input to INT Negative Edge Delay	t_{DSIL}	—	—	290	ns	Figure 34, 36	

Clock and Control Input Timing

Item	Symbol	min	typ	max	Unit	Test Condition	Applicable Pin
CLKI Cycle Time	t_{CYC}	100	—	1000	ns	Figure 40	CLKI *2
RCLK Cycle Time	t_{RCYC}	200	—	10^6	ns		RCLKI *2
TCLK Cycle Time *3	t_{TCYC}	—	($2\times t_{CYC}$)	—	ns		TCLK
TSCAN Pulse Width *3	t_{TSW}	($2\times t_{CYC}$)	—	—	ns		T/RSCAN
RSCAN Pulse Width *3	t_{RSW}	($2\times t_{RCYC}$)	—	—	ns		
$\overline{RST}$ Pulse Width *3	t_{RSTW}	($2\times t_{CYC}$)	—	—	ns		$\overline{RST}$
TRIG Pulse Width *3	t_{TRIG}	(8)	—	—	µs		TRIG

*2) Both CLKI and RCLKI input frequencies provide duty cycle of 50%.
*3) Values for reference.

Serial Output Timing

Item	Symbol	min	typ	max	Unit	Test Condition	Applicable Pin
CLKI Input to TMSK Positive Edge Delay	t_{TMDTLH}	—	—	160	ns	Figure 41	TMSK
CLKI Input to TMSK Negative Edge Delay	t_{TMDTHL}	—	—	160	ns		
TDATA Positive Edge Delay	t_{TDDLH}	—	—	160	ns		T/RDATA
TDATA Negative Edge Delay	t_{TDDHL}	—	—	160	ns		
TCLK Positive Edge Delay	t_{TCH}	—	—	150	ns		T/RCLK
TCLK Negative Edge Delay	t_{TCL}	—	—	140	ns		
RCLKI Output to TMSK Positive Edge Delay	t_{TMDRLH}	—	—	(160)*3	ns	Figure 42	TMSK
RCLKI Output to TMSK Negative Edge Dalay	t_{TMDRHL}	—	—	(160)*3	ns		
RDATA Positive Edge Delay	t_{RDDLH}	—	—	(160)*3	ns		T/RDATA
RDATA Negative Edge Delay	t_{RDDHL}	—	—	(160)*3	ns		
RCLK Positive Edge Delay	t_{RCH}	—	—	(150)*3	ns		T/RCLK
RCLK Negative Edge Delay	t_{RCL}	—	—	(140)*3	ns		

*3) Values for reference.

Applicate Output and Sensor Interface Timing

Item	Symbol	min	typ	max	Unit	Test Condition	Applicable Pin
TIMO Output Delay	t_{TO}	—	—	150	ns	Figure 43	TIMO
LNST/IWIN Output Delay	t_{LN}	—	—	200	ns	Figure 43 (IWIN)	LNST/IWIN
ϕTG Output Positive Edge Delay	$t_{\phi TLH}$	—	—	150	ns	Figure 44	ϕTG
ϕTG Output Negative Edge Delay	$t_{\phi THL}$	—	—	140	ns		
ϕ1 Output Positive Edge Delay	$t_{\phi 1LH}$	—	—	100	ns		ϕ1
ϕ1 Output Negative Edge Delay	$t_{\phi 1HL}$	—	—	120	ns		
ϕR Positive Edge Delay	$t_{\phi RD}$	—	—	100	ns	Figure 46	ϕR
ϕR Negative Edge Hold	$t_{\phi RH}$	10	—	—	ns		
ϕR Pulse Width	$t_{\phi RW}$	—	$(t_{CYC}/2)$*2	—	ns		

*2) Values for reference.

Memory Bus Interface Timing

Item	Symbol	min	typ	max	Unit	Test Condition	Applicable Pin
MAS/MDS Positive Edge Delay	t_{MASLH}	—	—	150	ns	Figure 47, 49, 51, 52, 53	MAS/MDS
MAS/MDS Negative Edge Hold	t_{MASHL}	—	—	150	ns		
LNSL Positive Edge Delay	t_{LSDH}	—	—	180	ns	Figure 47, 52	LNSL
LNSL Negative Edge Delay	t_{LSDL}	—	—	180	ns		
MA8 to 11 Output Delay *4	t_{MAUD}	—	—	180	ns		MA8/$\overline{MIWR}$ to MA11/ $\overline{PDEN}$/MBE
$\overline{LRD}$ Negative Edge Delay	t_{LRHL}	—	—	150	ns		$\overline{LRD}$
$\overline{LRD}$ Positive Edge Hold	t_{LRLH}	—	—	150	ns		
$\overline{LWR}$ Negative Edge Delay	t_{LWHL}	—	—	150	ns		$\overline{LWR}$
$\overline{LWR}$ Positive Edge Delay	t_{LWLH}	—	—	120	ns		
MAD0 to 7 Delay *4	t_{MADD}	—	—	200	ns	Figure 47 etc.	MAD0-7
MAD0 to 7 Hold *4	t_{MADH}	20	—	—	ns		
MAD0 to 7 Setup Time *5	t_{RDS}	50	—	—	ns	Figure 47	
MAD0 to 7 Hold Time *5	t_{RDH}	80	—	—	ns		
MBE Negative Edge Delay	t_{MBEL}	—	—	180	ns	Figure 48	MBE
MBE Positive Edge Delay	t_{MBEH}	—	—	180	ns		
$\overline{T/RDACK}$ Input to MAS Negative Edge Delay	t_{BASL}	—	—	150	ns	Figure 50	MAS/MDS
$\overline{T/RDACK}$ Input to MAS Positive Edge Delay	t_{BASH}	—	—	150	ns		
$\overline{T/RDACK}$ Input to T/RDRQ *4 Negative Edge Delay	t_{BTDR}	—	—	180	ns		T/RDRQ
LNSTN Positive Edge Delay	t_{MLNH}	—	—	200	ns	Figure 49, 50, 51	MA9/LNSTN
LNSTN Negative Edge Delay	t_{MLNL}	—	—	200	ns		
$\overline{PRD}$ Negative Edge Delay	t_{PRHL}	—	—	150	ns	Figure 49, 52	$\overline{PRD}$
$\overline{PRD}$ Positive Edge Delay	t_{PRLH}	—	—	150	ns		
$\overline{PWR}$ Negative Edge Delay	t_{PWHL}	—	—	150	ns	Figure 51, 53	$\overline{PWR}$
$\overline{PWR}$ Positive Edge Delay	t_{PWLH}	—	—	150	ns		
$\overline{MIWR}$ Negative Edge Delay	t_{MIWL}	—	—	180	ns	Figure 49	MA8/$\overline{MIWR}$
$\overline{MIWR}$ Positive Edge Delay	t_{MIWH}	—	—	180	ns		
$\overline{MPRD}$ Negative Edge Delay	t_{MPRL}	—	—	180	ns	Figure 51	MA10/$\overline{MPRD}$
$\overline{MPRD}$ Positive Edge Delay	t_{MPRH}	—	—	180	ns		
$\overline{PDEN}$ Negative Edge Delay	t_{PDEL}	—	—	180	ns		MA11/$\overline{PDEN}$/ MBE

*4) Values for reference.
*5) CLKI↑ reference.

Internal Analog Circuits

DC Characteristics (AV_{DD} = 5.0 V±5%, AV_{SS} = 0 V, Ta = 0 to +70°C)

Item	Detailed Item		Symbol	min	typ	max	Unit	Test Condition
Input Current	V_{BL}		I_{BL}	—	—	1.0	mA	V_{BL}=3.5 V
Input Voltage Range	ISIN1, 2		$V_{ISI1,2}$	1.5	—	3.5	V	
	PEAKI		V_{INP}	0	—	3.0		
	SLICE1		V_{INS1}	1.5	—	3.5		APEAK=Disable V_{BL}=3.5 V
	SLICE2		V_{INS2}	1.5	—	3.5		
	V_{BL}		V_{IBL}	—	3.5	—		
	V_{CL}		V_{ICL}	—	3.5	—		
Output Current	I_{OUT}		I_{OIO}	−16.0	−7.0	−4.0	mA	V_{OUT}=0 V
	PEAKO		I_{OPK}	−5.0	−2.0	−0.7		
	DAO		I_{ODO}	−6.0	−2.0	−0.7		
Output Voltage	PEAKO	Resistance Chain Step 0	V_{P0}	3.20	—	3.40	V	V_{CL}=V_{BL}=3.4 V PEAKI=1.5 V
		Resistance Chain Step 255	V_{P255}	1.25	—	1.65		
	DAO	Resistance Chain Step 0	V_{D0}	1.40	—	1.60		
		Resistance Chain Step 127	V_{D127}	2.60	—	3.00		
	IOUT		V_{OUT}	2.40	—	2.65		V_{ISIN1}=2.5 V
Input Leakage Current	ISIN1		I_{LIS1}	−10	—	10	µA	V_{IN}=0 to AV_{DD}
	ISIN2		I_{LIS2}					
	PEAKI		I_{LPI}					
	SLICE1		I_{LSL1}					
	SLICE2		I_{LSL2}					
	VCL		I_{LVCL}					

AC Characteristics (AV_{DD} = 5.0 V±5%, AV_{SS} = 0 V, Ta = 0 to +70°C)

Item	Detailed Item	Symbol	min	typ	max	Unit	Test Condition
Input Voltage Range	Peak to Peak Voltage	V_{IP}	0.1	—	2.0	V	CLKI=10 MHz
Operating Frequency	Image Signal Reading Frequency	V_{IF}	0.5	—	5.0	MHz	

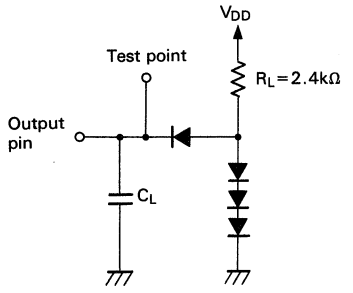
Capacitance

Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	C_{IN}	—	—	12.5	pF	f=100 kHz
Output Capacitance	C_{OUT}	—	—	12.5	pF	
Input/Output Capacitance	$C_{in/out}$	—	—	12.5	pF	

* These parameters are sample values.

Supply Current (V_{DD} = AV_{DD} = 5.0 V±5%, V_{SS} = AV_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	min	typ	max	Unit	Test Condition
Supply Current	Standby	I_{DS}	—	—	1	mA	
	Operating	I_{DD}	—	—	6.0		CLKI=10 MHz



Notes 1. C_L=120pF (D0 to D7)
C_L=60pF (Other output and I/O pins. Excluding analog pins)
2. C_L includes stray capacitance caused by the probe and load capacitance.
3. Diodes are 1S2074 Ⓗ or equivalents.

Figure 32 Bus Timing Test Loads

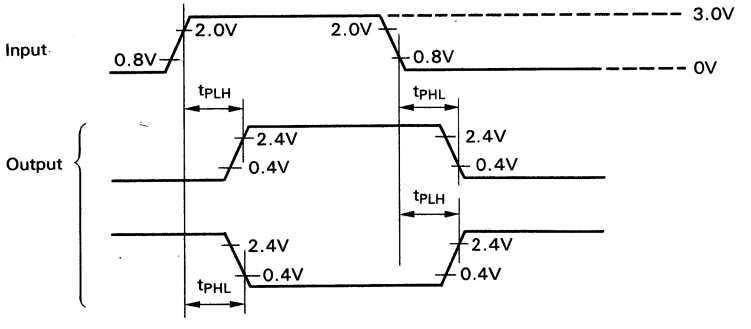


Figure 33 I/O Signal Test Point

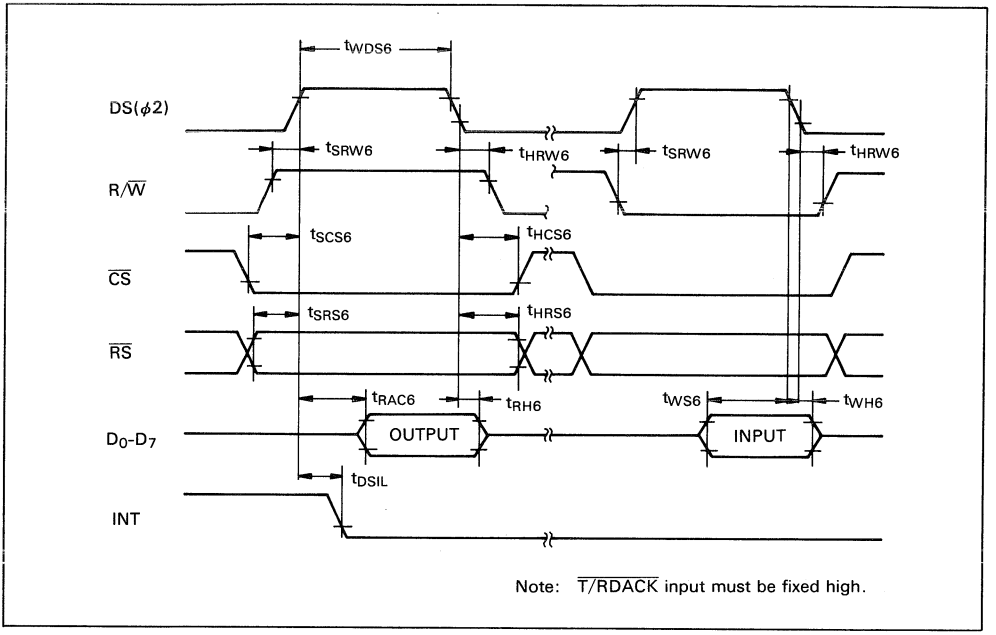


Figure 34 68 Type MPU Access Timing

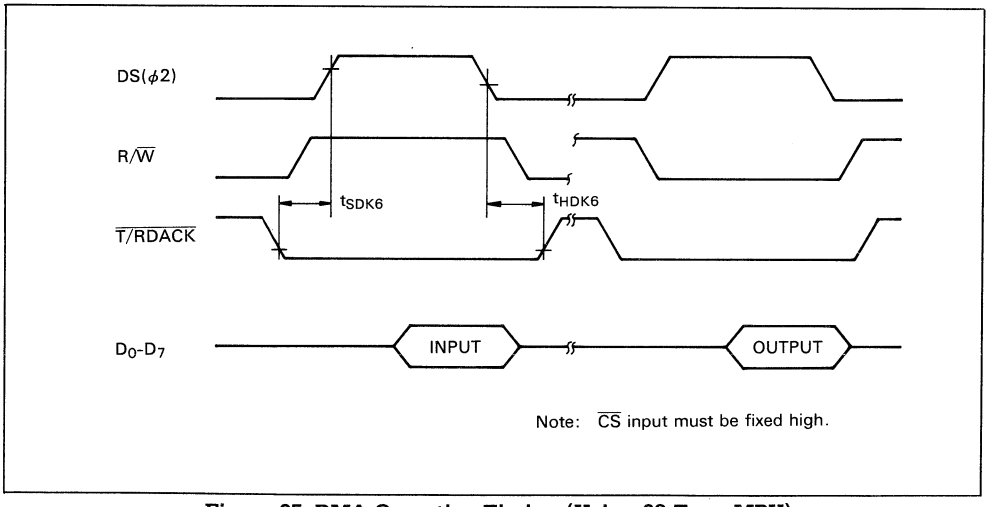


Figure 35 DMA Operation Timing (Using 68 Type MPU)

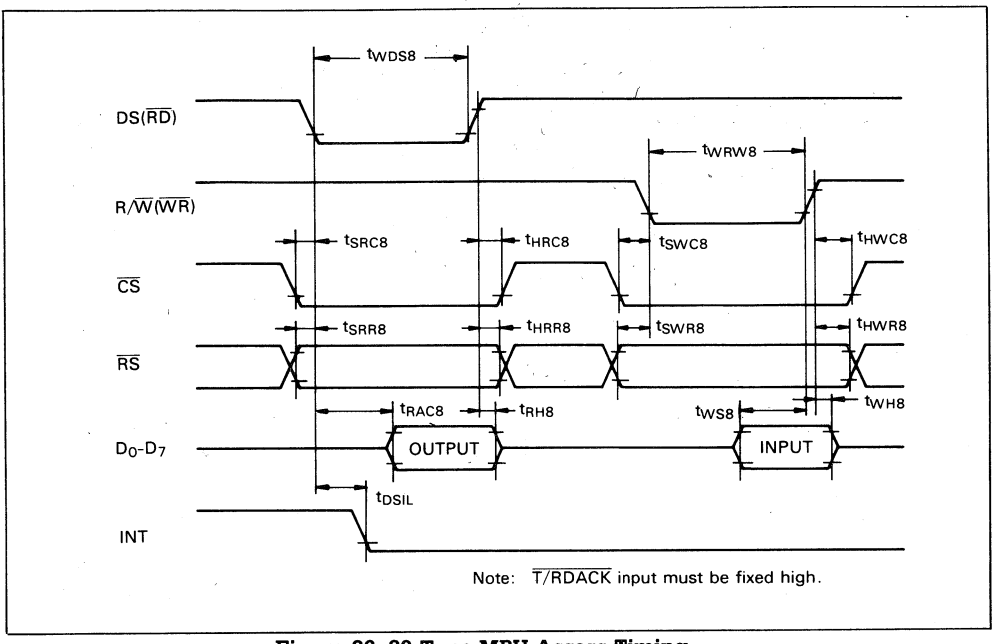


Figure 36 80 Type MPU Access Timing

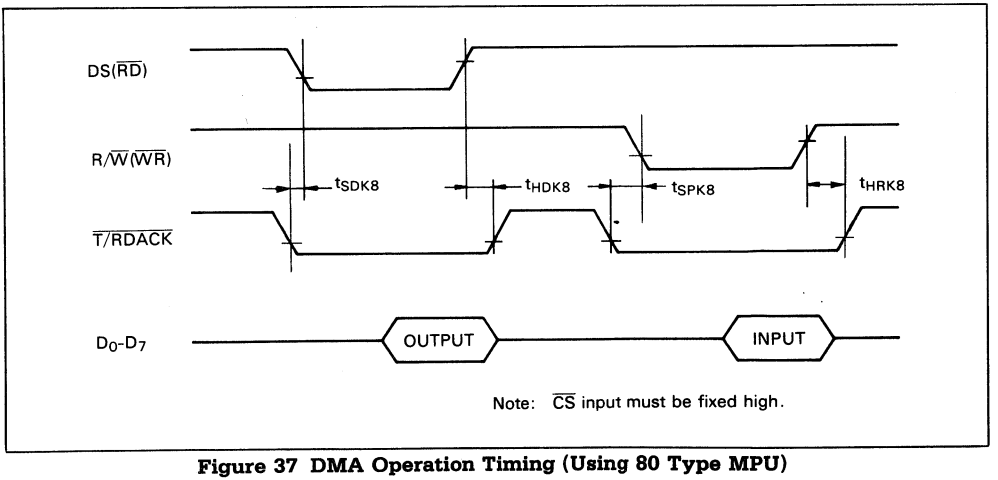


Figure 37 DMA Operation Timing (Using 80 Type MPU)

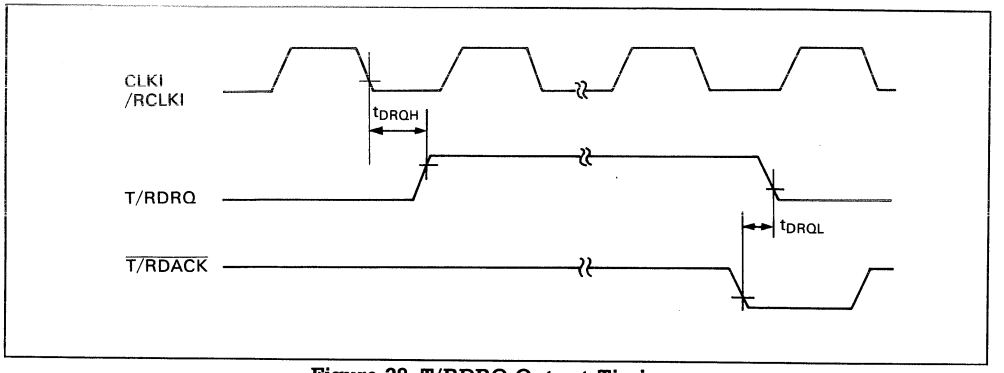


Figure 38 T/RDRQ Output Timing

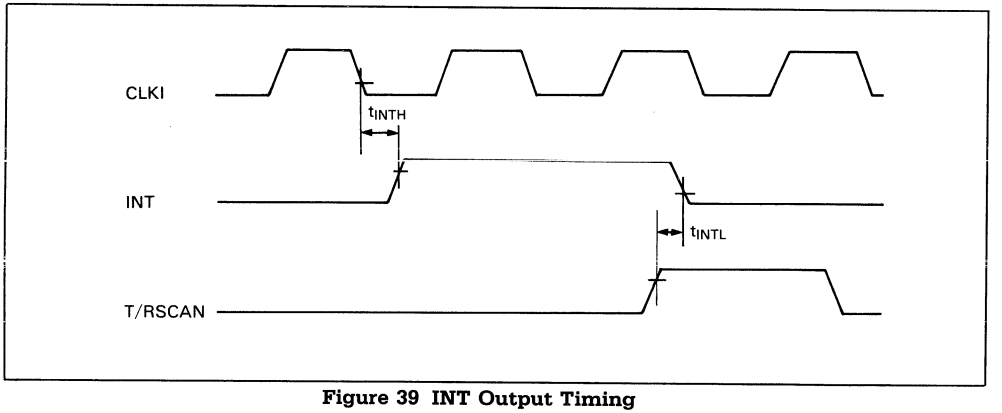


Figure 39 INT Output Timing

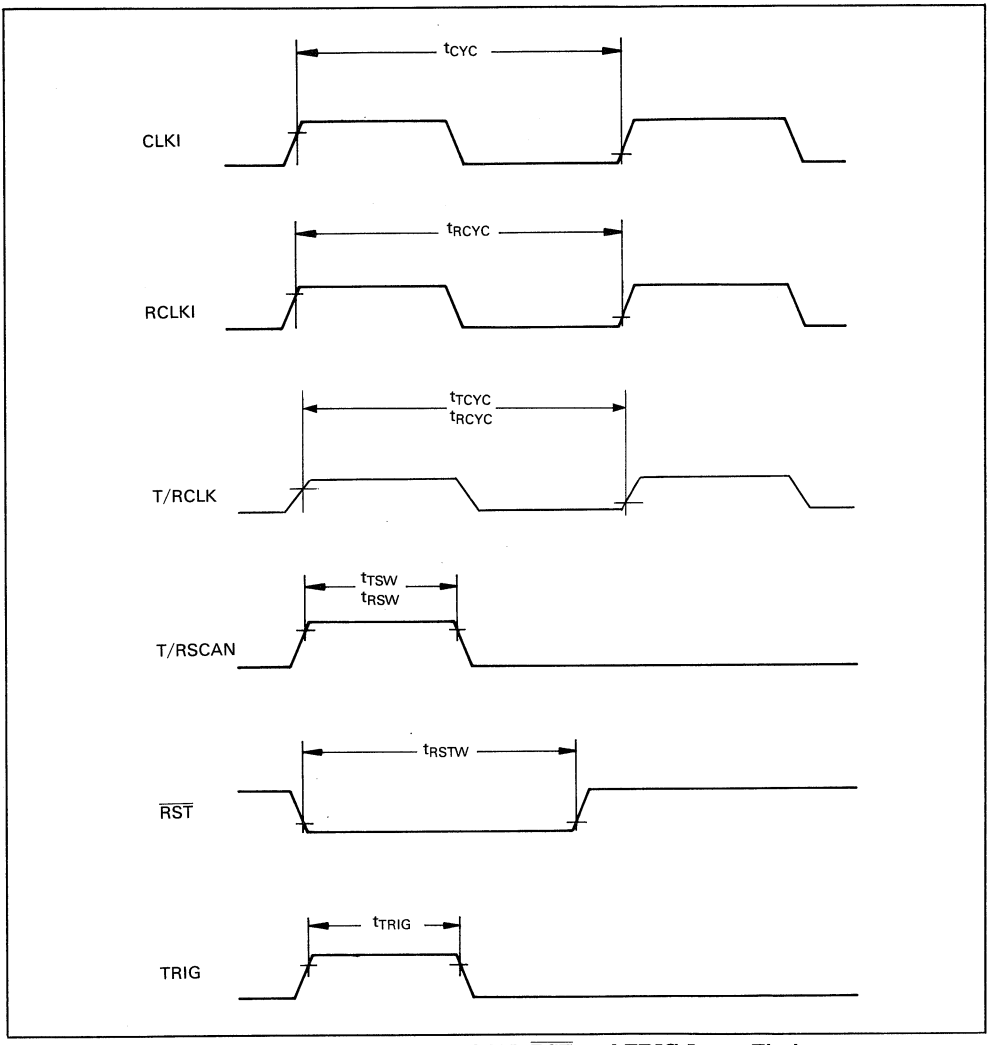


Figure 40 CLKI, RCLKI, T/RSCAN, $\overline{RST}$ and TRIG Input Timing, T/RCLK Output Timing

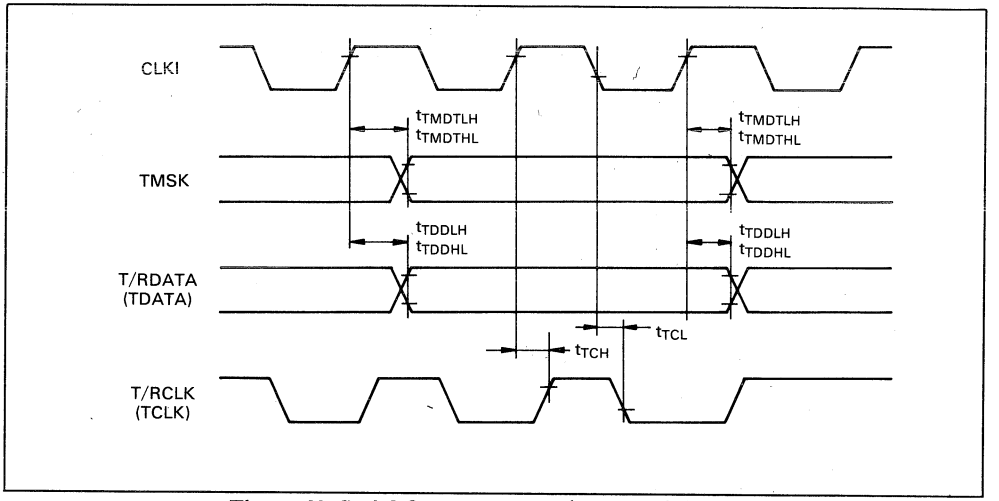


Figure 41 Serial Output Timing (in Read (T) Mode)

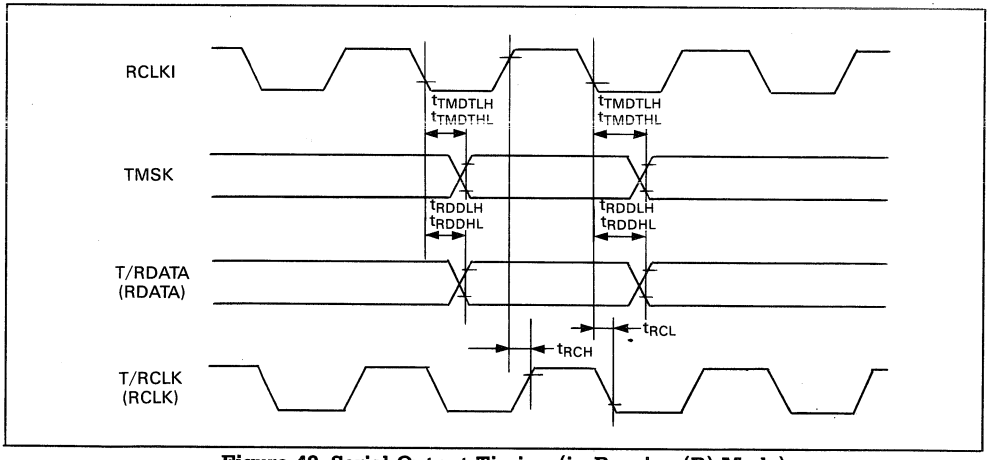


Figure 42 Serial Output Timing (in Receive (R) Mode)

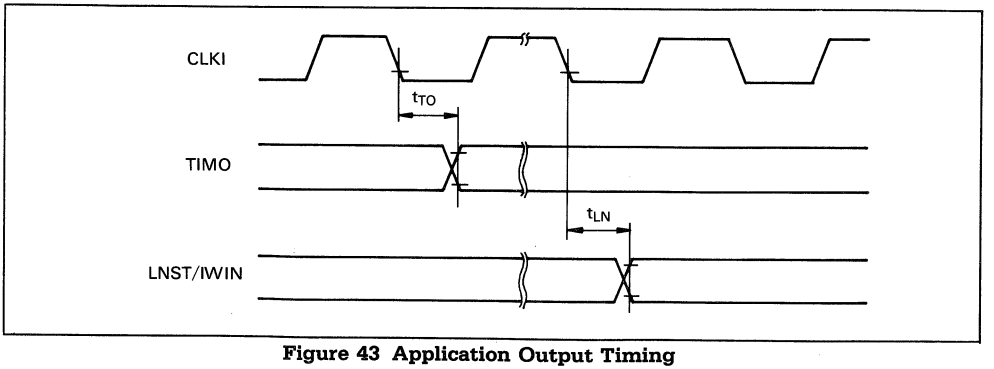
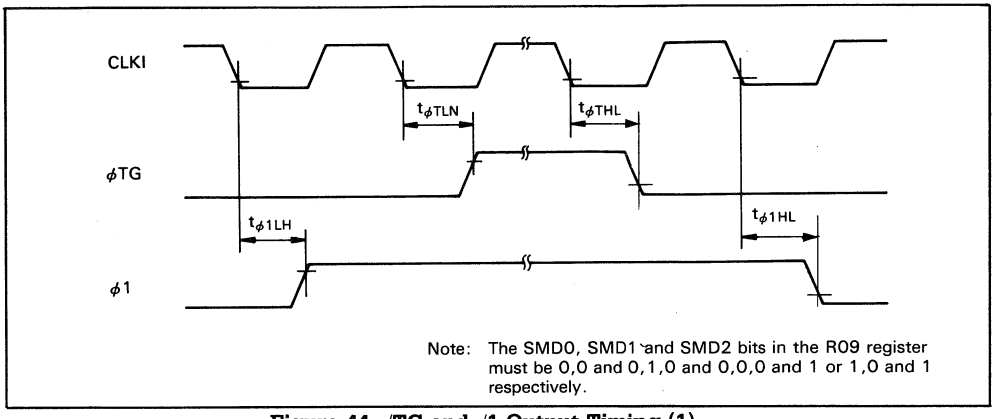
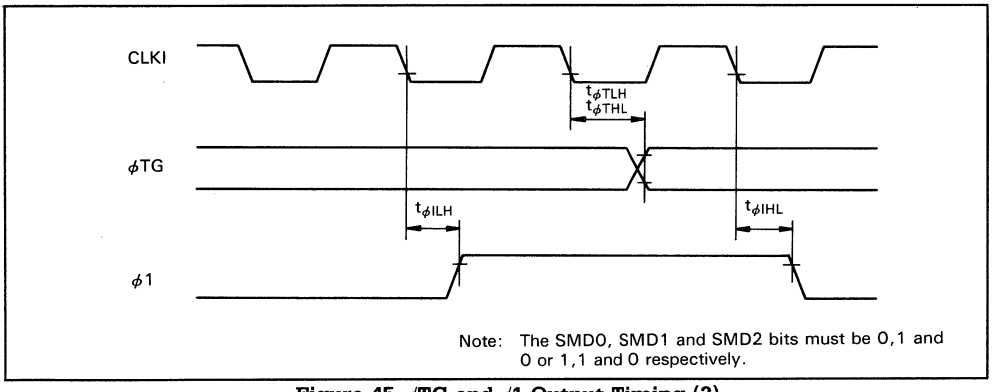


Figure 43 Application Output Timing



Note: The SMD0, SMD1 and SMD2 bits in the R09 register must be 0,0 and 0,1,0 and 0,0,0 and 1 or 1,0 and 1 respectively.

Figure 44 ϕTG and ϕ1 Output Timing (1)



Note: The SMD0, SMD1 and SMD2 bits must be 0,1 and 0 or 1,1 and 0 respectively.

Figure 45 ϕTG and ϕ1 Output Timing (2)

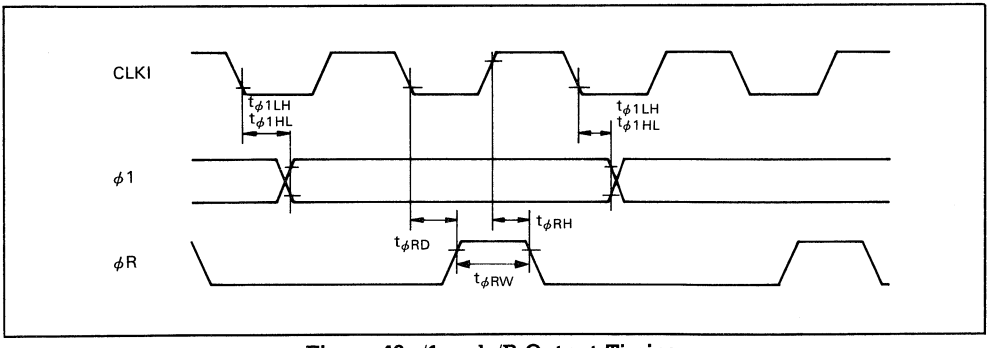


Figure 46 ϕ1 and ϕR Output Timing

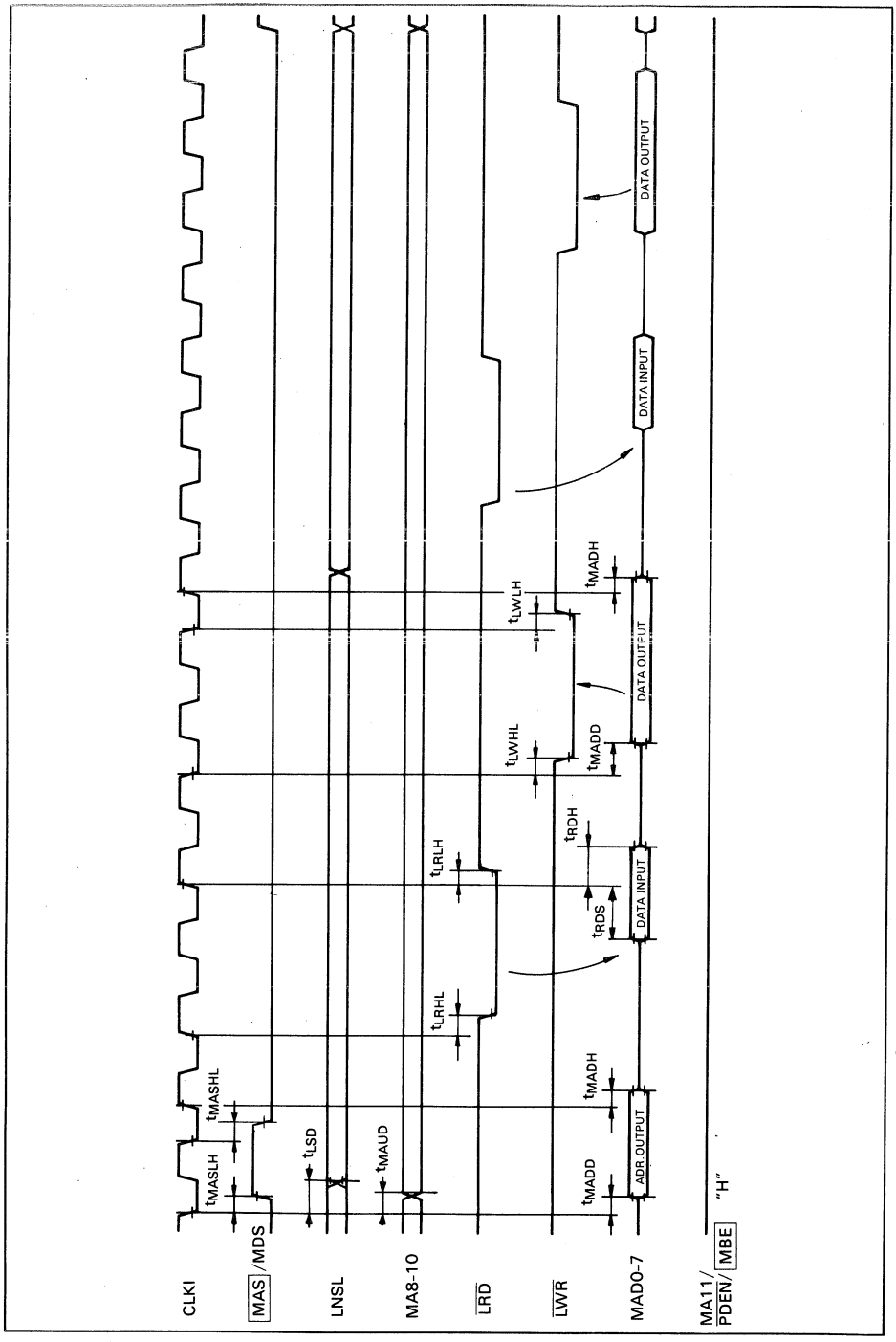


Figure 47 Memory Bus Interface Timing in A Mode (1) During Image Data Processing

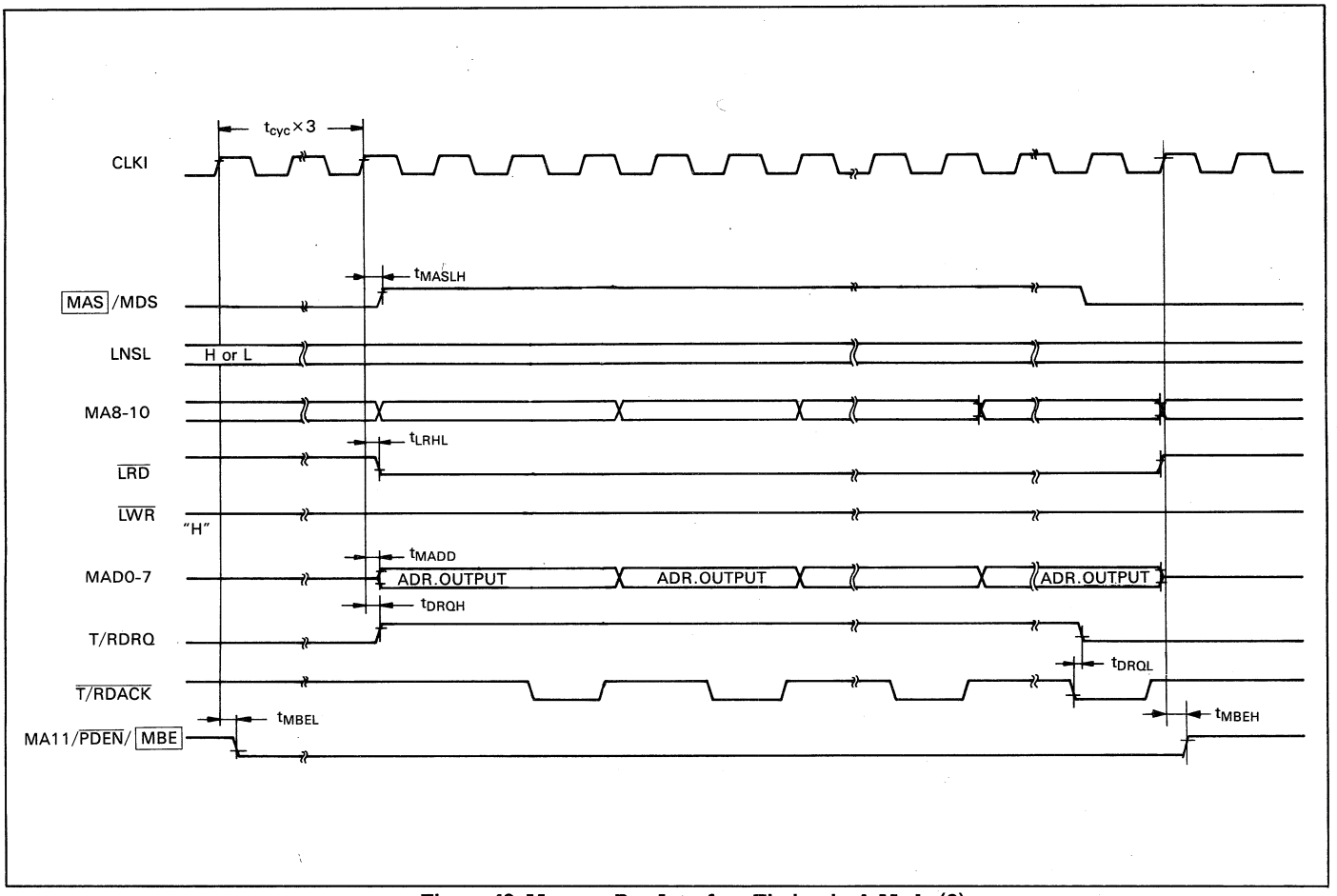


Figure 48 Memory Bus Interface Timing in A Mode (2) During Burst DMA Transfer

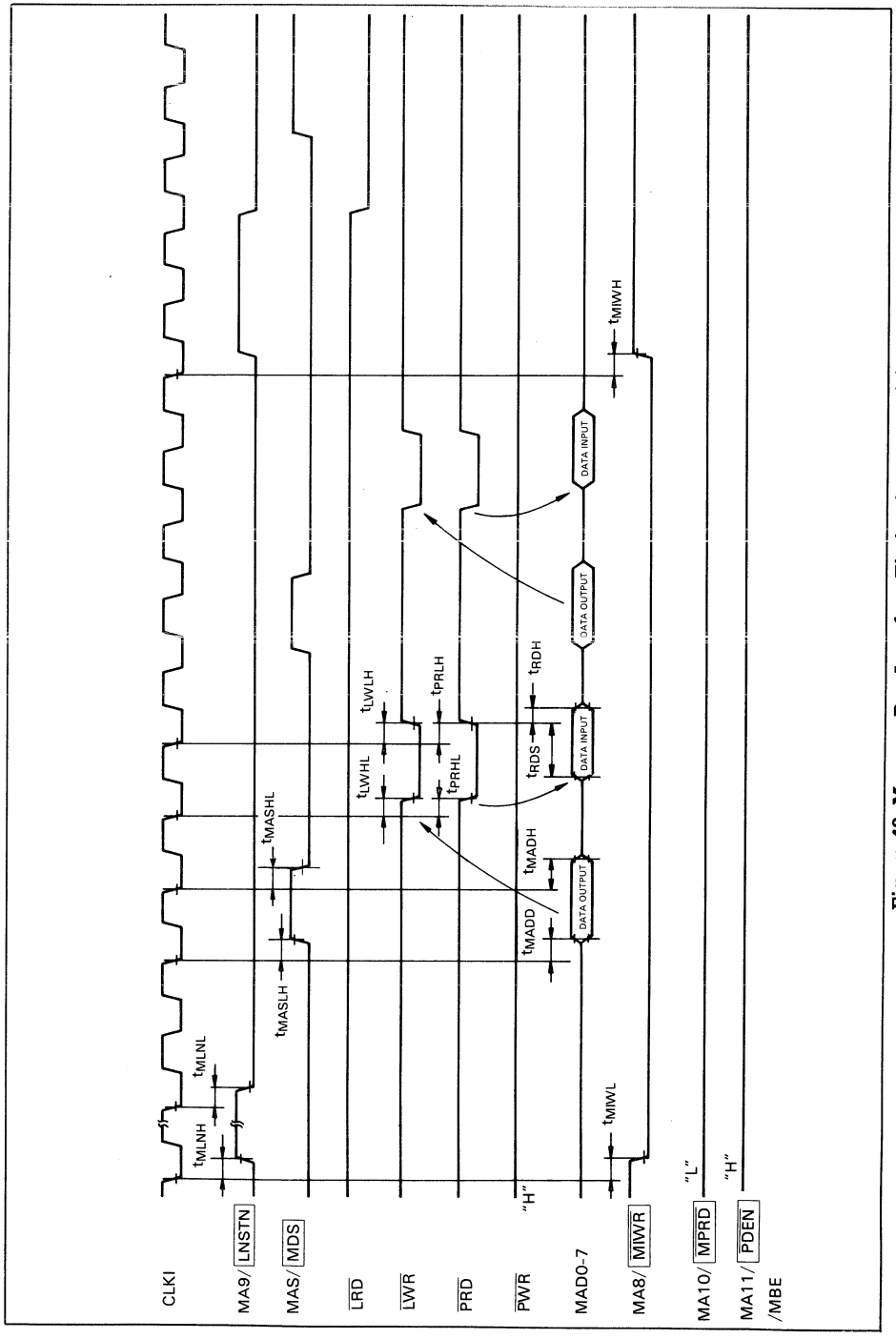


Figure 49 Memory Bus Interface Timing in B Mode (1)
During 4-bit Coded Data Output

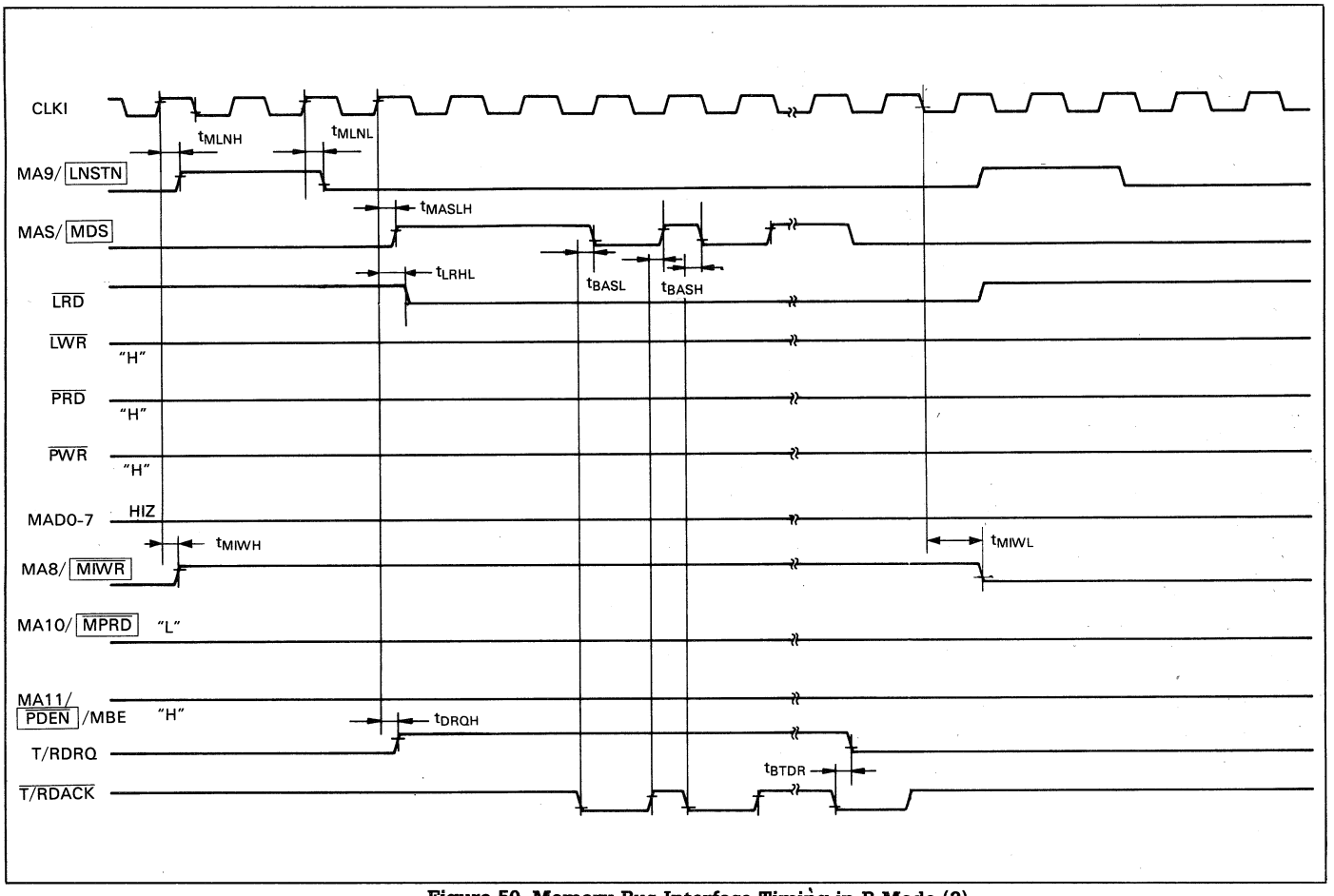


Figure 50 Memory Bus Interface Timing in B Mode (2) During Burst DMA Transfer

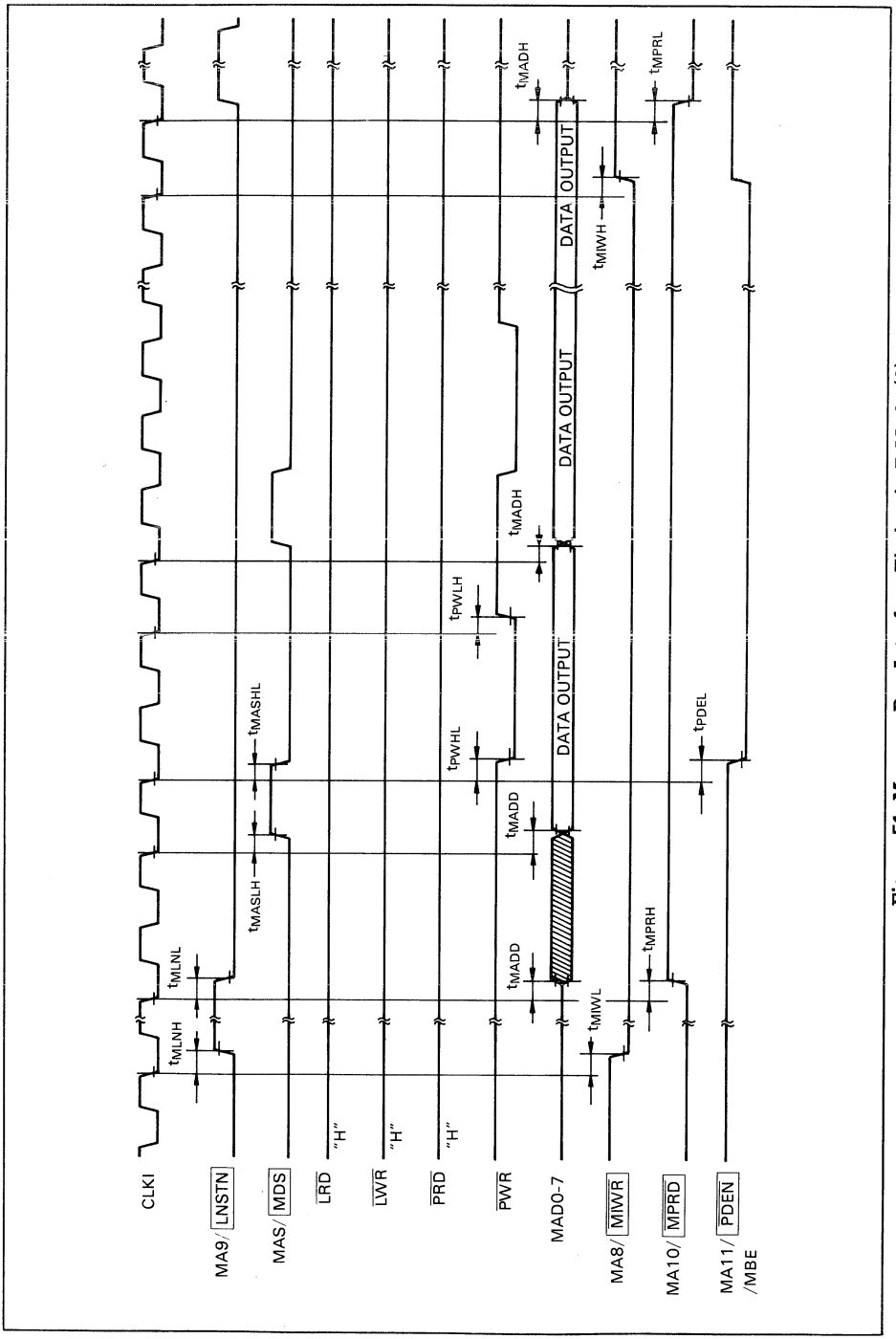


Figure 51 Memory Bus Interface Timing in B Mode (3)
During Pel Correction Data Detection

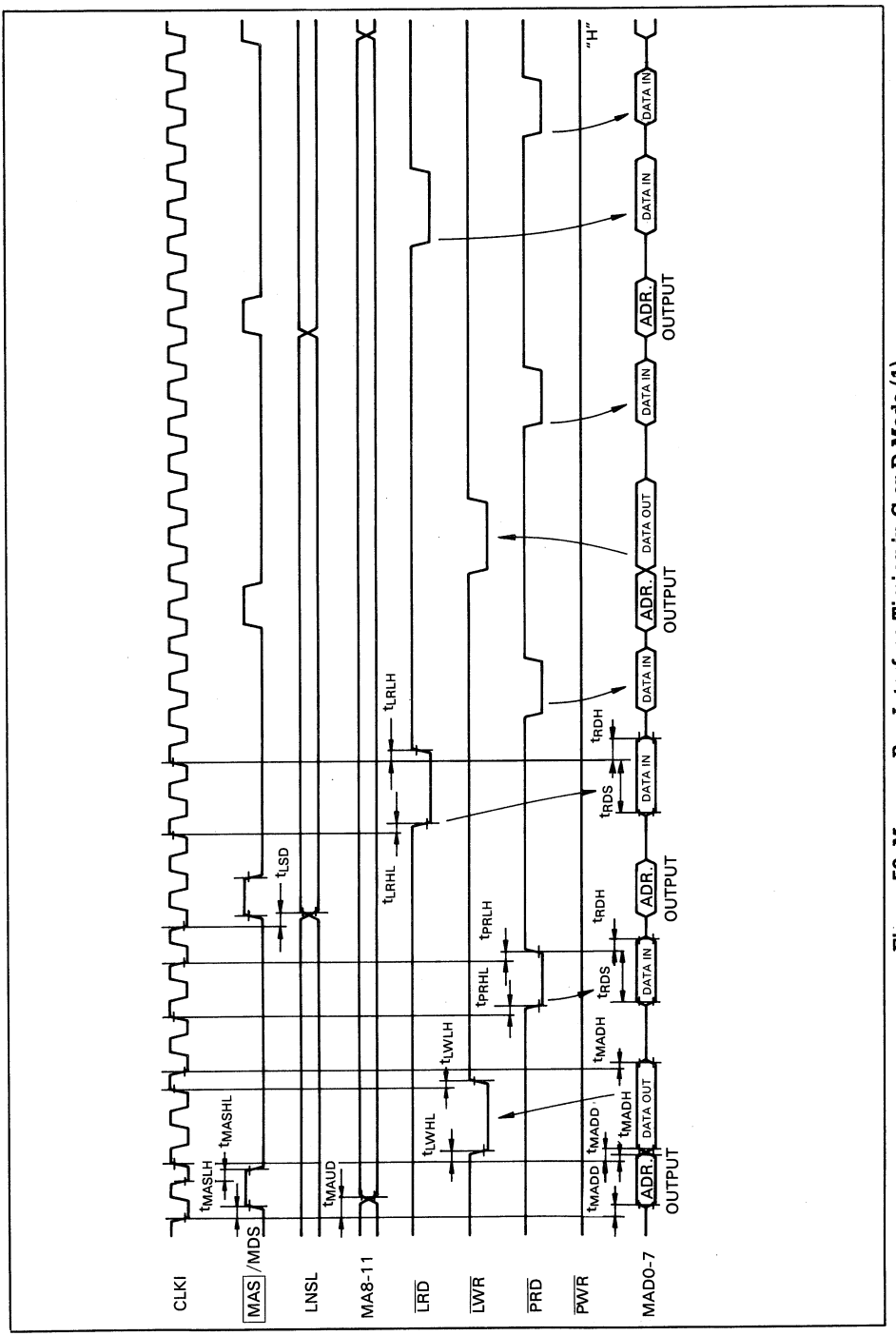


Figure 52 Memory Bus Interface Timing in C or D Mode (1)
During Image Data Processing

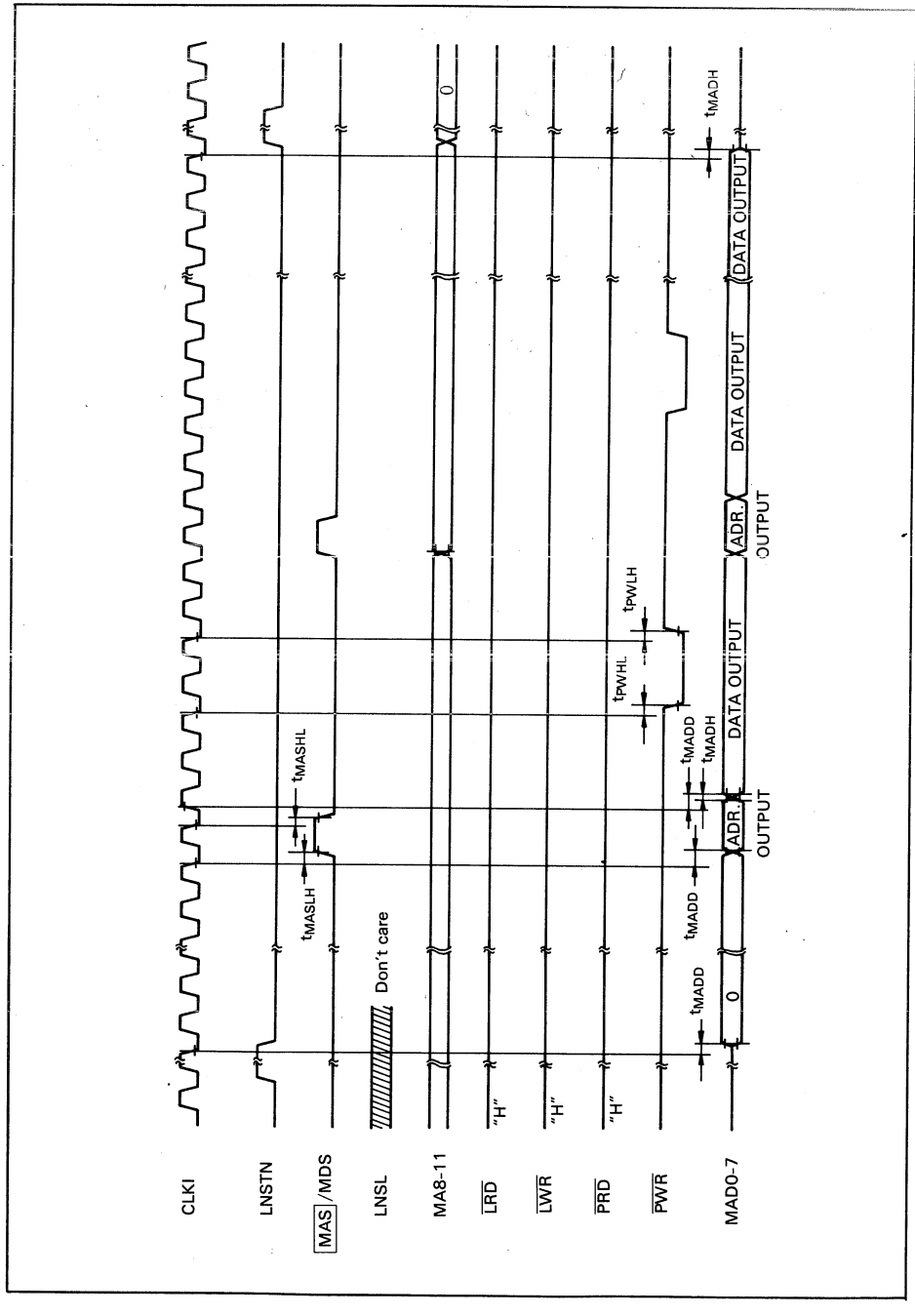


Figure 53 Memory Bus Interface Timing in C or D Mode (2)
During Pel Correction Data Detection

Refer to user's manual (No. AD-E0124) for detail of this product.

HD63085

Document Image Compression and Expansion Processor (DICEP)

The DICEP is an LSI that performs compression (encoding) and expansion (decoding) of the digital (two-value) data representing a document image.
The DICEP is used in G3 and G4 facsimile apparatus, intelligent copiers, word processors, telex, terminals, laser beam printers, file servers and other office automation systems.
The DICEP uses Modified Huffman (MH) coding scheme, Modified READ (MR) coding scheme and Modified MR (M^2R) coding scheme which are compatible with the CCITT (Comité Consultatif International Télégraphique et Téléphonique) recommendations for Group 3 and Group 4 facsimile apparatus.

Features

- Compatible with the CCITT Recommendations for Group 3 and Group 4 facsimile apparatus
- Simple MPU Command
  As the DICEP stores coding and decoding algorithms in the microprogram ROM as firmware, a single MPU command allows this LSI to encode (i.e. compress) or decode (i.e. expand) a scan line of digital data.
- High Speed Coding and Decoding
  The DICEP realizes high speed coding and decoding by:
  - including a changing pels* detector which can detect a changing pel contained in a word (8 bits/16 bits) of document image data within an instruction cycle time (at least 125nsec), and
  - including a decoded pels generator which can generate a word (8 bits/16 bits) of document image data within an instruction cycle time.

  *: The term 'picture element' is abbreviated to 'pel' in this document.
- Flexible System Configuration
  - Either 68 type MPU or 80 type MPU can be interfaced.
    The system bus has the size of 8 bits.
  - The DICEP has two bus interfaces; the system bus interface and the document image bus interface.
  - The DICEP may be interfaced with two independent buses (i.e. the system bus and the document image bus), while it may be interfaced with a common bus.
  - The size of the document image bus is selectable (8 bits/16 bits) depending on the word size of document image memory.
- High Speed DMA Transfer
  - The DICEP can perform direct memory access (DMA) transfer between an I/O device (scanner or printer) and the document image memory. The maximum transfer rate is 4M byte/sec.
  - With a DMA controller (DMAC) on the system bus, DMA transfers can be performed between a memory on the system bus and the DICEP.
- A Variety of Programmable Parameters
  Internal programmable registers present the DICEP flexibility to allow application to many kinds of systems.
  - The parameters can be changed before initiation of every command.
  - The length of a scan line is programmable from the word size of the document image memory (8 bits/16 bits) to 64K bits.
  - One of coding operation, decoding operation and transfer operation can be selected.
  - One of MH coding scheme, MR coding scheme, M^2R coding scheme and run length coding scheme can be selected.
  - The minimum length of a coded scan line is programmable from 0 to $2^{16}-1$ bits.
  - The number of End of Line (EOL) code words is programmable from 0 to $2^{16}-1$.
  - The number of Return to Control (RTC) code words is programmable from 0 to $2^{16}-1$.
  - The DICEP can code and decode a desired part of a document on a word (8 bits/16 bits) basis.
- Data Transfer between Buses
  The DICEP can perform data transfer between the system bus and the document image bus without coding or decoding.
- Octet Mode
  The DICEP provides Octet Mode. In this mode, a coded scan line or a coded page is 8-bit boundary conditioned.
- Run Length Coding Scheme
  The DICEP provides run length coding scheme in addition to MH coding, MR

coding and M²R coding.

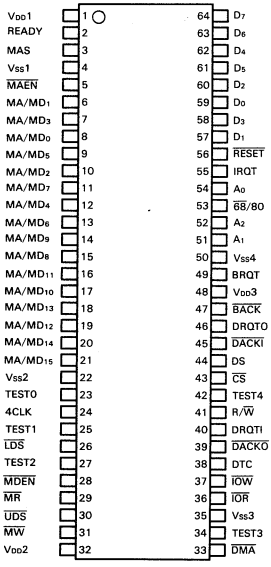
- High Operating Speed
  - —Instruction cycle time is 125 nsec min. (at system clock of 8 MHz max.)
  - —Input clock frequency is 32 MHz max.
- Package
  - —64 pin plastic shrink DIP (DP-64S)
  - —72 pin ceramic PGA (PC-72)

Ordering Information

Type No.	Input Clock	Package
HD63085P	2MHz to 32MHz	64 pin plastic shrink DIP (DP-64S)
HD63085YR		72 pin ceramic PGA (PC-72)

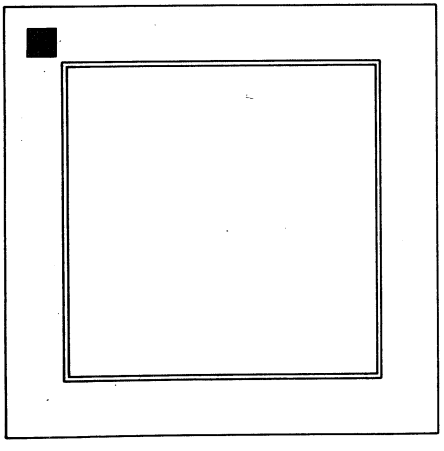
Pin Arrangement

●DP-64S

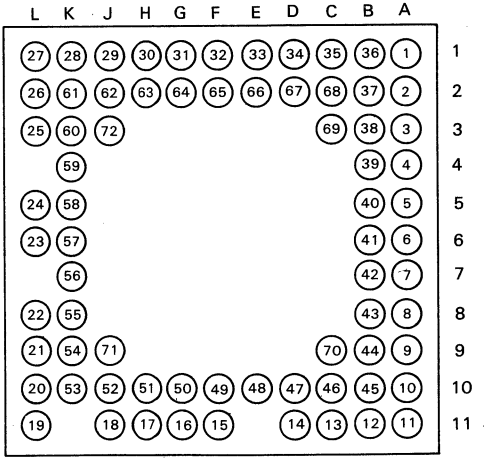


(Top View)

●PC-72



(Top View)



(Bottom View)

Pin Code	Pin No.	Mnemonic
A1	1	MA/MD_0
A2	2	MA/MD_2
A3	3	MA/MD_4
A4	4	MA/MD_6
A5	5	MA/MD_8
A6	6	MA/MD_{10}
A7	7	MA/MD_{12}
A8	8	MA/MD_{14}
A9	9	V_{SS}
A10	10	$TEST_0$
A11	11	4CLK
B1	36	MA/MD_1
B2	37	MA/MD_3
B3	38	MA/MD_5
B4	39	MA/MD_7
B5	40	MA/MD_9
B6	41	MA/MD_{11}
B7	42	MA/MD_{13}
B8	43	MA/MD_{15}
B9	44	V_{SS}
B10	45	$TEST_1$
B11	12	TDATA
C1	35	MAS
C2	68	$\overline{MAEN}$
C3	69	NC
C9	70	NC
C10	46	$\overline{LDS}$
C11	13	$\overline{UDS}$
D1	34	READY
D2	67	NC
D10	47	$\overline{MDEN}$
D11	14	$\overline{MW}$
E1	33	V_{DD}
E2	66	V_{DD}
E10	48	$\overline{MR}$
F1	32	D_6
F2	65	D_7
F10	49	$\overline{DMA}$
F11	15	SET
G1	31	D_4
G2	64	D_5
G10	50	V_{SS}
G11	16	V_{SS}
H1	30	D_2
H2	63	D_3
H10	51	$\overline{IOW}$
H11	17	$\overline{IOR}$
J1	29	D_0
J2	62	D_1
J3	72	NC
J9	71	NC
J10	52	$\overline{DACKO}$
J11	18	DTC
K1	28	V_{DD}
K2	61	V_{DD}
K3	60	IRQT
K4	59	A_0
K5	58	A_2
K6	57	BRQT
K7	56	DRQTO
K8	55	$\overline{CS}$
K9	54	NC
K10	53	DRQTI
L1	27	$\overline{RESET}$
L2	26	NC
L3	25	68/80
L5	24	A_1
L6	23	$\overline{BACK}$
L8	22	$\overline{DACKI}$
L9	21	DS
L10	20	AGE
L11	19	$R/\overline{W}$

Pin Descriptions (1 of 4)

〈System Bus Interface Pins〉

Signal	Pin No. PC-72	Pin No. DP-64S	I/O	Descriptions
$\overline{68}$/80	25	53	I	68/80 Mode select If $\overline{68}$/80 is low, it indicates that a 68 type MPU is interfaced with the DICEP. If high, it indicates that an 80 type MPU is interfaced.
A0 A1 A2	59 24 58	54 51 52	I	Addresses 0 to 2. These pins are connected to the 3 low-order bits of the system address bus to address the DICEP internal registers.
D0 D1 D2 D3 D4 D5 D6 D7	29 62 30 63 31 64 32 65	59 57 60 58 62 61 63 64	I/O, 3-state output	Data 0 to 7. These pins are interfaced with the system data bus to provide bidirectional communication between the MPU and the DICEP. The MPU can read/write the DICEP internal registers via D0 to D7 pins.
$\overline{CS}$	55	43	I	Chip select. A low level on this pin indicates that the MPU accesses a DICEP internal register.
DS	21	44	I	Data strobe. This pin must be connected to ϕ 2 clock pin of 68 type MPU or $\overline{RD}$ pin of 80 type MPU.
R/$\overline{W}$	19	41	I	Read/Write. This pin is connected to R/$\overline{W}$ pin of 68 type MPU or $\overline{WR}$ pin of 80 type MPU.
$\overline{RESET}$	27	56	I	A low level on $\overline{RESET}$ initializes the DICEP.
4CLK	11	24	I	4 Clock. The clock frequency is four times as high as the DICEP system clock frequency.
IRQT	60	55	O	Interrupt Request. The DICEP sends an interrupt request to the MPU by diving IRQT high upon completion of a command, end of a DMA transfer, occurrence of decoding error or reception of Return to Control (RTC) code words. MPU can know the cause of an interrupt by reading the Interrupt Request Register (IRR). When the MPU reads the IRR, IRQT returns to the low state.
DRQTO	56	46	O	DMA Request Output. The DICEP can drive DRQTO high to provide DMA request to the DMA Controller (DMAC) when: (1) coded data of more than 1 byte are stored in the FIFO during coding operation, (2) the FIFO has empty space of more than 1 byte during decoding operation or (3) Data Buffer Register (DBR) is ready for a read or write operation during data transfer between the system bus and the document image bus.
$\overline{DACKI}$	22	45	I	DMA Acknowlege Input. This input is a response to DRQTO. When $\overline{DACKI}$ goes low during coding operation or decoding operation, the FIFO is accessed. If $\overline{DACKI}$ goes low during data transfer between the system bus and the document image bus, the DBR is accessed. $\overline{CS}$ and $\overline{DACKI}$ must not be pulled low together.

DICEP Pin Descriptions (2 of 4)

〈Document Image Bus Interface Pins〉

Signal	Pin No. PC-72	Pin No. DP-64S	I/O	Descriptions
$\overline{BRQT}$	57	49	O	Bus Request. When BRQT is driven high by DICEP, it indicates to all other potential bus master devies on the document image bus that the DICEP desires to become the bus master. When the document image bus has no other potential master device, BRQT does not have to be connected to any line.
$\overline{BACK}$	23	47	I	Bus Acknowledge. This input is a response to the BRQT. A low level on $\overline{BACK}$ indicates that the DICEP is granted to be the master of the document image bus. This pin must be fixed low when the document image bus has no potential bus master devices other than the DICEP.
$\overline{MAEN}$	68	5	O	Memory Address Enable. When $\overline{MAEN}$ is driven low by DICEP, it indicates that the DICEP has become the master of the document image bus. If $\overline{MAEN}$ is high, all of three-state outputs interfaced with the document image bus are in high impedance state.
MAS	35	3	O	Memory address Strobe. When the DICEP drives MAS high, it indicates that the DICEP outputs an address onto MA/MD0 through MA/MD15.
$\overline{UDS}$	13	30	3-state output	When $\overline{UDS}$ is driven low by DICEP, it indicates that the DICEP uses the high-order byte of the document image bus.
$\overline{LDS}$	46	26	3-state output	When $\overline{LDS}$ is driven low by DICEP, it indicates that the DICEP uses the low-order byte of the document image bus.
$\overline{MDEN}$	47	28	O	Memory Data Bus Enable. When $\overline{MDEN}$ is driven low by DICEP, it indicates that there is a valid data on MA/MD0 through MA/MD15. This output is used to control the output of bidirectional bus buffer on the MA/MD0 through MA/MD15.
MA/MD0	1	8	I/O, 3-state output	Memory Address Data Bus. This is multiplexed address/data bus for document image bus operation. MA/MD0 to MA/MD15 are used as follows: 1) Output address lines when the $\overline{MAEN}$ is low and the MAS is high. 2) Input data lines when both $\overline{MAEN}$ and $\overline{MDEN}$ are low during read cycle. 3) Output data lines when both $\overline{MAEN}$ and $\overline{MDEN}$ are low during write cycle.
MA/MD1	36	6		
MA/MD2	2	10		
MA/MD3	37	7		
MA/MD4	3	12		
MA/MD5	38	9		
MA/MD6	4	13		
MA/MD7	39	11		
MA/MD8	5	15		
MA/MD9	40	14		
MA/MD10	6	17		
MA/MD11	41	16		
MA/MD12	7	19		
MA/MD13	42	18		
MA/MD14	8	20		
MA/MD15	43	21		

DICEP Pin Descriptions (3 of 4)

<Document Image Bus Interface Pins> (continued)

Signal	Pin No. PC-72	Pin No. DP-64S	I/O	Descriptions
$\overline{MR}$	48	29	3-state output	Memory Read. The DICEP drives $\overline{MR}$ low to read data from the document image memory.
$\overline{MW}$	14	31	3-state output	Memory Write. The DICEP drives $\overline{MW}$ low to write data into the document image memory.
$\overline{IOR}$	17	36	3-state output	I/O Read. The DICEP drives $\overline{IOR}$ low to read data from an I/O device on the document image bus. However, $\overline{IOR}$ is used only for data transfer between buses or for DMA transfer through the document image bus during coding operation.
$\overline{IOW}$	51	37	3-state output	I/O Write. The DICEP drives $\overline{IOW}$ low to write data into an I/O device on the document image bus. However, $\overline{IOW}$ is used only for data transfer between buses or for DMA transfer through the document image bus during decoding operation.
DRQTI	53	40	I	DMA Request Input. DRQTI is driven high when an I/O device on the document image bus sends a DMA request to the DICEP.
$\overline{DACKO}$	52	39	O	DMA Acknowledge Output. When this output is driven low, it notifies the peripherals on the document image bus that they have been granted a DMA operation.
$\overline{DMA}$	49	33	O	Direct Memory Access. When $\overline{DMA}$ is driven low, it indicates that the DICEP is executing a DMA transfer. During coding operation, data is transferred from the I/O device (scanner) to the document image memory. During decoding operation, data is transferred from the document image memory to the I/O device (printer).
DTC	18	38	O	DMA Terminal Count. When DTC is driven high, it indicates that DMA transfer of a scan line has been completed.
READY	34	2	I	When READY is high during a read or write to the document image memory or the I/O devices, it indicates that the memory or I/O device is ready to send or receive data. If READY is low, the DICEP will wait until READY becomes high.

DICEP Pin Descriptions (4 of 4)

<Power Supplies And Other>

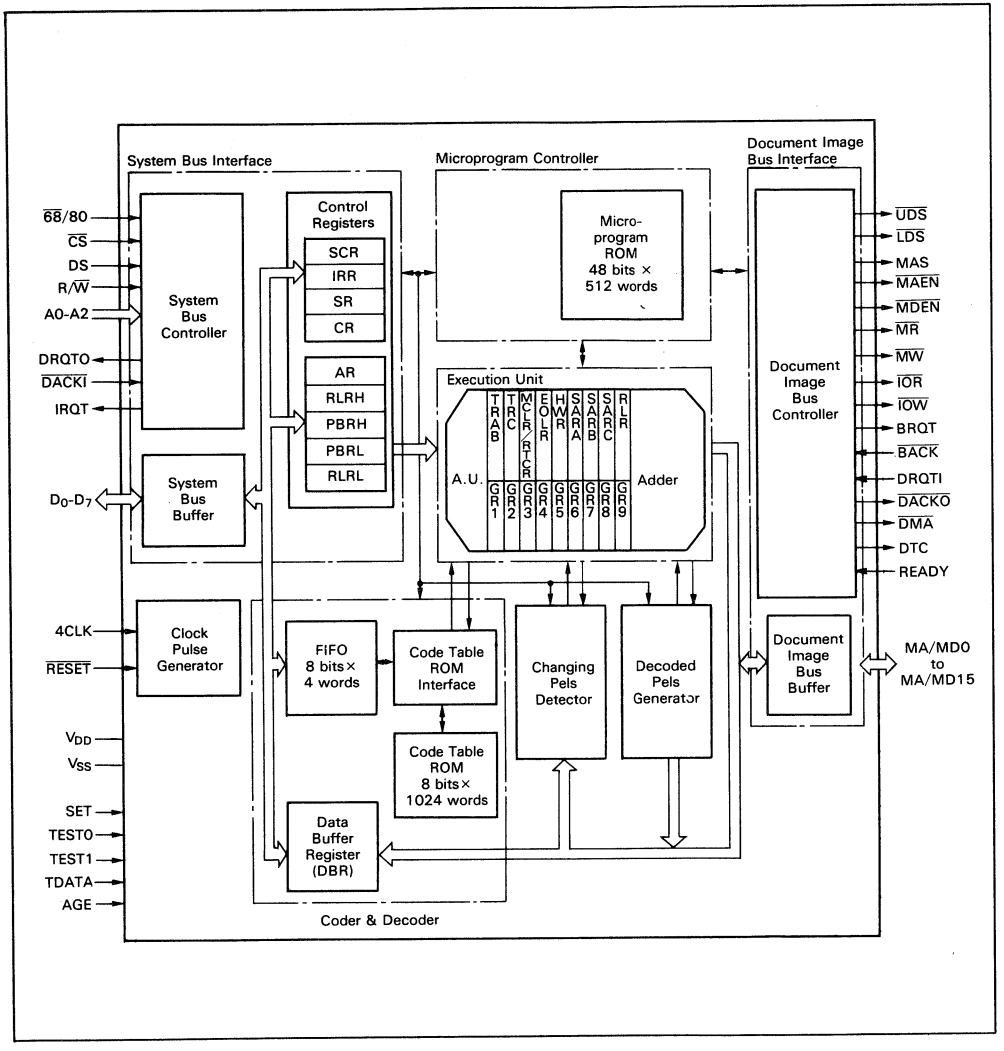
Signal	Pin No. PC-72	Pin No. DP-64S	I/O	Descriptions
V_{DD}	28,33, 61,66	1,32, 48	–	Supply voltage (+5V)
V_{SS}	9,16, 44,50	4,22, 35,50	–	Ground
SET	15	34	I	These pins must be fixed low.
TEST0	10	23		
TEST1	45	25		
TDATA	12	27		
AGE	20	42		

DICEP Functional Summary

Item	Function
Coding Scheme	HM, MR, M^2R, Run Length
Maximum Scan-line Length	64k pels
Document Image Bus Memory Address Space size	Document Image Memory ·····64k bytes I/O Devices ·····64k bytes
Maximum DMA Transfer Rate	4M byte/sec *
Maximum Changing Pels Detect Speed	3.2M byte/sec *
Maximum Decoded Pels Generation Speed	3.2M byte/sec *

* : Input clock frequency is 32 MHz.

Block Diagram



Block Configurations

System Bus Interface

The system bus interface has a timing specification compatible with 8-bit MPUs (HD6800/HD64180). This block includes control registers which can be directly accessed by the MPU.

Microprogram Controller

The microprogram controller stores coding and decoding programs in the microprogram ROM to control all other blocks of the DICEP. This block consists of the microprogram ROM with 512 words of 48 bits, the sequence controller and the pipeline register.

Execution Unit

The execution unit generates document image memory addresses, and calculates the position of changing pels, run lengths, and the relative distance between changing pels on the coding line and those on the reference line.
This block consists of eighteen 16-bit registers, the arithmetic unit (A.U.) and the adder. Nine registers (TRAB, TRC, MCLR/RTCR, EOLR, HWR, SARA, SARB, SARC, and RLR) can be programmed by the MPU via the control registers in the system bus interface. These nine registers are called "parameter registers".

Coder and Decoder

The coder generates the addresses of the code table ROM from input run lengths or relative distances, and generates appropriate code words by looking up the code table ROM.
On the other hand, the decoder generates the addresses of the code table ROM from input code words, and generates run lengths or relative addresses by looking up the code table ROM.

This block consists of the code table ROM with 1024 words of 8 bits, the code table ROM interface, the First-In First-Out memory (FIFO) with 4 words of 8 bits, and the Data Buffer Register (DBR). The code table ROM stores the data which is referenced for coding and decoding operations. The code table ROM interface generates the addresses of the code table ROM. The FIFO temporarily stores code words during coding or decoding operation. The DBR is a intermediate buffer which is used to transfer data between the system bus and the document image bus.

Changing Pels Detector

The changing pels detector detects a changing pel whose color (white or black) is different from that of the previous pel on the same scan line. It can detect a changing pel in a word (8 bits/16 bits) of the document image memory within an instruction cycle time.
This block consists of two changing pels detectors: the reference line detector and the coding line detector. For detailed infomation of the reference line and the coding line.

Decoded Pels Generator

The decoded pels generator can generate at most a word (8 bits/16 bits) of decoded pels within an instruction cycle time, using the information of the positions of changing pels.

Document Image Bus Interface

The document image bus interface provides an interface between the DICEP and the document image bus. It has a 16-bit multiplexed address/data bus.
This block has the following functions:
- it has bus arbitration technique.
- it outputs control signals for the document image bus.

System Configurations

Independent Bus System

Figure 1 shows a system configuration diagram as an example of the independent bus system.
The features of this system are as follows:

- This system includes two independent buses (the system bus and the document image bus)
- The DICEP can perform document image bus operation independently of the MPU, which enhances the system throughput.
- This type of system can also be used in G4 facsimile apparatus.

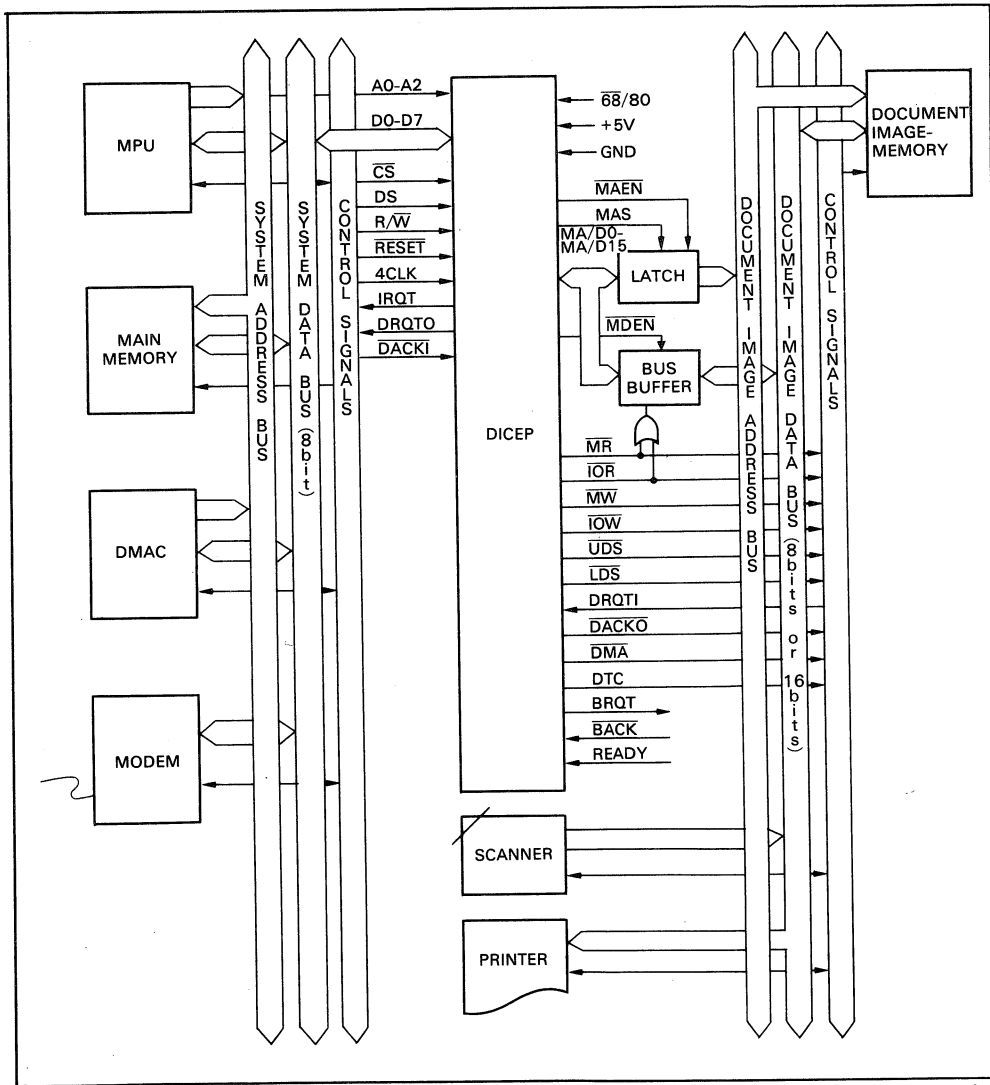


Figure 1 System Configuration Diagram (an Example of Independent Bus System)

Common Bus System

Figure 2 shows a system configuration diagram as an example of the common bus system.

The features of this system are as follows:

- This system includes a common bus which is used as both the system bus and the document image bus.
- The bus arbitration technique realizes this system.
- The MPU can read/write document image data directly.
- This type of system is recommended to be used in G3 facsimile apparatus.

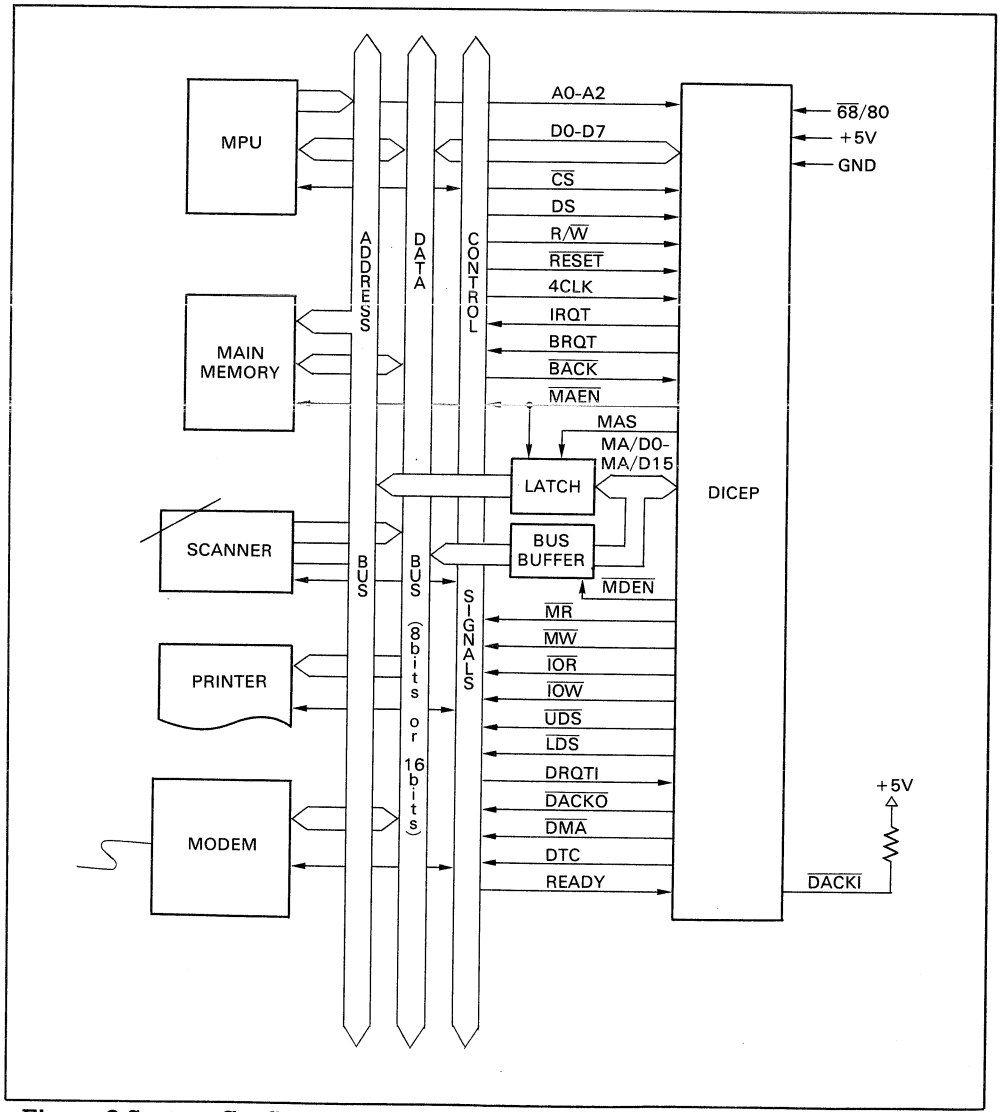


Figure 2 System Configuration Diagram (an Example of the Common Bus System)

Internal Registers

Figure 3 illustrates a DICEP register programming model. DICEP registers can be classified into two groups: registers that are directly accessible by the MPU, and registers that can be accessed via the parameter buffer registers (PBRH, PBRL). The following describes the access methods used for each type of register.

1. Registers directly accessible from the MPU

The control registers (CR), data buffer register (DBR) and FIFO can be accessed directly from the MPU, in accordance with A_0 to A_2, when $\overline{CS}$ is low level.

Table 1 shows the directly accessible registers.

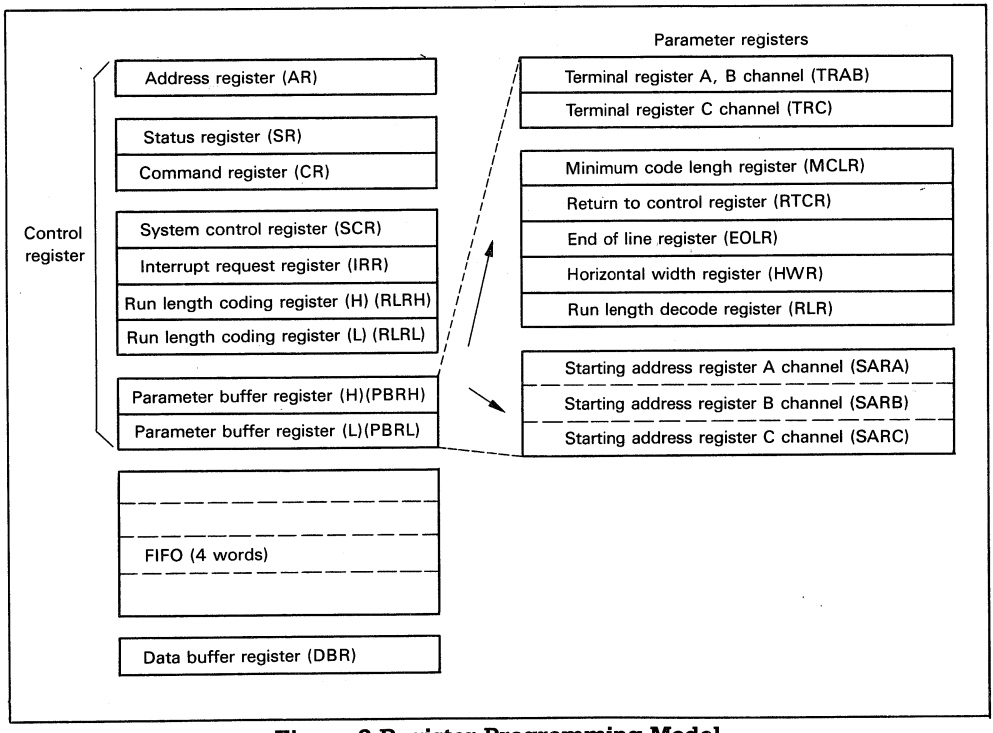


Figure 3 Register Programming Model

Table 1 Control Registers, FIFO and DBR

Address			R/W	Symbol	Full Name
A2	A1	A0			
0	0	0	R/W	SCR	System Control Register
0	0	1	R	IRR	Interrupt Request Register
0	1	0	R	SR	Staus Register
			W	CR	Command Register
0	1	1	R/W	FIFO	First-In First-Out Memory
1	0	0	R/W	DBR	Data Buffer Register
1	0	1	R/W	AR	Address Register
1	1	0	R	RLRH	Run Length coding Register High
			W	PBRH	Parameter Buffer Register High
1	1	1	R	RLRL	Run Length coding Register Low
			W	PBRL	Parameter Buffer Register Low

Table 2 Command

3	2	1	0	Command
0	0	0	0	Encode Initial Command
0	0	0	1	MH Coding Command
0	0	1	1	Transfer Command
0	1	0	1	MR One Dimensional Coding Command
0	1	1	0	MR Two Dimensional Coding Command
1	0	0	0	Decode Initial Command
1	0	0	1	MH Decoding Command
1	0	1	0	MR Decoding Command
1	0	1	1	Transfer Command

System Control Register (SCR)

The SCR is an 8-bit read/write register which controls several DICEP options.
The MPU must write desired bits to the SCR before issuing a command. Reading this register, the MPU can know the current status information of the DICEP.
During reset, the SCR is initialized to zero.
The SCR is shown in figure 4 and the individual bits are defined in the following paragraphs.

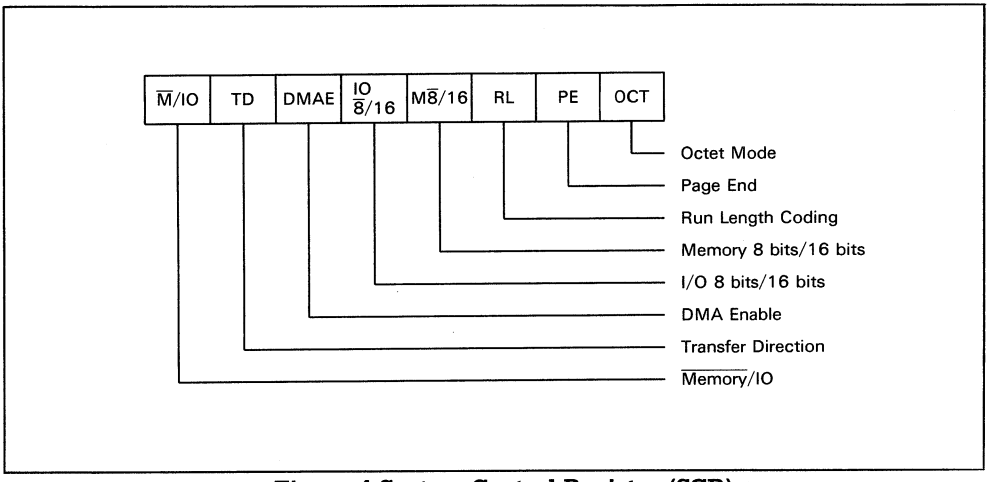


Figure 4 System Control Register (SCR)

Bit 0 Octet Mode bit (OCT)

If this bit is set, coded data must be 8-bit boundary conditioned.
when resulting coded data does not meet this requirement, Fill bits will be automatically added just after a data line to ensure that coded data is 8-bit boundary conditioned.
If this bit is clear, all of the coded data may not be sent to a memory on the system bus, because the transfer of data through the system bus is performed on 8-bit basis.
In M^2R coding scheme, however, fill bits must not added in any other place than the end of a page. Thus, when this coding scheme is used, OCT bit can be set only at the end of a page.

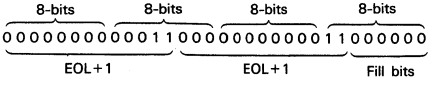
Bit 1 Page End bit (PE)

This bit must be set when a page of data has been coded.
If the MPU issues a coding command with PE set, the DICEP will generate the following RTC code words:

- If the MPU issues MH coding command, the DICEP will generate EOL code words. The number of EOLs must be specified by End of Line Register (EOLR)*.
- If the MPU issues MR one dimensional coding command, the DICEP will generate EOL + 1 code words. The number of EOL + 1 code words must be specified by EOLR.
- If the MPU issues MR two dimensional coding command, the DICEP will generate EOL + 0 code words. The number of EOL + 0 code words must be specified by EOLR.

(Note *) The End of Line Register (EOLR) specifies the number of EOL code words to be generated by the DICEP.

If the MPU issues MR one dimensional coding command when the EOLR contains "2" and both OCT bit and PE bit are set, the DICEP will generate the following code bits (provided preceding coded data are 8-bit boundary conditioned).



Bit 2 Run Length Coding bit (RL)

If the MPU issues MH coding command, MR one dimensional coding command or MH decoding command when Run Length coding bit is set, the DICEP will perform run length coding or decoding.
However, the MPU must not issue MR two dimensional coding command or MR decoding command with this bit set.

Bit 3 Memory 8 bits/16 bits (M8/16)

The M8/16 bit is used to specify the size of the document image bus. If the M8/16 bit is set, the document image bus has a 16-bit size; if clear, the size is 8 bits.

Bit 4 I/O 8 bits/16 bits (IO8/16)

The IO8/16 bit is used to specify the word size of the I/O devices on the document image bus.
If the IO8/16 bit is set, the I/O devices has a 16-bit wide size; if clear, the size is 8 bits.

!!CAUTION!!

When the document image bus has a 8-bit size, the I/O devices must not have a 16-bit word size. Thus, if M8/16 is clear, IO8/16 must not be set.

Bit 5 DMA Enable bit (DMAE)

The DMAE bit is used to enable DMA operation between the I/O devices and the document image memory.
If the DMAE bit is set, the DICEP accepts the DRQTI signal from the I/O devices.
The DMAE bit is cleared at the completion of DMA transfer of a scan line.

Bit 6 Transfer Direction bit (TD)

The TD bit is used to determine the direction of data transfer between the system bus and the document image bus. If the TD bit is clear, data is transferred from the system bus to the document image bus; if set, data is transferred from the document image bus to the system bus.

Bit 7 $\overline{\text{Memory}}$/IO bit ($\overline{\text{M}}$/IO)

The $\overline{\text{M}}$/IO bit is used during data transfer between the system bus and the document image bus. If the M/IO bit is clear, data will be transferred from or to the document image memory; if set, data will be transferred from or to the I/O devices.

Command Register (CR)

The CR is a 4-bit write-only register which is used to specify a command for the DICEP operation.
Responding to an MPU write to the CR, the DICEP starts execution of an indicated command. In other words, the MPU can issue the desired command by setting the corresponding CR bits.
All of the CR bits are cleared after initialization by $\overline{\text{RESET}}$ input.
When using this register, the user must give consideration to the followings:

- If the MPU writes a new data into the CR during a command execution, the DICEP may enter a new command execution without completing the current command.
- The state of Bit 3 in the CR determines the direction of DMA transfer through the document image bus.
  Be careful that changing the state of this bit during DMA transfer changes the direction of transfer.
- The direction of DMA transfer when an encode command is issued while DMA transfer is being performed is from I/O to image memory. Conversely, the direction of DMA transfer when a decode command is issued while DMA transfer is being performed is from image memory to I/O.

Figure 5 shows the relationship between the individual CR bits and the commands to be specified.

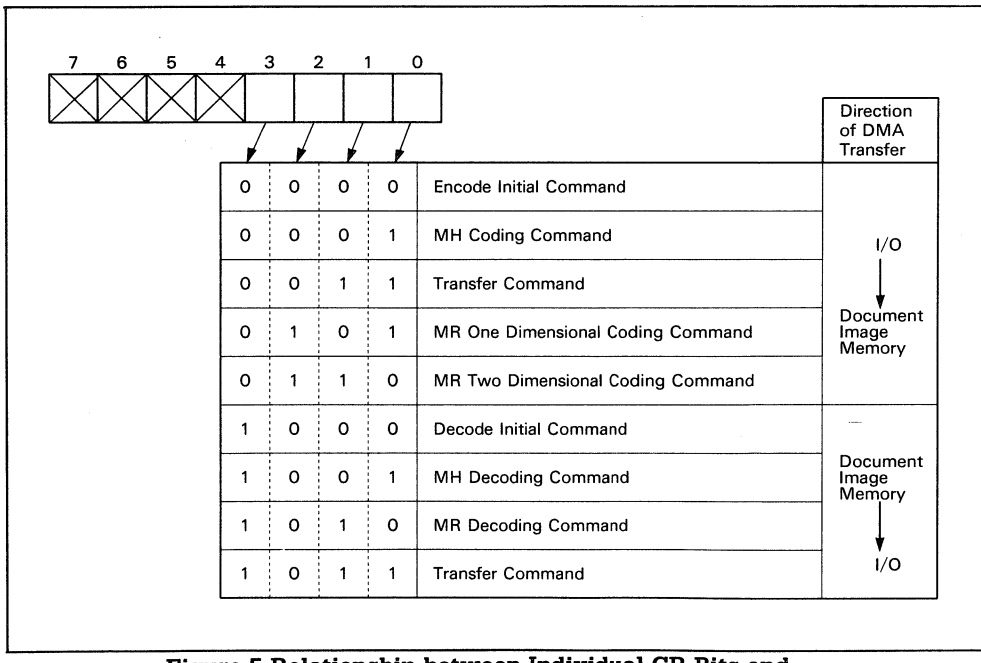


Figure 5 Relationship between Individual CR Bits and the Command to be Specified

The individual commands to be specified are described in the following paragraphs.

Encode Initial Command

The Encode Initial Command initializes the DICEP for coding operation, which clears the FIFO and clears the FIFO Ready Flag bit in the Status Register (SR). We recommend that this command should be issued at the start of a page coding.
The MPU must not issue the Encode Initial Command during DMA operation, because no interrupt is requested to the MPU at the completion of this command.

MH Coding Command

When the MPU issues the MH coding command, the DICEP will execute MH coding if the RL bit in the SCR is clear; if the RL bit is set, the DICEP executes run length coding.

MR One Dimensional Coding Command

When the MPU issues the MR one dimensional coding command, the DICEP will execute the one dimensional coding in the MR coding scheme if the RL bit is clear; if the RL bit is set, the DICEP executes run length coding.

MR Two Dimensional Coding Command

When the MPU issues the MR two dimensional coding command, the DICEP will execute the two dimensional coding in the MR coding scheme or the M^2R coding.

Transfer Command

When the MPU issues the transfer command, the DICEP will execute the transfer of data between the system bus and the document image bus. The direction of the transfer depends on the TD bit in the SCR.

Decode Initial Command

When the MPU issues the decode initial command, the DICEP is initialized for decoding operation. The FIFO is cleared and the FIFO Ready Flag bit in the Status Register (SR) is set to one.
The decode initial command must not be issued during DMA transfer.

MH Decoding Command

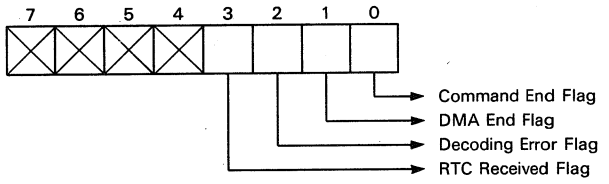
When the MPU issues the MH decoding command, the DICEP will execute the MH decoding if the RL bit in the SCR is clear; if the RL bit is set, the DICEP executes the run length decoding.

MR Decoding Command

When the MPU issues the MR decoding command, the DICEP will execute the MR decoding or the M^2R decoding.

Interrupt Request Register (IRR)

The IRR is a 4-bit read-only register. When the MPU receives an interrupt request from the DICEP, it can know what is the cause of the interrupt by reading the IRR. After reset, the IRR is cleared to zero. Figure 6 shows the relationship between the causes of interrupts and the states of individual IRR bits.



3	2	1	0	Indicates:
0	0	0	1	Completion of a Command
0	1	0	1	Occurrence of Decoding Error
1	0	0	1	Reception of RTC Code
		1	0	Completion of DMA Transfer
		0	0	No Interrupt Cause

Figure 6 Relationship between Causes of Interrupts and States of IRR Bits

The individual bits are defined as follows.

Bit 0 Command End Flag bit

This bit is set to indicate that a command has been executed to completion. During a decoding operation, this bit can give the MPU more information depending on the state of bit 2 or bit 3.

Bit 1 DMA End Flag bit

This bit is set to indicate that DMA transfer of a scan line has been completed.
When a command execution or a DMA operation is completed, either Bit 0 or Bit 1 is set to one to assert the IRQT. Bit 0 and Bit 1 never be set together. An MPU read of IRR clears Bit 0 and Bit 1 to negate the IRQT.
If the MPU reads the IRR when the IRQT is negated, the interrupt which occurs during the read cycle may not affect the IRR or the IRQT.

Bit 2 Decoding Error Flag bit

If both the Decoding Error Flag bit and the Command End Flag bit are set during a decoding operation, it indicates that an error has been found in the coded data.

Bit 3 RTC Received Flag bit

If both the RTC Received Flag bit and the Command End Flag bit are set during a decoding operation, it indicates that the DICEP has received RTC codes.
Both Bit 2 and Bit 3 are cleared to zero after a new command is issued.

First-In First-Out Memory (FIFO)

The FIFO is 4 words × 8 bits memory which is positioned in the Encoder and Decoder block of the DICEP. The FIFO stores coded data temporarily when the DICEP performs a coding or decoding operation.
During a coding operation, the DICEP encodes an image data and stores the coded data in the FIFO. Then either the MPU or the DMAC transfers the data into a memory on the system bus.
During a decoding operation, either the MPU or the DMAC transfers a coded data from a memory on the system bus to the FIFO. Then the DICEP decodes the data.
The state of the FIFO affects the FIFO Ready Fiag bit in the Status Register (SR) and the DRQTO signal.

Data Buffer Register (DBR)

The DBR is a bidirectional register which stores data temporarily during data transfer between the system bus and the document image bus.
If the TD bit in the SCR is zero, either the MPU or the DMAC transfers data from a memory on the system bus to the DBR.
Then the DICEP writes the data into the peripherals on the document image bus responding to the transfer command.
If the TD bit is one, the DICEP reads a data from a peripheral on the document image bus and writes the data into the DBR responding to the transfer command. Then either the MPU or the DMAC reads the data from the DBR.
The state of the DBR affects the DBR Ready Flag bit in the Status Register (SR) and the DRQTO signal.

Address Register (AR)

The AR is used to specify the address of a parameter register. In addition, the MPU can know which parameter is specified by reading the AR.
The MPU must verify that the PBR Ready Flag bit is set before changing the contents of the AR.
The AR is shown in figure 7.

The five low-order bits of the AR can be read and written, but Bit 7 is read-only bit.

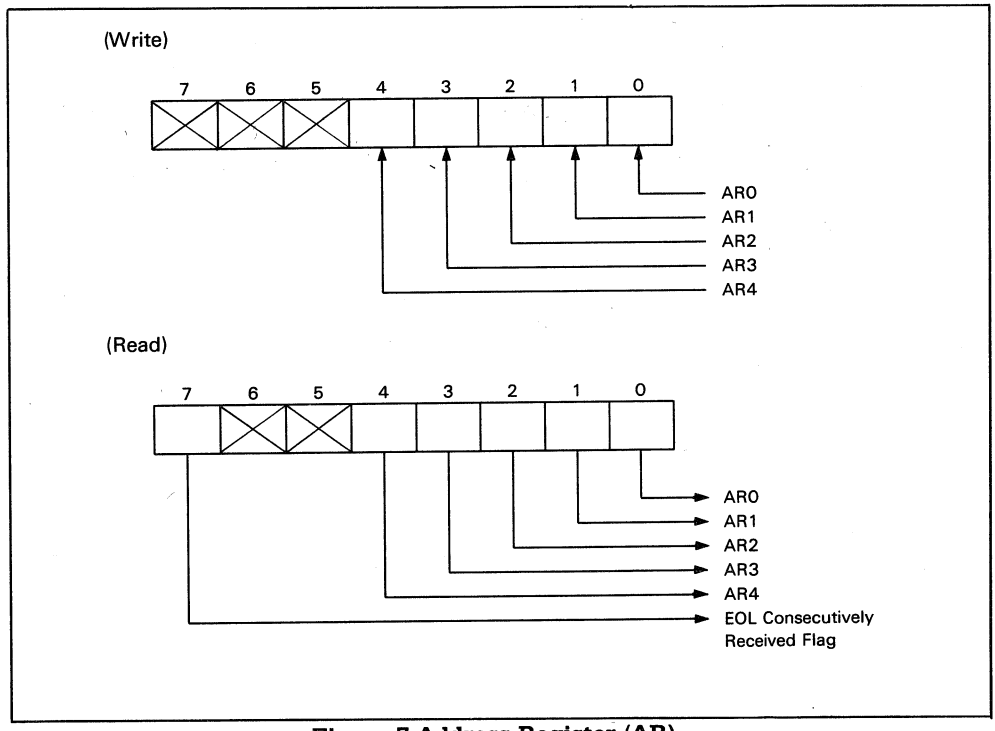


Figure 7 Address Register (AR)

Bit 7 in the Address Register has following features:

- becomes zero when the DICEP has received two or more consecutive EOLs, and
- becomes one after the $\overline{\text{RESET}}$ input or an initiation of a decoding command.

Because of these features, the Bit 7 is used as EOL Consecutively Received Flag bit during a decoding operation.

Figure 8 shows the relationship between the coded data received by the DICEP during a decoding operation and the Bit 7.

When receiving an EOL, the DICEP recognizes that a command is completed, then applies an interrupt to the MPU. Responding to this interrupt, the MPU issues a decoding command.
Issuing an decoding command clears the Bit 7 to one. Then if the DICEP receives another EOL code word, the Bit 7 is set to zero. If the DICEP does not receive any more EOL code word, the Bit 7 remains one.

Thus, if the MPU reads the AR after a decoding of a scan line prior to an initiation of a new command, the state of the Bit 7 indicates whether the DICEP has received two or more consecutive EOL code words at the start of the decoded scan line.

If the Bit 7 is zero, it indicates that the DICEP has received two or more EOL code words just before the data line. If the Bit 7 is one, it indicates that the DICEP has received an EOL code word just before the data line.

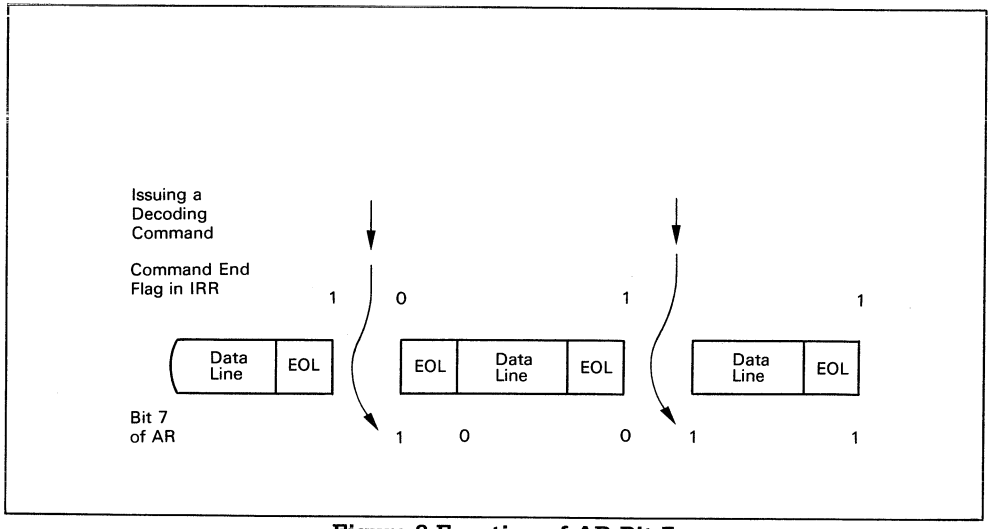


Figure 8 Function of AR Bit 7

Parameter Buffer Register Low and Parameter Buffer Register High (PBRL & PBRH)

If the MPU writes a data into the PBRH, then the PBRL, the data will be automatically written as a parameter into a parameter register specified by the AR.
The MPU must verify that the PBR Ready Flag bit is set before the write to the PBRH and the PBRL.
The AR, the PBRL and the PBRH will contain the current data until a new data is written.

Run Length Register Low and Run Length Register High (RLRL & RLRH)

The MPU can monitor the run length by reading the RLRH, then the RLRL during the run length coding operation.
Before the read of these registers, the MPU must verify that the RLR Ready Flag bit in the Status Register (SR) is set.

Status Register (SR)

This 4-bit read-only register indicates to the MPU the current status information of the FIFO, the DBR, the PBRH, the PBRL, the RLRH and the RLRL.
The SR is shown in figure 9 and the individual bits are defined as follows.

Bit 4 RLR Ready Flag bit

This bit is set to indicate that the RLRH and the RLRL contain valid run length codes. This bit is cleared after the MPU issues a new command.

Bit 5 FIFO Ready Flag bit

If this bit is set during a coding opration, it indicates that the FIFO contains valid coded data of more than 1 byte, which allows either the MPU or the DMAC to read the data from the FIFO.
If set during a decoding operation, it indicates that the FIFO has empty area of more than 1 byte, which allows either the MPU or the DMAC to write coded data into the FIFO. Thus, this bit is cleared after the MPU issues the encode initial command and set after the MPU issues the decode initial command.
During a coding or decoding operation, the state of this flag bit affects the DRQTO signal.
This bit is cleared after initialization by the $\overline{\text{RESET}}$ input.

Bit 6 DBR Ready Flag bit

During the transfer of data from the system bus to the document image bus (that is, when the TD bit in the SCR is clear), this flag is set to indicate that the DBR is empty, which allows either the MPU or the DMAC to write data into the DBR.
During the transfer of data from the document image bus to the system bus (that is, when the TD bit is set), this flag is set to indicate that the DBR contains valid data, which allows either the MPU or the DMAC to read the data from the DBR.
If the MPU issues the data transfer command with the TD bit clear, the DBR Ready Flag bit will be set to one. If the MPU issues the transfer command when the TD bit is set, the DBR Ready Flag bit will be clear until the DICEP writes a new data into the DBR.
While the transfer command is executed, this flag affects the DRQTO signal.

Bit 7 PBR Ready Flag bit

This bit is set to indicate that both the PBRL and the PBRH are empty, which indicates that the MPU can write a new data into the PBRL and the PBRH. This flag bit is set after initialization by the $\overline{\text{RESET}}$ input or the initiation of a new command.

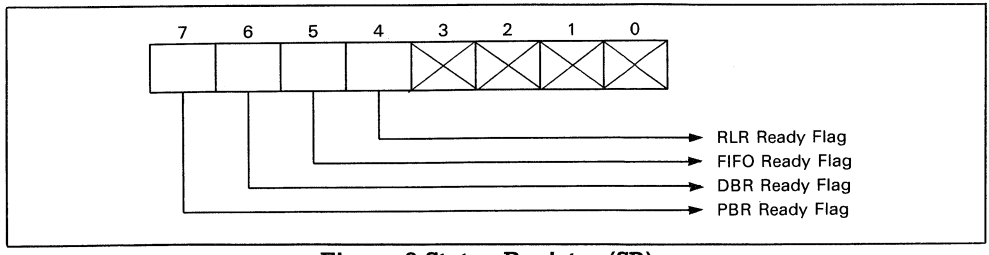


Figure 9 Status Register (SR)

Parameter Registers

The DICEP provides Parameter registers as listed in table 3

Table 3 Parameter Registers

Address (AR)							
AR4	**AR3**	**AR2**	**AR1**	**AR0**	**Coding**	**Decoding**	**Name**
0	0	0	0	0	○	○	Terminal Register A, B Channel (TRAB)
0	0	0	0	1	○	○	Terminal Register C Channel (TRC)
0	0	0	1	0	○	Not Uesd	Minimum Code Length Register (MCLR)
					Not Uesd	○	Return to Control Register (RTCR)
0	0	0	1	1	○	○	End of Line Register (EOLR)
0	0	1	0	0	○	○	Horizontal Width Register (HMR)
0	0	1	0	1	○	○	Starting Address Register A Channel (SARA)
0	0	1	1	0	○	○	Starting Address Register B Channel (SARB)
0	0	1	1	1	○	○	Starting Address Register C Channel (SARC)
0	1	0	0	0	×	○	Run Length Decode Register (RLR)

(Note 1) ○·····Writable ×·····Not Writable
(Note 2) The other addresses than above listed must not be written in the AR.
(Note 3) A Channel is :
- the coding line during the coding operation
- the decoding line during the decoding operation
- the transfer line during the data transfer

B Channel is : the reference line
C Channel is : the DMA line

Register accessible via the parameter buffer registers (PBRH, PBRL)

The parameter registers can be accessed via the parameter buffer registers (PBRH, PBRL). The MPU specifies a parameter register using the address register (AR). A parameter written to the parameter buffer registers is then written to the corresponding parameter register. The MPU writes parameters to parameter registers in the following sequence:

The MPU can write a desired parameter data into these registers by a sequence which :

- verifies that the PBR Ready Flag bit is set,
- writes the address of an intended parameter register into the AR, then
- writes a desired parameter data into PBRH then PBRL.

An MPU write to PBRL indicates to the DICEP that the address and the parameter data are ready. Then the parameter data is written into the parameter register specified by the address.

Registers other than the SARA, the SARB and the SARC hold the written data.
The individual parameter registers will be described in the following paragraphs.

Terminal Register A, B Channel (TRAB)

The TRAB specifies the number of pels along an A or B channel scan line to be processed on a bit basis.
When the document image bus has an 8-bit size, the three least significant bits of this register must be zeroes. When the document image bus has a 16-bit size, the four least significant bits must be zeroes.

(ex.) If the number of pels along an A or B channel line to be processed is 1728 pels, the individual bits of TRAB will be as follows.

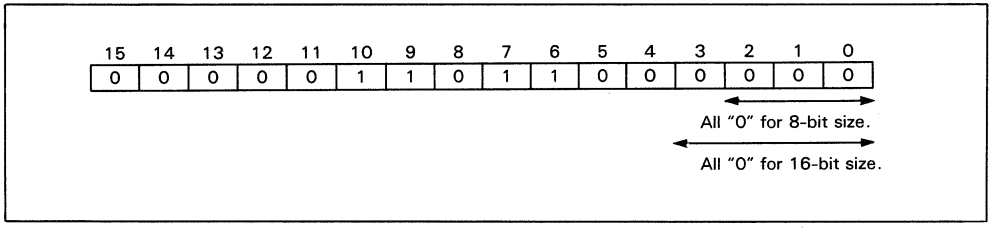


Figure 10 Terminal Register A, B Channel (TRAB)

Terminal Register C Channel (TRC)

The TRC specifies the number of bits on a scan line to be processed during a DMA transfer through the document image bus. When the document image bus has an 8-bit size, the three least significant bits of this register must be zeroes. When the document image bus has a 16-bit size, the four least significant bits must be zeroes.

Minimum Code Length Register (MCLR)

The MCLR specifies the minimum length of a coded scan line on a bit basis. If the actual coded line is shorter than the specified one, the Fill bits will be added.
The MCLR can be used to specify the minimum transmission time of a coded scan line. The MPU can specify the minimum transmission time of 10 msec for the facsimile with transmission rate of 9600 bit/sec by writing 96 into the MCLR.
Clearing the MCLR leads the DICEP to generate no Fill bits.

Return to Control Register (RTCR)

The RTCR contains the number of consecutive EOL code words which should be recognized as a RTC code word during a decoding operation.

End of Line Register (EOLR)

During a coding operation, the EOLR is used to specify the number of EOL code words which will be generated at the start of every coded line. If the EOLR is clear, the DICEP generates no EOL code word.
The EOLR is also used to specify the number of EOL code words which should be recognized as a RTC code word at the end of a page (when the PE bit in the SCR is set).
During a decoding operation, either one or zero is writtin to the EOLR. If zero has been written, it indicates that the coded data includes no EOL code word.

Horizontal Width Register (HWR)

The Horizontal width Register specifies the lingth of a scan line on a byte basis. When the document image bus has a 16-bit size, the least significant bit must be zero.
The width of an ISO A4 document is 1728 pels. However, when the document is to be coded, it is recommended to set 2048 pels as the scan-line length for effective use of 64k Byte of document image memory.

(ex.) If the scan-line length is 2048 pels, 256 is written into the HMR. (2048÷8=256)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

(ex.) 256 is written into the HWR

Figure 11 Horizontal Width Register (HWR)

Starting Address Register A Channel (SARA)

The Starting Address Register A Channel specifies the starting address of a document memory space which stores the current A channel line.
As the SARA stores parameters on a byte basis, if the document image bus has a 16-bit size, the least significant bit of the SARA must be zero. However, when the data transfer is performed between 8-bit word size I/O device and the system bus, this requirement is ignored.
During a coding operation, the SARA specifies the starting address of a document image memory space which stores image data to be coded.
During a decoding operation, the SARA specifies the starting address of a document image memory space which will store decoded image data.
During a data transfer between two buses, the SARA specifies the starting address of a document image memory space which stores the data transferred to or from the system bus.
Upon completion of coding, decoding or transfer of every line, the SARA is automatically updated to the following value.

(Current Value of SARA)+(Value of HWR)=(New Value of SARA)

If the starting address of the next scan line is the same as the automatically updated address, the MPU don't have to write the starting address to this register on every scan line.

Starting Address Register B Channel (SARB)

The starting Address Register B Channel specifies the starting address of the document image memory space which stores the current reference line.
As the SARB stores parameters on a byte basis, if the document image bus has a 16-bit size, the least significant bit must be zero.
This register is automatically updated on every scan line in the same way as the SARA.

(CAUTION)
If an error is detected during a decoding operation, the contents of SARA or SARB will not updated.

Starting Address Register C Channel (SARC)

The Starting Address Register C Channel specifies the starting address of the document image memory space which stores the current DMA line.
As the SARC stores parameters on a byte basis, if the document image bus has a 16-bit size, the least significant bit of the SARC must be zero.
The content of this register is automatically updated on every scan line in the same way as SARA and SARB.

Run Length Register (RLR)

The Run Length Register contains run length codes during a run length decoding operation. When a line of run length codes are written into the RLR, the DICEP will decode the data.

Coding and Decoding Scheme

MH Coding scheme

In the MH coding scheme, one dimensional coding is performed on all lines of data, One dimensional coding encodes run lengths of white pels and black pels which alternate on a scan line.
A one dimensionally coded scan line is made of a data line, End of Line code words and, if necessary, Fill bits.

MR Coding Scheme

In MR coding scheme, the one dimensional coding is performed on a scan line, then the two dimensional coding is performed on at most K-1 successive lines. The maximum value of K shall be 2 if standard vertical resolution is used and shall be 4 if higher vertical resolution is used.

M^2R Coding Scheme

M^2R coding scheme is used for the Group 4 facsimile apparatus. In this scheme, all lines of data are coded two dimensionally. At the coding of the first line of a page, a white reference line is imaginarily set immediately above the coding line. This scheme requires neither fill bits nor line synchronization code words.

Run Length Coding Scheme

In addition to the above mentioned coding schemes, the DICEP provides run length coding scheme. In run length coding scheme, the run length of all white or black is generated without data compression (below shown figure 12).

The DICEP is designed to realize a wide variety of user applications. These applications are organized into two groups, that is the independent bus system and the common bus system.
This section offers examples of the two types of applications.

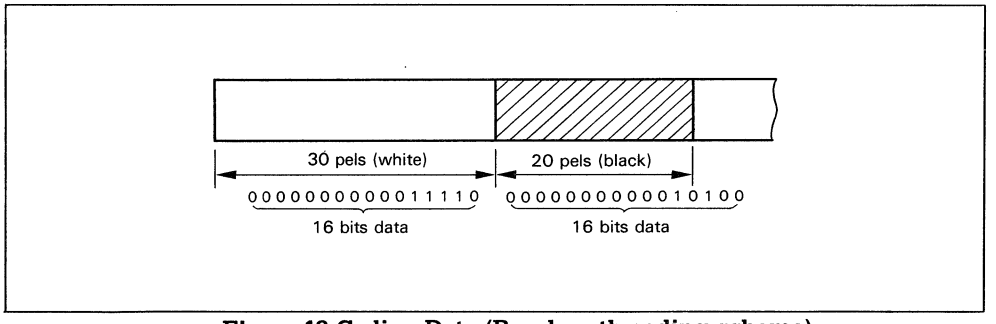


Figure 12 Coding Data (Run length coding scheme)

Absolute Maximum Rating

Item	Symbol	Value	Unit
Supply Voltage	V_{DD} *	-0.3 to +0.7	V
Input Voltage	V_{in} *	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150 (PC-72)	°C
		-55 to +125 (DP-64S)	

* Voltages referenced to V_{SS}=0V.

Recommended Operating Conditions

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{DD} *	4.75	5	5.25	V
Input Voltage	V_{IL} *	-0.3	–	0.8	V
	V_{IH}	2.2	–	V_{DD}+0.3	V
Operating Temperature	T_{OPR}	0	25	70	°C

* Voltages referenced to V_{SS}=0V.

<Use Precautions>

(1) Pay attention to dielectric breakdown. In handling, ground your body through a high resistance (500 or 600k to 1MΩ).
(2) This device operates at a high speed. Wire its signal lines with care to prevent noise caused by crosstalk of reflection.
(3) It is recommended to put a bypass capacitor between V_{DD} and V_{SS} (GND) to eliminate wire noise. (C=1μF min.)
(4) CMOS has the following specific problem: If the input signal level goes to the intermediate value (V_{IL} MAX ≦ V_{IN} ≦ V_{IH} MIN), I_{DD} increases and may cause a latch-up event. Pay special attention to the case as the buses, input terminals or unused terminals float at a power-on time.

Electrical Charcteristics

DC Characteristics (V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Condition
Input High Voltage	V_{IH}	2.2	–	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	-0.3	–	0.8	V	
Input Leakage Voltage	I_{IN}	-10	–	10	μA	V_{in}=0 to 5.25V
Three-State (Off State) Leakage Current	I_{TSI}	-10	–	10	μA	V_{in}=0 to 5.25V
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH}=-400μA
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL}=2mA
Power Dissipation	P_D	–	150	250	mW	

AC Characteristics

Clock Timing (V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
4CLK Cycle Time	ϕ_{4CLK}	31.25	–	500	ns	4CLK	Figure 13

System Bus Timing

Using a 68 Type MPU
(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C Cout=140pF unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
DS Cycle Time	t_{CYCE}	500	–	–	ns	DS	Figure 14, 17
DS Pulse Width	PW_{EH} PW_{EL}	220	–	–	ns	DS	
DS Rise or Fall Time	t_{Er} t_{Ef}	–	–	25	ns	DS	
Address Setup Time	t_{AS}	70	–	–	ns	$\overline{CS}$, A0-A2, R/$\overline{W}$	Figure 14
Address Hold Time	t_{AH}	30	–	–	ns	$\overline{CS}$, A0-A2, R/$\overline{W}$	
Output Data Delay Time	t_{DDR}	–	–	180	ns	D0-D7	Figure 14, 17
Output Data Hold Time	t_{DHR}	10	–	–	ns	D0-D7	
Input Data Setup Time	t_{DSW}	60	–	–	ns	D0-D7	
Input Data Hold Time	t_{DHW}	40	–	–	ns	D0-D7	
IRQT Inactive Delay Time	t_{IRQT}	ϕ_{4CLK} ×4+180	–	ϕ_{4CLK} ×8+180	ns	IRQT	Figure 14
$\overline{DACKI}$ Setup Time	t_{AS}	70	–	–	ns	$\overline{DACKI}$	Figure 17
$\overline{DACKI}$ Hold Time	t_{AH}	30	–	–	ns	$\overline{DACKI}$	
DRQTO Inactive Delay Time	t_{DRQTO}	–	(90)	180	ns	DRQTO	

Using an 80 Type MPU

(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C Cout=140pF unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
Address Setup Time	t_{AR}	70	–	–	ns	$\overline{CS}$, A0-A2,	Figure 15
Address Hold Time	t_{RA}	30	–	–	ns	$\overline{CS}$, A0-A2,	
Output Data Delay Time	t_{RD}	–	–	180	ns	D0-D7	Figure 15, 18
Output Data Hold Time	t_{DR}	10	–	–	ns	D0-D7	
Read Pulse Width	t_{RW}	200	–	–	ns	DS	
Adress Setup Time	t_{AW}	70	–	–	ns	$\overline{CS}$, A0-A2	Figure 16
Adress Hold Time	t_{WA}	30	–	–	ns	$\overline{CS}$, A0-A2	
Input Data Setup Time	t_{WD}	60	–	–	ns	D0-D7	Figure 16, 19
Input Data Hold Time	t_{DW}	40	–	–	ns	D0-D7	
Write Pulse Width	t_{WW}	200	–	–	ns	R/$\overline{W}$	
IRQT Inactive Delay	t_{IRQT}	ϕ_{4CLK} ×4+180	–	ϕ_{4CLK} ×8+180	ns	IRQT	Figure 15
$\overline{DACKI}$ Setup Time	t_{AR}	70	–	–	ns	$\overline{DACKI}$	Figure 18
$\overline{DACKI}$ Hold Time	t_{RA}	30	–	–	ns	$\overline{DACKI}$	
$\overline{DACKI}$ Setup Time	t_{AW}	70	–	–	ns	$\overline{DACKI}$	Figure 19
$\overline{DACKI}$ Hold Time	t_{WA}	30	–	–	ns	$\overline{DACKI}$	
DRQTO Inactive Delay	t_{DRQTO}	–	(90)	180	ns	DRQTO	Figure 18, 19

Document Image Bus Timing

V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C Cout=140pF unless otherwise noted. However, the values in the parentheses are the values at Cout=50pF.

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
Address Enable Active Delay Time	t_{DAEL}	–	(70)	150	ns	$\overline{MAEN}$	Figure 20, 21
Address Enable Inactive Delay Time	t_{DAEH}	–	(70)	140	ns	$\overline{MAEN}$	
Address Strobe Active Delay Time	t_{DASH}	–	(70)	140	ns	MAS	
Address Strobe Inactive Delay Time	t_{DASL}	–	(60)	120	ns	MAS	
Data Strobe Valid Delay Time	t_{DDSV}	–	(60)	140	ns	$\overline{UDS}$, $\overline{LDS}$	
Data Strobe Active Delay Time	t_{DDSL}	–	(75)	140	ns	$\overline{UDS}$, $\overline{LDS}$	
Data Strobe Inactive Delay Time	t_{DDSH}	–	(75)	140	ns	$\overline{UDS}$, $\overline{LDS}$	
Data Enable Active Delay Time	t_{DDEL}	–	(80)	130	ns	$\overline{MDEN}$	Figure 20
Data Enable Inactive Delay Time	t_{DDEH}	–	(75)	140	ns	$\overline{MDEN}$	
Read Valid Delay Time	t_{DRDV}	–	(60)	140	ns	$\overline{IOR}$, $\overline{MR}$	Figure 20, 21
Read Active Delay Time	t_{DRDL}	–	(70)	140	ns	$\overline{IOR}$, $\overline{MR}$	
Read Inactive Delay Time	t_{DRDH}	–	(75)	140	ns	$\overline{IOR}$, $\overline{MR}$	

(to be continued)

(continued)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
Write Valid Delay Time	t_{DWRV}	–	(60)	140	ns	$\overline{IOW}$, $\overline{MW}$	Figure 20, 21
Write Active Delay Time	t_{DWRL}	–	(70)	140	ns	$\overline{IOW}$, $\overline{MW}$	
Write Inactive Delay Time	t_{DWRH}	–	(80)	140	ns	$\overline{IOW}$, $\overline{MW}$	
Address Valid Delay Time	t_{MAV}	–	(75)	140	ns	MA/MD0-MA/MD15	
Address Hold Delay Time	t_{MAH}	25	(50)	–	ns	MA/MD0-MA/MD15	
Data Setup Time (Read)	t_{DSR}	10	(10)	–	ns	MA/MD0-MA/MD15	Figure 20
Data Hold Time (Read)	t_{DHR}	70	(70)	–	ns	MA/MD0-MA/MD15	
Data Delay Time (Write)	t_{DDW}	–	(95)	170	ns	MA/MD0-MA/MD15	
Data Hold Time (Write)	t_{DHW}	15	(15)	–	ns	MA/MD0-MA/MD15	
DMA Acknowlege Active Delay Time	t_{DAKL}	–	(60)	140	ns	$\overline{DACKO}$	Figure 21
DMA Acknowlege Inactive Delay Time	t_{DAKH}	–	(65)	140	ns	$\overline{DACKO}$	
DMA Active Delay Time	t_{DDMAL}	–	(80)	140	ns	$\overline{DMA}$	
DMA Inactive Delay Time	t_{DDMAH}	–	(70)	140	ns	$\overline{DMA}$	
DTC Active Delay Time	t_{DDTCH}	–	$\begin{pmatrix}\phi_{4CLK}\\+75\end{pmatrix}$	ϕ_{4CLK} +140	ns	DTC	
DTC Inactive Delay Time	t_{DDTCL}	–	(50)	130	ns	DTC	

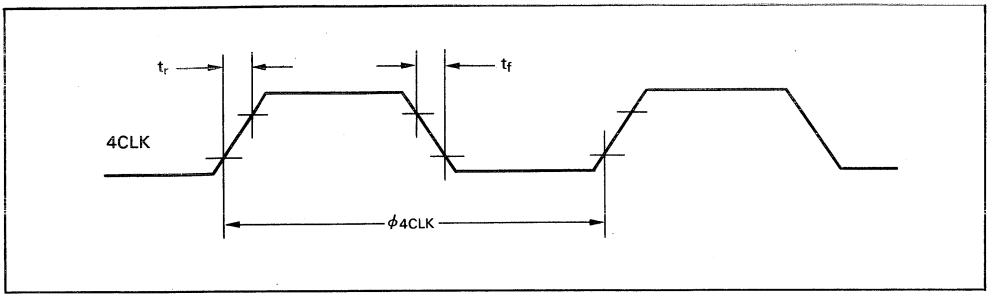


Figure 13 Clock Timing

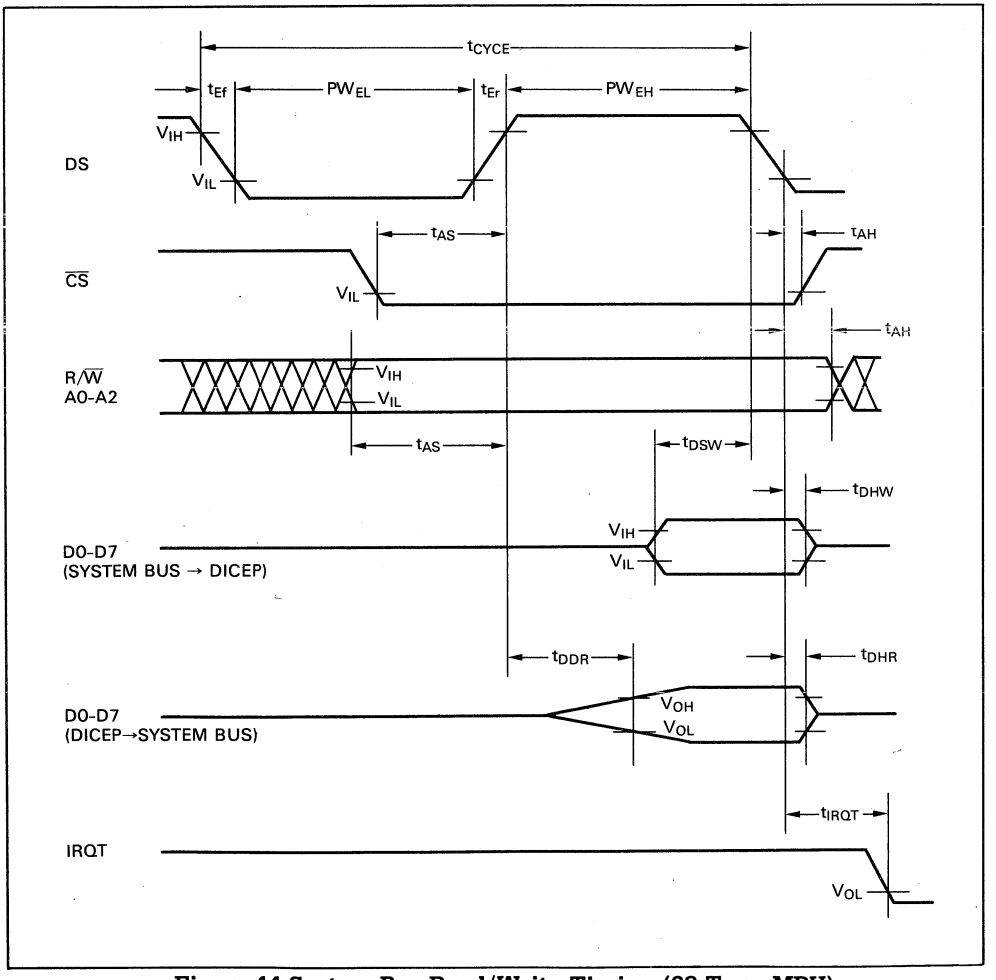


Figure 14 System Bus Read/Write Timing (68 Type MPU)

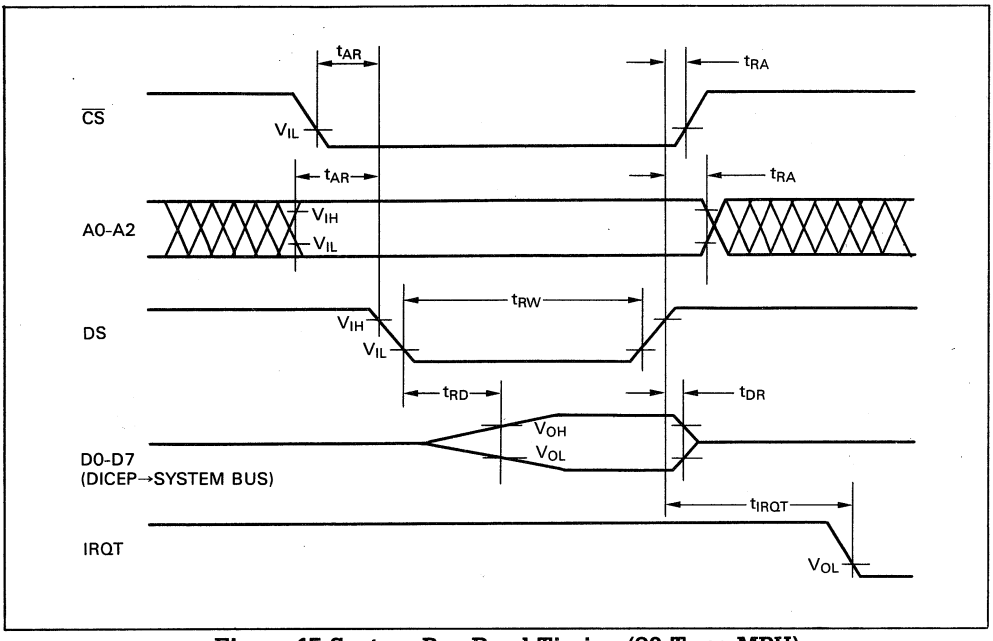


Figure 15 System Bus Read Timing (80 Type MPU)

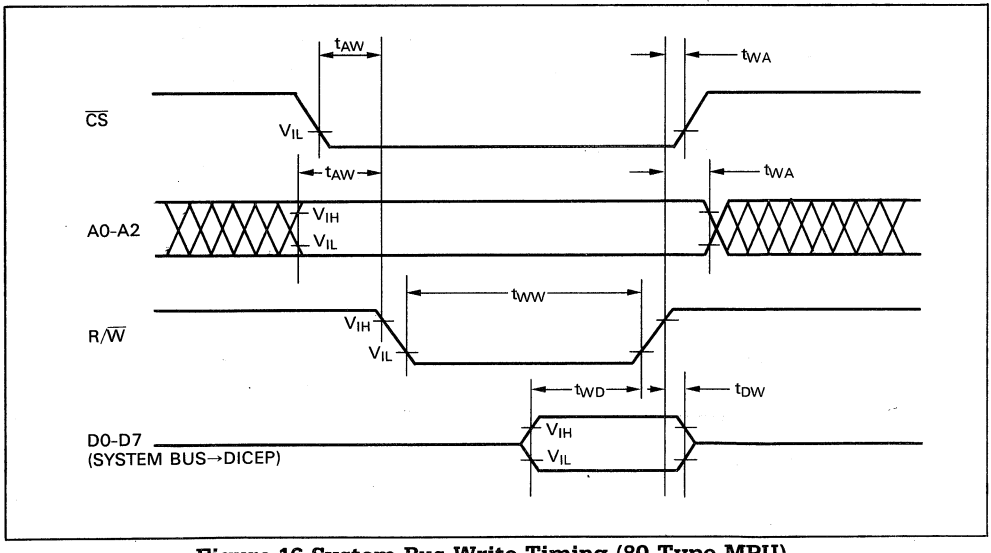


Figure 16 System Bus Write Timing (80 Type MPU)

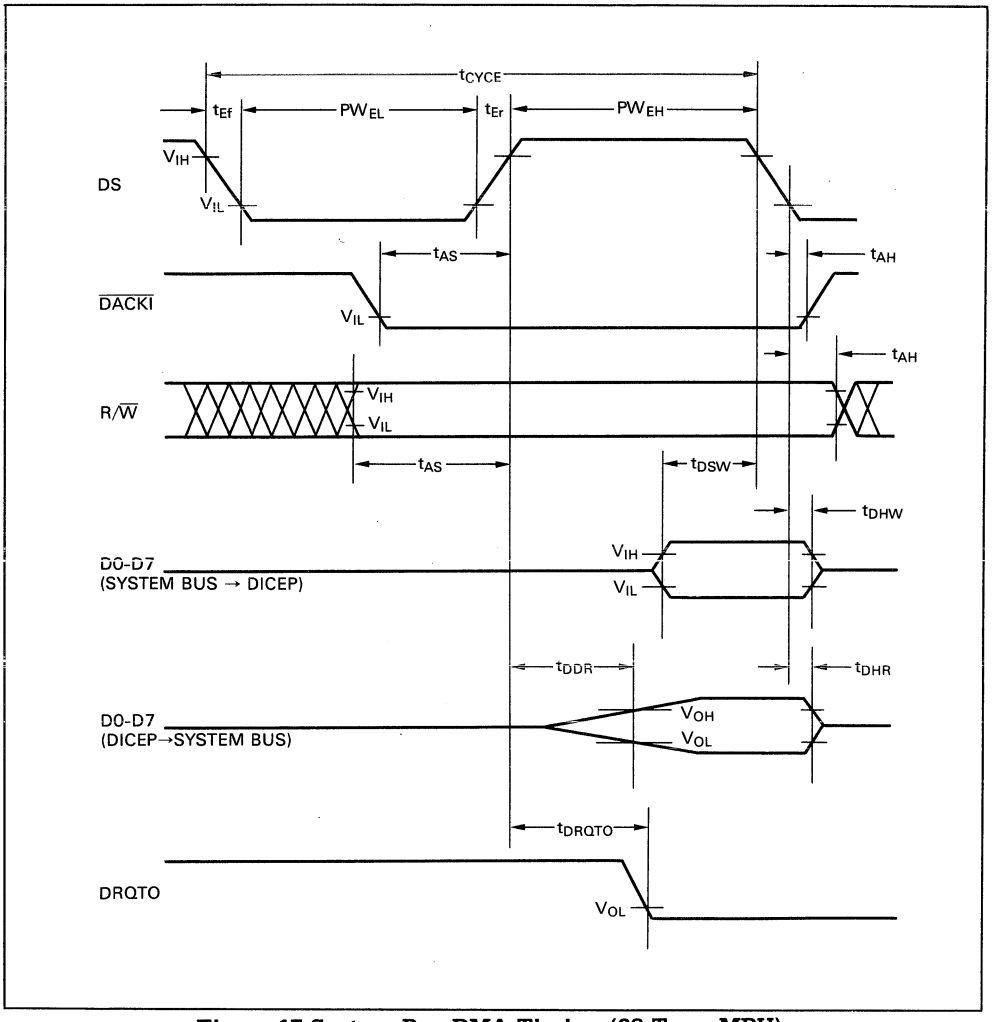


Figure 17 System Bus DMA Timing (68 Type MPU)

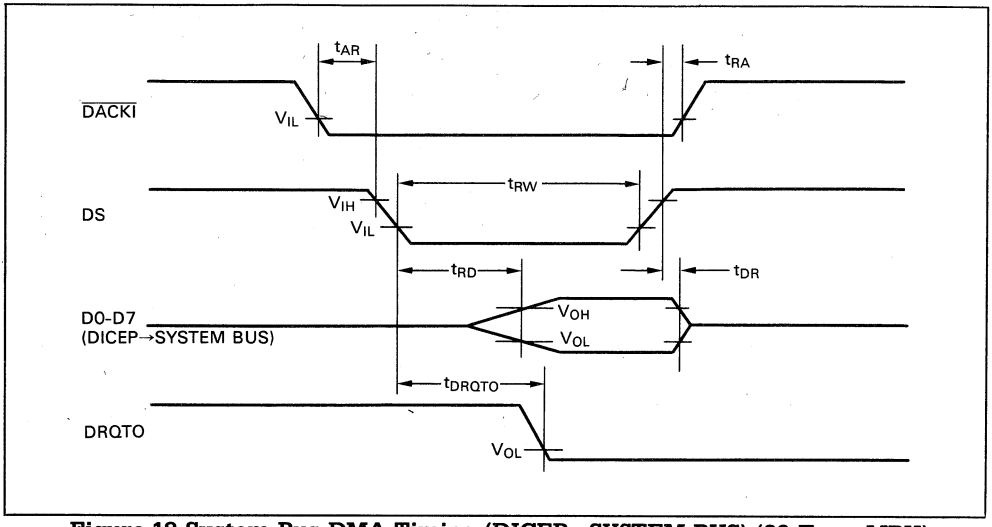


Figure 18 System Bus DMA Timing (DICEP→SYSTEM BUS) (80 Type MPU)

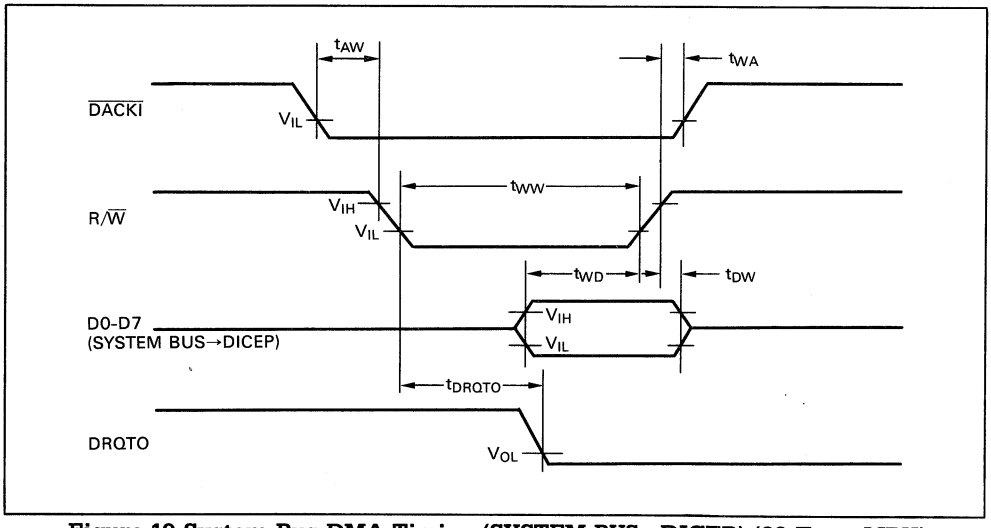


Figure 19 System Bus DMA Timing (SYSTEM BUS→DICEP) (80 Type MPU)

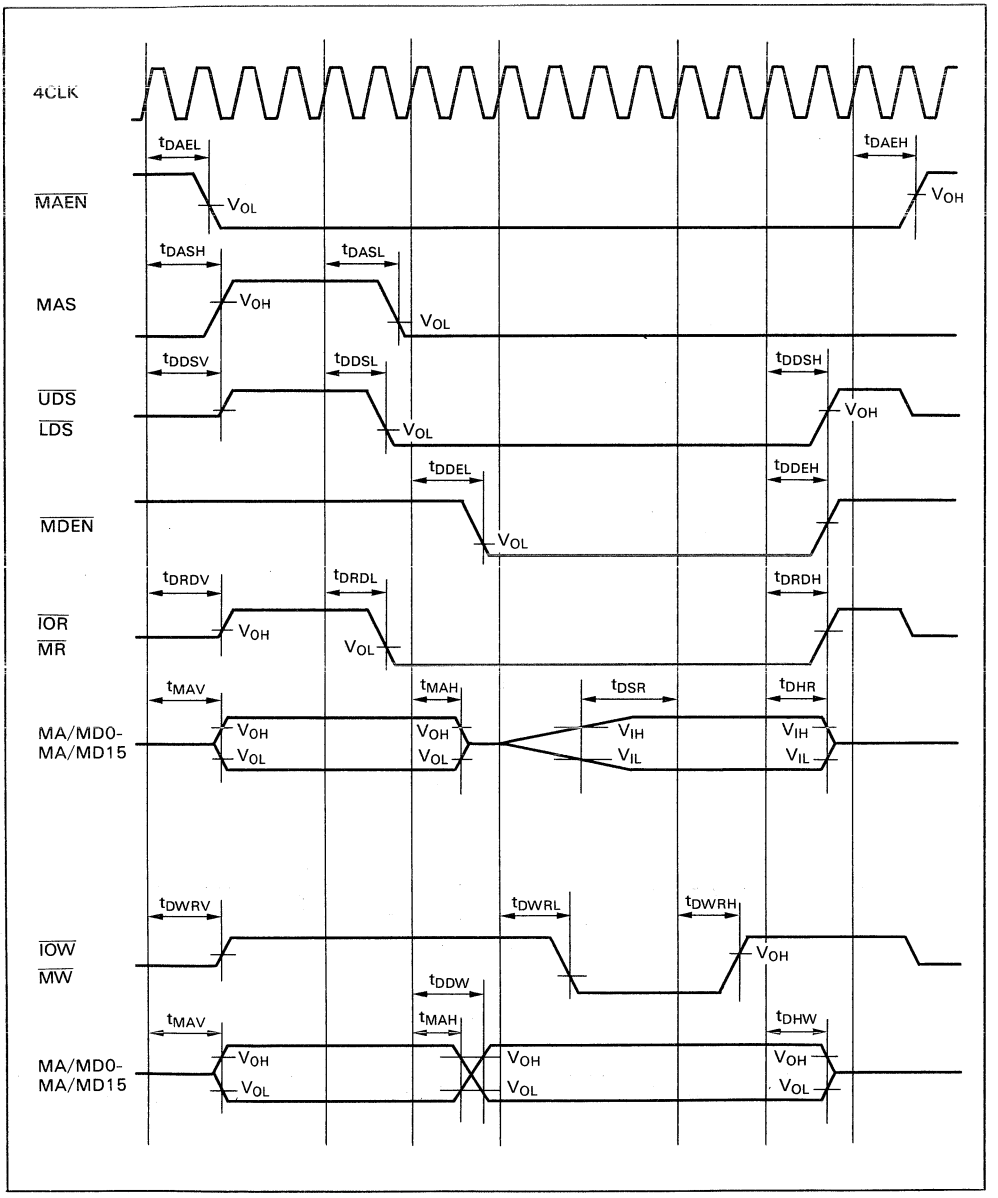


Figure 20 Document Image Bus Read/Write Timing

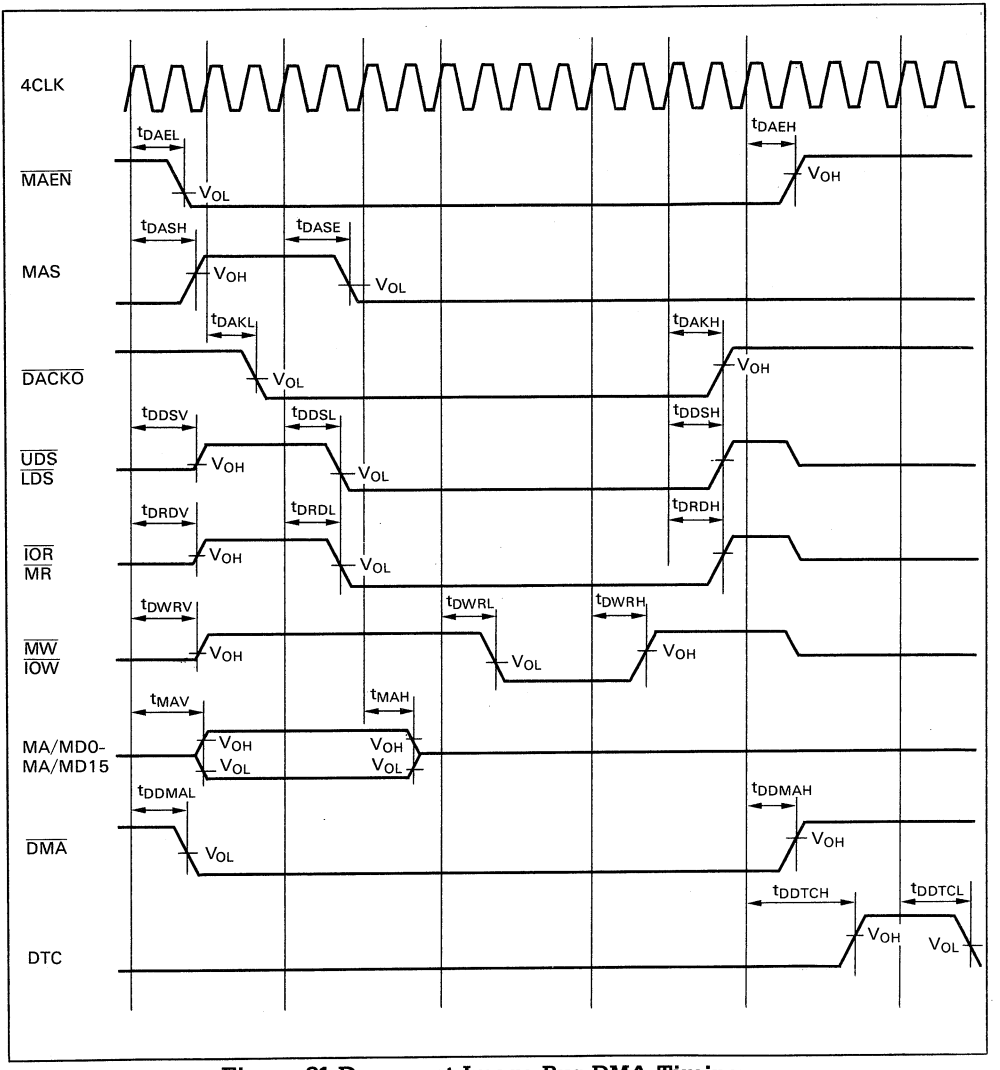


Figure 21 Document Image Bus DMA Timing

Refer to user's manual (No. AD-E0088) for detail of this product.

HD63183

Document Image Compression and Expansion Processor Advanced (DICEP-A)

HD63183 DICEP-A performs compression (encoding) and expansion (decoding) of the digital (two-value) data that represent an image, and applies DICEP-A to result in an enhanced, improved version of the HD63085 DICEP.

Compared with the previous DICEP, DICEP-A expands the address space from 64 kbytes to 4 Mbytes. Since DICEP-A allows such operations as encoding and decoding to be performed on one-page blocks, system throughput is increased substantially. In addition, existing DICEP software is upwardly compatible, so it can be used with DICEP-A.

Features

- Compatible with the CCITT Recommendations for Group 3 and Group 4 facsimile apparatus
- Upward compatibility with DICEP (HD63085)
  The DICEP-A contains a FP-80A (HD63183FP) flat package type and a DP-64S (HD63183P) shrink package type. The latter is compatible with the DICEP (HD63085P).
  The DICEP-A software program is upward-compatible with the DICEP. The DICEP-A internal state after a power-ON reset is also in the same mode as the DICEP.
  The memory address space size on the image bus side is 4 Mbytes for FP-80A (HD63183FP) type and 64 kbytes for DP-64S (HD63183P) type.
- Simple MPU Command
  As the DICEP-A stores coding and decoding algorithms in the microprogram ROM as firmware, a single MPU command allows this LSI to encode (i.e. compress) or decode (i.e. expand) a scan line of digital data.
- Two types of FIFO
  The DICEP-A includes two types of FIFO (encode FIFO (E-FIFO) and decode FIFO (D-FIFO)). Therefore, the previous coded data can be retained as it is even through an alternate operation of coding and decoding.
- High Speed Coding and Decoding
  The DICEP-A realizes high speed coding and decoding by:
  - —including a changing pels* detector which can detect a changing pel contained in a word (8 bits/16 bits) of document image data within an instruction cycle time (at least 125nsec), and
  - —including a decoded pels generator which can generate a word (8 bits/16 bits) of document image data within an instruction cycle time.

  (NOTE *) The term 'picture element' is abbreviated to 'pel' in this document.
- Flexible System Configuration
  - —Either 68 type MPU or 80 type MPU can be interfaced. The system bus has the size of 8 bits.
  - —The DICEP-A has two bus interfaces; the system bus interface and the document image bus interface.
  - —The DICEP-A may be interfaced with two independent buses (i.e. the system bus and the document image bus), while it may be interfaced with a common bus.
  - —The size of the document image bus is selectable (8 bits/16 bits) depending on the word size of document image memory.
- High Speed DMA Transfer
  - —The DICEP-A can perform direct memory access (DMA) transfer between an I/O device (scanner or printer) and the document image memory. The maximum transfer rate is 4 Mbyte/sec.
  - —With a DMA controller (DMAC) on the system bus, DMA transfers can be performed between a memory on the system bus and the DICEP-A.
- A Variety of Programmable Parameters
  Internal programmable registers present the DICEP-A flexibility to allow application to many kinds of systems.
  - —The parameters can be changed before initiation of every command.
  - —The length of a scan line is programmable from the word size of the document image memory (8 bits/16 bits) to 64 kbits.
  - —One of coding operation, decoding operation and transfer operation can be selected.
  - —One of MH coding scheme, MR coding scheme, M^2R coding scheme and run length coding scheme can be selected.
  - —The minimum length of a coded scan line is programmable from 0 to 2^{16} - 1

bits.
—The number of End of Line (EOL) code words is programmable from 0 to 2^{16} - 1.
—The number of Return to Control (RTC) code words is programmable from 0 to 2^{16} - 1.
—The DICEP-A can code and decode a desired part of a document on a word (8 bits/16 bits) basis.
—The number of lines to be processed is programmable from 1 to 2^{16} - 1.
—In DMA transfer, the number of lines to be transferred is programmable from 1 to 2^{16} - 1.
—In MR coding, the number of lines to be two-dimensionally coded following one dimensional coding is programmable from 0 to 2^{16} - 1 (K parameter.).

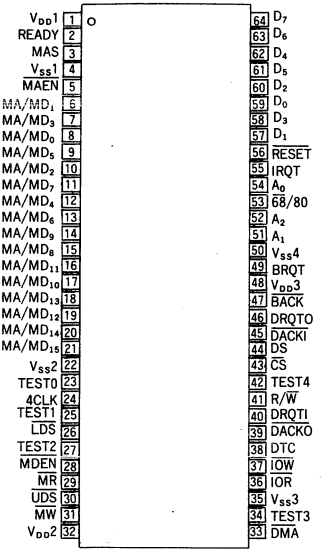
- Data Transfer between Buses
  The DICEP-A can perform data transfer between the system bus and the document image bus without coding or decoding.
- Octet Mode
  The DICEP-A provides Octet Mode. In this mode, a coded scan line or a coded page is 8-bit boundary conditioned.
- Run Length Coding Scheme
  The DICEP-A provides run length coding scheme in addition to MH coding scheme, MR coding scheme and M^2R coding scheme.
- High Operating Speed
  —Instruction cycle time is 125nsec min. (at system clock of 8 MHz max.)
  —Input clock frequency is 32 MHz max.
- Package
  —64pin plastic shrink DIP (DP-64S)
  —80pin plastic QFP (FP-80A)

Ordering Information

Type No.	Input Clock	Package
HD63183P	2MHz to 32MHz	64pin plastic shrink DIP (DP-64S)
HD63183FP		80pin plastic QFP (FP-80A)

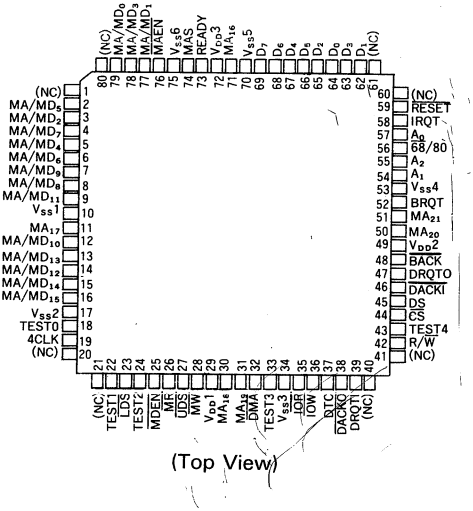
Pin Arrangement

● DP-64S



(Top View)

● FP-80A



(Top View)

(Note) The memory address space size on the image bus side is 64 kbytes.
Pin and software program compatibilty with HD63085P DICEP.

Pin Descriptions

System Bus Interface Pins

Signal	Pin No. DP64S	Pin No. FP80A	I/O	Descriptions
$\overline{68}$/80	53	56	I	68/80 Mode select. If $\overline{68}$/80 is low, it indicates that a 68 type MPU is interfaced with the DICEP-A. If high, it indicates that an 80 type MPU is interfaced.
A0 A1 A2	54 51 52	57 54 55	I	Addresses 0 to 2. These pins are connected to the 3 low-order bits of the system address bus to address the DICEP-A internal registers.
D0 D1 D2 D3 D4 D5 D6 D7	59 57 60 58 62 61 63 64	64 62 65 63 67 66 68 69	I/O, 3-state output	Data 0 to 7. These pins are interfaced with the system data bus to provide bidirectional communication between the MPU and the DICEP-A. The MPU can read/write the DICEP-A internal registers via D0 to D7 pins.
$\overline{CS}$	43	44	I	Chip select. A low level on this pin indicates that the MPU accesses a DICEP-A internal register.
DS	44	45	I	Data strobe. This pin must be connected to $\phi 2$ clock pin of 68 type MPU or $\overline{RD}$ pin of 80 type MPU.
R/$\overline{W}$	41	42	I	Read/Write. This pin is connected to R/$\overline{W}$ pin of 68 type MPU or $\overline{WR}$ pin of 80 type MPU.
$\overline{RESET}$	56	59	I	Reset. A low level on $\overline{RESET}$ initializes the DICEP-A.
4CLK	24	19	I	4 Clock. The clock frequency is four times as high as the DICEP-A system clock frequency.
IRQT	55	58	O	Interrupt Request. The DICEP-A sends an interrupt request to the MPU by driving IRQT high upon completion of a command, end of a DMA transfer, occurrence of decoding error or reception of Return to Control (RTC) code words. MPU can know the cause of an interrupt by reading the Interrupt Request Register (IRR). When the MPU reads the IRR, IRQT returns to the low state.
DRQTO	46	47	O	DMA Request Output. The DICEP-A can drive DRQTO high to provide DMA request to the DMA Controller (DMAC) when : (1) Coded data of more than 1 byte are stored in the E-FIFO during coding operation, (2) The D-FIFO has empty space of more than 1 byte during decoding operation or (3) Data Buffer Register (DBR) is ready for a read or write operation during data transfer between the system bus and the document image bus.
$\overline{DACKI}$	45	46	I	DMA Acknowledge Input. This input is a response to DRQTO. When $\overline{DACKI}$ goes low during coding operation or decoding operation, the E-FIFO, the D-FIFO is accessed. If $\overline{DACKI}$ goes low during data transfer between the system bus and the document image bus, the DBR is accessed. $\overline{CS}$ and $\overline{DACKI}$ must not be pulled low together.

Document Image Bus Interface Pins

Signal	Pin No. DP64S	Pin No. FP80A	I/O	Descriptions
BRQT	49	52	O	Bus Request. When BRQT is driven high by DICEP-A, it indicates to all other potential bus master devices on the document image bus that the DICEP-A desires to become the bus master. When the document image bus has no other potential master device, BRQT does not have to be connected to any line.
$\overline{\text{BACK}}$	47	48	I	Bus Acknowledge. This input is a response to the BRQT. A low level on $\overline{\text{BACK}}$ indicates that the DICEP-A is granted to be the master of the document image bus. This pin must be fixed low when the document image bus has no potential bus master devices other than the DICEP-A.
$\overline{\text{MAEN}}$	5	76	O	Memory Address Enable. When $\overline{\text{MAEN}}$ is driven low by DICEP-A, it indicates that the DICEP-A has become the master of the document image bus. If $\overline{\text{MAEN}}$ is high, all of three-state outputs interfaced with the document image bus are in high impedance state.
MAS	3	74	O	Memory Address Strobe. When the DICEP-A drives MAS high, it indicates that the DICEP-A outputs an address onto MA/MD0 through MA/MD15 and MA16 through MA21.
$\overline{\text{UDS}}$	30	27	3-state output	Upper Data Strobe. When $\overline{\text{UDS}}$ is driven low by DICEP-A, it indicates that the DICEP-A uses the high-order byte of the document image bus.
$\overline{\text{LDS}}$	26	23	3-state output	Lower Data Strobe. When $\overline{\text{LDS}}$ is dviven low by DICEP-A, it indicates that the DICEP-A uses the low-order byte of the document image bus.
$\overline{\text{MDEN}}$	28	25	O	Memory Data Bus Enable. When $\overline{\text{MDEN}}$ is driven low by DICEP-A, it indicates that there is a valid data on MA/MD0 through MA/MD15. This output is used to control the output of bidirectional bus buffer on the MA/MD0 through MA/MD15.
MA/MD0	8	79	I/O, 3-state output	Memory Address Date Bus 0 to 15. This is multiplexed address/data bus for document image bus operation. MA/MD0 to MA/MD15 are used as follows: 1) Output address lines when the $\overline{\text{MAEN}}$ in low and the MAS is high. 2) Input data lines when both $\overline{\text{MAEN}}$ and $\overline{\text{MDEN}}$ are low during read cycle. 3) Output data lines when both $\overline{\text{MAEN}}$ and $\overline{\text{MDEN}}$ are low during write cycle.
MA/MD1	6	77		
MA/MD2	10	3		
MA/MD3	7	78		
MA/MD4	12	5		
MA/MD5	9	2		
MA/MD6	13	6		
MA/MD7	11	4		
MA/MD8	15	8		
MA/MD9	14	7		
MA/MD10	17	12		
MA/MD11	16	9		
MA/MD12	19	14		
MA/MD13	18	13		
MA/MD14	20	15		
MA/MD15	21	16		
MA16	—	71	3-state output	Memory Address Bus 16 to 21. These are used as an output address line when $\overline{\text{MAEN}}$ is low and MAS is high.
MA17	—	11		
MA18	—	30		
MA19	—	31		
MA20	—	50		
MA21	—	51		

Document Image Bus Interface Pins (continued)

Signal	Pin No. DP64S	Pin No. FP80A	I/O	Descriptions
$\overline{MR}$	29	26	3-state output	Memory Read. The DICEP-A drives $\overline{MR}$ low to read data from the document image memory.
$\overline{MW}$	31	28	3-state output	Memory Write. The DICEP-A drives $\overline{MW}$ low to write data into the document image memory.
$\overline{IOR}$	36	35	3-state output	I/O Read. The DICEP-A drives $\overline{IOR}$ low to read data from an I/O device on the document image bus. However, $\overline{IOR}$ is used only for data transfer between buses or for DMA transfer through the document image bus during coding operation.
$\overline{IOW}$	37	36	3-state output	I/O Write. The DICEP-A drives $\overline{IOW}$ low to write data into an I/O device on the document image bus. However, $\overline{IOW}$ is used only for data transfer between buses or for DMA transfer through the document image bus during decoding operation.
DRQTI	40	39	I	DMA Request Input. DRQTI is driven high when an I/O device on the document image bus sends a DMA request to the DICEP-A.
$\overline{DACKO}$	39	38	O	DMA Acknowledge Output. When this output is driven low, it notifies the peripherals on the document image bus that they have been granted a DMA operation.
$\overline{DMA}$	33	32	O	Direct Memory Access. When DMA is driven low, it indicates that the DICEP-A is executing a DMA transfer. During coding operation, data is transferred from the I/O device (scanner) to the document image memory. During decoding operation, data is transferred from the document image memory to the I/O device (printer).
DTC	38	37	O	DMA Terminal Count. When DTC is driven high, it indicates that DMA transfer of a scan line has been completed.
READY	2	73	I	Ready. When READY is high during a read or write to the document image memory or the I/O devices, it indicates that the memory or I/O device is ready to send or receive data. If READY is low, the DICEP-A will wait until READY becomes high.

Power Pins and Others

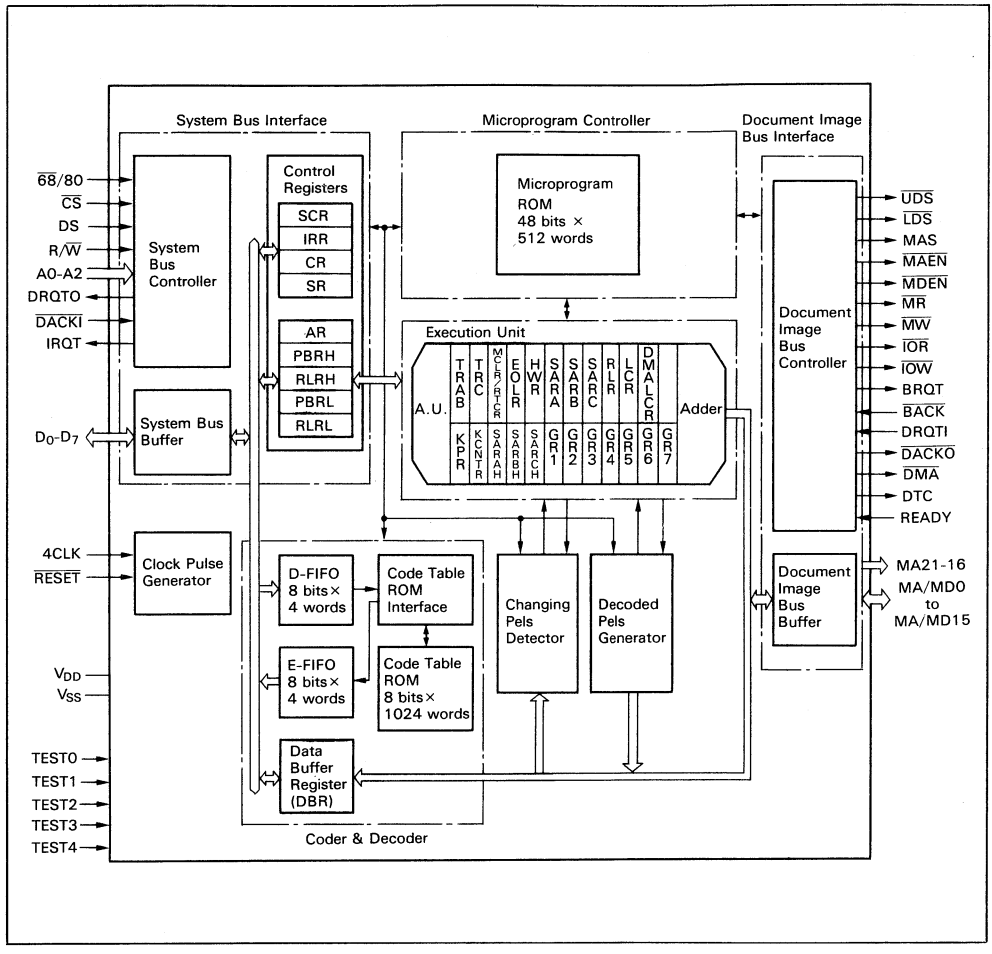
Signal	Pin No. DP64S	Pin No. FP80A	I/O	Descriptions
$V_{DD}1$	1	29	—	Supply Voltage (+5V)
$V_{DD}2$	32	49	—	
$V_{DD}3$	48	72	—	
$V_{SS}1$	4	10	—	Ground
$V_{SS}2$	22	17	—	
$V_{SS}3$	35	34	—	
$V_{SS}4$	50	53	—	
$V_{SS}5$	—	70	—	
$V_{SS}6$	—	75	—	
TEST0	23	18	I	<Others>
TEST1	25	22	I	These pins must be fixed low.
TEST2	27	24	I	
TEST3	34	33	I	
TEST4	42	43	I	

Functional Summary

Item		Function
Coding Scheme		MH, MR, M²R, Run Length
Maximum Scan-line Length		64k pels
Document Image Bus Memory Address Space Size	HD63183FP	Document Image Memory ·····4 Mbytes I/O Devices ·····4 Mbytes
	HD63183P	Document Image Memory ·····64 kbytes I/O Devices ·····64 kbytes
Maximum DMA Transfer Rate		4 Mbyte/sec *1
Maximum Changing Pels Detect Speed		3.2 Mbyte/sec *1
Maximum Decoded Pels Generation Speed		3.2 Mbyte/sec *1

*1: Input clock frequency is 32 MHz.

Block Diagram



Block Configurations

System Bus Interface

The system bus interface has a timing specification compatible with 8-bit MPUs (ex. HD6800/HD64180). This block includes control registers which can be directly accessed by the MPU.

Microprogram Controller

The microprogram controller stores coding and decoding programs in the microprogram ROM to control all other blocks of the DICEP-A.

This block consists of the microprogram ROM with 512 words of 48 bits, the sequence controller and the pipeline register.

Execution Unit

The execution unit generates document image memory addresses, and calculates the position of changing pels, run lengths, and the relative distance between changing pels on the coding line and those on the reference line.

This block consists of twenty three 16-bit registers, the artithmetic unit (A.U.) and the adder. Sixteen registers (TRAB, TRC, MCLR/RTCR, EOLR, HWR, SARA, SARB, SARC, RLR, LCR, DMALCR, KPR and KCNTR) can be programmed by the MPU via the control registers in the system bus interface. These sixteen registers are called "parameter registers".

Coder and Decoder

The coder generates the addresses of the code table ROM from input run lengths or relative distances, and generates appropriate code words by looking up the code table ROM.

On the other hand, the decoder generates the addresses of the code table ROM from input code words, and generates run lengths or relative addresses by looking up the code table ROM.

This block consists of the code table ROM with 1024 words of 8 bits, the code table ROM interface, the two types of First-In First-Out memory (encode FIFO and decode FIFO) with 4 words of 8 bits, and the Data Buffer Register (DBR). The code table ROM stores the data which is referenced for coding and decoding operations. The code table ROM interface generates the addresses of the code table ROM. The FIFO temporarily stores code words during coding or decoding operation. The DBR is a intermediate buffer which is used to transfer data between the system bus and the document image bus.

Changing Pels Detector

The changing pels detector detects a changing pel whose color (white or black) is different from that of the previous pel on the same scan line. It can detect a changing pel in a word (8 bits/16 bits) of the document image memory within an instruction cycle time.

This block consists of two changing pels detectors: the reference line detector and the coding line detector.

Decoded Pels Generator

The decoded pels generator can generate at most a word (8 bits/16 bits) of decoded pels within an instruction cycle time, using the information of the positions of changing pels.

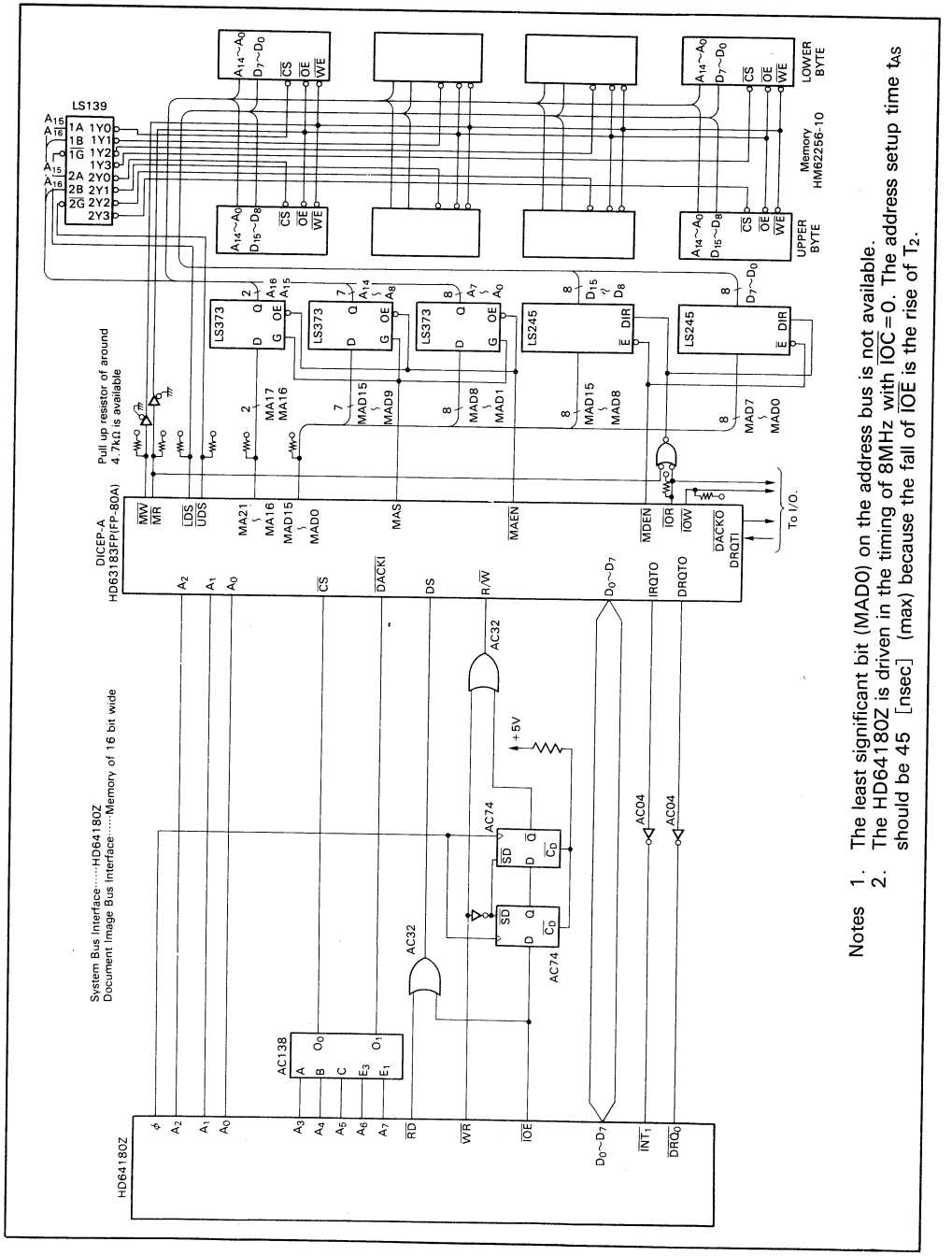
Document Image Bus Interface

The document image bus interface provides an interface between the DICEP-A and the document image bus. It has a 16-bit multiplexed address/data bus.

This block has the following functions:

- It has bus arbitration technique.
- It outputs control signals for the document image bus.

System Configuration



Notes 1. The least significant bit (MAD0) on the address bus is not available.
2. The HD641802Z is driven in the timing of 8MHz with $\overline{IOC}$=0. The address setup time t_{AS} should be 45 [nsec] (max) because the fall of $\overline{IOE}$ is the rise of T_2.

Internal Registers

Figure 1 illustrates a DICEP-A register programming model. DICEP-A registers can be classified into two groups: registers that are directly accessible by the MPU, and registers that can be accessed via the parameter buffer registers (PBRH, PBRL). The following describes the access methods used for each type of register.

Registers directly accessible from the MPU

The control registers (CR), data buffer register (DBR), and FIFO can be accessed directly from the MPU, in accordance with A_0 to A_2 when CS is L-level.
Table 1 shows the directly accessible registers.

Registers accessible via parameter buffer registers (PBRH, PBRL)

The parameter registers can be accessed via the parameter buffer registers (PBRH, PBRL). The MPU specifies a parameter register using the address register (AR). A parameter written to the parameter buffer registers is then written to the corresponding parameter register. The MPU writes parameters to parameter registers in the following sequence:

1. The PBR ready flag of the status register (SR) is checked for a 1.
2. The desired parameter register is specified by the address register (AR).
3. The parameter is written to the parameter buffer registers (PBRH, PBRL).
4. When the parameter is written to PBRL, DICEP-A determines if the address and parameter preparation are complete, and then writes the parameter to the specified register.

Table 2 shows the parameter registers.

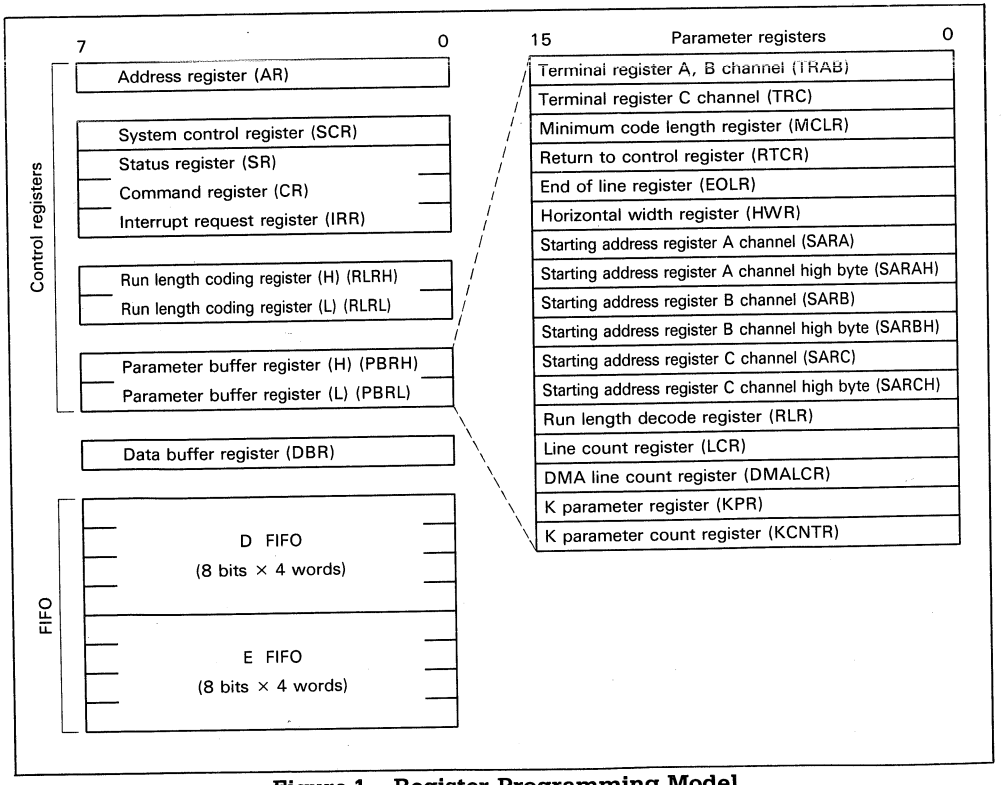


Figure 1 Register Programming Model

Table 1 Control Registers, FIFO and DBR

Address					
A2	**A1**	**A0**	**R/W**	**Symbol**	**Full Name**
0	0	0	R/W	SCR	System Control Register
0	0	1	R	IRR	Interrupt Request Register
0	1	0	R	SR	Status Register
			W	CR	Command Register
0	1	1	R	E-FIFO	First-In First-Out Memory
			W	D-FIFO	
1	0	0	R/W	DBR	Data Buffer Register
1	0	1	R/W	AR	Address Register
1	1	0	R	RLRH	Run Length Coding Register High
			W	PBRH	Parameter Buffer Register High
1	1	1	R	RLRL	Run Length Coding Register Low
			W	PBRL	Parameter Buffer Register Low

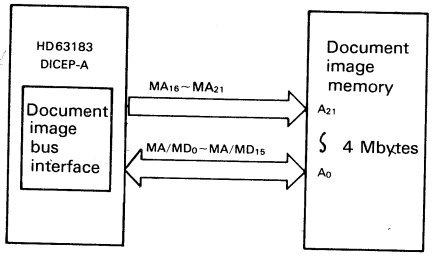
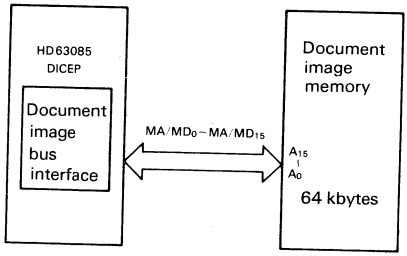
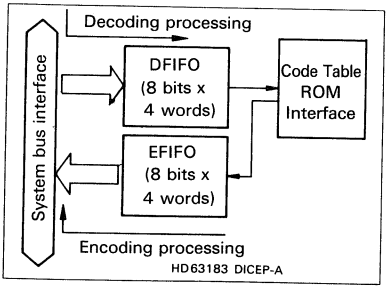
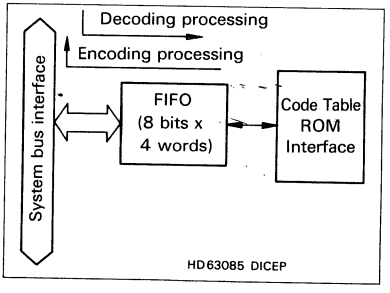
Table 2 Parameter Registers

Address (AR)							
AR4	AR3	AR2	AR1	AR0	Coding	Decoding	Name
0	0	0	0	0	◎	◎	Terminal Register A, B Channel (TRAB)
0	0	0	0	1	◎	◎	Terminal Register C Channel (TRC)
0	0	0	1	0	◎	Not Used	Minimum Code Length Register (MCLR)
					Not Used	◎	Return to Control Register (RTCR)
0	0	0	1	1	◎	◎	End of Line Register (EOLR)
0	0	1	0	0	◎	◎	Horizontal Width Register (HWR)
0	0	1	0	1	◎	◎	Starting Address Register A Channel (SARA)
0	0	1	1	0	◎	◎	Starting Address Register B Channel (SARB)
0	0	1	1	1	◎	◎	Starting Address Register C Channel (SARC)
0	1	0	0	0	×	◎	Run Length Decode Register (RLR)
0	1	0	0	1	◎	◎	Line Count Register (LCR)
0	1	0	1	0	◎	◎	DMA Line Count Register (DMALCR)
0	1	0	1	1	◎	×	K Parameter Register (KPR)
0	1	1	0	0	◎	×	K Parameter Count Register (KCNTR)
0	1	1	0	1	◎	◎	Starting Address Register A Channel High Byte (SARAH)
0	1	1	1	0	◎	◎	Starting Address Register B Channel High Byte (SARBH)
0	1	1	1	1	◎	◎	Starting Address Register C Channel High Byte (SARCH)

(Note 1) ◎·····Writable ×·····Not Writable
(Note 2) The other addresses than above listed must not be written in the AR.
(Note 3) A Channel is:
- the coding line during the coding operation
- the decoding line during the decoding operation
- the transfer line during the data transfer

(Scanning line for transfer.)
B Channel is: the reference line
C Channel is: the DMA line
(Scanning line for MDA transfer)

HD63183 DICEP-A Enhancements

HD63183 DICEP-A	HD63085 DICEP
1. Expanded image memory address space size	
$MA_{16}-MA_{21}$ have been added to $MA/MD_0-MA/MD_{15}$ for expansion of the image memory address space up to 4 Mbytes (Eight A4 size pages of data).	64 kbytes of image memory address space, $MA/MD_0-MA/MD_{15}$ ($\frac{1}{10}$ A4 size pages of data).
	
2. Dual FIFO memory system	
A dual FIFO memory system provides an 8-bit x 4-word decode FIFO (DFIFO) and encode FIFO (EFIFO). This means that EFIFO contents can be retained during decoding, and DFIFO contents can be retained during encoding.	With DICEP, data for encoding or decoding is temporarily stored in FIFO. A single 8-bit x 4-word FIFO is used for both encoding and decoding, so decoded data is cleared by encoding and vice versa.
	

HD63183 DICEP-A	HD63085 DICEP

3. Addition of a page mode (page processing)

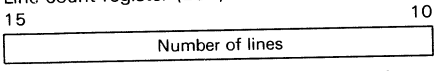
A total of seven parameter registers, including the line count register, are added for a dramatic increase in system throughput.

Parameter registers

Terminal register A, B channel (TRAB)
Terminal register C channel (TRC)
Minimum code length register (MCLR)
Return to control register (RTCR)
End of line register (EOLR)
Horizontal width register (HWR)
Starting address register A channel (SARA)
Starting address register B channel (SARB)
Starting address register C channel (SARC)
Run length decode register (RLR)
Line count register (LCR)
DMA line count register (DMALCR)
K parameter register (KPR)
K parameter count register (KCNTR)
Starting address register A channel high byte (SARAH)
Starting address register B channel high byte (SARBH)
Starting address register C channel high byte (SARCH)

1. Document image processing function

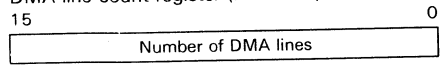
Line count register (LCR)



This register is used to specify the number of lines for image processing within the range of 0–65535. Following the processing of approximately one page, a command end interrupt is generated and sent to the MPU for efficient image processing.

2. DMA transfer function

DMA line count register (DMALCR)



This register is used to specify the number of lines for DMA transfer between the image bus I/O and memory within the range of 0–65535. DMA transfer is possible for one page of data.

Ten parameter registers are used, and a command end interrupt is generated and sent to the MPU following the processing of one line of image data.

Parameter registers

Terminal register A, B channel (TRAB)
Terminal register C channel (TRC)
Minimum code length register (MCLR)
Return to control register (RTCR)
End of line register (EOLR)
Horizontal width register (HWR)
Starting address register A channel (SARA)
Starting address register B channel (SARB)
Starting address register C channel (SARC)
Run length decode register (RLR)

HD63183 DICEP-A	HD63085 DICEP
3. 2-dimensional encoding function K parameter register (KPR) 15 0 K parameter K: Number of lines of 2-dimensional MR encoding K parameter count register (KCNTR) 15 0 K parameter count KPR is used when processing multiple lines during MR encoding KPR specifies the number of 2-dimensional MR encoding lines following the 1-dimensional MR encoding. The number of lines can be specified within the range of 0–65535. KPR is only valid during 1-dimensional MR encoding command processing. When a 1-dimensional MR encoding command is issued, DICEP-A performs one line of 1-dimensional MR encoding and then performs 2-dimensional MR encoding in accordance with the value specified in KPR. As each line is processed, DICEP-A decrements the KCNTR value by one. When this value becomes zero, the KPR value is loaded into KCNR and 1-dimensional encoding of the next line is performed. Example–when KPR=3 1st Line: 1-dimensional MR encoding 2nd Line: 2-dimensional MR encoding 3rd Line: 2-dimensional MR encoding 4th Line: 2-dimensional MR encoding 4. Expanded address space DICEP-A allows access of up to 4 Mbytes of image memory address space. The high bytes of the start address registers A, B, and C (SARA, SARB, SARC) are specified using start address high byte registers A, B, and C (SARAH, SARBH, SARCH). Start address A 15 5 4 3 2 1 0 – MA_{21} MA_{20} MA_{19} MA_{18} MA_{17} MA_{16} (SARAH) MA_{15} MA_0 (SARA) Start address B 15 5 0 – MA_{21} MA_{20} MA_{19} MA_{18} MA_{17} MA_{16} (SARBH) MA_{15} MA_0 (SARB) Start address C 15 5 0 – MA_{21} MA_{20} MA_{19} MA_{18} MA_{17} MA_{16} (SARCH) MA_{15} MA_0 (SARC)	No K parameter register is used. 1-dimensional MR encoding commands and 2-dimensional MR encoding commands are issued line-by-line as required.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage *1	V_{DD}	-0.3 to +7.0	V
Input Voltage *1	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation *2	P_C	500	mW

*1 Value based on V_{SS}=0V
*2 Tolerance at Ta=25°C

Recommended Operating Conditions

Item	Symbol	min	typ	max	Unit
Supply Voltage *	V_{DD}	4.75	5	5.25	V
Input Voltage *	V_{IL}	-0.3	—	0.8	V
	V_{IH}	2.2	—	V_{DD}+0.3	V
Operating Temperature	T_{OPR}	0	25	70	°C

* Value based on V_{SS}=0V

<Use Precautions>
(1) Pay attention to dielectric breakdown.
In handling, ground your body through a high resistance (500 or 600k to 1MΩ).
(2) This device operates at a high speed. Wire its signal lines with care to prevent noise caused by crosstalk of reflection.
(3) It is recommended to put a bypass capacitor between V_{DD} and V_{SS} (GND) to eliminate wire noise. (C=1μF min.)
(4) CMOS has the following specific problem:
If the input signal level goes to the intermediate value (V_{IL} max≦V_{IN}≦V_{IH} min), I_{DD} increases and may cause a latch-up event. Pay special attention to the case as the buses, input terminals or unused terminals float at a power-on time.

Electrical Characteristics

DC Characteristics

(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Test Condition
Input High Voltage	V_{IH}	2.2	—	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	
Input Leakage Current	I_{IN}	-10	—	10	μA	V_{IN}=0 to 5.25V
Three-State (Off State) Leakage Current	I_{tsi}	-10	—	10	μA	V_{IN}=0 to 5.25V
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH}=-400μA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL}=2mA
Power Dissipation	P_D	—	150	250	mW	

AC Characteristics

Clock Timing

(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
4CLK Cycle Time	ϕ_{4CLK}	31.25	—	500	ns	4CLK	Fig. 2
4CLK Pulse Width	PW_H	10.5	—	—	ns	4CLK	
	PW_L	11.0	—	—	ns	4CLK	

System Bus Timing
Using a 68 Type MPU
(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
DS Cycle Time	t_{CYCE}	350	—	—	ns	DS	Fig. 3 Fig. 6
DS Pulse Width	PW_{EH} PW_{EL}	150	—	—	ns	DS	
DS Rise or Fall Time	t_{Er} t_{Ef}	—	—	25	ns	DS	
Address Setup Time	t_{AS}	20	—	—	ns	$\overline{CS}$, A_0-A_2, R/$\overline{W}$	Fig. 3
Address Hold Time	t_{AH}	20	—	—	ns	$\overline{CS}$, A_0-A_2, R/$\overline{W}$	
IRQT Inactive Delay Time	t_{IRQT}	ϕ_{4CLK} ×4+180	—	ϕ_{4CLK} ×8+180	ns	IRQT	
Output Data Delay Time	t_{DDR}	—	—	150	ns	D_0-D_7	Fig. 3 Fig. 6
Output Data Hold Time	t_{DHR}	10	—	—	ns	D_0-D_7	
Input Data Setup Time	t_{DSW}	20	—	—	ns	D_0-D_7	
Input Data Hold Time	t_{DHW}	30	—	—	ns	D_0-D_7	
$\overline{DACKI}$ Setup Time	t_{AS}	20	—	—	ns	$\overline{DACKI}$	Fig. 6
$\overline{DACKI}$ Hold Time	t_{AH}	20	—	—	ns	$\overline{DACKI}$	
DRQTO Inactive Delay Time	t_{DRQTO}	—	—	180	ns	DRQTO	

Using an 80 Type MPU
(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
Address Setup Time	t_{AR}	20	—	—	ns	$\overline{CS}$, A_0-A_2	Fig. 4
Address Hold Time	t_{RA}	20	—	—	ns	$\overline{CS}$, A_0-A_2	
IRQT Inactive Delay Time	t_{IRQT}	ϕ_{4CLK} ×4+180	—	ϕ_{4CLK} ×8+180	ns	IRQT	
Output Data Delay Time	t_{RD}	—	—	150	ns	D_0-D7	Fig. 4 Fig. 7
Output Data Hold Time	t_{DR}	10	—	—	ns	D_0-D_7	
Read Pulse Width	t_{RW}	150	—	—	ns	DS	
Address Setup Time	t_{AW}	20	—	—	ns	$\overline{CS}$, A_0-A_2	Fig. 5
Address Hold Time	t_{WA}	20	—	—	ns	$\overline{CS}$, A_0-A_2	
Input Data Setup Time	t_{WD}	20	—	—	ns	D_0-D_7	Fig. 5 Fig. 8
Input Data Hold Time	t_{DW}	30	—	—	ns	D_0-D_7	
Write Pulse Width	t_{WW}	150	—	—	ns	R/$\overline{W}$	
$\overline{DACKI}$ Setup Time	t_{AR}	20	—	—	ns	$\overline{DACKI}$	Fig. 7
$\overline{DACKI}$ Hold Time	t_{RA}	20	—	—	ns	$\overline{DACKI}$	
$\overline{DACKI}$ Setup Time	t_{AW}	20	—	—	ns	$\overline{DACKI}$	Fig. 8
$\overline{DACKI}$ Hold Time	t_{WA}	20	—	—	ns	$\overline{DACKI}$	
DRQTO Inactive Delay Time	t_{DRQTO}	—	—	180	ns	DRQTO	Fig. 7 Fig. 8

Document Image Bus Timing
(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C, unless otherwise noted. However, the values in the parentheses are the values at Cout=60pF.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
Address Enable Active Delay Time	t_{DAEL}	—	—	120	ns	$\overline{MAEN}$	Fig. 9 Fig. 10
Address Enable Inactive Delay Time	t_{DAEH}	—	—	110	ns	$\overline{MAEN}$	
Address Strobe Active Delay Time	t_{DASH}	—	—	110	ns	MAS	
Address Strobe Inactive Delay Time	t_{DASL}	—	—	100	ns	MAS	
Data Strobe Valid Delay Time	t_{DDSV}	—	—	110	ns	$\overline{UDS}$, $\overline{LDS}$	
Data Strobe Active Delay Time	t_{DDSL}	—	—	130	ns	$\overline{UDS}$, $\overline{LDS}$	
Data Strobe Inactive Delay Time	t_{DDSH}	—	—	110	ns	$\overline{UDS}$, $\overline{LDS}$	
Data Enable Active Delay Time	t_{DDEL}	—	—	110	ns	$\overline{MDEN}$	Fig. 9
Data Enable Inactive Delay Time	t_{DDEH}	—	—	110	ns	$\overline{MDEN}$	
Read Valid Delay Time	t_{DRDV}	—	—	110	ns	$\overline{IOR}$, $\overline{MR}$	Fig. 9 Fig. 10
Read Active Delay Time	t_{DRDL}	—	—	120	ns	$\overline{IOR}$, $\overline{MR}$	
Read Inactive Delay Time	t_{DRDH}	—	—	100	ns	$\overline{IOR}$, $\overline{MR}$	
Write Valid Delay Time	t_{DWRV}	—	—	110	ns	$\overline{IOW}$, $\overline{MW}$	
Write Active Delay Time	t_{DWRL}	—	—	110	ns	$\overline{IOW}$, $\overline{MW}$	
Write Inactive Delay Time	t_{DWRH}	—	—	120	ns	$\overline{IOW}$, $\overline{MW}$	
Address Valid Delay Time	t_{MAV}	—	—	140	ns	MA/MD_0-MA/MD_{15} MA_{16}-MA_{21}	
Address Hold Time	t_{MAH}	25	—	—	ns	MA/MD_0-MA/MD_{15} MA_{16}-MA_{21}	
Data Setup Time (Read)	t_{DSR}	10	—	—	ns	MA/MD_0- MA/MD_{15}	Fig. 9
Data Hold Time (Read)	t_{DHR}	70	—	—	ns	MA/MD_0- MA/MD_{15}	
Data Delay Time (Write)	t_{DDW}	—	—	140	ns	MA/MD_0- MA/MD_{15}	
Data Hold Time (Write)	t_{DHW}	20	—	—	ns	MA/MD_0- MA/MD_{15}	
DMA Acknowledge Active Delay Time	t_{DAKL}	—	—	110	ns	$\overline{DACKO}$	Fig. 10

(continued)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
DMA Acknowledge Inactive Delay Time	t_{DAKH}	—	—	100	ns	$\overline{DACKO}$	Fig. 10
DMA Active Delay Time	t_{DDMAL}	—	—	120	ns	$\overline{DMA}$	
DMA Inactive Delay Time	t_{DDMAH}	—	—	110	ns	$\overline{DMA}$	
DTC Active Delay Time	t_{DDTCH}	—	—	ϕ_{4CLK} +110	ns	DTC	
DTC Inactive Delay Time	t_{DDTCL}	—	—	100	ns	DTC	
BRQT Rise	t_{DBRQH}	—	—	100	ns	BRQT	Fig. 11
BRQT Fall	t_{DBRQL}	—	—	110	ns	BRQT	

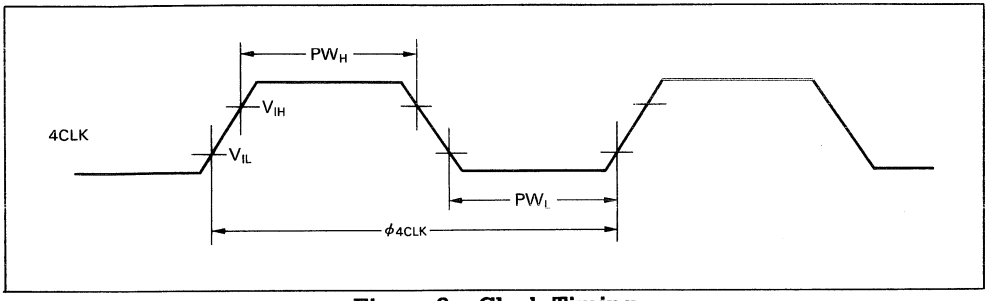


Figure 2 Clock Timing

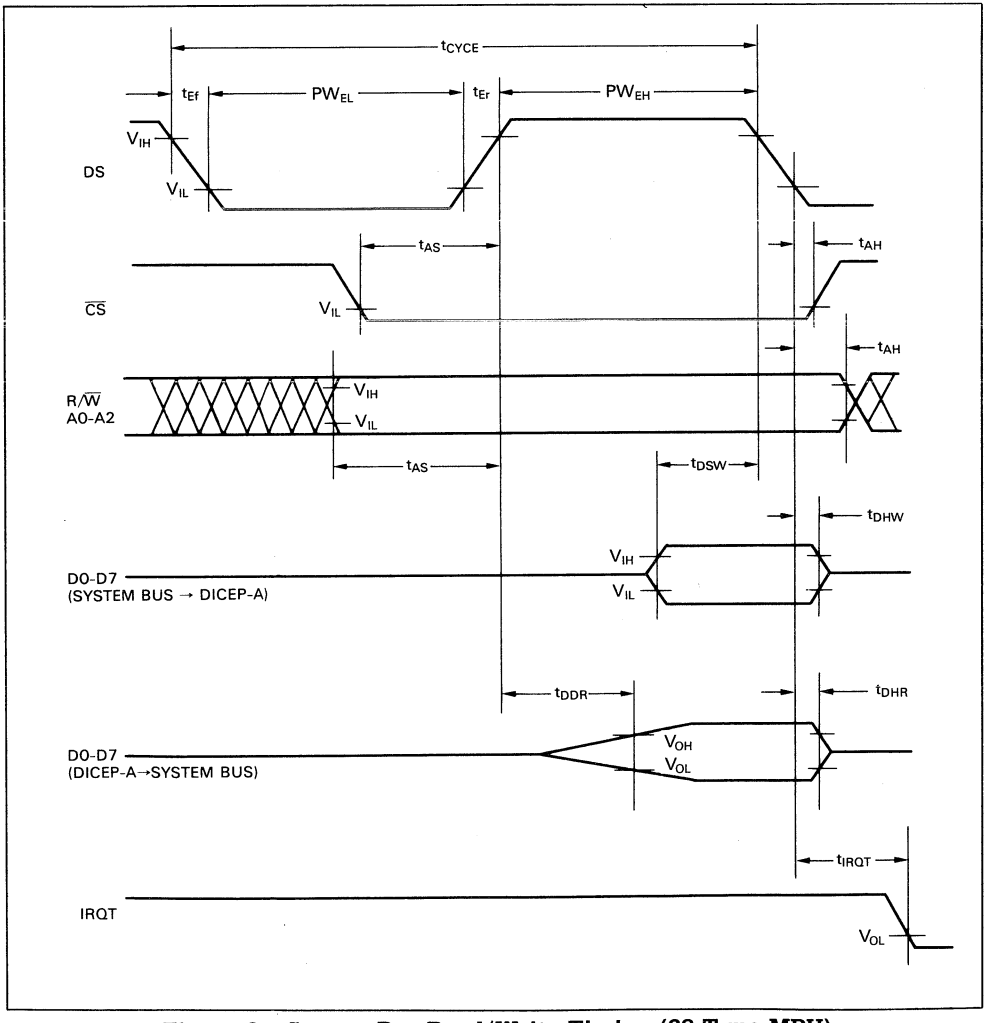


Figure 3 System Bus Read/Write Timing (68 Type MPU)

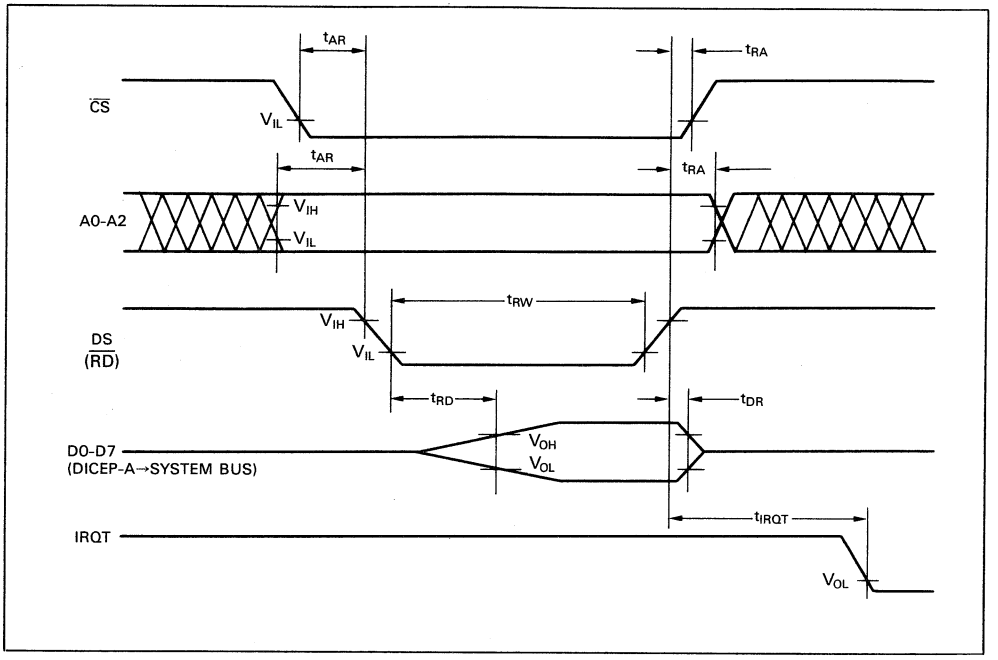


Figure 4 System Bus Read Timing (80 Type MPU)

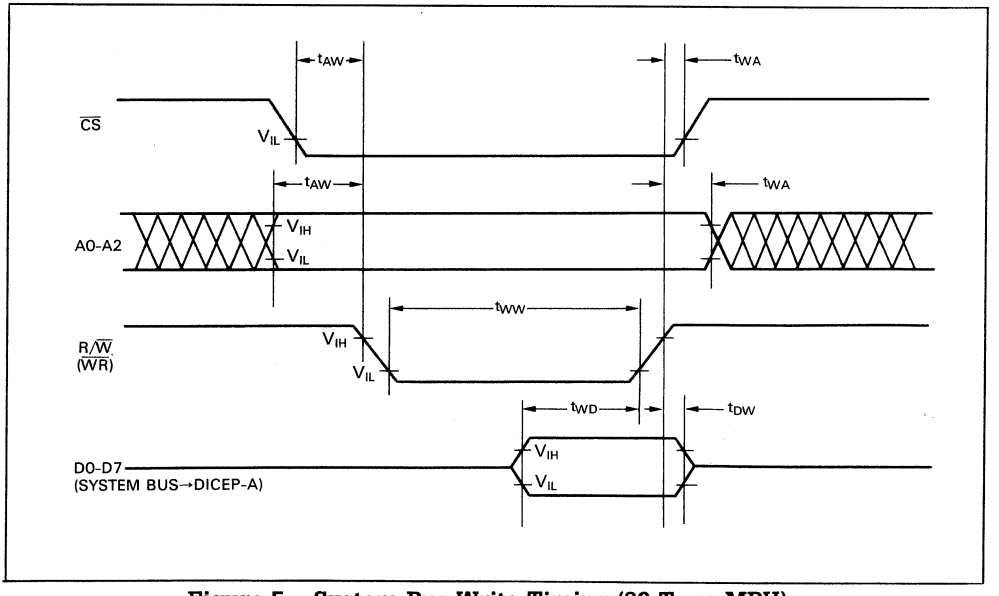


Figure 5 System Bus Write Timing (80 Type MPU)

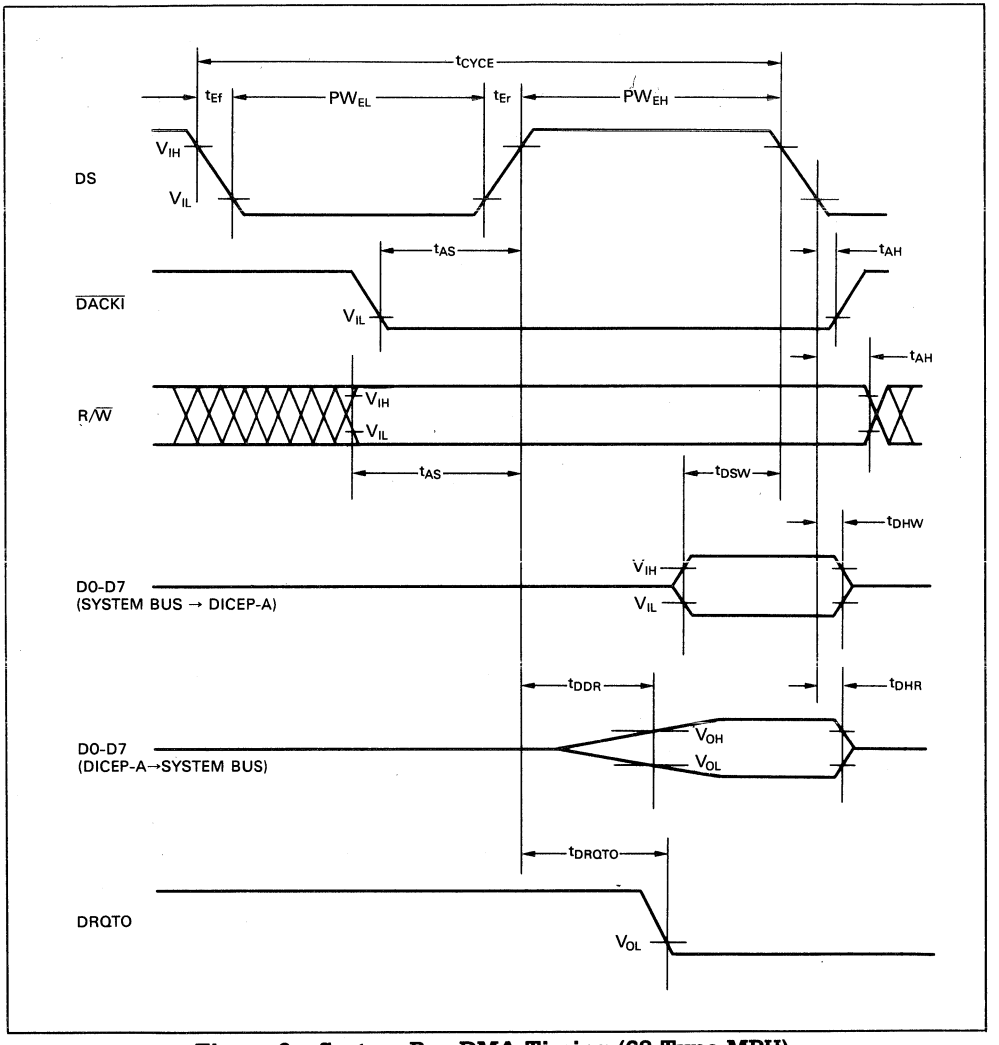


Figure 6 System Bus DMA Timing (68 Type MPU)

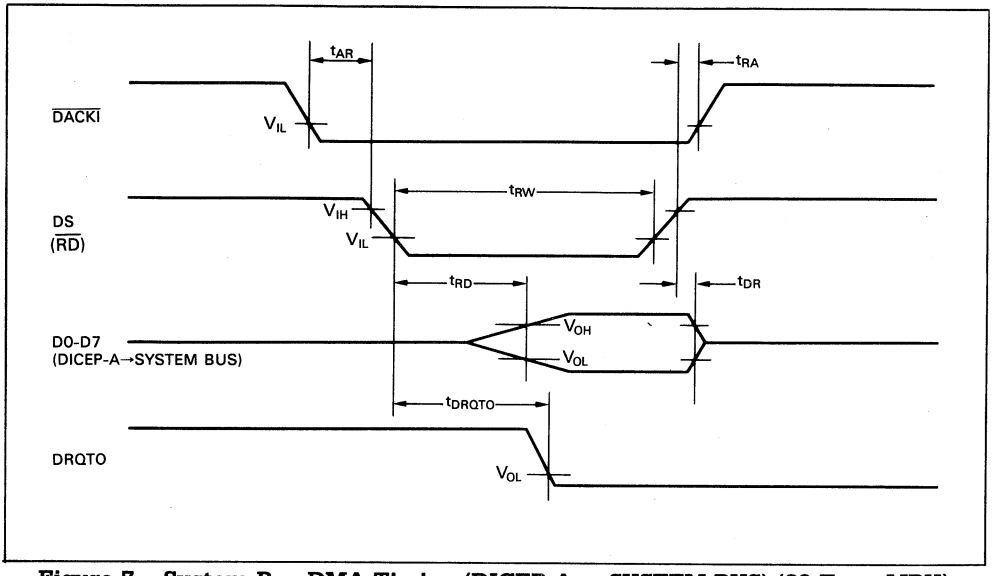


Figure 7 System Bus DMA Timing (DICEP-A → SYSTEM BUS) (80 Type MPU)

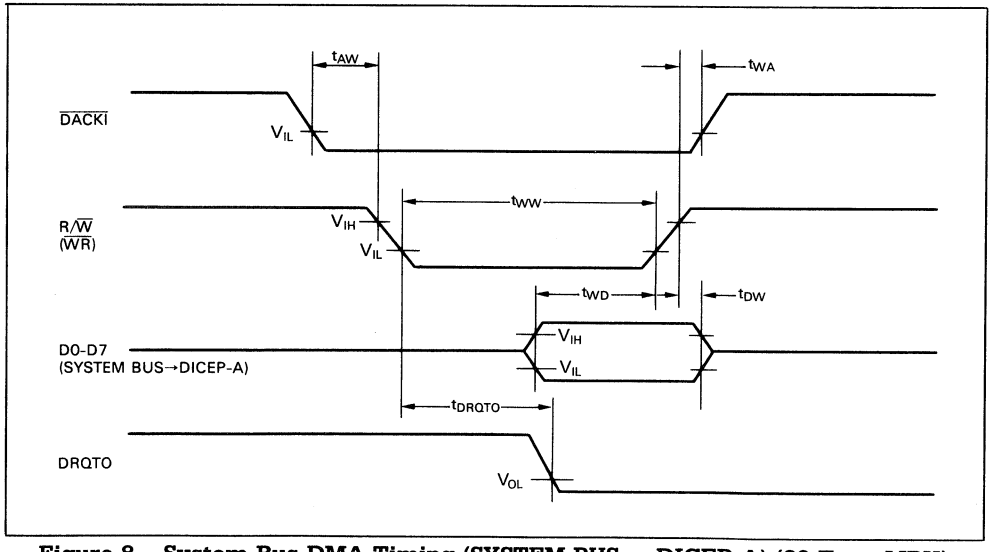


Figure 8 System Bus DMA Timing (SYSTEM BUS → DICEP-A) (80 Type MPU)

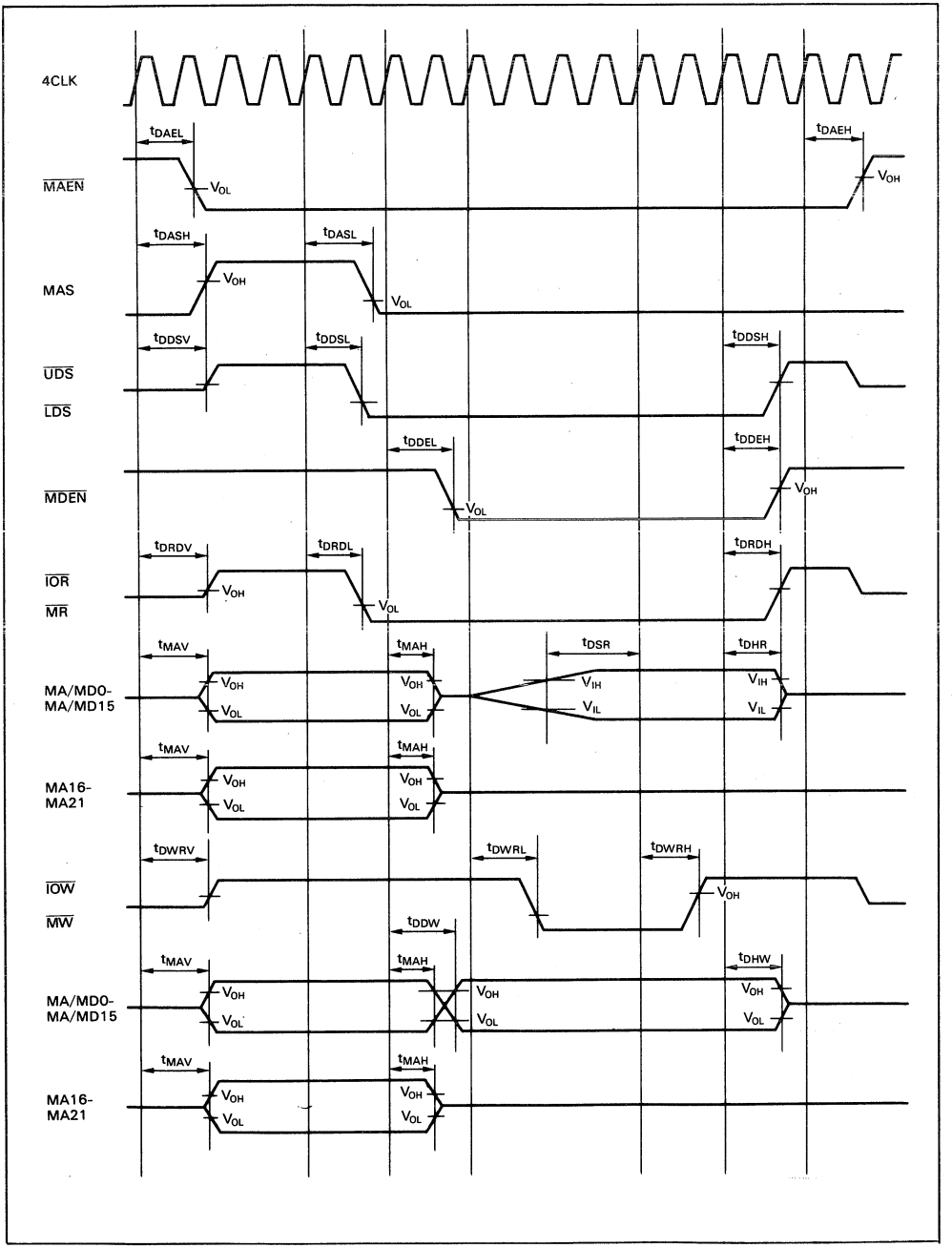


Figure 9 Document Image Bus Read/Write Timing

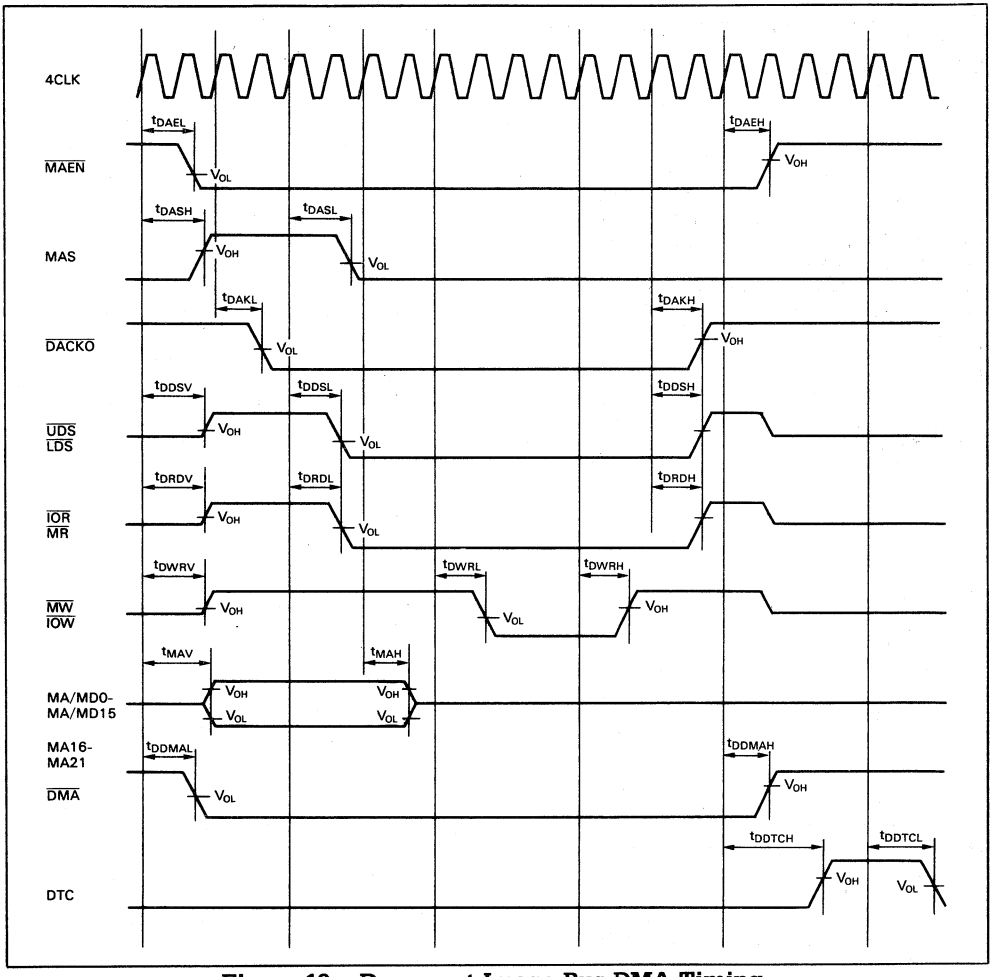


Figure 10 Document Image Bus DMA Timing

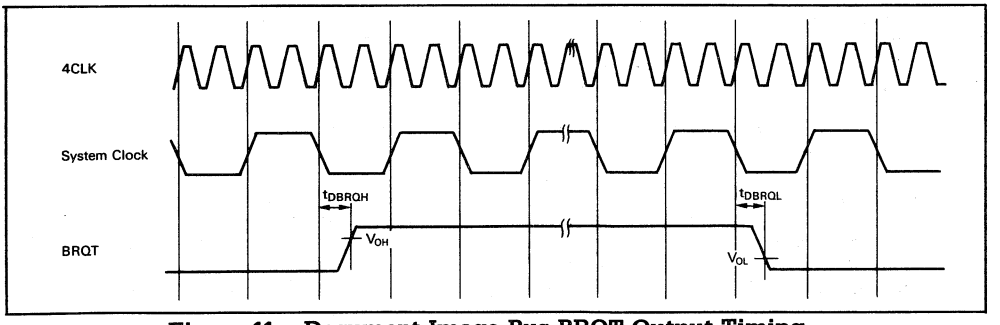


Figure 11 Document Image Bus BRQT Output Timing

Refer to user's manual (No. ADE-607-001) for detail of this product.

HD63185

Under Development

Document Image Compression and Expansion Processor Enhanced (DICEP-E)

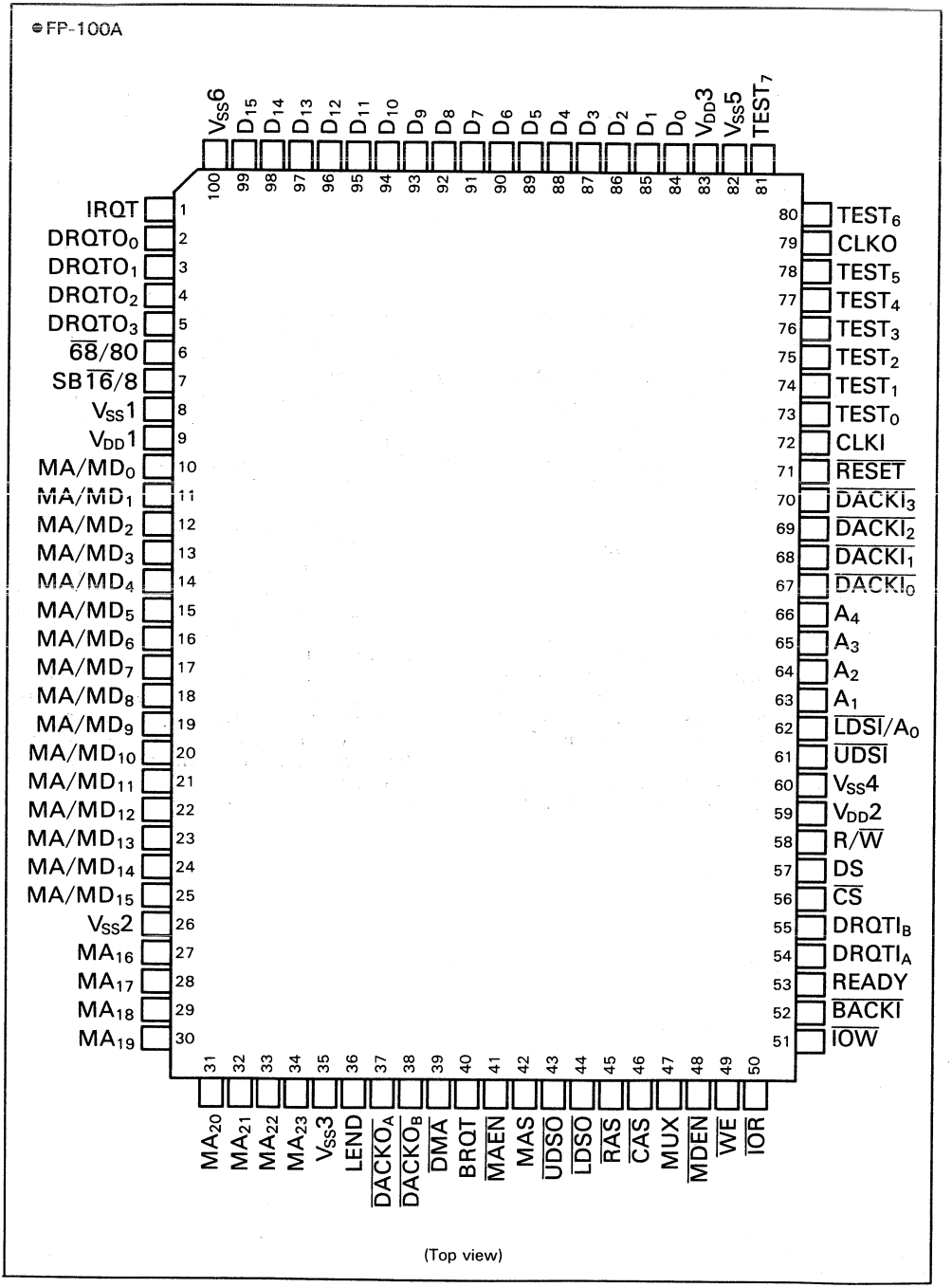
DICEP-E is an LSI that performs compression (encoding) and expansion (decoding) of 2-value data used to represent a document image. It is positioned at the high end of the DICEP (HD63085) and DICEP-A (HD63183), and has been designed for application in such electronic office devices as facsimiles apparatus (G3, G4), intelligent copiers, image workstations, terminals, and filing systems. DICEP-E adopts the MH (Modified Huffman), MR (Modified Relative Element Address Designate) and M²R (Modified MR) coding scheme, which are the G3 and G4 standards recommended by CCITT (International Telegraph and Telephone Consultative Committee).

Features

- Compatible with the CCITT recommendations for G3 and G4 facsimile apparatus
- Bit unit page processing using simple MPU instructions
  The number of picture elements in each line and the line length can be specified in bit units. Encoding (compression) and decoding (expansion) of 2-value data for multiple scan lines can also be performed.
- On-chip line memory for high-speed encoding and decoding
  An on-chip line memory (6,144 bits/line) for reference and code lines provides high-speed encoding and decoding.
  —Transfer of data to the on-chip line memory is performed by accessing 1 word (8-bit/16-bit) in 5 machine cycles (312.5ns minimum) for 1-line continuous access.
  —On-chip line memory also allows reference line access during 2-dimensional encoding to be performed by accessing 1 word in 3 cycles, and parallel processing is also possible.
  —An on-chip changed picture element detector and decoded picture element generator perform changed picture element detection and image data generation for 1 word of data per cycle.
- Specification of split processing memory area for encoding/decoding
  Byte-by-byte split processing of code data and image data can be performed in any memory area, and processing can be restarted from any address. This allows split processing in memory block units, rather than line units.
- Flexible system configuration
  —Connectable with either 68 Series or 80 Series MPU.
  —Two bus interfaces: system bus interface and image bus interface. Both the system bus and image bus sizes are selectable between 8-bit and 16-bit.
  —The port for code data and image data write to and read from DICEP-E can be selected as desired for connection to the system bus interface.
- Line-by-line alternate encode/decode
  Line-by-line alternate encoding and decoding, or time sharing simultaneous processing of inter-bus transfers and decoding can be performed.
- High-speed DMA transfer
  —2-channel simultaneous DMA transfer can be performed for transfer between the I/O device on the image bus and image memory, and between two image memories. Maximum transfer speed is 6.4M bytes/second.
  —Including a DMA controller on the system bus of the DICEP-E allows 4-channel (write to/read from FIFO and line memory) independent DMA transfer.
- Code-code conversion
  Code data can be converted to different code data without using external memory.
- A selection of coded data configurations
  The configuration of code generated during the encode procedure can be specified as MSB first or LSB first.
- Conversion of memory data configuration on the image bus
  During DMA transfer between memories, memory data on the image bus can be converted to four different configurations in 8-bit or 16-bit unis.
- Read-modify-write
  During decoding, logical operations can be performed using the decoded data in the on-chip line memory and the image data stored in external memory. Up to 16 logical operations, including AND, OR, and EOR are available, and operations can be performed line by line.
- DRAM control signal
  Memory ROW and COLUMN switching signals ($\overline{RAS}$, $\overline{CAS}$, MUX) are output for image memory DRAM on the image bus.

- A host of programmable parameters
  On-chip programmable registers provide flexibility for application in a wide variety of systems.
  - —Parameters can be changed before issuance of each instruction.
  - —Scan line length is programmable in 1-bit units, ranging from the image memory word size (8-bit/16-bit) up to 6,144 bits.
  - —Encoding, decoding, and data transfer can be selected individually or in any combination.
  - —MH, MR or M^2R coding scheme can be selected.
  - —The minimum number of code bits per line is programmable within the range of $0-2^{16}$-1.
  - —The number EOLs (end of line) is programmable within the range of $0-2^{16}$-1.
  - —The number RTCs (return to control) is programmable within the range of $0-2^{16}$-1.
  - —The number lines that must be processed is programmable within the range of $1-2^{16}$-1.
  - —The number lines that must be transferred during DMA transfer is programmable within the range of $1-2^{16}$-1.
  - —The number lines that are 2-dimension encoded following 1-dimension encoding during MR encoding is programmable within the range of $0-2^{16}$-1.
  - —The area for document image data area which is read and the area for the code data which is written during encoding can be specified within the range of $1-2^{16}$-1 bytes.
  - —The area for document image data area which is generated and the area for the code data which is read during decoding can be specified within the range of $1-2^{16}$-1 bytes.
- Data transfer between buses
  Data can be transferred between the system bus and image bus via the on-chip line memory, without encoding/decoding. Burst DMA transfer is performed in line units, also, access from the system bus is performed using write to and read from the control register line memory, allowing access from the MPU.
- Desired part of a document
  Specific portions of the original can be specified in bit units for cut and encoding/decoding. Also, data can be cut out during DMA transfer on the image bus in units that are the same size as the bus width of the I/O device.
- Octet mode
  Each line or the total number of code bits per page can be set in 8-bit or 16-bit units, depending on the bus size.
- High-speed operation
  - —Minimum instruction cycle time of 62.5ns
  - —Maximum input clock frequency of 16HMz
- Output of 1-line processing end signal
  In the multi-line processing mode, a line processing end signal is output from the LEND pin after completion of processing for 1 line. During encoding, this signal is output following generation of 1 line's code (when it is set in the register immediately before E-FIFO), and during decoding it is output following writing from internal line memory to external memory.
- 100-pin plastic QFP (FP-100A)

Pin Arrangement



(Top view)

Functional Summary

Item	Function
Coding scheme	MH, MR, M^2R
Maximum scan-line length	6,144 picture elements/line
Number of processing lines	64k lines (2^{16}-1)
Image memory address space	8M words (16M bytes)
Picture element processing units	Bit units (number of processing picture elements, line length)
Maximum DMA transfer rate	6.4M bytes/second
Internal line memory maximum access speed	6.4M bytes/second
Maximum split processing memory area (image data, code data)	64k bytes (byte units)
Generated code configuration	LSB/MSB first
Read-modify-write	Operation processing—16 types (AND, OR, EOR, etc.)
Coding speed	See figure 1

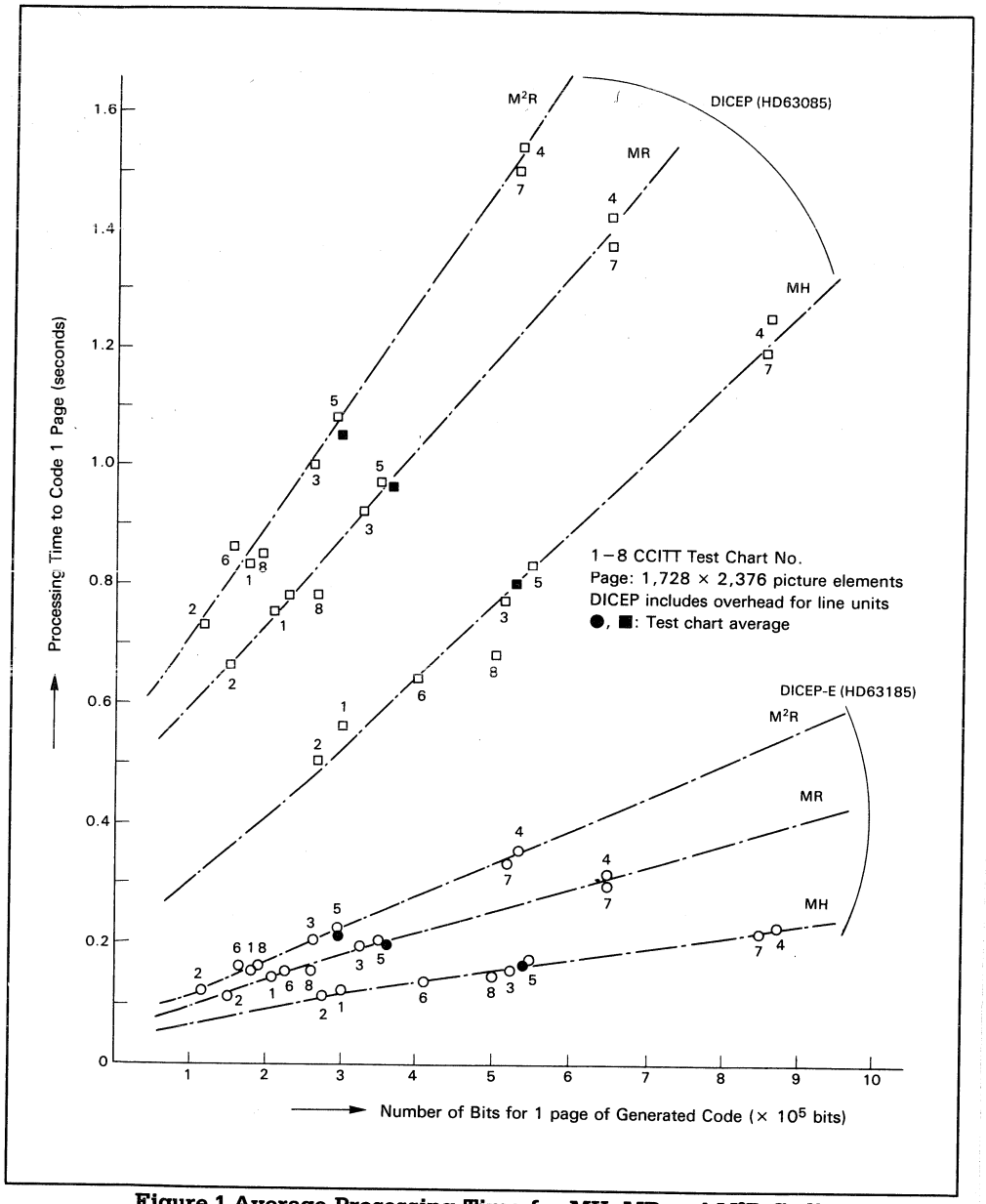


Figure 1 Average Processing Time for MH, MR and M²R Coding

Functional Comparison of DICEP Family

	DICEP (HD63085)	DICEP-A (HD63183)	DICEP-E (HD63185)
Coding scheme	MH, MR, M^2R run length	MH, MR, M^2R run length	MH, MR, M^2R
Image memory address space	64k bytes	4M bytes (FP) 64k bytes (P)	16M bytes
Bus width (system/image)	(S) 8 bits (D) 8/16 bits	(S) 8 bits (D) 8/16 bits	(S) 8/16 bits (D) 8/16 bits
Page mode function	×	○	○
Picture element processing unit	Byte	Byte	Bit
Coding time (M^2R) (standard chart average, including overhead)	1.06 seconds/A4 page	0.94 seconds/A4 page	0.22 seconds/A4 page
Bus interface	1-channel FIFO	2-channel FIFO	Line internal memory (6kb × 2) 2-channel FIFO

Block Diagrams

System Bus Interface

The system bus interface allows interfacing with such 16-bit MPUs such as the H16 Series and 68000, and with 8-bit MPUs such as the 6800 Series and 64180 Series. This block includes control registers that can directly access the MPU, and can also accommodate a 4-channel DMA for data transfer to FIFO and line memory during encoding/decoding.

Microprogram Controller

The microprogram controller stores the encoded/decoded program in microprogram ROM and controls all of the other blocks.

This block consists of a 48-bit × 512-word microprogram ROM, and sequence controller and a pipeline registers.

Execution Unit

The execution unit generates image memory addresses, and calculates run lengths, the position of the changed picture elements and the relative distance between changed picture elements on the code line and those on the reference line.

This block consists of 38 16-bit registers, and arithmetic unit (AU), and an adder. Registers can contain any value sent from the MPU, via the system bus interface control registers.

Coder and Decoder

The coder generates code table ROM addresses in accordance with the input run lengths and relative distances, and references the code table ROM to generate an appropriate code. The decoder, on the other hand, generates a code table ROM address based on the input code, and references the code table ROM to generate references or relative distances.

This block consists of 8-bit × 1024-word code table ROM, a code table ROM interface, 16-bit × 2-word or 8-bit × 4-word (optional) encode FIFO (E-FIFO) and decode FIFO (D-FIFO). The code table ROM stores data for reference during encoding and decoding, while the code table ROM interface generates code table ROM addresses. E-FIFO is used for temporary storage of code during encoding, while D-FIFO is used for temporary storage of code during decoding.

Changed Picture Element Detector

The changed picture element detector detects picture elements whose color (black/white) is different from the immediately preceding picture element on the same scan line. This circuit can detect changed picture elements for 1 word (16 bits) of image memory per instruction cycle.

This block consists of two changed picture element detectors — a reference line detector and an encoded line detector.

Decoded Picture Element Generator

The decoded picture element generator can generate 1 word (16 bits) per instruction cycle of restored picture element data, based on changed picture element position data.

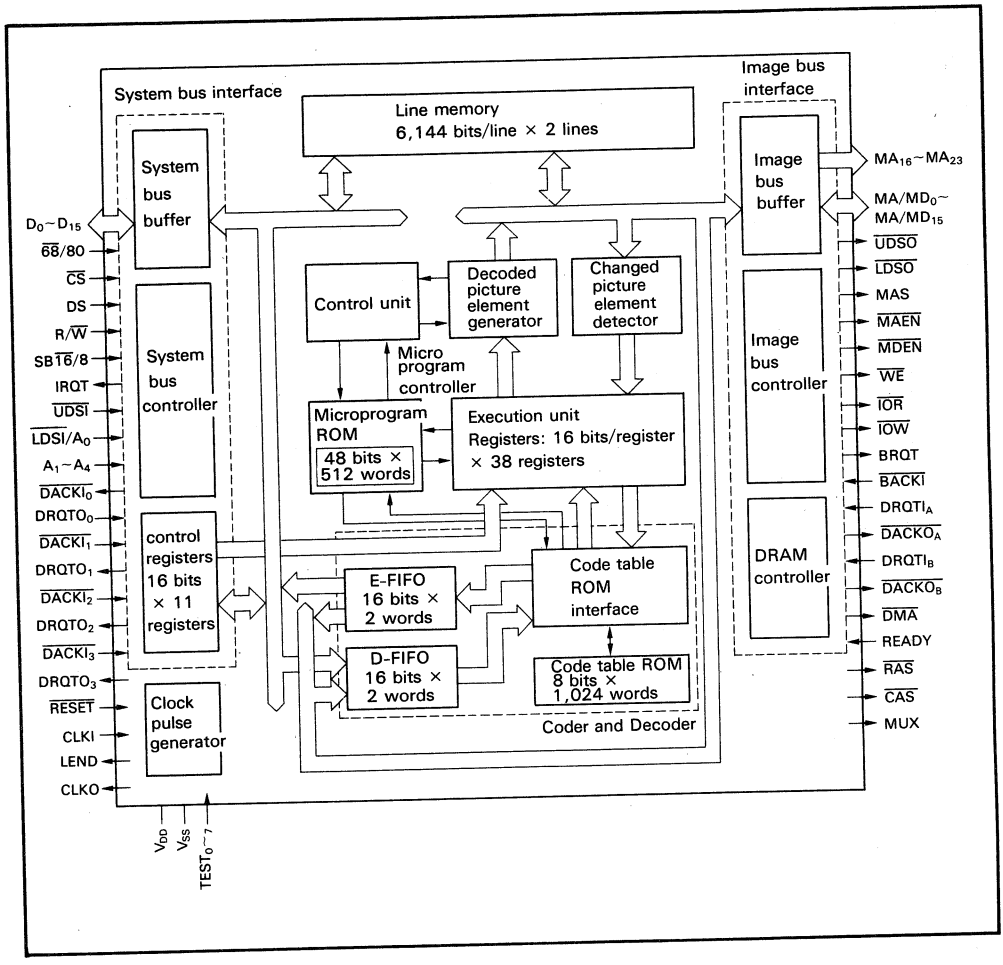
Line Memory

Line memory can be used for accumulation of 2-lines of image data during encoding/decoding, or as buffer memory during data transfer between the system bus and image bus.

This memory is consists of static RAM, in the capacity of 6,144 bits per line. One line of line memory is used as the encode/decode reference line, while another line is used to store data during encoding and data transfer between buses.

Document Image Bus Interface

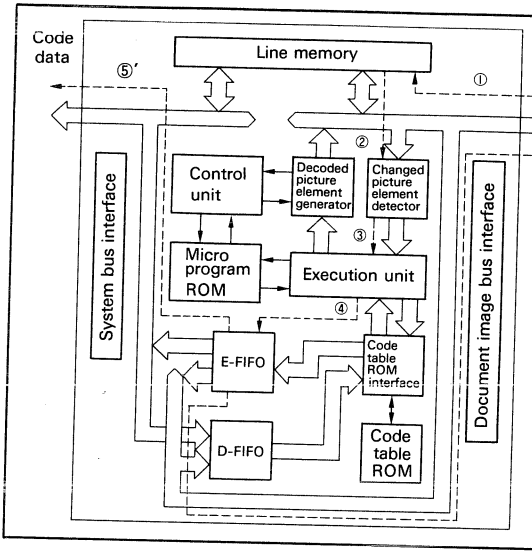
The document image bus interface provides an interface between DICEP-E and the image bus, with a multiplexed 16 bits for addresses and data, and 8 bits for the upper 8 bits of the address. In addition to a bus arbitration function, this block outputs signals for controls of such image bus functions as 2-channel DMA control.


System bus interface
Image bus interface
Line memory
6,144 bits/line × 2 lines
System bus buffer
Image bus buffer
System bus controller
Image bus controller
DRAM controller
Control unit
Decoded picture element generator
Changed picture element detector
Micro program controller
Microprogram ROM
48 bits × 512 words
Execution unit
Registers: 16 bits/register
× 38 registers
control registers 16 bits × 11 registers
E-FIFO 16 bits × 2 words
D-FIFO 16 bits × 2 words
Code table ROM interface
Code table ROM 8 bits × 1,024 words
Coder and Decoder
Clock pulse generator
D0~D15
68/80
CS
DS
R/W
SB16/8
IRQT
UDSI
LDSI/A0
A1~A4
DACKI0
DRQTO0
DACKI1
DRQTO1
DACKI2
DRQTO2
DACKI3
DRQTO3
RESET
CLKI
LEND
CLKO
VDD
VSS
TEST0~7
MA16~MA23
MA/MD0~ MA/MD15
UDSO
LDSO
MAS
MAEN
MDEN
WE
IOR
IOW
BRQT
BACKI
DRQTIA
DACKOA
DRQTIB
DACKOB
DMA
READY
RAS
CAS
MUX

Data Processing Flow

Encoding Flow

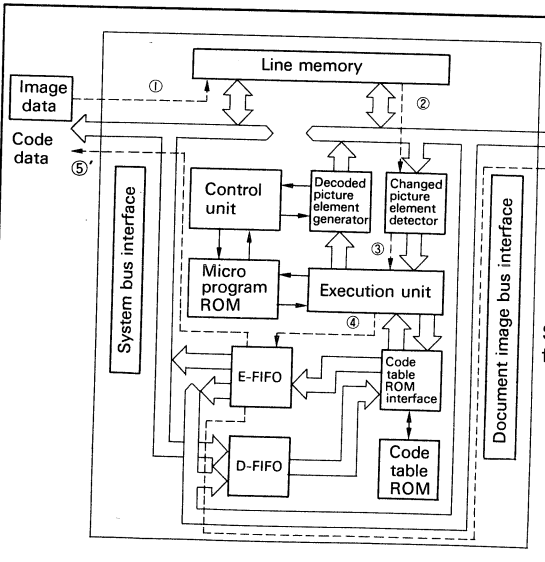
See figure 2 and 3 for encoding flow.



Encoding Flow (1)

1. Image data on the image bus are accessed and stored in line memory.
2. Line memory is accessed and changed points (changed pixels) are detected.
3. Run length calculation is performed and the mode is determined.
4. Code table ROM is accessed, code is generated, and code data are set in encode FIFO (E-FIFO).
5. Code data are written to the image bus via the image bus buffer.
   or
   5′. E-FIFO is accessed by external DMAC and code data are transferred to the system bus ($DRQTO_0$, $\overline{DACKI_0}$).

Figure 2 DICEP-E Encoding Flow (1)



Encoding Flow (2)

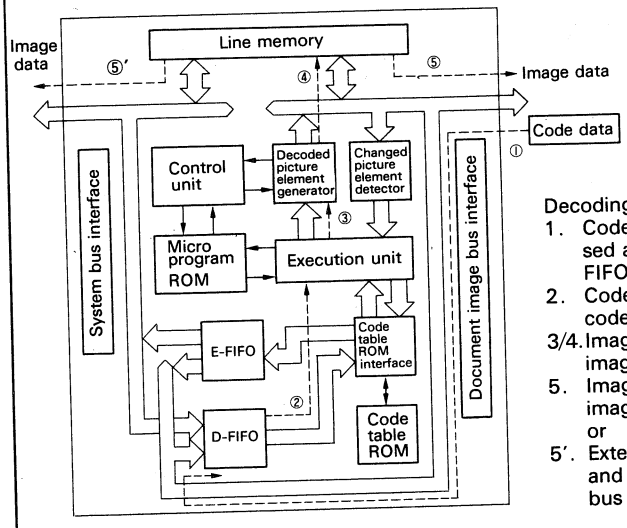
1. External DMAC transfers image data on the system bus to line memory ($DRQTO_2$, $\overline{DACKI_2}$)

Steps 2 through 5 (5′) are the same as those for Encoding Flow (1).

Figure 3 DICEP-E Encoding Flow (2)

Decoding Flow

See figure 4 and 5 for decoding flow.



Decoding Flow (1)

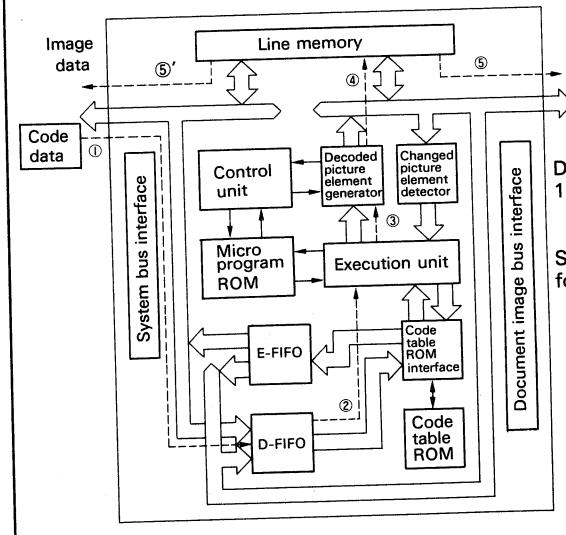
1. Code data on the image bus are accessed and code data are set in the decode FIFO (D-FIFO).
2. Code table ROM is accessed and the code is determined.

3/4. Image data are set in line memory via the image data restore circuit.

5. Image data are written to memory on the image bus via the image bus buffer.
   or

5′. External DMAC accesses line memory and transfers image data to the system bus ($\overline{DRQTO_3}$, $\overline{DACKI_3}$).

Figure 4 DICEP-E Decoding Flow (1)



Decoding Flow (2)

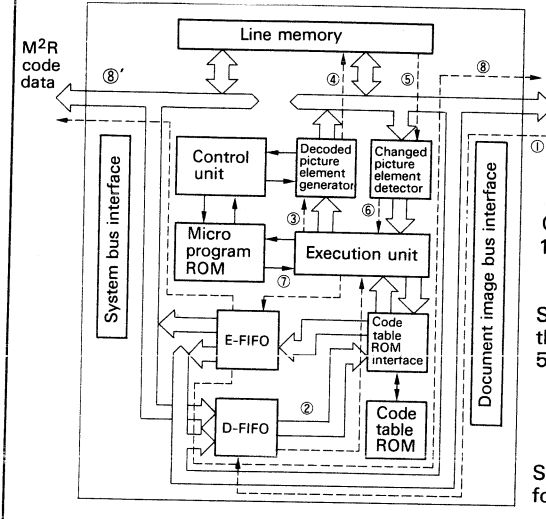
1. External DMAC transfers code data on the system bus to D-FIFO ($\overline{DRQTO_1}$, $\overline{DACKI_1}$).

Steps 2 through 5 (5′) are the same as those for Decoding Flow (1).

Figure 5 DICEP-E Decoding Flow (2)

Code-Code Conversion Flow

The example shown here is for conversion of MH code data into M²R code data. Other combinations are also possible.



Code-Code Conversion Flow (1)

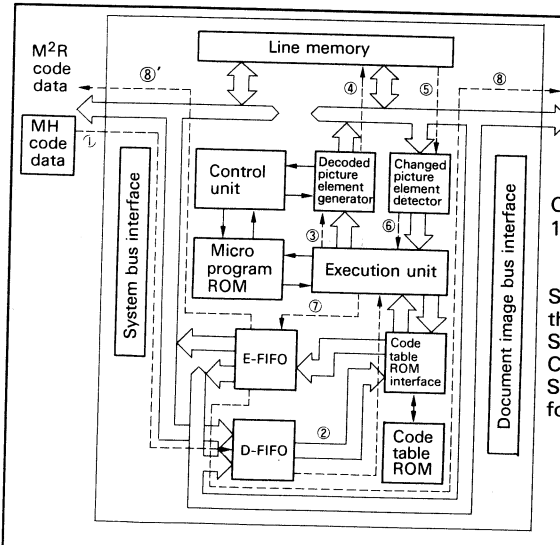
1. Code data on the image bus are accessed and code data are set in decode FIFO (D-FIFO).

Steps 2, 3, and 4 are the same as those for the decoding flow.

5. While referencing the reference line of the image data being restored in line memory, the data are converted to M²R format. At this time, the reference line data in the first line is reset.

Steps 6 through 8 (8') are the same as that for the encoding flow.

Figure 6 DICEP-E Code/Code Conversion Flow (1)



Code-Code Conversion Flow (2)

1. External DMAC transfers code data on the system bus to D-FIFO ($\overline{DRQTO_1}$, $\overline{DACKI_1}$).

Steps 2, 3, and 4 are the same as those for the decoding flow.

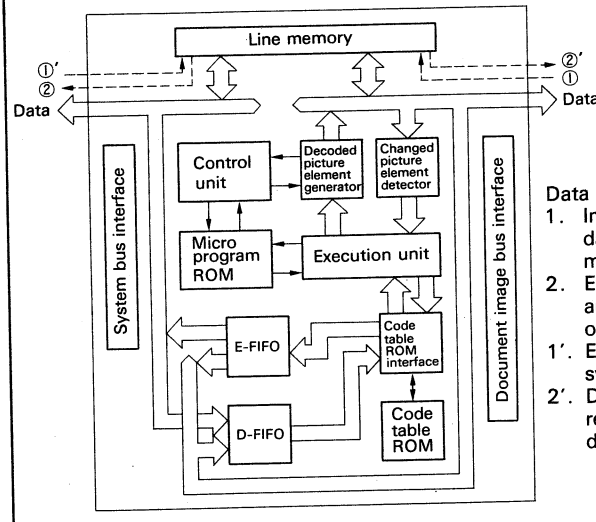
Step 5 is the same as that for Code-Code Conversion Flow (1).

Steps 6 through 8 (8') are the same as those for the encoding flow.

Figure 7 DICEP-E Code/Code Conversion Flow (2)

Data Transfer Between Buses Flow

The following shows the flow for transfer between the system bus and document image bus without data encoding/decoding.



Data Transfer Between Buses-Flow

1. Image bus memory data or I/O device data are accessed and stored in line memory.
2. External DMAC accesses line memory and transfers data to the system bus.
   or
1'. External DMAC transfers data on the system bus to line memory.
2'. Data stored in line memory are transferred to image bus memory or an I/O device.

Figure 8 DICEP-E Data Transfer Between Buses Flow

System Configuration

DICEP-E has been designed to allow the widest possible application. It features both an image bus and system bus, and data encoding/decoding can be performed using either one of these busses or both of them. Figure 9 shows a sample of a system that applies DICEP-E.

MPU

- Can be used with 8-bit or 16-bit system data bus.
- Can be interfaced with 68 Series or 80 Series.

Main Mamory

Both image data and code data can be stored in main memory via the system bus.

DMAC

The following 4-channel independent DMA transfer operations are possible:

- Read of code data from encode FIFO (E-FIFO). ($DRQTO_0$, $\overline{DACKI_0}$)
- Write of code data to decode FIFO (D-FIFO). ($DRQTO_1$, $\overline{DACKI_1}$)
- Image data read to or write from line memory during encoding or inter-bus data transfer. ($DRQTO_2$, $\overline{DACKI_2}$)
- Image data read to or write from line memory during decoding. ($DRQTO_3$, $\overline{DACKI_3}$)

Image Memory

Both image data and code data can be stored in image memory via the image bus. Such functions as read-modify-write and data bit configuration change are available for transfer of data between the on-chip line memory and image memory, and between two image memories. DRAM control signals $\overline{RAS}$, $\overline{CAS}$, and MUX are output to support DRAM operations.

I/O Devices

A 2-channel DMA function allows independent control of such I/O devices as scanners, printers, etc. ($DRQTI_A$, $\overline{DACKO_A}$, $DRQTI_B$, $\overline{DACKO_B}$).

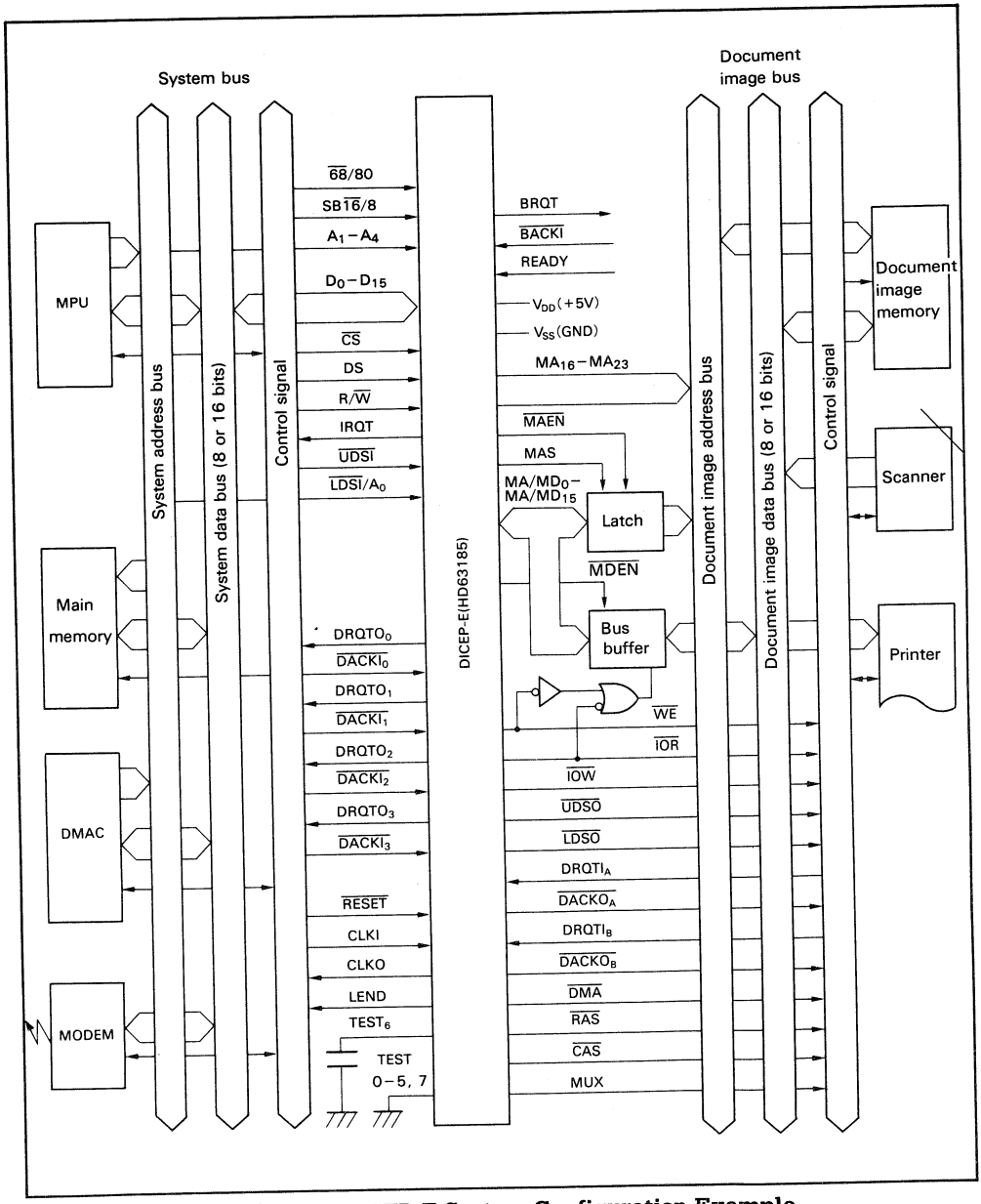


Figure 9 DICEP-E System Configuration Example

Internal Registers

DICEP-E registers can be classified into two groups: control registers that are directly accessible by the MPU, and parameter registers that can be accessed via the parameter buffer registers (PBR). The following details the access methods used for each type of register.

Registers directly accessible from the MPU

The control registers (CR), data buffer register (DBR), and FIFO can be accessed directly from the MPU, in accordance with A1—A4, when $\overline{CS}$ is L-level.

Teble 1 shows the directly accessible registers.

Registers accessible via the parameter buffer registers (PBR)

The parameter registers can be accessed via the parameter buffer registers (PBR). The MPU specifies a parameter register using the address register (AR), and a parameter written to the parameter buffer registers is written to the corresponding parameter register. The MPU writes parameters to parameter registers in the following sequence:

1. The PBR ready flag of the status register (SR) is checked to see if it is 1.
2. The desired parameter register is specified using the address register (AR).
3. The parameter is written to the parameter buffer registers (PBR).
4. When the parameter is written to PBR, DICEP-E judges whether address and parameter preparation are complete, and then writes the parameter to the specified register.

Table 2 shows the parameter registers.

Table 1 Control Registers

Address				R/W	Symbol	Register Name	Register Bits														
A4	A3	A2	A1				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	W	SCR	System control register	×	×	×	×	DFIFO ENB	EFIFO ENB	LMMEM ENB	CODE	RMW3	RMW2	RMW1	RMW0	DMABE	DMAAE	IOW/B	MW/B
				R	SSR	System status register	PBRWR RDY	PBRRD RDY	×	×	DFIFO ENB	EFIFO ENB	LMMEM ENB	CODE	RMW3	RMW2	RMW1	RMW0	DMABE	DMAAE	IOW/B	MW/B
0	0	0	1	R	IRR	Interrupt request register	×	×	×	DFEND FLG	EFEND FLG	MEMED FLG	DINI FLG	EINI FLG	ERR FLG	RTC FLG	×	INI FLG	DMAB FLG	DMAA FLG	DCE FLG	ECE FLG
0	0	1	0	W	ENCCR	Encoding control register	×	×	×	×	×	EM/IO	ENCS	ENCD	EC CNV	OCTET	"0"	PE	"0"	EC2	EC1	EC0
				R	ENCSR	Encoding status register	ECRWR RDY	LM RDYE	EFIFO RDY	×	×	EM/IO	ENCS	ENCD	EC CNV	OCTET	"0"	PE	"0"	EC2	EC1	EC0
0	0	1	1	W	DECCR	Decoding control register	×	×	×	×	×	"0"	DECS	DECD	DC CNV	RMWE	"0"	EOLE	"0"	DC2	DC1	DC0
				R	DECSR	Decoding status register	DCRWR RDY	LM RDYD	DFIFO RDY	×	×	"0"	DECS	DECD	DC CNV	RMWE	"0"	EOLE	"0"	DC2	DC1	DC0
0	1	0	0	W	DMACR	DMAA control register	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	DMAA ST
				R	DMASR	DMAA status register	DMAWR RDY	×	×	×	×	×	×	×	×	×	×	×	×	×	×	DMAA ST
0	1	0	1	W	DMBCR	DMAB control register	×	×	×	×	×	×	×	×	×	×	BC1	BC0	MTOM1	MTOM0	MTOME	DMAB ST
				R	DMBSR	DMAB status register	DMBWR RDY	×	×	×	×	×	×	×	×	×	BC1	BC0	MTOM1	MTOM0	MTOME	DMAB ST
0	1	1	0	R	EFIFO	Encode FIFO																
				W	DFIFO	Decode FIFO																
0	1	1	1	R/W	LM	Line memory																
1	0	0	0	R/W	AR	Address register	×	×	×	×	×	×	×	×	×	×	AR5	AR4	AR3	AR2	AR1	AR0
1	0	0	1	R/W	PBR	Parameter buffer register																

Table 2 Parameter Registers

Address (AR)						Operation Mode			Register Name	
AR5	AR4	AR3	AR2	AR1	AR0	Encode	Decode	Transfer	Symbol	Name
0	0	0	0	0	0	○			ERSARH	Encode reference line start address (H)
0	0	0	0	0	1	○			ERSARL	Encode reference line start address (L)
0	0	0	0	1	0	○	○	○	EESARH	Encode code line start address (H)
0	0	0	0	1	1	○	○	○	EESARL	Encode code line start address (L)
0	0	0	1	0	0	○		○	ESBAR	Encode start bit address register
0	0	0	1	0	1	○		○	EPNR	Number of encode bits register
0	0	0	1	1	0	○		○	EHWR	Encode scan-line length register
0	0	0	1	1	1	○		○	ELNR	Number of encode lines register
0	0	1	0	0	0	○			EEOLR	Encode EOL register
0	0	1	0	0	1	○			EMCLR	Minimum number of encode bits register
0	0	1	0	1	0	○			EKPR	Encode K parameter register
0	0	1	0	1	1	○			EKCNTR	Encode K counter register
0	0	1	1	0	0	○			ECSARH	Encode code area start address (H)
0	0	1	1	0	1	○			ECSARL	Encode code area start address (L)
0	0	1	1	1	0	○			ECBLKR	Encode code area size register
0	0	1	1	1	1		○		DRSARH	Decode reference line start address (H)
0	1	0	0	0	0		○		DRSARL	Decode reference line start address (L)
0	1	0	0	0	1		○		DDSARH	Decode code line start address (H)
0	1	0	0	1	0		○		DDSARL	Decode code line start address (L)
0	1	0	0	1	1		○		DSBAR	Decode start bit address register
0	1	0	1	0	0		○		DPNR	Number of decode bits register
0	1	0	1	0	1		○		DHWR	Decode scan-line length register
0	1	0	1	1	0		○		DLNR	Number of decode lines register
0	1	0	1	1	1		○		DRTCR	Decode RTC register
0	1	1	0	0	0		○		DCSARH	Decode code area start address (H)
0	1	1	0	0	1		○		DCSARL	Decode code area start address (L)
0	1	1	0	1	0		○		DCBLKR	Decode code area size register
0	1	1	0	1	1	○	○	○	MBLKR	Image memory block register
0	1	1	1	0	0	(○)	(○)	(○)	DMASAH	DMAA channel start address register (H)
0	1	1	1	0	1	(○)	(○)	(○)	DMASAL	DMAA channel start address register (L)
0	1	1	1	1	0	(○)	(○)	(○)	DMABSR	DMAA channel block size register
0	1	1	1	1	1	(○)	(○)	(○)	DMAHWR	DMAA channel scan-line length register

(to be continued)

(continued)

Address (AR)						Operation Mode			Register Name	
AR5	AR4	AR3	AR2	AR1	AR0	Encode	Decode	Transfer	Symbol	Name
1	0	0	0	0	0	(○)	(○)	(○)	DMALNR	Number of DMAA channel processing lines register
1	0	0	0	0	1	(○)	(○)	(○)	DMBSAH	DMAB channel start address register (H)
1	0	0	0	1	0	(○)	(○)	(○)	DMBSAL	DMAB channel start address register (L)
1	0	0	0	1	1	(○)	(○)	(○)	DMBBSR	DMAB channel block size register
1	0	0	1	0	0	(○)	(○)	(○)	DMBHWR	DMAB channel scan-line length register
1	0	0	1	0	1	(○)	(○)	(○)	DMBLNR	Number of DMAB channel processing lines register

File LSI

HD63265

Floppy Disk Controller (FDC)

HD63265 is a floppy disk controller (FDC) VLSI circuit which is capable of controlling up to 3.5", 5.25", or 8" floppy disk drives receiving commands from a microprocessor in a 68 or 80-series microcomputer system. Since the FDC has 20 types of high-performance function commands, a floppy disk drive can early be integrated into a system by simple software. In addition, by incorporating a high accuracy VFO circuit and a precompensation circuit, it greatly simplify hardware design. Moreover, since it features a CMOS circuit structure with sleep mode and low power dissipation, it can be used in a wide range of systems from laptop computers to larger systems.

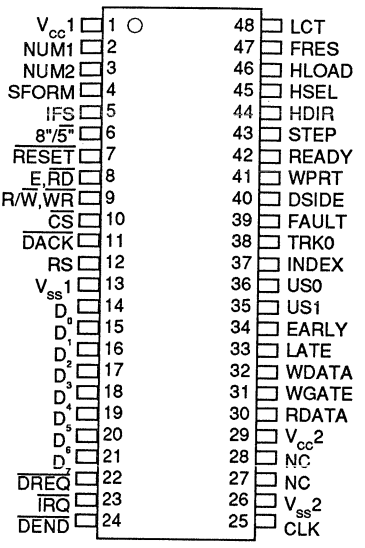
Features

- On-chip high accuracy data separator (adjustment free analog VFO system)
  - No adjustment required
- On-chip write precompensation circuit
  - Delay time programmable in the range from 0 to 750nsec by 62.5nsec increments
  - Delay time independently selectable for inner and outer tracks.
  - Outer to inner switch over programmable in the range of 1 to 255
- Command code compatible with standard FDCs
- Compatible with both 68 and 80-series microprocessors
- Low power dissipation
  - CMOS circuit plus SLEEP command
- Selectable recording
  - FM and MFM
- Serial data transfer rate
  - FM mode : 125, 150, 250 kbps
  - MFM mode : 250, 300, 500 kbps
- Selectable DMA and Non-DMA host data transfers
- Formatting
  - Both IBM and ECMA (ISO) track formats supported
- Error checking
  - 16-bit CRC generator and checker incorporated ($X^{16} + X^{12} + X^5 + 1$)
- Multi-sector and multi-track Read/Write capability
- Data Scan Capability-scans a single sector or an entire cylinder compare byte-for-byte host memory and disk data.
- Multi-drive parallel seek capability
- Stepping rate, head load time, and head unload time programmable
  - Stepping rate programmable by 1 msec increments when using 5" mode
- Drive control range (Max. value)
  - Number of drives : 4
  - Number of heads : 2 heads/drive
  - Number of cylinders : 255 cylinders/drive
  - Number of sectors : 255 sectors/track
- Sector length programmable
  - 128, 256, 512, 1024, 2048, 4096, 8192 bytes/sector

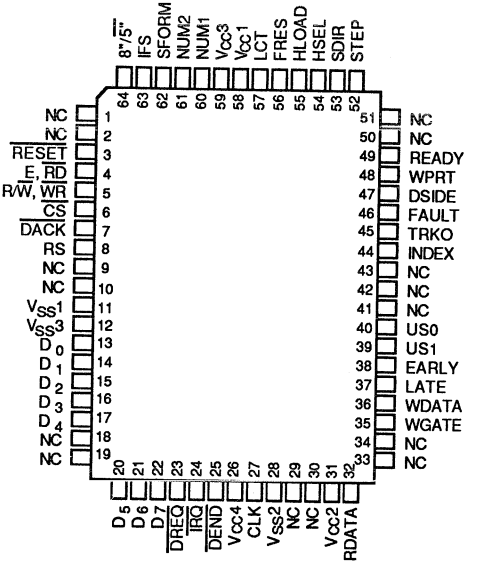
Ordering Information

Type No.	Clock Frequency	Package
HD63265P	16 MHz, 19.2 MHz	48-pin plastic DIP (DP-48)
HD63265FP		64-pin plastic QFP (FP-64)

Pin Arrangement



(DP-48)



(FP-64)

(Top View)

$V_{cc}1$-$V_{cc}4$	+5V
$V_{ss}1$-$V_{ss}3$	Ground
NUM1	Not User Mode 1
NUM2	Not User Mode 2
SFORM	Select Format
IFS	Interface select
8"/5"	8"/5" Mode Select
RESET	Reset
E, RD	Enable, Read
R/W, WR	Read/Write, Write
CS	Chip Select
DACK	DMA Acknowledge
RS	Register Select
D_0	Data Bus 0-7
D_1	
D_2	
D_3	
D_4	
D_5	
D_6	
D_7	
DREQ	DMA Request
IRQ	Interrupt Request
DEND	DMA End

LCT	Low Current
FRES	Fault Reset
HLOAD	Head Load
HSEL	Head Select
HDIR	Head Direction
STEP	Step
READY	Ready
WPRT	Write Protected
DSIDE	Double Sided
FAULT	Fault
TRK0	Track 00
INDEX	Index
US0	Unit Select 0
US1	Unit Select 1
EARLY	Early
LATE	Late
WDATA	Write Data
WGATE	Write Gate
RDATA	Read Data
NC	No Connection
CLK	Clock

Pin Function

Table 1. Pin Functions

Type	Pin No. DP-48	FP-64	Symbol	Pin Name	Input/Output
Power	1	58	$V_{cc}1$	$V_{cc}1$	–
Supply,	13	11	$V_{ss}1$	$V_{ss}1$	–
Clock	29	31	$V_{cc}2$	$V_{cc}2$	–
	26	28	$V_{ss}2$	$V_{ss}2$	–
	25	27	CLK	Clock	Input
		59	$V_{cc}3$	$V_{cc}3$	–
		26	$V_{cc}4$	$V_{cc}4$	–
		12	$V_{ss}3$	$V_{ss}3$	–
MPU	7	3	$\overline{RESET}$	Reset	Input
Interface	8	4	E,$\overline{RD}$	Enable, Read	Input
	9	5	R/$\overline{W}$, $\overline{WR}$	Read/Write, Write	Input
	10	6	$\overline{CS}$	Chip select	Input
	12	8	RS	Register select	Input
	14-21	13-22	D0-D7	Data bus, bits 0-7	Input/Output
	23	24	$\overline{IRQ}$	Interrupt request	Output
DMA	11	7	$\overline{DACK}$	DMA acknowledge	Input
Control	22	23	$\overline{DREQ}$	DMA request	Output
	24	25	$\overline{DEND}$	DMA end	Input
FDD	30	32	RDATA	Read data	Input
Interface	31	35	WGATE	Write gate	Output
	32	36	WDATA	Write data	Output
	33	37	LATE	Late	Output
	34	38	EARLY	Early	Output
	35	39	US1	Unit select 1	Output
	36	40	US0	Unit select 0	Output
	37	44	INDEX	Index	Input
	38	45	TRK0	Track 0	Input
	39	46	FAULT	Fault	Input
	40	47	DSIDE	Double sided	Input
	41	48	WPRT	Write protect	Input
	42	49	READY	Ready	Input
	43	52	STEP	Step	Output
	44	53	HDIR	Head direction	Output
	45	54	HSEL	Head select	Output
	46	55	HLOAD	Head load	Output
	47	56	FRES	Fault reset	Output
	48	57	LCT	Low current	Output

SIGNAL DESCRIPTION

Power Supply, Clock

$V_{cc}1$-$V_{cc}4$, $V_{ss}1$-$V_{ss}3$ (Power Supply): $V_{cc}1$, $V_{cc}3$, $V_{cc}4$, $V_{ss}1$ and $V_{ss}3$ are the power and ground for the logic area (+5 V ±5 %). $V_{ss}1$ and $V_{ss}3$ are connected to ground. $V_{cc}2$ and $V_{ss}2$ are the power and ground for the internal VFO (+5 V ±5 %). $V_{ss}2$ is connected to ground.
CLK (Clock): CLK is the 16 MHz clock input (19.2 MHz for 150 and 300 kbps).

MPU Interface

$\overline{\text{RESET}}$ (Reset): $\overline{\text{RESET}}$ sets the $\overline{\text{DREQ}}$ and $\overline{\text{IRQ}}$ signals high and sets all the other output signals low. It forces D0-D7 into the input state.
E, $\overline{\text{RD}}$ (Enable, Read), R/$\overline{\text{W}}$, $\overline{\text{WR}}$ (Read/Write, Write): The functions of E, $\overline{\text{RD}}$ and R/$\overline{\text{W}}$, $\overline{\text{WR}}$ depend on the IFS input (table 2).

$\overline{\text{CS}}$ (Chip Select): $\overline{\text{CS}}$ selects the chip and enables the read/write of the internal registers.

Table 1. Pin Functions (cont)

Type	Pin No. DP-48	FP-64	Symbol	Pin Name	Input/Output
FDC	4	62	SFORM	Select format	Input
Function	5	63	IFS	Interface select	Input
Switching	6	64	8"/$\overline{5}$"	8"/5" mode select	Input
Others	2	60	NUM1	Not-user mode 1	Input
	3	61	NUM2	Not-user mode 2	Input
	27	1, 2	NC	No Connection	
	28	9, 10			
		18, 19			
		29, 30			
		33, 34			
		41-43			
		50, 51			

Table 2. E, $\overline{\text{RD}}$ and R/$\overline{\text{W}}$, $\overline{\text{WR}}$ Function

Signal	IFS		Function
E, $\overline{\text{RD}}$	0	$\overline{\text{RD}}$	Accepts the 80-series Read signal
	1	E	Accepts the 68-series Enable signal
R/$\overline{\text{W}}$, $\overline{\text{WR}}$	0	$\overline{\text{WR}}$	Accepts the 80-series Write signal
	1	R/$\overline{\text{W}}$	Accepts the 68-series Read/Write signal

RS (Register Select): RS selects the internal register on which an MPU read/write is performed (table 3).

D0-D7 (Data Bus): D0-D7 form the bidirectional 8-bit data bus, enabled by read/write.
$\overline{IRQ}$ (Interrupt Request): $\overline{IRQ}$ requests data transfer with the MPU in Non-DMA mode. It informs the MPU that a READ, WRITE, or SEEK command has been completed. When IFS is high, $\overline{IRQ}$ becomes an open drain output.

DMA Control

$\overline{DACK}$ (DMA Acknowledge): $\overline{DACK}$ receives the DMA acknowledge signal from the DMAC during a DMA transfer.
$\overline{DREQ}$ (DMA Request): $\overline{DREQ}$ requests the DMAC to perform a DMA transfer.
$\overline{DEND}$ (DMA End): $\overline{DEND}$ receives the DMA end signal from the DMAC and terminates the DMA transfer .

FDD Interface

RDATA (Read Data): RDATA inputs the read data signal from the FDD.
WGATE (Write Gate): WGATE outputs the write control signal to the FDD.
WDATA (Write Data): WDATA outputs the write data signal to the FDD.
LATE, EARLY (Late, Early): The LATE and EARLY output the write precompensation control signals used to advance or delay the write data before sending it to the FDD.
US1, US0 (Unit Select 1, 0): The US1 and US0 unit select outputs select the FDD.
A maximum of 4 FDDs can be selected by decoding US1 and US0 (table 4).

Table 3. RS Function

RS	Register Selected	Conditions
0	Status Register	Read
	Abort Register	Write
1	Data Register	Read/Write

Table 4. FDD Selection

US1	US0	FDD
0	0	FDD 0
0	1	FDD 1
1	0	FDD 2
1	1	FDD 3

INDEX (Index): INDEX inputs the index signal from the FDD.
TRK0 (Track 0): TRK0 inputs the track 00 signal from the FDD.
FAULT (Fault): FAULT inputs the fault signal from the FDD.
DSIDE (Double Sides): DSIDE inputs the double sided signal from the FDD.
WPRT (Write Protect): WPRT inputs the write protected signal from the FDD.
READY (Ready): READY inputs the ready signal from the FDD.
STEP (Step): The STEP output moves the FDD head.
HDIR (Head Direction): The HDIR output controls the direction of FDD head movement. HDIR = 0 indicates outward direction (towards track 0), while HDIR = 1 indicates inward direction.
HSEL (Head Select): The HSEL output selects the FDD head.
HSEL = 0 selects head 0, while HSEL = 1 selects head 1.
HLOAD (Head Load): The HLOAD output directs the FDD to load the heads onto the disk.
FRES (Fault Reset): The FRES output resets the FDD fault status FF.
LCT (Low Current): The LCT output reduces the FDD write current for inner tracks. After the SPECIFY 1 command is issued, the most outer position of the low current tracks is specified as track 43. For tracks ≧ this track, LCT = 1. A different most outer track position can be specified by the SPECIFY 2 command.

FDC Function Switching

SFORM (Select Format): The SFORM input selects the track format for formatting.
SFORM high selects IBM format, SFORM low selects ECMA (ISO) format. SFORM is needed for formatting only. The FDC can read or write in either format regardless of the SFORM input level.
IFS (Interface Select): The IFS input specifies the host interface. IFS defines the functions of pins 8 and 9 (E, $\overline{RD}$ and R/$\overline{W}$, $\overline{WR}$) as shown in table 2.
IFS = 0 for 80-series interface. IFS = 1 for 68-series interface.
8"/$\overline{5}$" (8"/5" Mode Select): The 8"/$\overline{5}$" input selects the FDD type. It specifies the drive data rate depending on the modulation method selected (table 5).

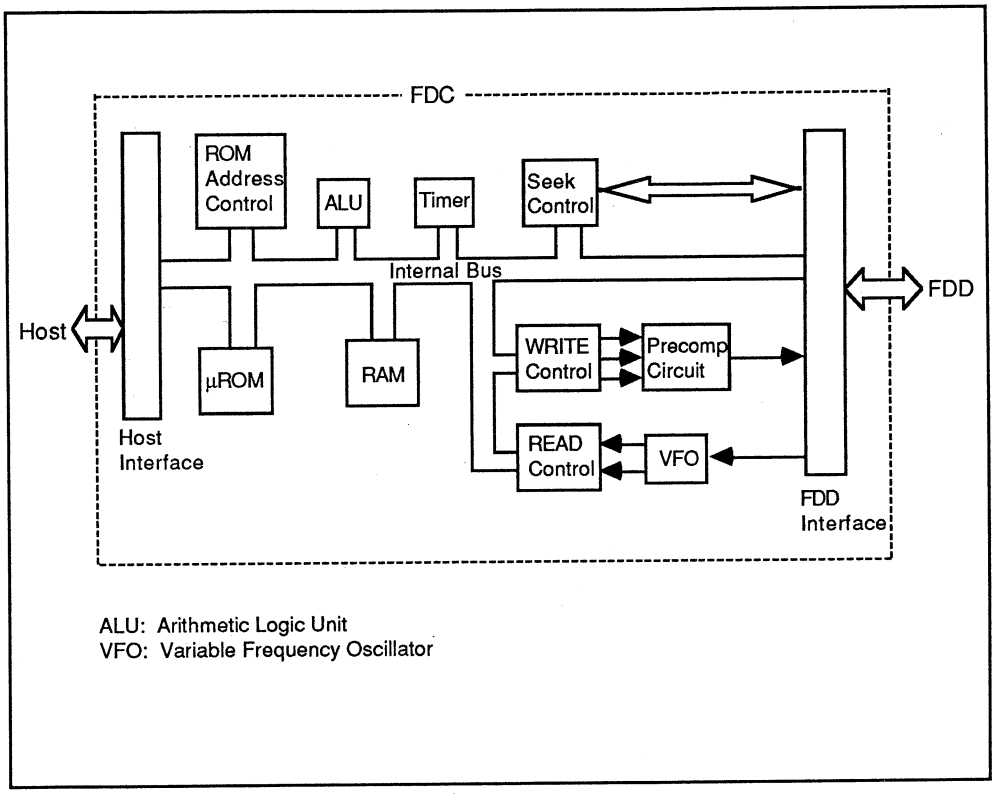
NUM1, NUM2 (Not-User Mode 1, 2): NUM1 and NUM2 are not for user applications. They must be tied to low.
NC (No Connection): NC pins require no connection.

Table 5. Drive Data Rate

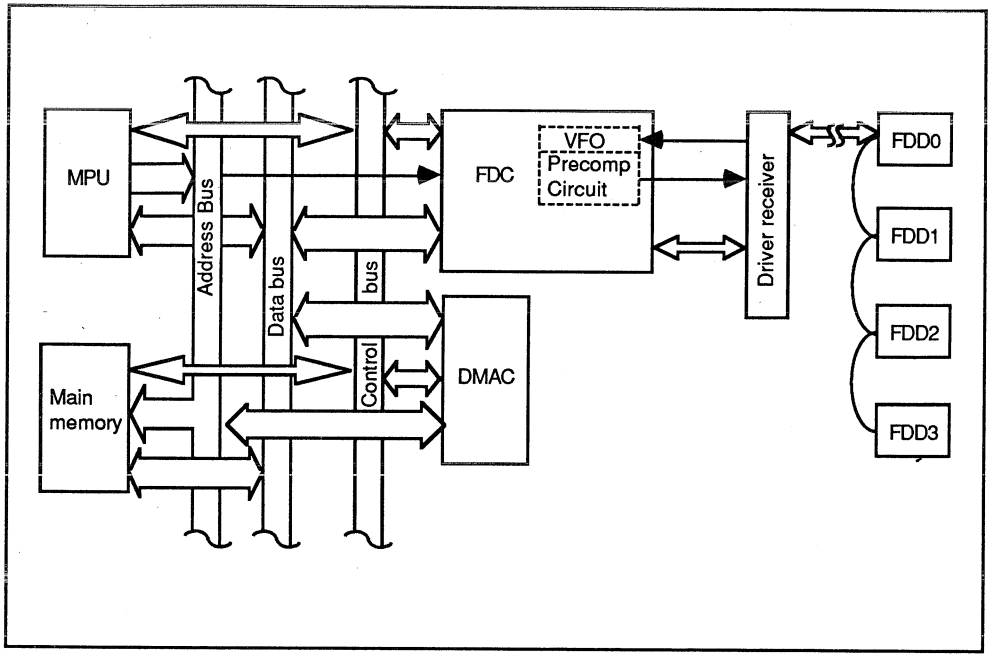
8"/$\overline{5}$"	FM	MFM
0	125 kbits/s	250 kbits/s
	150 kbits/s (Note)	300 kbits/s (Note)
1	250 kbits/s	500 kbits/s

Note: When CLK = 19.2 MHz

FDC Block Diagram



System Block Diagram



Host Interface

This FDC can easily be interfaced to the 68- as well as the 80-series 8-bit devices. IFS (pin 5) is used for selecting between 68- and 80-series interfaces.

68 Series Interface (IFS = 1)

QFP DIP
Pin 4 Pin 8: E
Pin 5 Pin 9: R/$\overline{W}$
Pin 24 Pin 23 ($\overline{IRQ}$): Open-drain output

For the 68-series interface only, the data flow direction controlled by R/$\overline{W}$ input (pin 9) is reversed between DMA and Non-DMA transfers (table 6). Here, DMA FDC access is by $\overline{DACK}$ signal (pin 11), and Non-DMA FDC access is by $\overline{CS}$ signal (pin 10). When the FDC is accessed by the $\overline{DACK}$ signal, the RS signal (pin 12) is ignored, and DTR (data register) is always accessed.

80 Series Interface (IFS = 0)

QFP DIP
Pin 4 Pin 8: $\overline{RD}$
Pin 5 Pin 9: $\overline{WR}$
Pin 24 Pin 23 $\overline{IRQ}$: CMOS output the same as the other output pins

Table 7 shows the data transfer signals.

Table 6. Data Transfer 68-Series

Mode	$\overline{DACK}$	$\overline{CS}$	R/$\overline{W}$	E	Data Transfer Direction
DMA	0	1	0	1	FDC ----------→ Main memory
	0	1	1	1	Main memory ----------→ FDC
Non-	1	0	0	1	Host ----------→ FDC
DMA	1	0	1	1	FDC ----------→ Host

Table 7. Data Transfer 80-Series

Mode	$\overline{DACK}$	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Data Transfer Direction
DMA	0	1	1	0	Main memory ----------→ FDC
	0	1	0	1	FDC ----------→ Main memory
Non-	1	0	1	0	Host ----------→ FDC
DMA	1	0	0	1	FDC ----------→ Host

Internal Registers

The host can access three registers: Data register (DTR), status register (STR), and abort register (ATR). These registers are selected by the RS signal and read/write operations (table 8).

Status Register

The status register (figure 1) is a read-only register which indicates the FDC status and also whether each FDD selected by signals US0 and US1 is currently performing a seek or recalibrate operation.

Bit 7 TXR (Transfer Ready): Bit 7 is set to 1 when DTR is in the read/write enabled state and it is cleared to 0 when data starts to be read or written by the host.

Bit 6 DIR (Data Direction): Bit 6 indicates the data transfer direction between the host and the FDC.

DIR = 0: The host writes data to the FDC.

DIR = 1: The host reads data from the FDC.

Bit 5 NDM (Non-DMA Mode): Bit 5 set to 1 indicates that the FDC transfers data in Non-DMA mode. But even when Non-DMA mode is selected by commands SPECIFY 1 and SPECIFY 2, this bit is cleared to 0, except during the execution of read/write related commands.

Bit 4 BSY (Controller Busy): Bit 4 is set to 1 when the FDC cannot accept the next command because it is decoding or executing a command. A new command, except for the ABORT command, must be issued only when BSY = 0.

Table 8. Register Selection

RS	Read/Write	Selected Register
0	Read	Status Register (STR)
	Write	Abort Register (ATR)
1	Read/Write	Data Register (DTR)

STR

Bit	7	6	5	4	3	2	1	0
Symbols	TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S

Figure 1. Status Register

Bit 0-3 D0S-D3S (Drivers 0-3 Seek): Bits 0-3 are set to 1 when the FDD selected by signals US0 and US1 is executing a SEEK or RECALIBRATE command. Bit 0 corresponds to FDD0 and bit 3 to FDD3. Bits D0S to D3S are 1's when the seek or recalibrate command is issued. Even if all of the step pulses are output, these bits stay as 1's until the SEEK and RECALIBRATE end status information is accepted by the CHECK INTERRUPT STATUS command.

Abort Register

Abort register is a write-only register used exclusively for the ABORT command. ABORT command is issued by writing HEX FF into this register. This command is valid when the $\overline{\text{RESET}}$ signal is inactive regardless of the state of the FDC. Values other than HEX FF written into this register are ignored by the FDC.

Data Register

Data register is a read/write register (actually a stack of registers with only one connected to the data bus at a time) which is used to receive commands and command parameters, transfer data, and read out result parameters.

COMMAND DESCRIPTION

Command Description List

This FDC supports 20 commands listed in Table 9.

READ LONG and WRITE LONG commands become valid only after command SPECIFY 2 has been issued.

Table 9. FDC Commands

Commands	Functions
READ DATA	Reads data from any specified sector (s) except the deleted sector (s)
READ DELETED DATA	Reads data from any specified sector (s) containing a data address mark of F8
READ ERRONEOUS DATA	Reads data from the first sector immediately after the index to the end of track regardless whether there are errors or not
READ ID	Reads the first errorfree ID encountered on a track
WRITE DATA	Writes data to any specified sector (s) using a data address mark of FB
WRITE DELETED DATA	Writes data to any specified sector (s) using a data address mark of F8
WRITE FORMAT	Formats the track where the head is currently positioned
SEEK	Moves the selected FDD's head to a specified track
RECALIBRATE	Moves the selected FDD's head to track 0
COMPARE EQUAL COMPARE LOW OR EQUAL COMPARE HIGH OR EQUAL	Compares the data read from the selected FDD with the data sent from the host according to the chosen command
CHECK DEVICE STATUS	Reads the selected FDD's status
CHECK INTERRUPT STATUS	Reads the interrupt causes
SPECIFY 1 SPECIFY 2*	Specifies the FDC operating mode and sets up the various timers in the FDC
SLEEP *	Sets the FDC to the low power dissipation mode
ABORT *	Software reset command
READ LONG *	Reads the CRC bytes as well as the data from a sector to the host
WRITE LONG*	Writes the CRC bytes as well as the data to a sector from the host

Note: Commands marked with * are newly added commands which are unique to this FDC. Rest of the commands are identical to other standard FDC commands.

Command Code List

Table 10 lists the FDC commands and the corresponding command codes.

Table 10. Command Codes

Commands	Command Codes							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
READ DATA	MT	MM	SD	0	0	1	1	0
READ DELETED DATA	MT	MM	SD	0	1	1	0	0
READ ERRONEOUS DATA	0	MM	0	0	0	0	1	0
READ ID	0	MM	0	0	1	0	1	0
WRITE DATA	MT	MM	0	0	0	1	0	1
WRITE DELETED DATA	MT	MM	0	0	1	0	0	1
WRITE FORMAT	0	MM	0	0	1	1	0	1
SEEK	0	0	0	0	1	1	1	1
RECALIBRATE	0	0	0	0	0	1	1	1
COMPARE EQUAL	MT	MM	SD	1	0	0	0	1
COMPARE LOW OR EQUAL	MT	MM	SD	1	1	0	0	1
COMPARE HIGH OR EQUAL	MT	MM	SD	1	1	1	0	1
CHECK DEVICE STATUS	0	0	0	0	0	1	0	0
CHECK INTERRUPT STATUS	0	0	0	0	1	0	0	0
SPECIFY 1	0	0	0	0	0	0	1	1
SPECIFY 2	0	A	H	0	1	0	1	1
SLEEP	0	0	0	0	1	1	1	0
ABORT	1	1	1	1	1	1	1	1
READ LONG	MT	MM	SD	1	0	0	1	0
WRITE LONG	MT	MM	0	1	0	1	1	0

MT: Multi Track
MT = 1 specifies read/write of multi tracks.

MM: MFM Mode
MM = 0 selects FM mode
MM = 1 selects MFM mode

SD: Skip DDAM
Sector with DDAM (deleted data address mark) is read or skipped depending on whether SD = 0 or 1. When SD = 1, sector with DDAM is skipped.

A: Auto precompensation
When A = 1, auto write precompensation is performed.

H: High speed seek
H = 1 selects high speed seek mode.

Command Functions

READ DATA

The READ DATA command (figure 2) transfers data to the host from the disk. The command parameters specify the location of the data on the disk. Multisector read is automatically performed. Multitrack read can also be performed if specified.

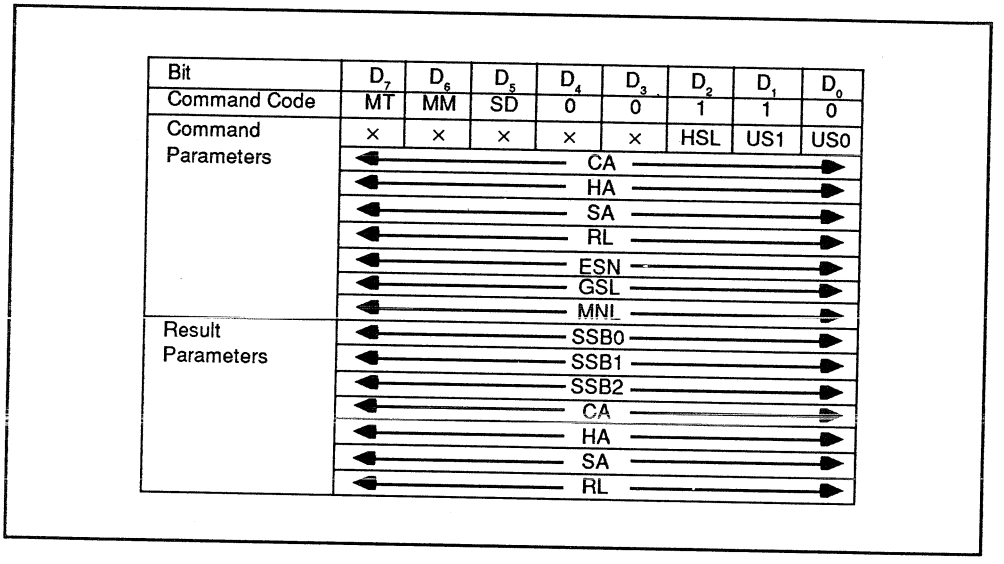


Figure 2. READ DATA Command

READ DELETED DATA

The READ DELETED DATA command (figure 3) is identical to the READ DATA command except that HEX FB and HEX F8 are regarded as the deleted data address mark and the data address mark, respectively.

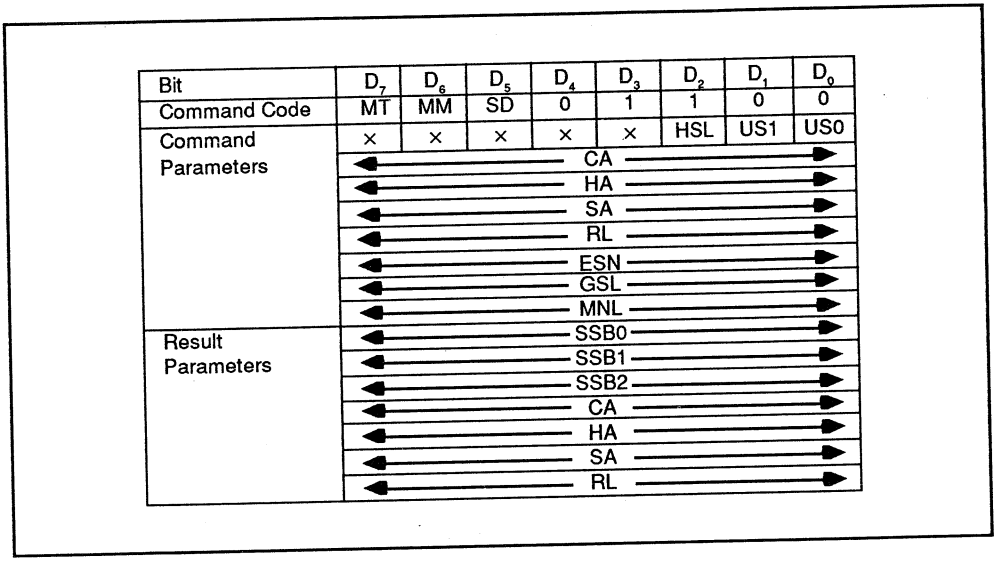


Figure 3. READ DELETED DATA Command

READ ERRONEOUS DATA

The READ ERRONEOUS DATA command (figure 4) reads the data starting from the first sector detected after the index to the end of the track regardless whether there are errors present or not. Sectors are read in the order, they occur after index pulse detection, independent of CA, HA, SA and RL. The SA byte of the command parameters is ignored and HEX 01 is specified in the FDC at the start of the command execution. Multisector read is performed by incrementing SA by 1. Multitrack read cannot be specified.

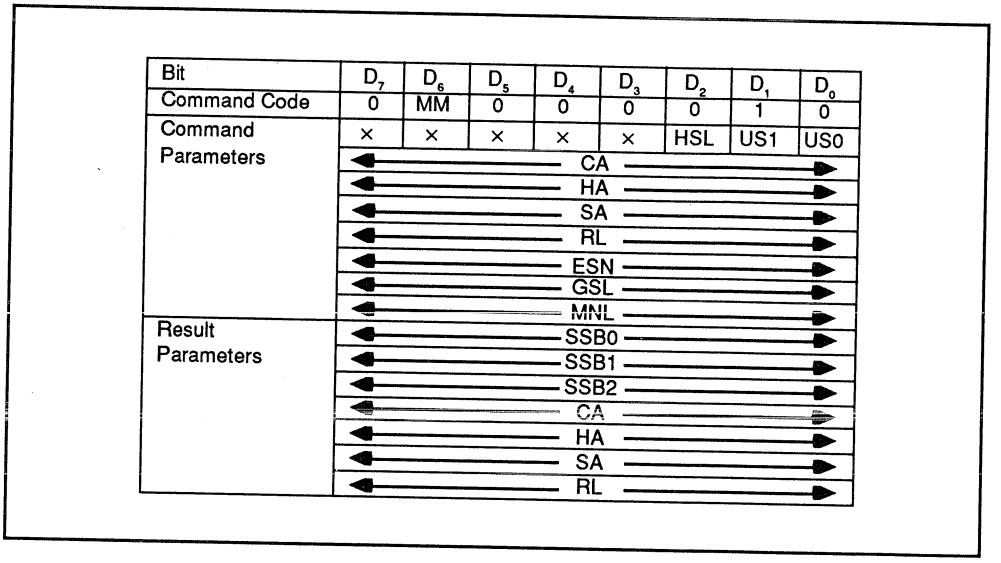


Figure 4. READ ERRONEOUS DATA Command

READ ID

The READ ID command (figure 5) transmits the first error-free ID detected after the command execution has started to the host as result parameters CA, HA, SA, and RL.

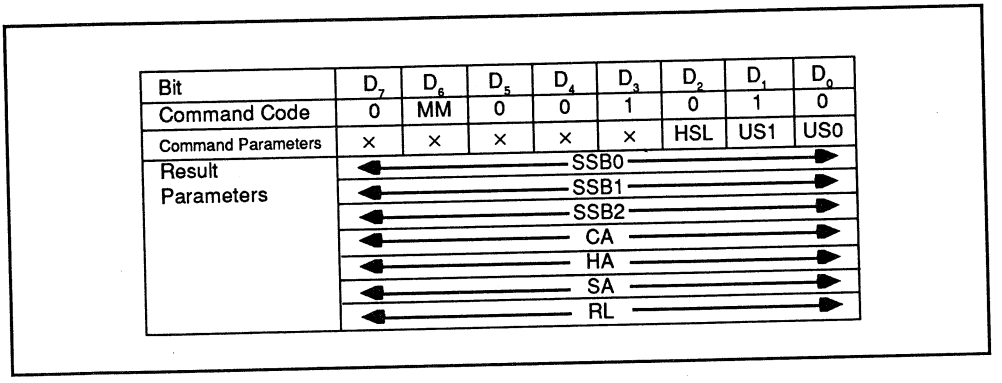


Figure 5. READ ID Command

WRITE DATA

The WRITE DATA command (figure 6) requests the data transfer from the host and writes it to a sector on a track specified by the command parameters at the current head position. Multisector write is automatically performed. Multitrack write can also be performed if specified.

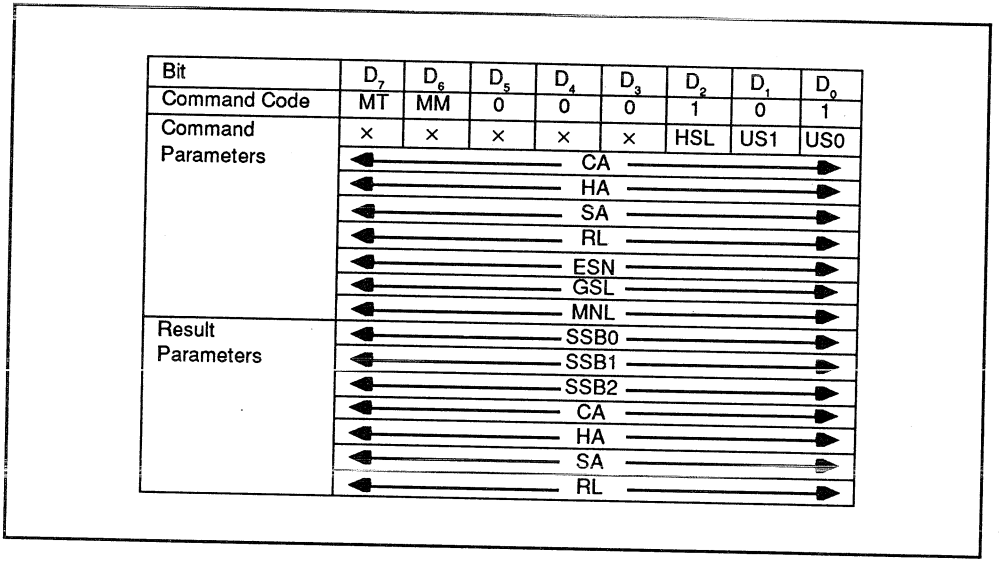


Figure 6. WRITE DATA Command

WRITE DELETED DATA

The WRITE DELETED DATA command (figure 7) is identical to the WRITE DATA command except that the following 1-byte and 4-byte deleted data address marks are written in the FM and MFM mode, respectively.

In FM mode
Data: HEX F8
Clock: HEX C7

In MFM mode
Data: HEX A1, HEX A1, HEX A1, HEX F8
Clock: HEX 0A, HEX 0A, HEX 0A, HEX 03

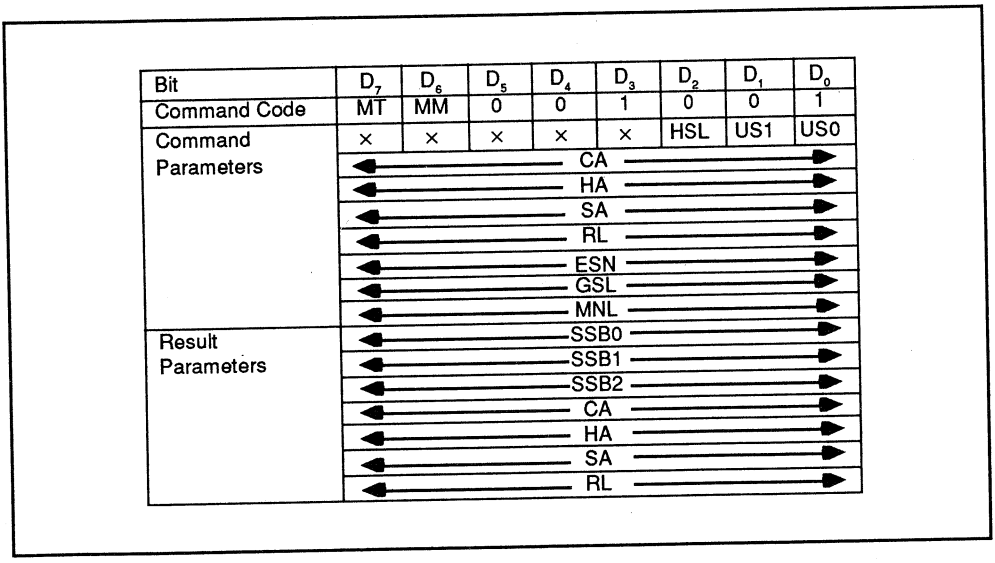


Figure 7. WRITE DELETED DATA Command

WRITE FORMAT

The WRITE FORMAT command (figure 8) formats a single track where the head is currently positioned depending on the SFORM input (pin 4).

SFORM = 1 : IBM format

SFORM = 0 : ECMA (ISO) format

When an index pulse is detected, the write gate signal is activated to begin the formatting operation.

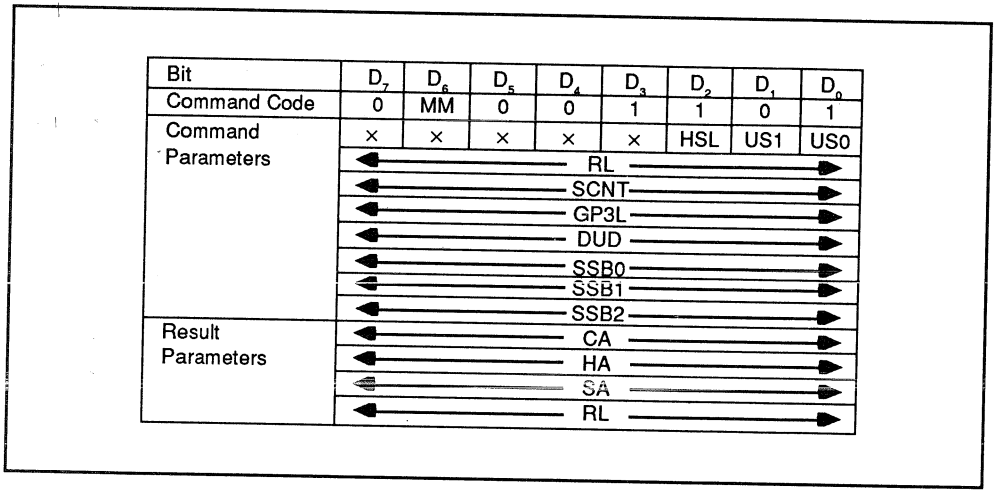


Figure 8. WRITE FORMAT Command

SEEK

In the SEEK operation (figure 9), a drive's head is moved onto the track specified by the command parameter's NCN (New Cylinder Number) byte. The stepping rate (step pulse interval) is specified by the SPECIFY command.

RECALIBRATE

The RECALIBRATE command (figure 10) moves a drive's head to track 0. Head movement speed is the stepping rate (step pulse interval) specified by the SPECIFY command.

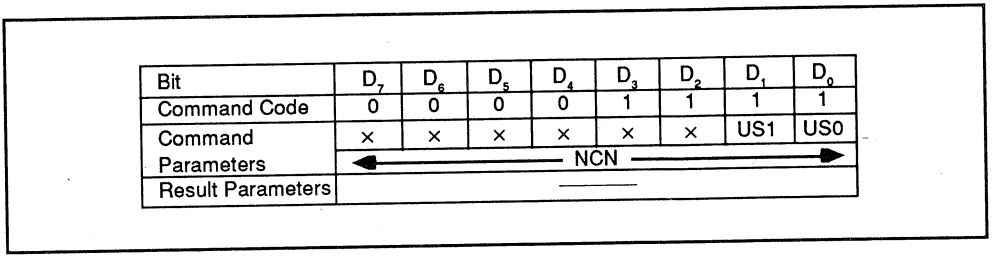


Figure 9. SEEK Command

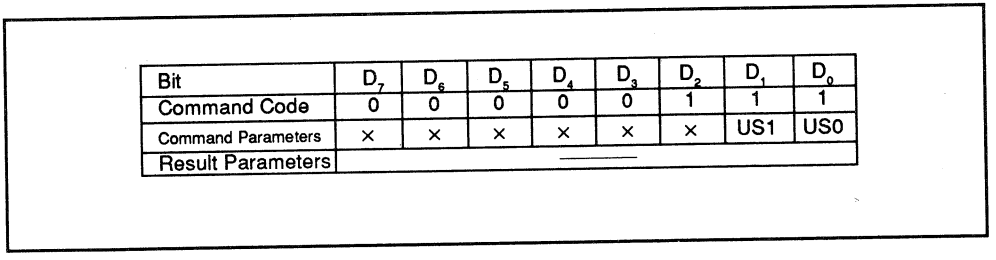


Figure 10. RECALIBRATE Command

COMPARE EQUAL

The COMPARE EQUAL command (figure 11) searches for a sector on disk such that data from the drive is equal to data from the host.

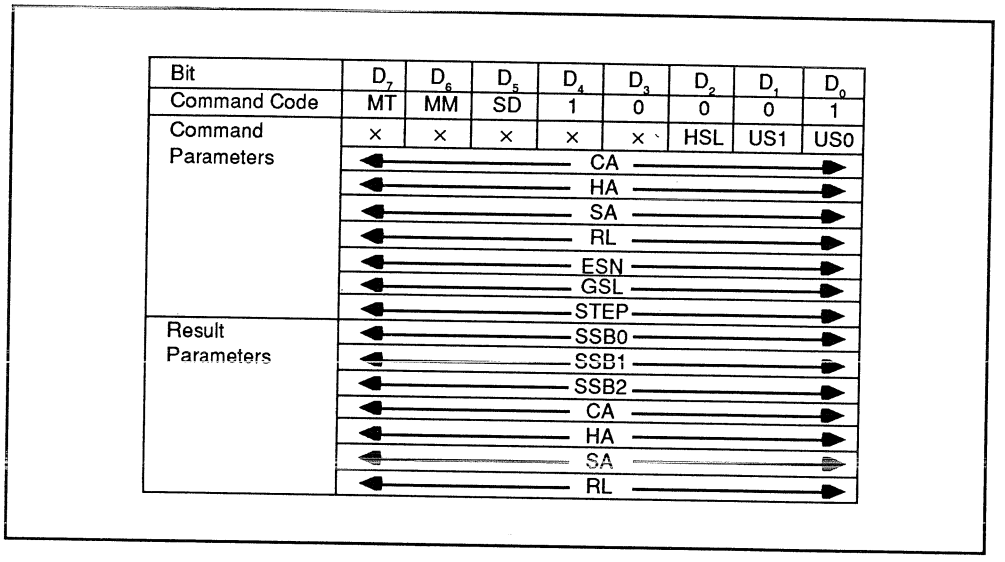


Figure 11. COMPARE EQUAL Command

COMPARE LOW OR EQUAL

The COMPARE LOW OR EQUAL command (figure 12) searches for a sector on disk such that data from the drive is less than or equal to data from the host.

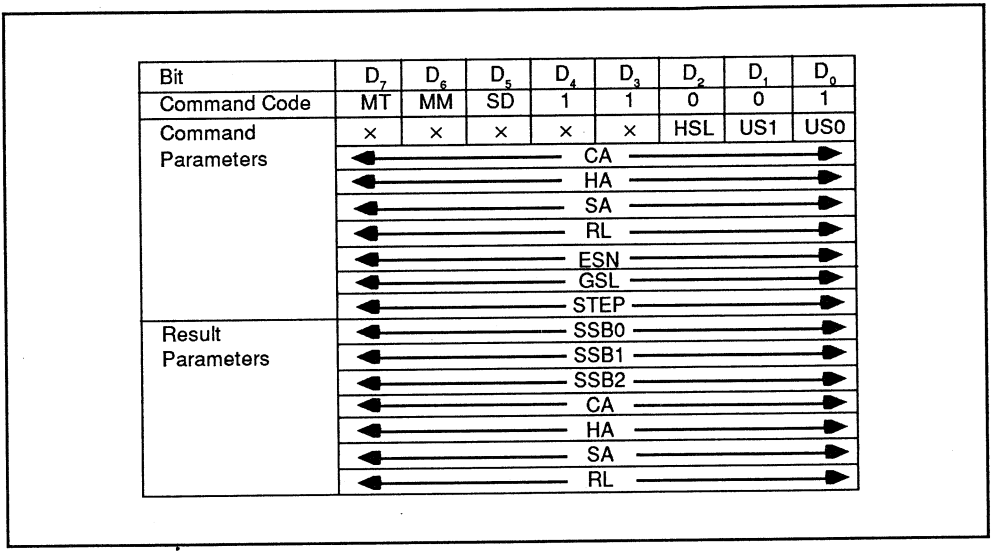


Figure 12. COMPARE LOW OR EQUAL Command

COMPARE HIGH OR EQUAL

The COMPARE HIGH OR EQUAL command (figure 13) searchs for a sector on disk such that data from the drive is greater than or equal to data from the host.

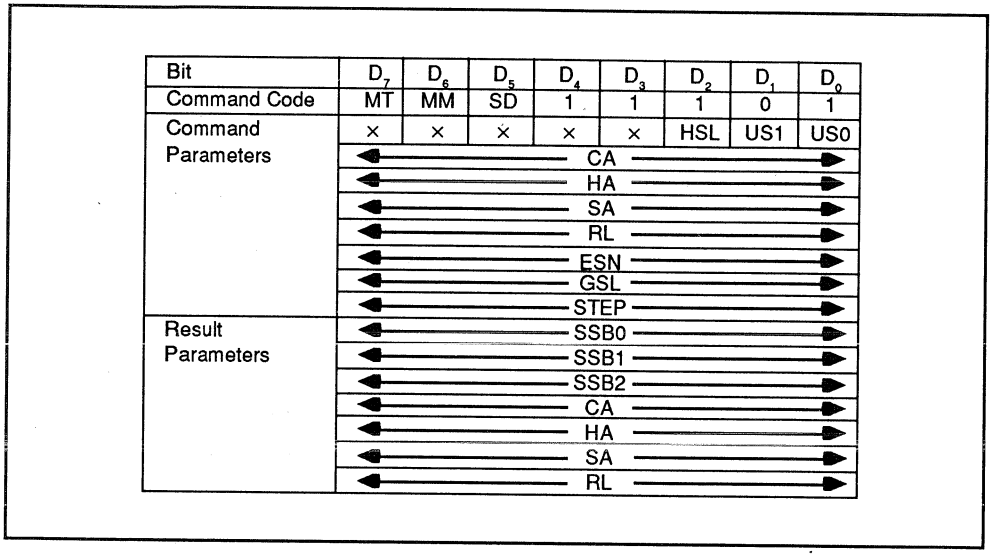


Figure 13. COMPARE HIGH OR EQUAL Command

CHECK DEVICE STATUS

The CHECK DEVICE STATUS command (figure 14) reads the status of a drive and sets it up in SSB3 transfer to the host. HSL, US1 and US0 bits of SSB3 are updated to contain exactly the same values as the respective command parameter values. This command can also be issued for a drive which is performing a seek or recalibrate operation. If the command is issued for a different drive than the one currently selected, then its heads must be immediately unloaded (HLOAD = 0).

CHECK INTERRUPT STATUS

The CHECK INTERRUPT STATUS command (figure 15) transfers to the host the causes of the interrupt request made by the FDC, when the status register value is HEX 8X (command waiting state). There are two types of interrupt causes:

- SEEK or RECALIBRATE command has ended normally or abnormally
- Ready signal has changed state since last polling

When the FDC does not have the Seek End (SED) or Ready Inversion (CDS) status, issuance of the CHECK INTERRUPT STATUS command is treated as an INVALID command.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	0	1	0	0
Command Parameters	×	×	×	×	×	HSL	US1	US0
Result Parameters	← SSB3 →							

Figure 14. CHECK DEVICE STATUS Command

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	1	0	0	0
Command Parameters	—							
Result Parameters	← SSB0 →							
	← PCN →							

Figure 15. CHECK INTERRUPT STATUS Command

SPECIFY 1

The SPECIFY 1 command (figure 16) specifies the stepping rate, head unload time, head load time, and Non-DMA mode (or DMA mode).

If a SPECIFY 1 command is issued after a SPECIFY 2 command, the auto-precompensation and high-speed seek modes specified under SPECIFY 2 command are reset, and the track position activating the LCT signal is specified as track 43.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	0	0	1	1
Command Parameters	STR				HDUT			
	HDLT							NDM
Result Parameters	—							

Figure 16. SPECIFY 1 Command

SPECIFY 2

The SPECIFY 2 command (figure 17) specifies the stepping rate, head unload time, head load time, Non-DMA mode, low write current starting track position, auto-precompensation mode, high-speed seek mode, precompensation delays for auto precompensation, and precompensation delay change track number. Command parameter 1 is required whenever this command is issued. Command parameter 2 is needed only when command code bit A = 1. When A = 0, the FDC cannot accept this parameter.

Auto-Precompensation Mode: When A = 1, the auto-precompensation mode is selected. In this mode, the write data which has been adjusted for the PC1 or PC0 specified precompensation delays is output (only in MFM mode), with the EARLY (pin 34) and LATE (pin 33) outputs fixed at low level. When A = 0, auto-precompensation is not performed, but the EARLY and LATE precompensation control signals are output (only in MFM mode).

High-Speed Seek Mode: When H = 1, the high-speed seek mode is selected. This mode allows the stepping rate to be set to a value ranging from 1 to 16 ms in 1 ms increments in the 5" mode (8"/$\overline{5}$" = low). In the 8" mode (8"/$\overline{5}$" = high), H has no meaning.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	A	H	0	1	0	1	1
Command Parameter 1	STR				HDUT			
	HDLT							NDM
	LCTK							
Command Parameter 2	PC1				PC0			
	PCDCT							
Result Parameter	—							

Figure 17. SPECIFY 2

SLEEP

The SLEEP command (figure 18) allows the FDC to dissipate lower power.
When the FDC receives this command,

1. HLOAD (Head Load) is set low,
2. US0 and US1 are set high,

and the SLEEP mode is entered. In this mode, no drive polling is performed.
In the SLEEP mode, the FDC's status register is set to HEX 80 indicating that the FDC is in the command waiting state. When the FDC receives a command in the SLEEP mode, it automatically releases the SLEEP mode and executes the command.
Power dissipation can be reduced by halting the FDC clock after saving the status conditions gathered immediately before the SLEEP mode is entered.

ABORT

The ABORT command (figure 19) resets the FDC by software.
Note: This command is issued by writing it into the abort register (ATR), and holding RS = 0.
The abort register can be accessed at any time, irrespective of the FDC state, except when the $\overline{\text{RESET}}$ input signal is active.
When the FDC receives the ABORT command:

1. FRES, HLOAD, STEP, EARLY, LATE, WDATA, and WGATE signals are set to low level.
2. $\overline{\text{DREQ}}$ and $\overline{\text{IRQ}}$ signals are set to high level
3. Status register (STR) is set to HEX 80 and the drive polling starts.

This command cannot reset FDC's cylinder numbers or the values specified by the SPECIFY command. However, when the ABORT command is issued during the execution of a SEEK or RECALIBRATE command, the cylinder number is the value set by the SEEK or RECALIBRATE command, although the remaining step pulses are no longer generated. Thus, in such a case, a RECALIBRATE command must be issued before the next command is issued.

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	0	0	0	0	1	1	1	0
Command Parameters				———				
Result Parameters				———				

Figure 18. SLEEP Command

Bit	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command Code	1	1	1	1	1	1	1	1
Command Parameters				———				
Result Parameters				———				

Figure 19. ABORT Command

READ LONG

The READ LONG command (figure 20) transfers the 2-byte CRC information as well as the data read from a sector to the host.

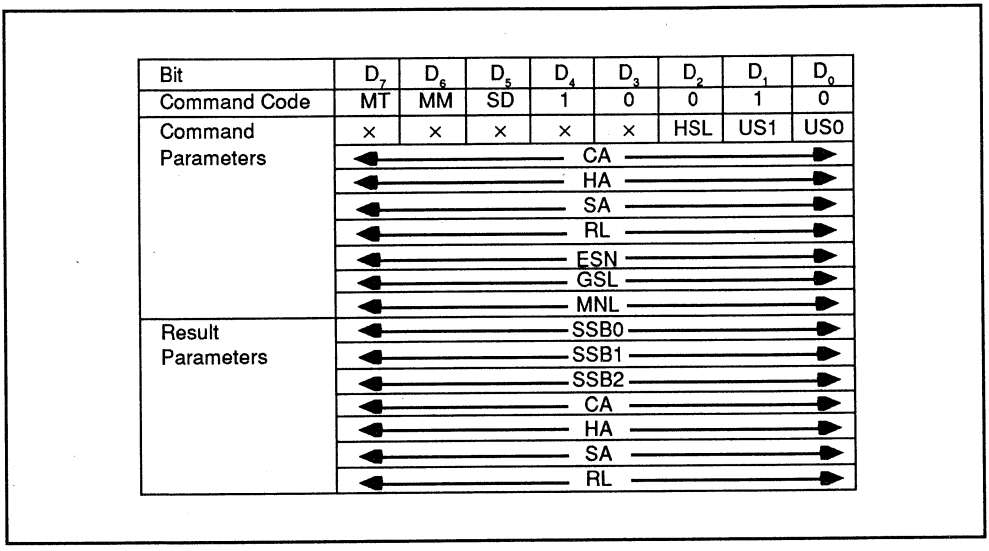


Figure 20. READ LONG Command

WRITE LONG

The WRITE LONG command (figure 21) writes to a disk the 2-byte CRC information as well as the data sent from the host.

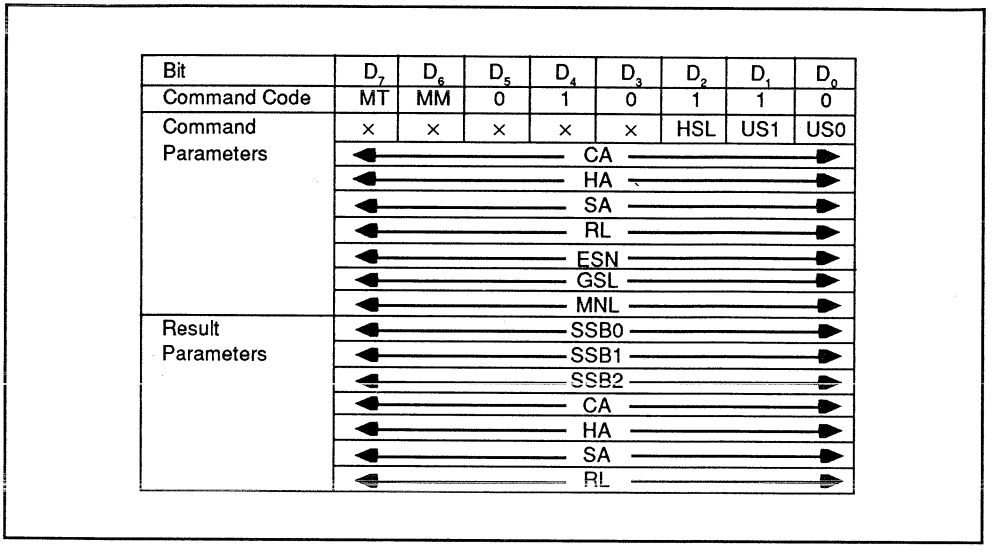


Figure 21. WRITE LONG Command

INVALID

The FDC processes the following cases as an INVALID command (Figure 22):

- Undefined command codes are written into the data register (DTR).
- HEX FF is written into DTR as a command.
- Issuing the CHECK INTERRUPT STATUS command when FDC has no Seek-end or Ready Inversion status informations.

SSB0 of the result parameter is HEX 80.

The following codes are not considered as INVALID commands after the SPECIFY 2 command has been issued:

HEX 10, 13, 14, 15, 17, 18, 1A, 1B, 1C, 1F, 57, 58

Consequently, if any of these codes is written into the FDC as a command, the FDC will malfunction. The ABORT command can be used to bring the FDC to the command waiting state, but the internal RAM contents may be destroyed.

To prevent this a SPECIFFY command followed by the RECALIBRATE command must be issued before any other command is issued. Do not write these codes into FDC as a command at SPECIFY 2 mode.

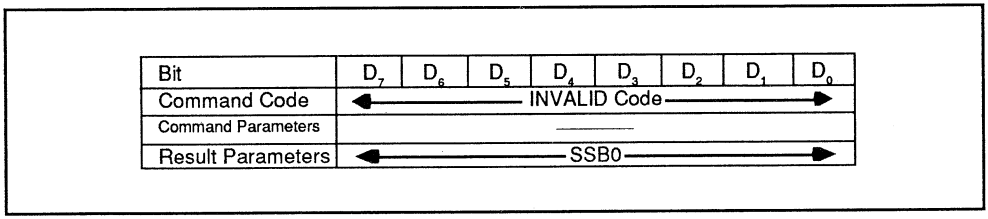


Figure 22. INVALID Command

COMMAND PARAMETERS

HSL-US: Head Select-Unit Select

US0 and US1 bits (figure 23) specify the FDD that performs the command.
HSL specifies the read/write head to be used. When SEEK and RECALIBRATE commands are issued, HSL has no meaning.

CA: Cylinder Address
CA (figure 24) specifies a sector's or track's cylinder address.
CA range: 0 to 255

HA: Head Address

HA (figure 25) specifies a sector's or track's head address as 0 or 1.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
×	×	×	×	×	HSL	US1	US0

×: Don't care
HSL: Head Select
US1: Unit Select 1
US0: Unit Select 0

Figure 23. Head Select-Unit Select

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
← Cylinder Address →							

Figure 24. Cylinder Address

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	HA

Figure 25. Head Address

SA: Sector Address

SA (Figure 26) specifies a sector's address (sector number).
SA range: 1 to 255

RL: Record Length

RL (figure 27) specifies the sector length using a 3-bit binary code.
Using values 0 to 6, different sector lengths are specified as in table 11.

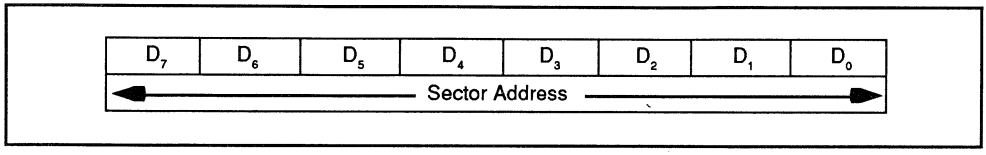


Figure 26. Sector Address

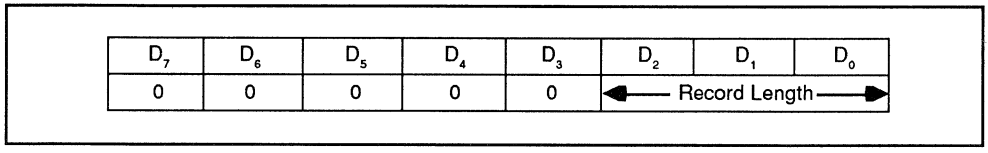


Figure 27. Record Length

Table 11. Record Length

RL	Sector Length
0	128 Bytes/sector
1	256 Bytes/sector
2	512 Bytes/sector
3	1024 Bytes/sector
4	2048 Bytes/sector
5	4096 Bytes/sector
6	8192 Bytes/sector

ESN: End Sector Number

ESN (figure 28) specifies the sector number of the last sector on the track.
This number need not be the same as the actual (physical) last sector number.
Read/Write access starts from the sector specified by SA, continues to and ends with the sector specified by ESN on the same track. However, if DEND signal is received during this time, the access terminates immediately.
ESN range: 1 to 255. However, for COMPARE commands, the range is 1 to 253.

GSL: Gap Skip Length

GSL (figure 29) specifies the number of bytes skipped in between sectors as GAP3.

MNL: Meaning Length

To access part of a sector, MNL (figure 30) specifies the byte count of data to be accessed. This function is valid only for sectors with RL = 0 (128 bytes/sector).
Values from 0 to 255 can be set for MNL. If a value exceeding 128 (HEX 80) is specified, it is treated as 128, and the entire sector is accessed. When sectors with RL ≠ 0 are accessed, MNL has no effect.

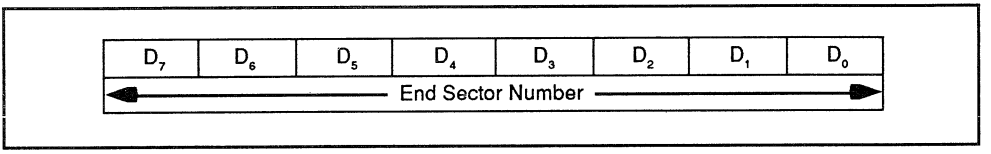


Figure 28. End Sector Number

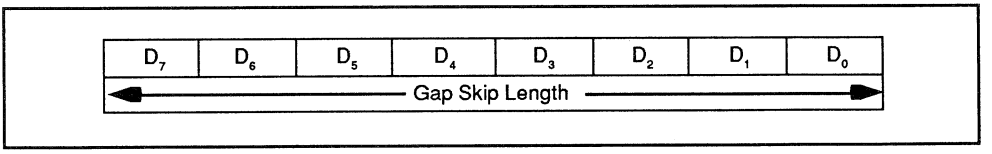


Figure 29. Gap Skip Length

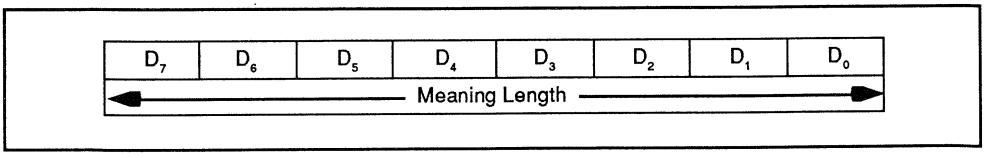


Figure 30. Meaning Length

SCNT: Sector Count

SCNT (figure 31) specifies the sector count for formatting a track.
SCNT range: 1 to 255

GP3L: Gap 3 Length

GP3L (figure 32) specifies in bytes the GAP3 length used in formatting a track.
GP3L range: 1 to 255

DUD: Dummy Data

DUD (figure 33) specifies the dummy data pattern to be written into a sector's data area when formatting.
DUD range: 0 to 255

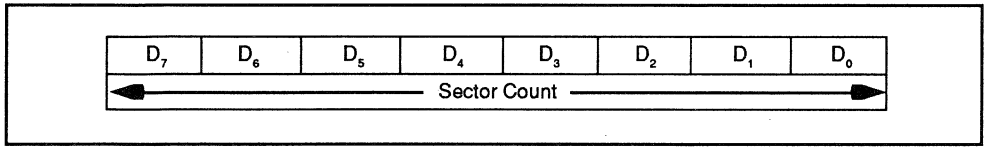


Figure 31. Sector Count

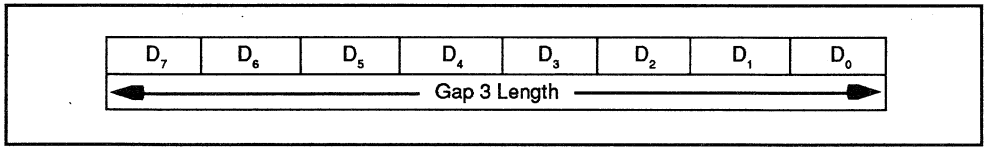


Figure 32. Gap 3 Length

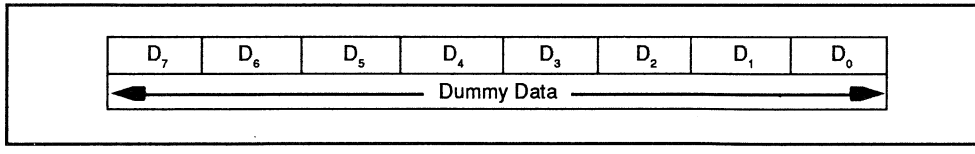


Figure 33. Dummy Data

STEP: Step

STEP (figure 34) specifies the sector increment for incrementing the sectors whose data is to be compared byte-by-byte with the data sent from the host using a COMPARE command.

STEP = 1: Data from contiguous sectors is used for comparison.

STEP = 2: Data from alternate sectors is used for comparison.

NCN: New Cylinder Number

NCN (figure 35) specifies the cylinder number to which the head is to be moved.
NCN range: 0 to 255.

STR-HDUT: Stepping Rate-Head Unload Time

STR-HDUT (figure 36) is a one-byte code in which the upper 4 bits represent STR (stepping rate) and the lower 4 bits represent HDUT (head unload time).

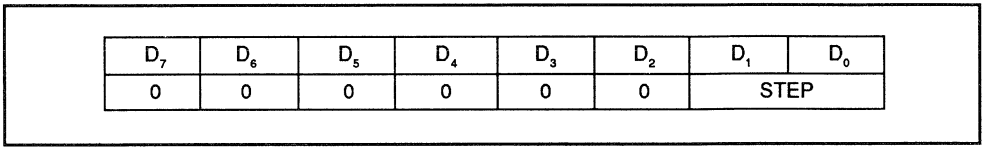


Figure 34. Step

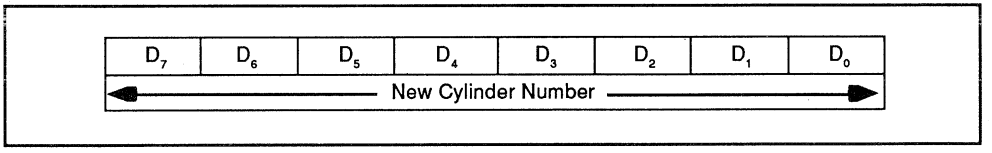


Figure 35. New Cylinder Number

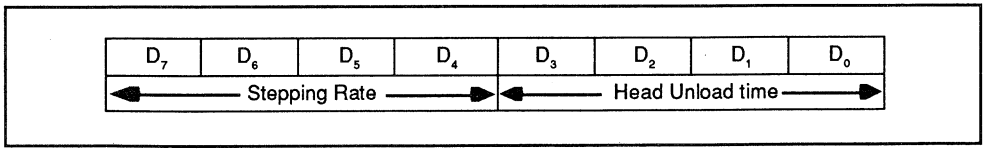


Figure 36. Stepping Rate-Head Unload Time

STR: STR specifies the step pulse interval (stepping rate) for the seek and recalibrate operations. Using values 1 to 15, different stepping rates are specified as in table 12.

Table 12. Stepping Rates

Values (Decimal)	Stepping Rate (ms)	
	8"/$\overline{5"}$ = 1 or high-speed seek mode is selected	8"/$\overline{5"}$ = 0 and high-speed seek mode is not selected
0	16	32
1	15	30
2	14	28
3	13	26
4	12	24
5	11	22
6	10	20
7	9	18
8	8	16
9	7	14
10	6	12
11	5	10
12	4	8
13	3	6
14	2	4
15	1	2

CLK = 16 MHz

HDUT: HDUT specifies the time to wait from the completion of the head-load associated command execution before deactivating the head load signal. Using values 0 to 15, different head unload times are specified as in table 13.

HDLT-NDM: Head Load Time-Non-DMA Mode

The upper 7 bits of HDLT-NDM (figure 37) denote HDLT (head load time) while the lowest bit denotes NDM (Non-DMA mode).

Table 13. Head Unload Times

Set Values (Decimal)	Head Unload Time (ms) 8"/5" = 1	8"/5" = 0
0	0	0
1	16	32
2	32	64
3	48	96
4	64	128
5	80	160
6	96	192
7	112	224
8	128	256
9	144	288
10	160	320
11	176	352
12	192	384
13	208	416
14	224	448
15	240	480

CLK = 16 MHz

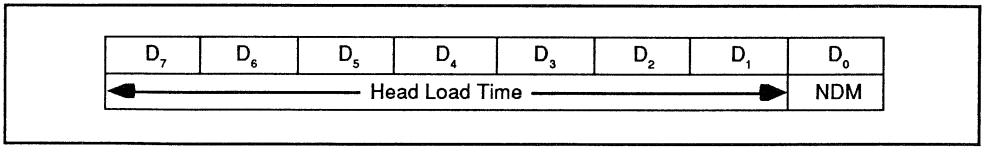


Figure 37. Head Load Time-Non-DMA Mode

HDLT: HDLT specifies the time to wait from setting the head load signal active to start the command execution. When specifying HDLT, an allowance for head settle waiting time should be made also. Using values 0 to 127, different head load times are specified as in table 18.

NDM: NDM specifies if DMA or Non-DMA mode is used for transferring data between the FDC and the host.

NDM = 0: DMA mode
NDM = 1: Non-DMA mode

LCTK: Low Current Track

LCTK (figure 38) specifies the cross-over track number beyond which the LCT signal (pin 48) becomes active in SPECIFY2 mode. With LCTK set to a value ranging from 1 to 255, the LCT signal becomes active for tracks exceeding the LCTK value. With LCTK set to 0, the LCT signal is inactive at every track.

Table 14. Head Load Times

Set Values (Decimal)	Head Load Time (ms) 8"/$\overline{5"}$ = 1	8"/$\overline{5"}$ = 0
0	0	0
1	2	4
2	4	8
3	6	12
4	8	16
5	10	20
6	12	24
7	14	28
8	16	32
|	|	|
|	|	|
↓	↓	↓
124	248	496
125	250	500
126	252	504
127	254	508

CLK = 16 MHz

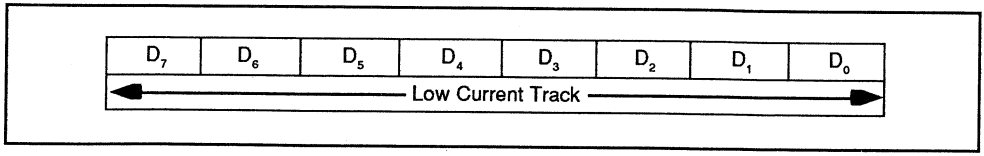


Figure 38. Low Current Track

PC1, PC0: Precompensation Delay 1, 0

PC1 and PC0 (figure 39) specify the amount of precompensation delays for the auto precompensation mode (table 15). PC0 specifies the delay for the outer tracks (smaller track numbers) and PC1 specifies the delay for the inner tracks (larger track numbers). The FDC switches between PC0 and PC1 automatically depending on the head position. The switch-over track position is specified by PCDCT. Maximum programmable values for PC1 and PC 0 are

- HEX C in 5" mode
- HEX 6 in 8" mode

Values exceeding the above limits may cause malfunction.

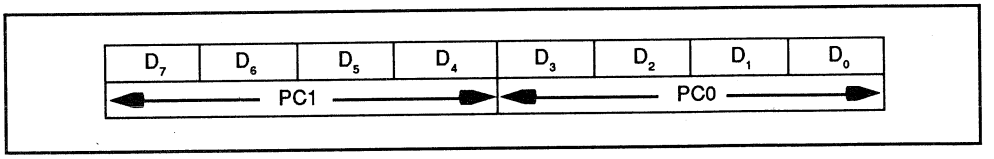


Figure 39. Precompensation Delay 1, 0

Table 15. Precompensation Delay

PC1, PC0	Delay (ns) CLK=16 MHz	CLK=19.2 MHz
HEX 0	0	0
HEX 1	62.5	52.1
HEX 2	125	104.2
HEX 6	375	312.5
HEX B	687.5	572.9
HEX C	750	625

PCDCT: Precompensation Delay Change Track

PCDCT (figure 40) specifies the track where the precompensation delay amount is changed in the auto precompensation mode. For tracks with a number equal to or larger than PCDCT, the delay amount is specified by PC1, and for tracks with a smaller number, the delay is specified by PC0.
PCDCT range: 1 to 255

RESULT PARAMETERS

CA, HA, SA, and RL: Cylinder Address, Head Address, Sector Address, Record Length

CA, HA, SA, and RL are provided as command execution results and their values depend on the command type and how the command execution ended, with or without errors.

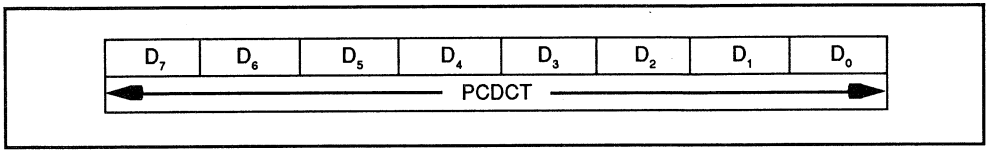


Figure 40. Precompensation Delay Change Track

SSB0: Sense Status Byte 0

INC (Interrupt Code) : INC (figure 41) indicates the cause of an interrupt request (table 16).
SED (Seek End): SED is set to 1 at the completion of SEEK and RECALIBRATE commands.
DER (Drive Error): DER is set to 1 when the fault signal is active during or at the completion of write related command execution, and when the track 0 signal cannot be detected from a drive to which 255 step pulses were applied during a RECALIBRATE command execution.
DNR (Drive Not Ready): DNR is set to 1 when a low level ready signal is detected from a drive at the start of or during the execution of drive access commands other than the CHECK DEVICE STATUS command.
HSL (Head Select): HSL indicates the head selected at the completion of command execution. In response to the CHECK INTERRUPT STATUS command, a zero is returned.
US1, US0 (Unit Select 1, 0): US1 and US0 indicate the drive number selected at the completion of a command execution or the one that caused an interrupt request.

SSB1: Sense Status Byte 1

NDE (No DMA End): NDE (figure 42) is set to 1 if the DEND signal is not received active even after the last sector data has been transferred with a read/write related command. The last sector is determined depending on the MT (multi track) bit value as follows:

Table 16. Interrupt Code

D7	D6	Code Symbol	Code Name	Meaning
0	0	NOR	Normal End	Command normally ended
0	1	ABE	Abnormal End	Command abnormally ended
1	0	IVC	Invalid Command	Issued command is invalid
1	1	CDS	Change in Drive Status	Ready signal level from a drive is inverted compared to the last time it was polled

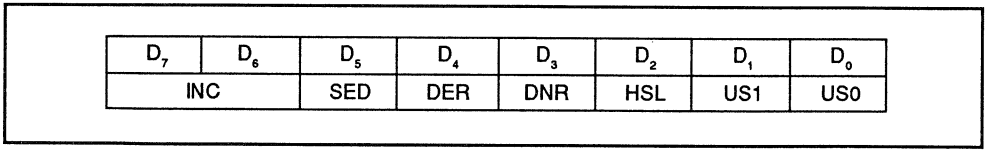


Figure 41. Sense Status Byte 0

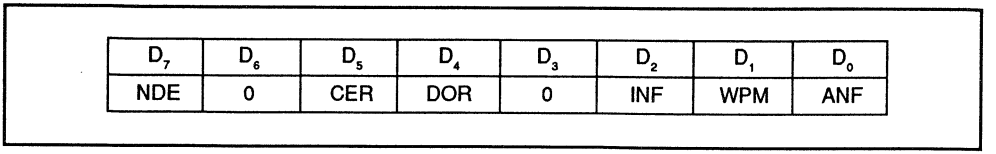


Figure 42. Sense Status Byte 1

- MT = 0: The last sector is specified by the ESN (end sector number) byte on the track of the side specified as part of the command parameters.
- MT = 1: The last sector is specified by the ESN byte but always corresponds to the track on side 1.

CER (CRC Error): CER is set to 1 when a CRC error is detected in the ID or data field. READ ID command does not have any effect on this bit. For CRC errors in the ID field, only the CER bit is set to 1. For CRC errors in the data field, the CDF bit of SSB2 as well as the CER bit are set to 1.

DOR (Data Overrun): DOR is set to 1 if the host cannot complete data transfer requested by the FDC within a specified time to satisfy the FDC data throughput requirements. For details, see section 6.5, "Command Functions".

INF (ID Not Found): The meaning of INF depends on its context.

1. In READ DATA, READ DELETED DATA, READ LONG, WRITE DATA, WRITE DELETED DATA, WRITE LONG, and COMPARE commands: INF is set to 1 if the sector number (CA, HA, SA, RL) specified by a command parameter or updated during a multisector read/write operation cannot be found by the time three index pulses are detected.
2. In READ ID command: INF is set to 1 when an address mark in the ID field was detected but a CRC error-free ID was not found by the time three index pulses were detected.
3. In READ ERRONEOUS DATA command: INF is set to 1 if ID data in the FDC does not match the ID found.

WPM (Write Protected Medium): WPM is set to 1 when an active write protected signal is detected at the start of write related command execution.

ANF (AM not Found): ANF is set to 1 if no ID address mark is detected by the time three index pulses are detected. ANF as well as the NAM bit of SSB2 are set to 1 when no address mark (data address mark or deleted data address mark) is detected in the data field within 1 ms after the desired ID was found, or when the first data other than HEX 00 found after the desired ID and at least 4 bytes (FM mode) or 5 bytes (MFM mode) of HEX 00 were detected is not AM.

SSB2: Sense Status Byte 2

DDA (Deleted Data Address Mark): DDA (figure 43) is set to 1 when a deleted data address mark is detected. In executing the READ DELETED DATA command, however, it is set to 1 when a normal data address mark is detected.
CDF (CRC Error in Data Field): CDF is set to 1 if a CRC error is detected in the data field.
CAU (Cylinder Address Unmatch): CAU is set to 1 when the disk ID's CA byte does not match the command parameter's CA byte, except when the disk ID's CA byte is HEX FF. However, CAU is not set by the READ ERRONEOUS DATA command.
CCS (Compare Condition Satisfied): CCS is set to 1 when the equal condition is satisfied while executing a COMPARE command.
CNS (Compare Condition Not Satisfied): CNS is set to 1 when the specified compare condition is not satisfied while executing a COMPARE command.
BDC (Bad Cylinder): BDC is set to 1 when the CA byte read from the disk does not match the command parameter's CA byte and also when the read CA byte is HEX FF. However, BDC is not set by the READ ERRONEOUS DATA command.
NAM (No Data Address Mark): NAM is set to 1 if no address mark (data address mark or deleted data address mark) is detected in the data field within 1 ms after the desired ID was found, or when the first data other than HEX 00 found after the desired ID and at least 4 bytes (FM mode) or 5 bytes (MFM mode) of HEX 00 were detected is not AM.

SSB3: Sense Status Byte 3

1) FLT,WPT, RDY, TRZ, and DSD: Sense bits FLT, WPT, RDY, TRZ, and DSD indicate the status of the drive specified in the CHECK DEVICE STATUS command.
2) HSL, US1, and US0: Sense bits HSL, US1, and US0 have the same values as HSL, US1, and US0 of the command parameters.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	DDA	CDF	CAU	CCS	CNS	BDC	NAM

Figure 43. Sense Status Byte 2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
FLT	WPT	RDY	TRZ	DSD	HSL	US1	US0

FLT: Fault
WPT: Write Protected
RDY: Ready
TRZ: Track 0
DSD: Double Sided
HSL: Head Select
US1: Unit Select 1
US0: Unit Select 0

Figure 44. Sense Status Byte 3

PCN: Physical Cylinder Number

PCN (figure 45) represents the physical address of the drive head position stored in the FDC (physical number of the track where a head is currently placed). If a SEEK or RECALIBRATE command ends abnormally, the PCN value may not match the head's current physical address. When the FDC is reset, the PCN values for all four drives are set to HEX 00. Accordingly, drives with an auto-recalibrate function (a function which automatically moves the heads onto track 0 at power on) do not require the RECALIBRATE command to be issued after the power on reset. The lower two bits of SSB0 read last indicate which drive the PCN value belongs to.

ISSUING COMMANDS

Writing Command Codes

Command can be issued by writing the desired command codes into the FDC. The status register must be read before issuing a command.

The FDC is ready to accept commands when the status register bits are as shown in figure 46.

When any of the D0S to D3S bits are set to 1:

1. CHECK DEVICE STATUS command and CHECK INTERRUPT STATUS command can be issued for all four drives. However, CHECK INTERRUPT STATUS command is treated as an invalid command when the FDC has no SEEK end and no READY inversion status.
2. SEEK and RECALIBRATE commands can be issued only for drives whose corresponding D0S to D3S bits are zeros.

Commands other than CHECK related and SEEK related commands can be issued when the status register value equals HEX 80.

An ABORT command can be issued independent of the status register value.

When a command code is written, the status register is set as shown in figure 47 and the FDC begins to decode the command.

If the Data Register is read in the command waiting state, the FDC will malfunction since the FDC considers it as a command issue. So, during command waiting state, do not attempt to read the Data Register.

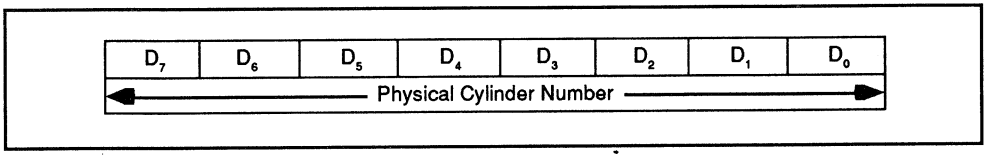


Figure 45. Physical Cylinder Number

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	0	0	0	×	×	×	×

Figure 46. Status Register Before Issuing a Command

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
0	0	0	1	×	×	×	×

Figure 47. Status Register After Issuring a Command

Writing Command Parameters

At the completion of command code decoding, for commands requiring command parameters, the FDC sets the status register as shown in figure 48 and wait for command parameters.

TXR bit is cleared to zero every time a command parameter byte is received.
When the FDC is ready to receive the next command parameter byte the TXR bit is again set to one and the next byte is transferred. After all the command parameter bytes have been received, no more transfer requests are made.

Transferring Data

Data transfer is performed during command execution in response to an FDC request. Data transfer requests are made by setting the $\overline{IRQ}$ signal active in Non-DMA mode or the $\overline{DREQ}$ signal active in DMA mode. Status register contents for both types of data transfer requests are shown in figure 49. Once data transfer begins, the $\overline{IRQ}$ and $\overline{DREQ}$ signals are made inactive and the TXR bit is cleared to zero.

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	0	0	1	×	×	×	×

Figure 48. Status Register Waiting for Command Parameters

Read request in Non-DMA mode

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	1	1	1	0	0	0	0

Write request in Non-DMA mode

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	0	1	1	0	0	0	0

Read request in DMA mode

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	1	0	1	0	0	0	0

Write request in DMA mode

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	0	0	1	0	0	0	0

Figure 49. Status Register Contents for Various Data Transfer Requests

Transferring Result Status

For commands having a result status, the FDC requests the host to accept the result parameter bytes at the completion of the command execution. Commands which have no result status are SEEK, RECALIBRATE, SPECIFY1, SPECIFY2, SLEEP, and ABORT. Commands which cause the status register to be set up as shown in figure 50 and request the host to accept the result parameters are: CHECK DEVICE STATUS, CHECK INTERRUPT STATUS, and INVALID.

The above commands do not activate the $\overline{IRQ}$ signal in order to transfer the result parameters.
After one byte of the result parameters has been transferred, TXR and DIR are cleared to zero. When the next byte of the result parameters is ready to be transferred, it is loaded into the data register. Then both the DIR and TXR bits of the status register are set to 1 requesting the host to accept the new parameter byte. After the last byte of the result parameters has been transferred, some dummy data is loaded into the data register, TXR is set to 1 and BSY is cleared to 0 to enter the command waiting state (DIR remains zero).
For all the other commands, the result status transfer is performed by setting the $\overline{IRQ}$ signal active and the status register as shown in figure 51. The $\overline{IRQ}$ signal is active only when the first byte of the result parameters is transferred, and becomes inactive after that.

The first byte of the result parameters is transferred according to the following sequence of operations.
- $\overline{IRQ}$ signal is set active
- DIR bit is set to 1
- Result parameter byte is loaded into the data register
- TXR bit is set to 1
- FDC waits for the result parameter byte to be transferred
- Host reads the result parameter byte and TXR bit is reset to 0.
- DIR bit is reset to 0.
- $\overline{IRQ}$ signal is set inactive.

The remaining bytes are transferred in the same way except that the $\overline{IRQ}$ signal is not activated again. After the last byte of the result parameters is transferred, some dummy data is loaded into the data register, TXR is set to 1 and BSY is cleared to 0 to enter the command waiting state (DIR remains zero).

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	1	0	1	×	×	×	×

Figure 50. Status Register Requesting Result Parameter Transfer (No $\overline{IRQ}$)

TXR	DIR	NDM	BSY	D3S	D2S	D1S	D0S
1	1	0	1	0	0	0	0

Figure 51. Status Register Requesting Result Parameter Transfer (with $\overline{IRQ}$)

DRIVE POLLING

This FDC performs drive polling every 1 ms (actually 1.024 ms) in 8" mode and every 2 ms (2.048 ms) in 5" mode during command waiting. During sleep and head loading, no polling is performed. Polling and seek operation (step pulse output) are performed concurrently.

US0 and US1 signals are changed (figure 52) and the Ready signals of all four drives are polled (figure 53). During this time, a step pulse is issued to the drive requiring it (figure 53). When high speed seek mode is specified using SPECIFY 2 command, 1 ms polling is performed even in 5" mode.

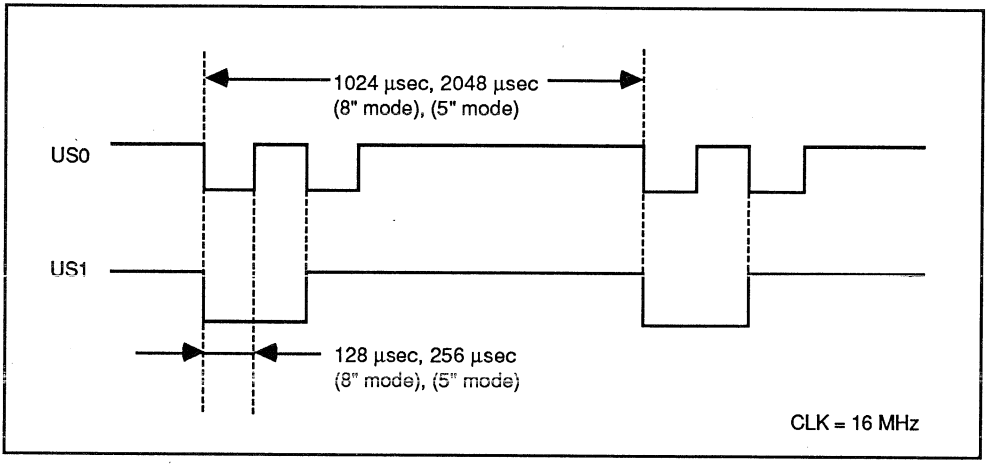


Figure 52. Drive Selection Timing during Polling

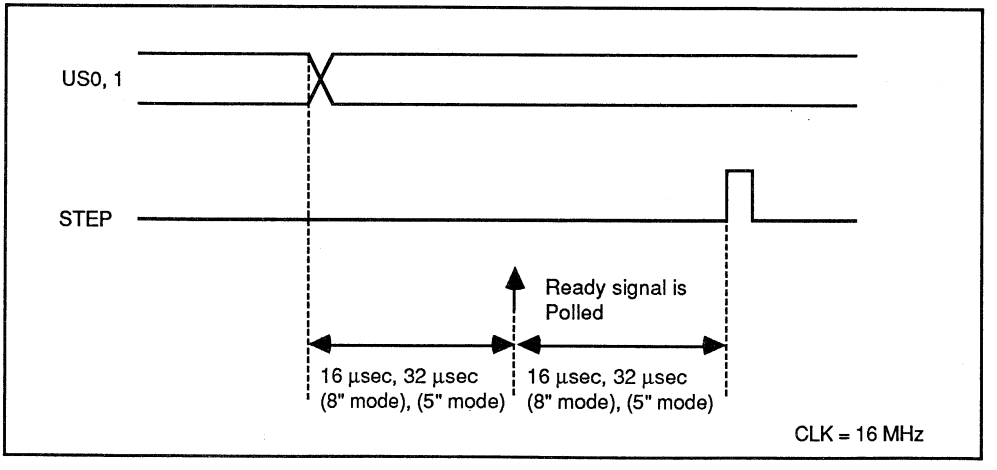


Figure 53. Ready Signal Polling and Step Pulse Output Timing

During polling, if the ready signal level is inverted compared to the last time it was polled:

- INC (interrupt code) bits of SSB0 are set to CDS (Change in Drive Status) code,
- US1 and US0 bits of SSB0 are updated to the drive number whose ready signal is inverted, and
- $\overline{IRQ}$ signal is set active to request the host to issue CHECK INTERRUPT STATUS command.

Also, when a drive completes a seek operation, $\overline{IRQ}$ is set active to make a request for CHECK INTERRUPT STATUS command.

When a CHECK INTERRUPT STATUS command request source is accepted from the FDC by the CHECK INTERRUPT STATUS command, if there is no Seek-End status information in the FDC, the next command request is not generated even if the Ready Signal Inversion status information is present. However, when the CHECK INTERRUPT STATUS command is issued, the command is not treated as the INVALID command; the Ready Signal Inversion status information can be accepted. When Ready Signal Inversion is detected while the $\overline{IRQ}$ signal is inactive, the CHECK INTERRUPT STATUS command is requested by activating the $\overline{IRQ}$ signal.

If the FDC has statuses for more than one CIS command request, it returns FDD statuses to the host each time a CIS command is issued, starting at the lowest-numbered FDD's status.

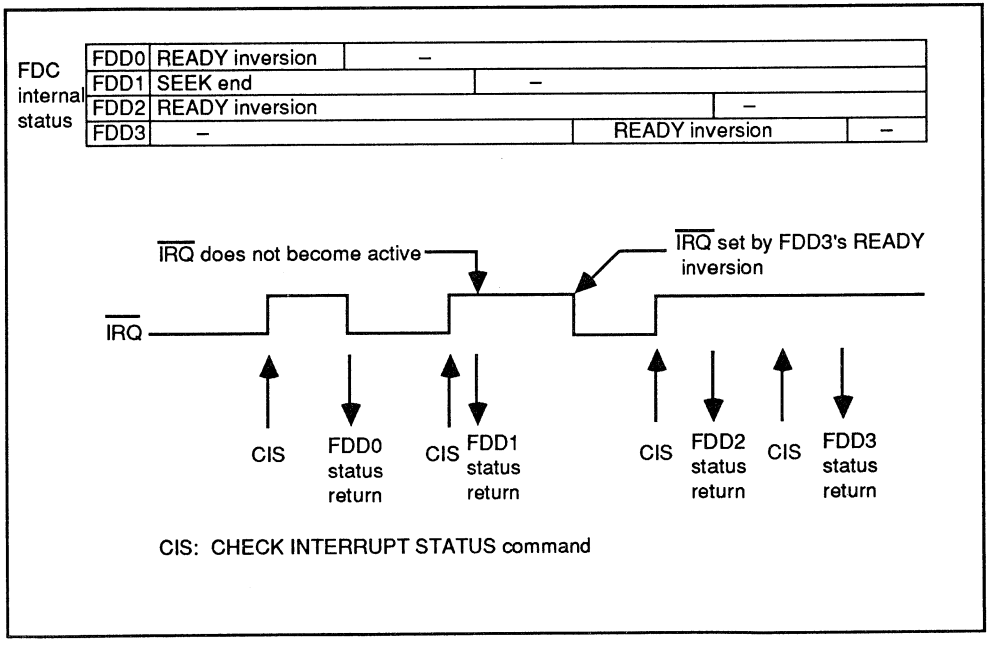


Figure 54. FDD status returning order and $\overline{IRQ}$ output

Internal Circuit Specification

VFO Circuit

- Analog PLL type VFO circuit
- Adjustment free and high accuracy with optimized PLL loop gain and stabler circuits
- No adjustment required
- Selectable data synchronization rate

FM mode: 125, 150, 250 kbps
MFM mode: 250, 300, 500 kbps

To synchronize to the data transferred at 150 kbps in FM mode or 300 kbps in MFM mode, a 19.2 MHz clock must be input to CLK pin with 8"/$\overline{5}$" pin tied low.

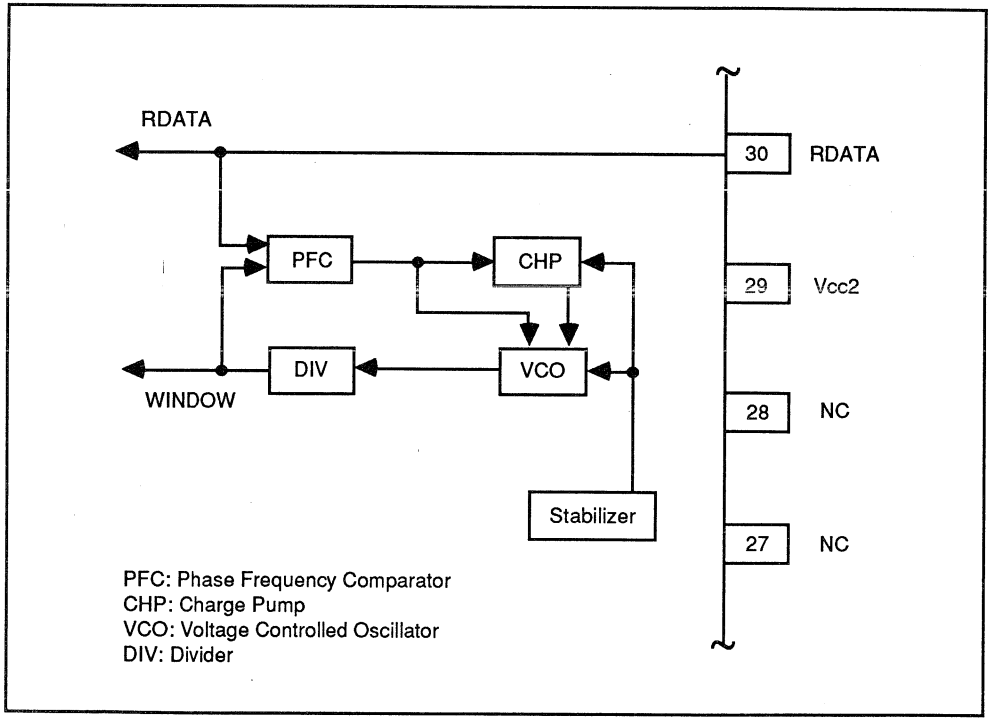


Figure 55. Internal Block Diagram

WRITE PRECOMPENSATION CIRCUIT

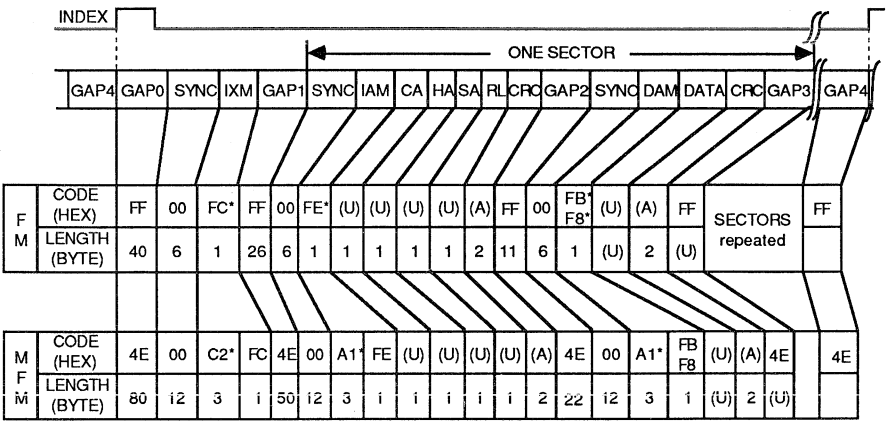
- Digital precompensation circuit
- Delay time programmable by software
- Delay time independently selectable for inner and outer tracks
- Outer to inner switchover track specifiable
- When auto-precompensation mode is not selected by command SPECIFY 2, the precompensation control signals (EARLY, LATE) are output. When auto-precompensation mode is selected, the control signals are not output; EARLY and LATE are fixed at low level.
- Delay time programmable by 62.5 ns increments (Note)
- Auto-precompensation and precompensation control signals are output in MFM mode only
- Range of delay time programmable (in MFM mode)
  250 kbps: 0 – 750 ns
  300 kbps: 0 – 625 ns (Note)
  500 kbps: 0 – 375 ns

  When a value beyond this range is specified, FDC may malfunction.

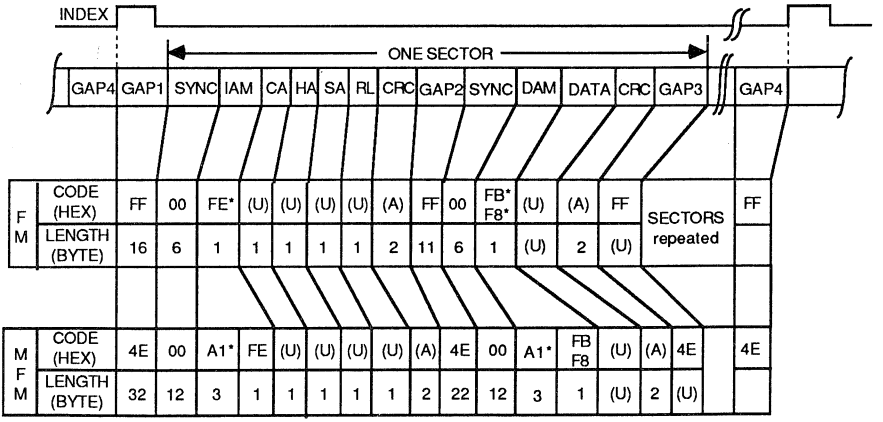
Note: CLK = 19.2 MHz delay time programmable by 52.1 ns increments at 300 kbps.

Track Format

SFORM = 1 IBM Format



SFORM = 0 ISO Format



(U) : User programmable
(A) : Automatically calculated

CA : Cylinder Address
HA : Head Address
SA : Sector Address
RL : Record Length

IXM : Index Mark
IAM : ID Address Mark
DAM : DATA (Deleted Data) Address Mark

GAP4 Length extends from the end of GAP3 in the last sector to the next Index pulse.
Codes marked asterisk (*) indicate that a code contains missing clock.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC} (Note 1)	– 0.3 to + 7.0	V
Input Voltage	V_{in} (Note 1)	– 0.3 to V_{CC} + 0.3	V
Allowable Output Current	$\|I_O\|$ (Note 2)	5	mA
Total Allowable Output Current	$\|\Sigma I_O\|$ (Note 3)	80	mA
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

Notes: 1. This value is in reference to V_{SS} = 0 V

2. The allowable output current is the maximum current that may be drawn from, or flow out to, output terminal or one input/output common terminal.
3. The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.
4. Using an LSI beyond its maximum ratings may result in its permanent destruction. LSI's should usually be used under recommended operating conditions. Exceeding any of these conditions may adversely affect its reliability.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} (Note)	4.75	5.0	5.25	V
Input Low Level Voltage	V_{IL} (Note)	0	–	0.8	V
Input High Level Voltage	V_{IH} (Note)	2.2	–	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

Note: This value is in reference to V_{SS} = 0 V

Electrical Characteristics

DC Characteristics

(V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, T_a = 0 to + 70 °C unless otherwise noted)

Item		Symbol	Measuring Conditions	Limits Min	Limits Max	Unit
Supply Voltage	$V_{CC}1$-$V_{CC}4$	V_{CC}		4.75	5.25	V
Input High Level Voltage	All Inputs	V_{IH}		2.2	V_{CC}	V
Input Low Level Voltage	All Inputs	V_{IL}		– 0.3	0.8	V
Input Leak Current	All Inputs except D0 – D7	I_{in}	V_{in} = 0 to V_{CC}	– 2.5	2.5	µA
Three State (Off State) Input Current	D0 – D7	I_{TSI}	V_{in} = 0.4 to V_{CC}	– 10	10	µA
Output High Level Voltage	All Outputs except $\overline{IRQ}$ when IFS = 1	V_{OH}	I_{OH} = – 400 µA	2.4	–	V
Output Low Level Voltage	All Outputs	V_{OL}	I_{OL} = 1.6 mA	–	0.5	V
Output Leak Current (Off State)	$\overline{IRQ}$ when IFS = 1	I_{LOH}	V_{OH} = V_{CC}	–	10	µA
Input Capacitance	All inputs and outputs	C_{in}	V_{in} = 0 V, T_a = 25 °C f = 1.0 MHz	–	15	pF
Current Consumption	$V_{CC}1$-$V_{CC}4$	I_{CC}	FDC unselected and Disk operation with data transfer in progress	–	40	mA
			FDC in sleep mode	–	10	mA

AC Timing Specification

No.	Item	Symbol	Min	Typ	Max	Unit
1	Clock cycle time	$t_{cyc}C$	50	62.5	80	ns
2	Clock high level width	PW_{HC}	15			ns
3	Clock low level width	PW_{LC}	15			ns
4	Clock falling time	t_{Cf}			20	ns
5	Clock rising time	t_{Cr}			20	ns
6	Read data high level width	PW_{HRDT}	40			ns
7	Read data low level width	PW_{LRDT}	40			ns
8	Write data high level width	PW_{HWDT}		4		$t_{cyc}C$[2]
9	Index signal high level width	PW_{IDX}	6[1]			$t_{cyc}C$
10	Fault reset signal high level width	PW_{FRS}	136[1]		140[1]	$t_{cyc}C$
11	$\overline{DEND}$ signal low level width	PW_{DEND}	40			ns
12	$\overline{RESET}$ signal low level width	PW_{RES}	28[1]			$t_{cyc}C$
13	Enable signal cycle time	$t_{cyc}E$	410			ns
14	Enable signal low level width	PW_{EL}	200			ns
15	Enable signal high level width	PW_{EH}	200			ns
16	Enable signal rising time	t_{Er}			20	ns
17	Enable signal falling time	t_{Ef}			20	ns
18	Address setup time	t_{AS}	0			ns
19	Address hold time	t_{AH}	0			ns
20	Data delay time	t_{DDR}			140	ns
21	Data hold time	t_{DHR}	20			ns
22	$\overline{IRQ}$ release time	t_{IRQ}			200	ns
23	Data setup time	t_{DSW}	60			ns
24	Data hold time	t_{DHW}	5			ns
25	$\overline{DREQ}$ signal release time	t_{DRQ}			200	ns
26	$\overline{RD}$ signal low level width	PW_{RDL}	200		1200[1]	ns
27	$\overline{WR}$ signal low level width	PW_{WRL}	200		1200[1]	ns
28	$\overline{DACK}$ signal low level width	t_{AA}	200			ns
29	$\overline{DACK}$ signal response time	t_{RA}	0			ns
30	$\overline{RD}$ signal response time 1	t_{RR}	0			ns
31	$\overline{WR}$ signal response time 1	t_{RW}	0			ns
32	Unit selection time	t_{US}		128[1]		µs
33	STEP signal timing	t_{UP}		32[1]		µs
34	STEP signal high level width	PW_{HSTP}		7[1]		µs
35	US0 signal switching time	t_{US0}		128[1]		µs
36	US1 signal low level width	t_{US1}		256[1]		µs
37	Polling cycle time	$t_{cyc}US$		1024[1]		µs
38	Head selection signal switching time	t_{HSL}		2[1]		ms
39	FDD selection time	t_{SFD}			3[1]	µs
40	EARLY, LATE signal high level width	PW_{ELH}		1[1]		µs

Notes: 1. These numbers are doubled for 5.25 inch mode.

2. $t_{cyc}C$ refers to a clock period of the input clock (CLK).

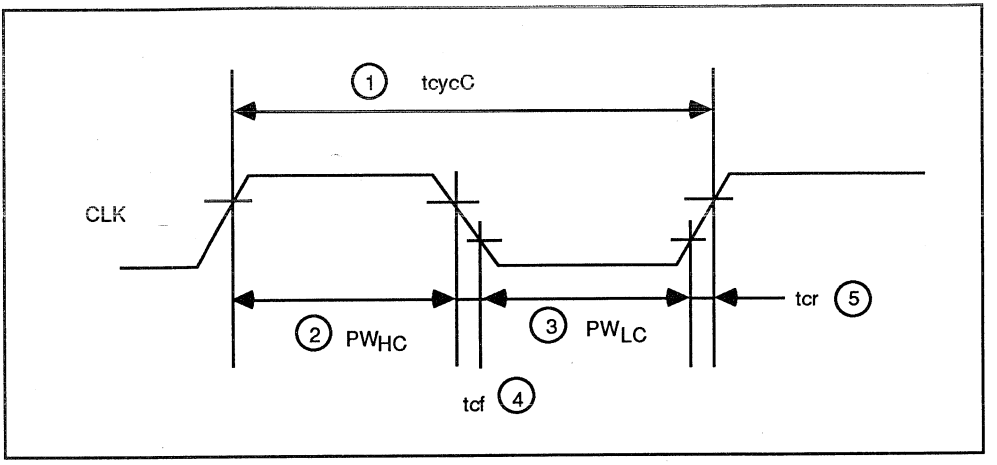


Figure 56. Clock Timing

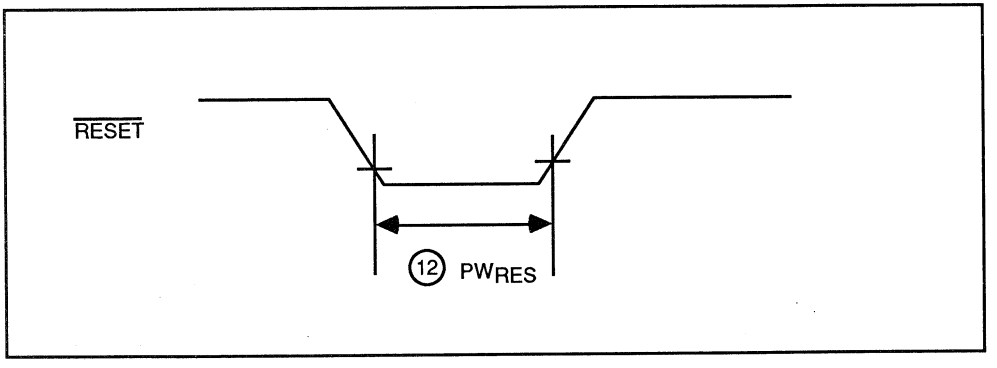


Figure 57. Reset Timing

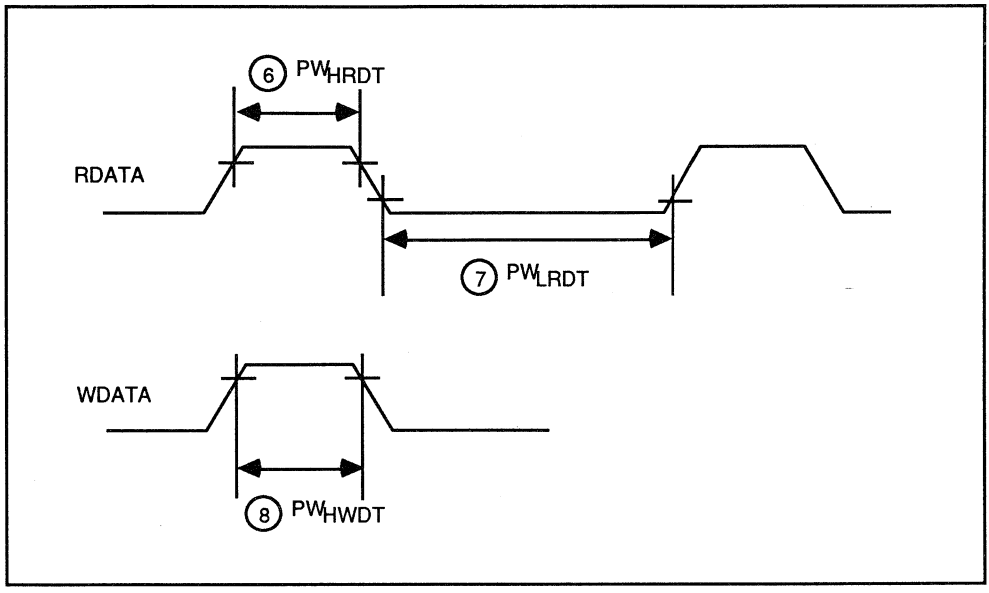


Figure 58. FDD Data Timing

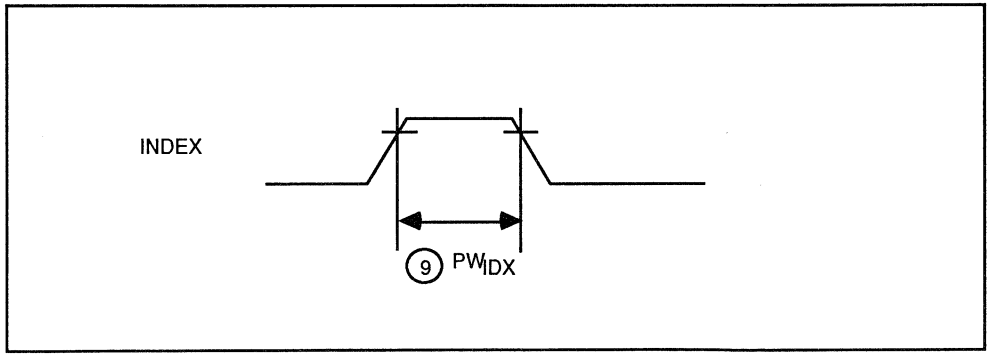


Figure 59. Index Timing

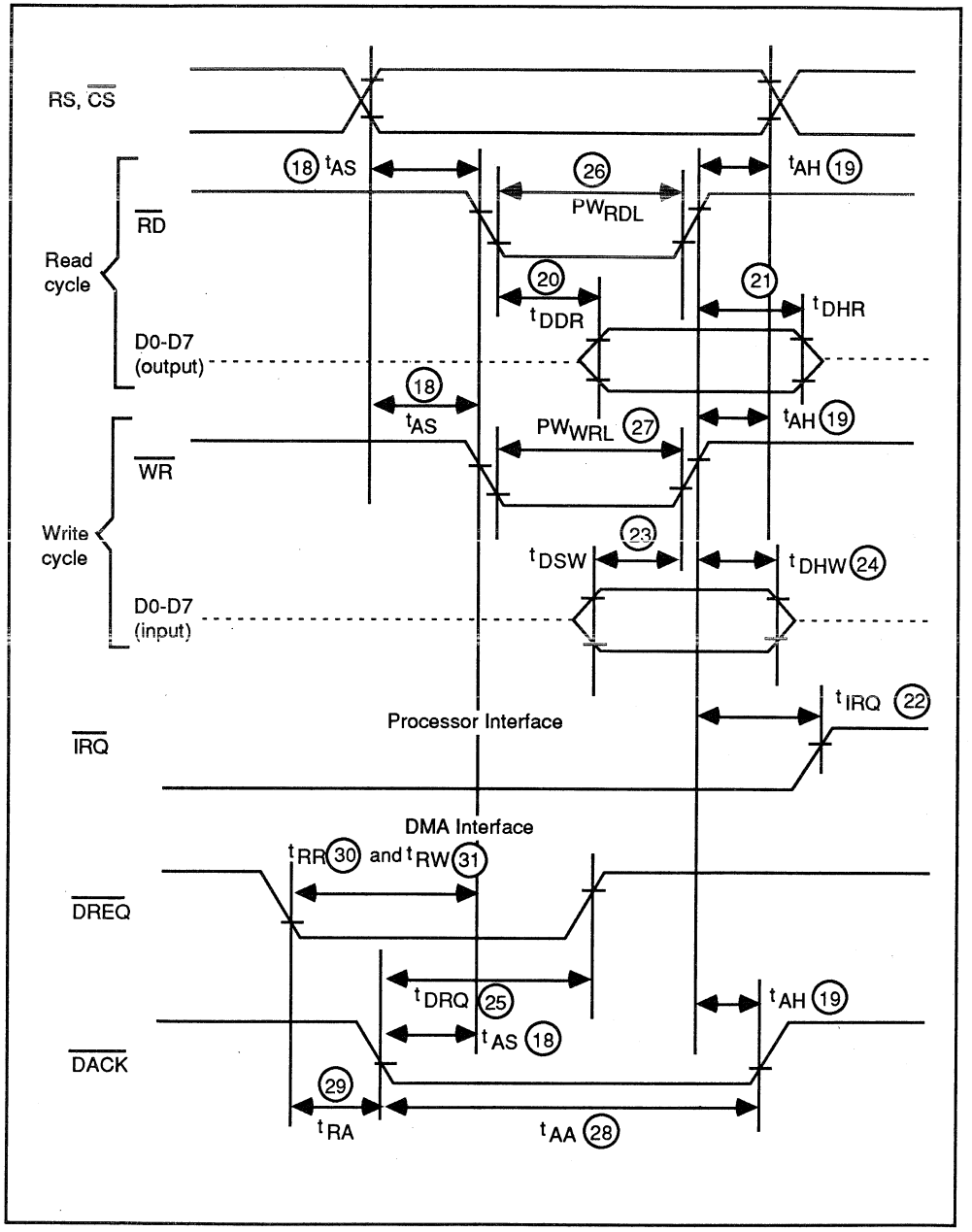


Figure 60. Data Transfer Timings for 80XX Interface

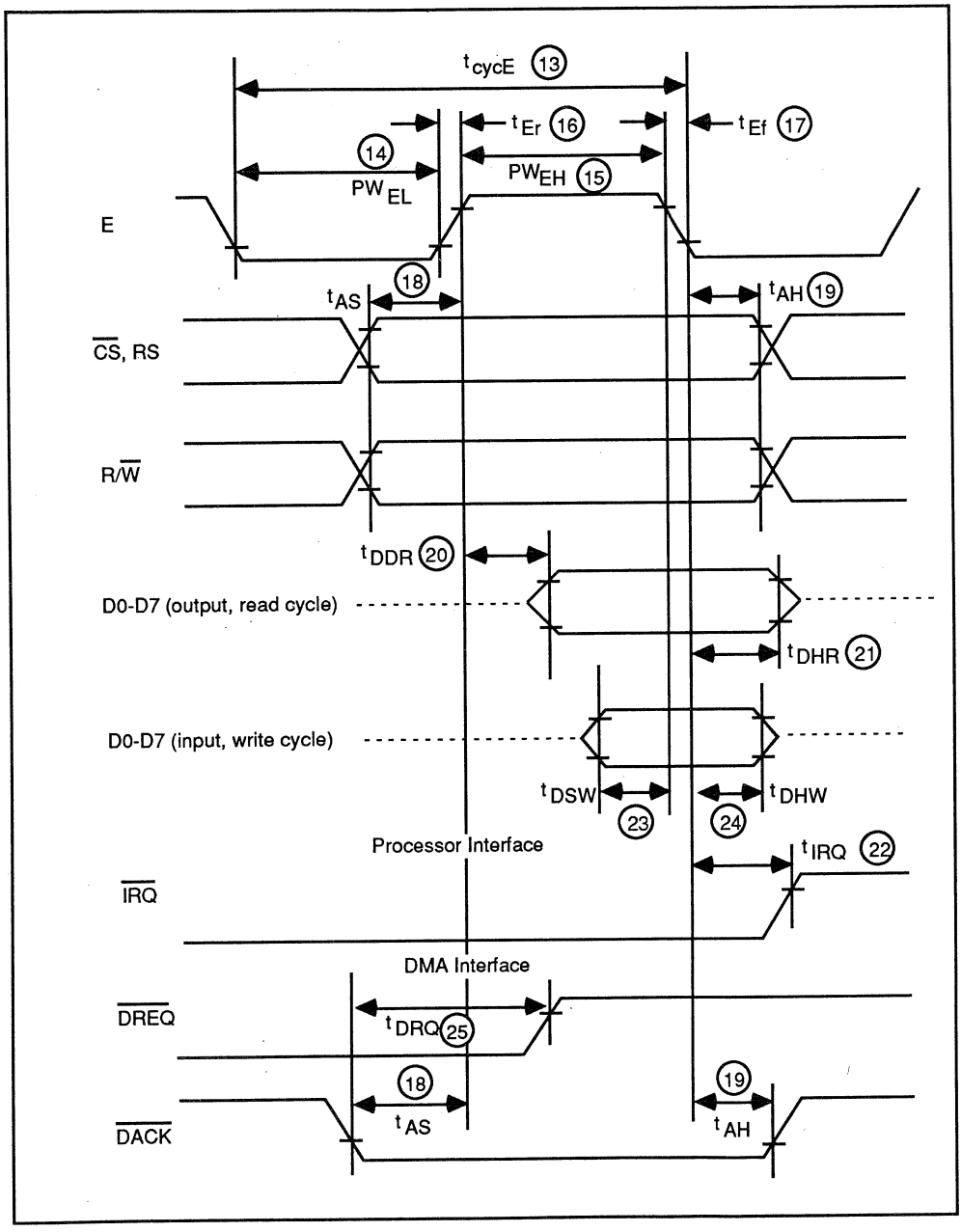


Figure 61. Data Transfer Timings for 68XX Interface

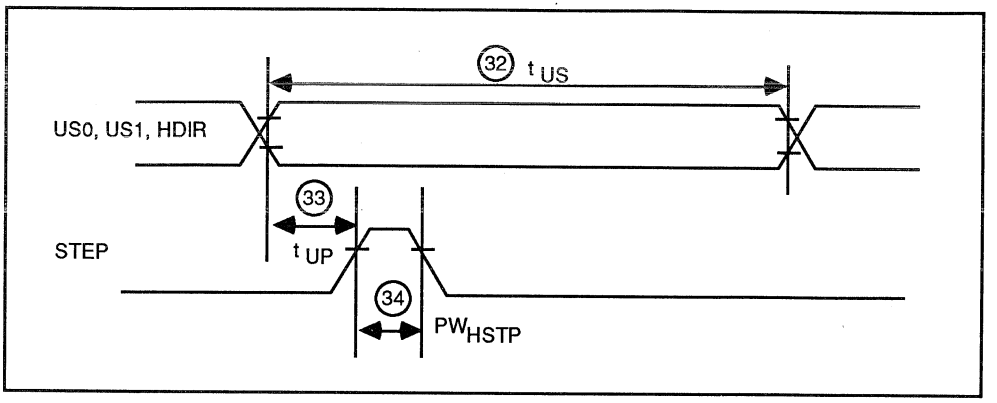


Figure 62. Seek, Recalibrate Timing

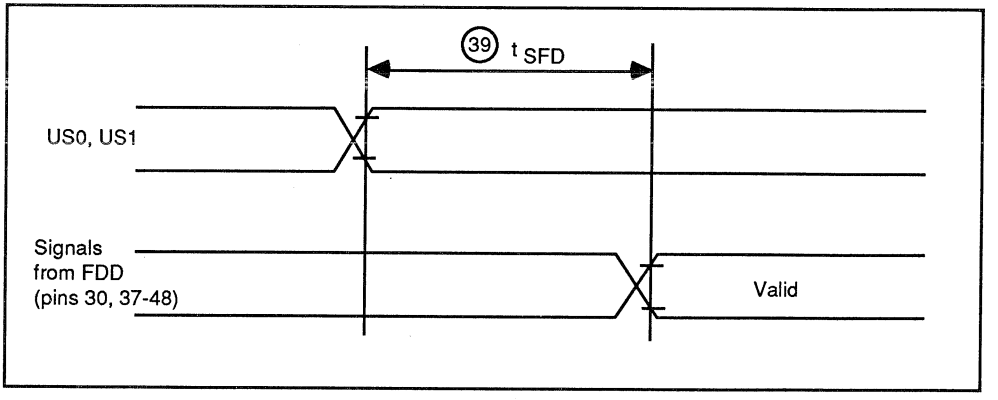


Figure 63. Drive Select Timing

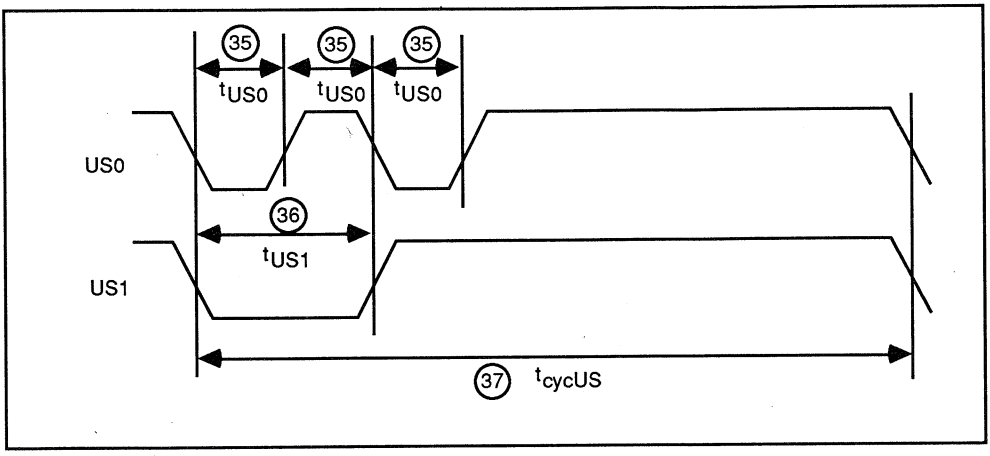


Figure 64. Automatic Polling Timing

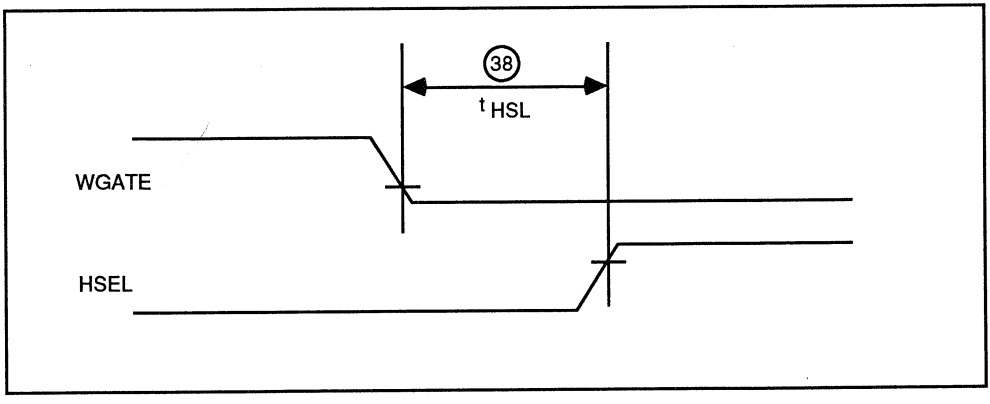


Figure 65. Multitrack Write Timing

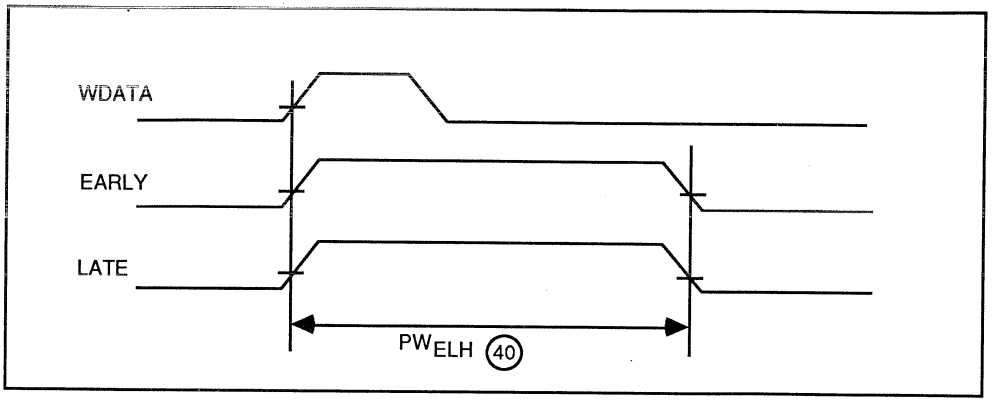


Figure 66. Precompensation Timing

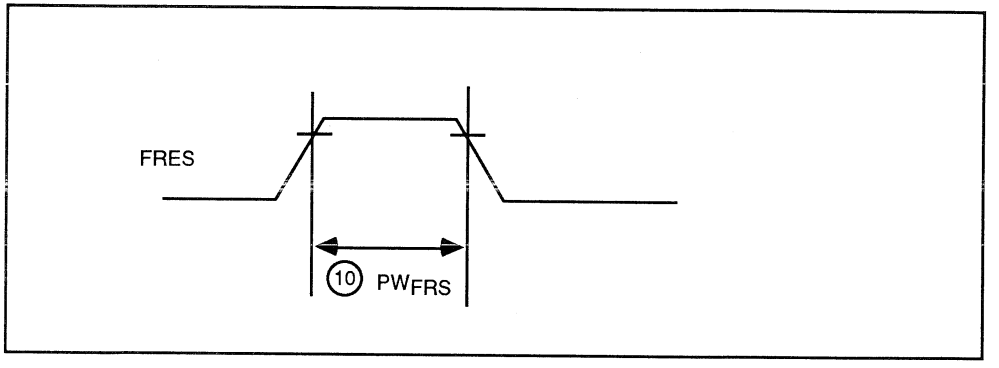


Figure 67. Fault Reset Timing

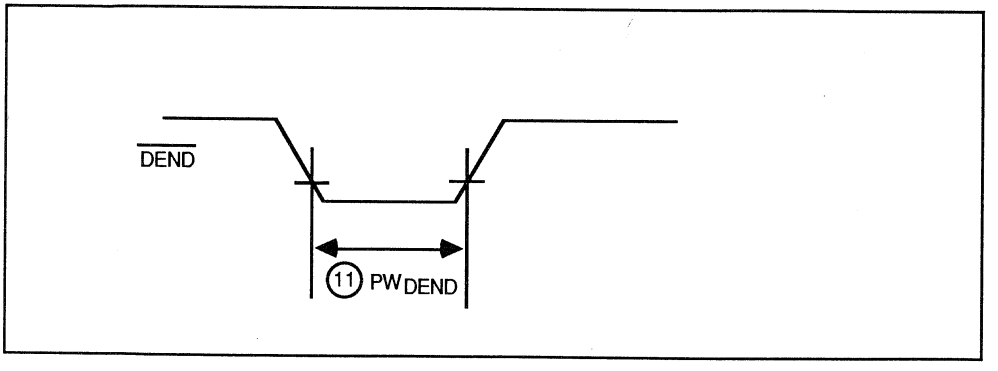
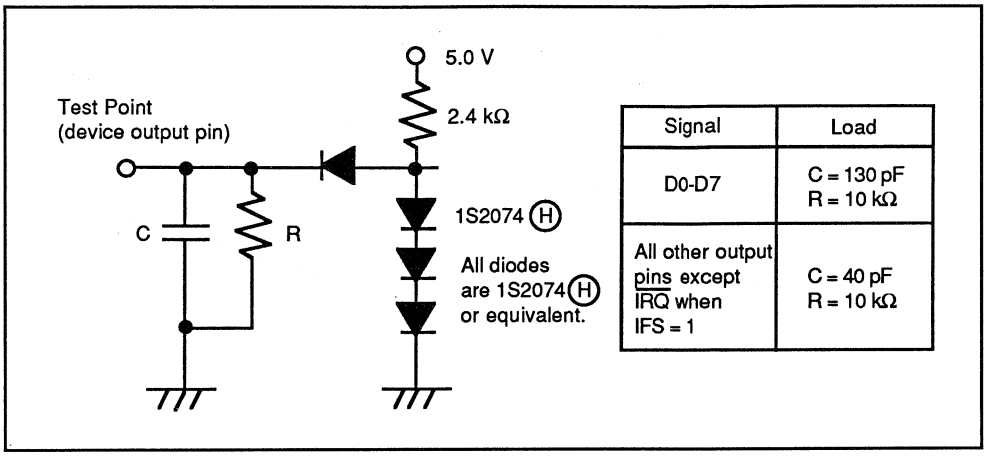


Figure 68. DMA End Timing



Signal	Load
D0-D7	C = 130 pF R = 10 kΩ
All other output pins except $\overline{IRQ}$ when IFS = 1	C = 40 pF R = 10 kΩ

Figure 69. Output Load Circuit for AC Testing

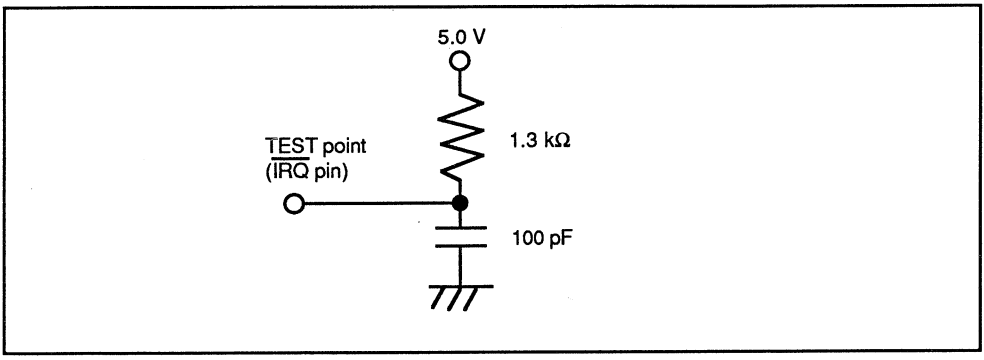


Figure 70. $\overline{IRQ}$ Load Circuit for AC Testing when IFS = 1

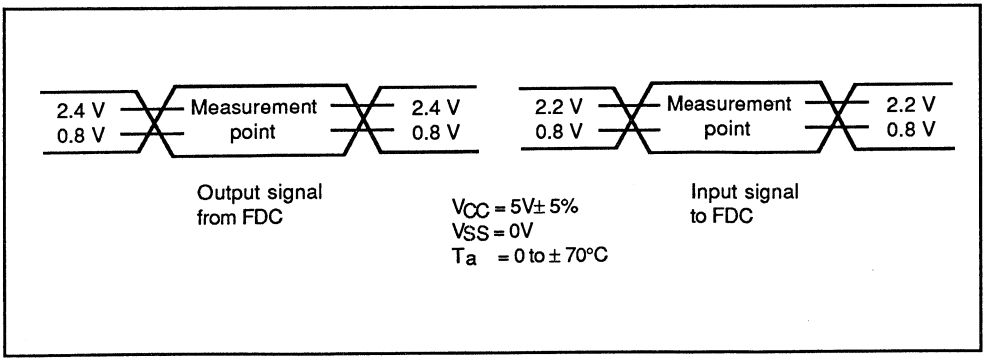


Figure 71. AC Testing Measurement Conditions

Refer to user's manual (No. ADE-602-001) for detail of this product.

HD63463

Hard Disk Controller (HDC)

DESCRIPTION

The HD63463 (HDC: Hard Disk Controller) is a CMOS device developed for use as a peripheral LSI for the 16-bit microprocessor HD68000 (MPU: Microprocessing Unit). The HDC connects the host system and the Winchester type hard disk device with or without HD68450 (DMAC: Direct Memory Access Controller).

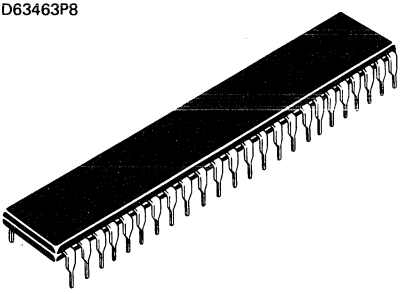
FEATURES

- Two types of disk interface, ST506/ST412/ST412HP and SMD
- Choice of data bus width – 16 or 8 bits
- Serial data transfer rate – max 20 Mbit/s [NRZ], max 10 Mbit/s [MFM]
- Step rate – max 1.1 MHz
- Internal data buffer (256 bytes x 2)
- Zero-sector interleave access
- Programmed I/O access
- Automatic error correction
- Zero pattern detector/generator, address mark detector/generator, write precompensation logic, etc internally provided
- 22 high-level function commands
- 25 error codes
- External circuit diagnosis command
- Low power dissipation – typ 250 mW

TYPE OF PRODUCTS

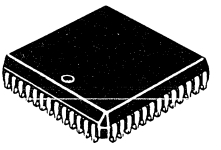
Type No.	Package	Clock Frequency (MHz)	
		Host	Drive
HD63463P8	DP-48	8.0	20.0
HD63463CP8	CP-52	8.0	20.0

HD63463P8



(DP-48)

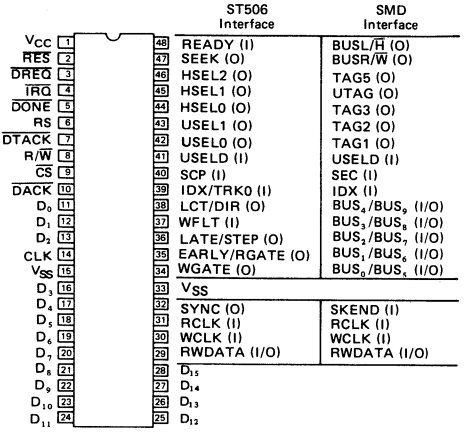
HD63463CP8



(CP-52)

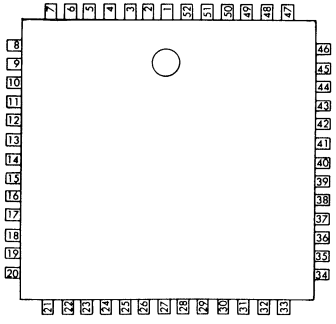
PIN ARRANGEMENT

DP-48



(Top View)

CP-52



(Top View)

Pin No.	ST506 Interface	SMD Interface	Pin No.	ST506 Interface	SMD Interface
1	V_{CC}		27	V_{CC}	
2	V_{CC}		28	D_{12} (I/O)	
3	$\overline{RES}$ (I)		29	D_{13} (I/O)	
4	$\overline{DREQ}$ (O)		30	D_{14} (I/O)	
5	$\overline{IRQ}$ (O)		31	D_{15} (I/O)	
6	$\overline{DONE}$ (I)		32	RWDATA (I/O)	RWDATA (I/O)
7	RS (I)		33	WCLK (I)	WCLK (I)
8	$\overline{DTACK}$ (O)		34	RCLK (I)	RCLK (I)
9	R/$\overline{W}$ (I)		35	SYNC (O)	SKEND (I)
10	CS (I)		36	V_{SS}	
11	$\overline{DACK}$ (I)		37	V_{SS}	
12	D_0 (I/O)		38	WGATE (O)	BUS_0/BUS_5 (I/O)
13	D_1 (I/O)		39	EARLY/RGATE (O)	BUS_1/BUS_6 (I/O)
14	D_2 (I/O)		40	LATE/STEP (O)	BUS_2/BUS_7 (I/O)
15	CLK (I)		41	WFLT (I)	BUS_3/BUS_8 (I/O)
16	V_{SS}		42	LCT/DIR (O)	BUS_4/BUS_9 (I/O)
17	V_{SS}		43	IDX/TRK0 (I)	IDX (I)
18	D_3 (I/O)		44	SCP (I)	SEC (I)
19	D_4 (I/O)		45	USELD (I)	USELD (I)
20	D_5 (I/O)		46	USEL0 (O)	TAG1 (O)
21	D_6 (I/O)		47	USEL1 (O)	TAG2 (O)
22	D_7 (I/O)		48	HSEL0 (O)	TAG3 (O)
23	D_8 (I/O)		49	HSEL1 (O)	UTAG (O)
24	D_9 (I/O)		50	HSEL2 (O)	TAG5 (O)
25	D_{10} (I/O)		51	SEEK (O)	BUSR/$\overline{W}$ (O)
26	D_{11} (I/O)		52	READY (I)	BUSL/$\overline{H}$ (O)

SIGNAL LINES

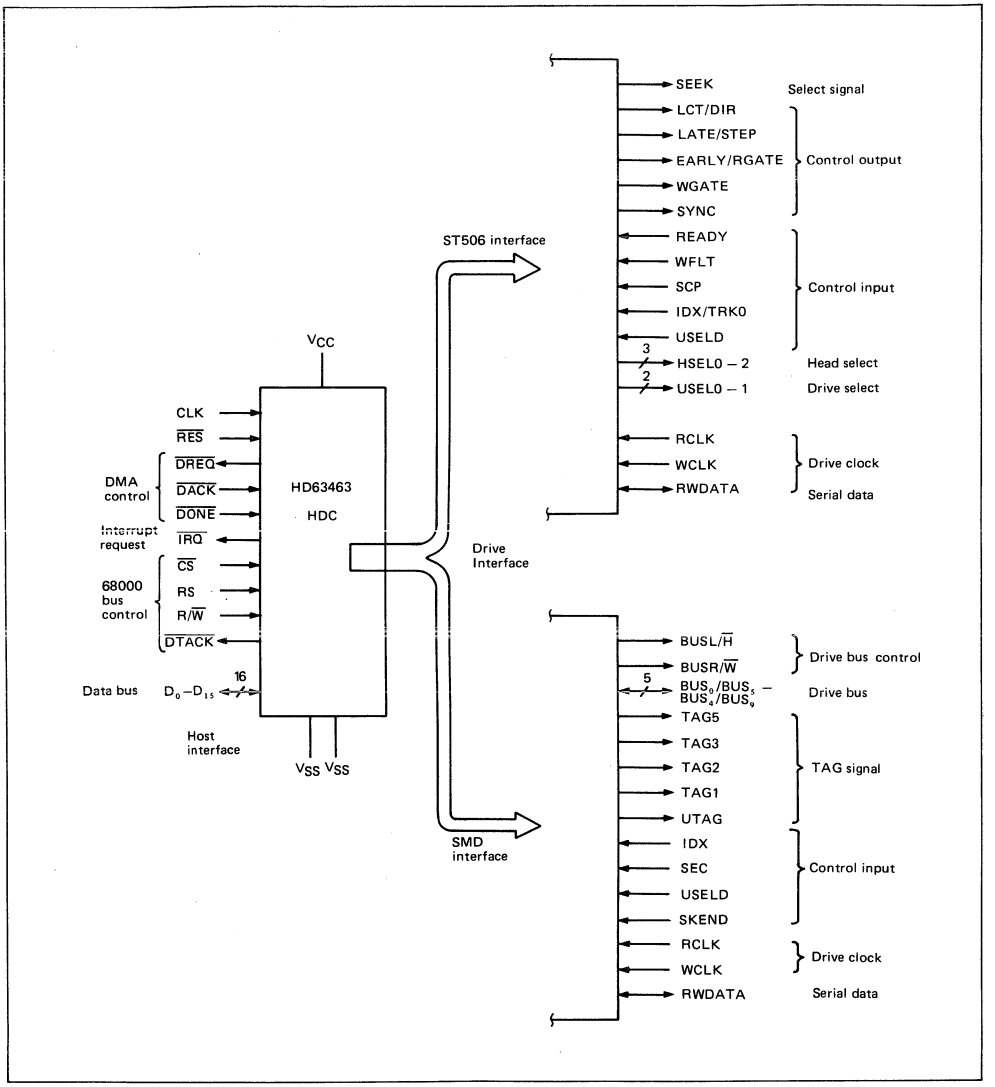


Figure 1 Input/Output Signals

MAJOR FUNCTIONS OF HDC

Drive Interface	ST506*	Number of Heads	Max 8
		Number of Drives	Max 4
		Write Precompensation	Controlled
		High-Speed Seek	Step rate min 875 ns (CLK: 8 MHz)
	Storage Module Drive (SMD)	Number of Heads	Max 32
		Number of Drives	Max 8
		Track Offset	Controlled
		Data Strobe	Controlled
	Serial Data Format	NRZ or MFM (selectable)	
	Serial Data Transfer Rate	Max 20 Mbps (NRZ), max 10 Mbps (MFM)	
	Multiple Sector Access	Multiple sector, multiple track	
	Parallel Seek	Possible	
	Diagnosis	External circuit diagnosis	
Disk Format	Data Length	256, 512, 1024, 2048, or 4096 bytes (selectable)	
	Number of Sectors	Max 255 (hard sector), max 128 (soft sector)	
	Number of Cylinders	Max 1024	
	Sector Format	Hard sector or soft sector (selectable)	
Error Processing	Processing Code	16-bit CRC (error detection), 2 types	
		32-bit ECC (error detection or correction)	
	Error Correction Capability	Automatic correction of single burst error (up to 11 bits)	
On-Chip Data Buffer	Capacity	256 bytes x 2	
	Data Transfer	Simultaneous transfer on host side and drive side	
	Addressing	Stack type (pointer can be updated)	
Host Interface	Operation Cycle Time	Max 8 MHz	
	Data Bus Width	16 or 8 bits (selectable)	
	DMA Transfer	Burst or cycle steal mode (selectable)	
	Programmed I/O	Possible	
Commands	Seek	2 commands	
	Disk Read/Write	8 commands	
	Data Buffer	4 commands	
	Drive Check	2 commands	
	Others	6 commands	

*ST506/ST412/ST412HP is referred to as "ST506" in this document.

HARDWARE DESCRIPTION

SYSTEM CONFIGURATION

An HDC-based system configuration is illustrated in figure 2. The HDC is used to connect more than one hard disk drives (also called "drive" in this manual) to the host system. The host system consists of the MPU (Microprocessing Unit), the main memory and the DMAC (Direct Memory Access Controller). The HDC requires minimum number of external circuits that are connected to the host system including the HD68000 (MPU) and the HD68450 (DMAC).

If the host system does not require a high throughput, then the DMAC is not necessary. A few additional external circuits allow the HDC to be connected to another host system other than the HD68000.

The HDC may control either up to four ST506 drives or up to eight SMD drives.

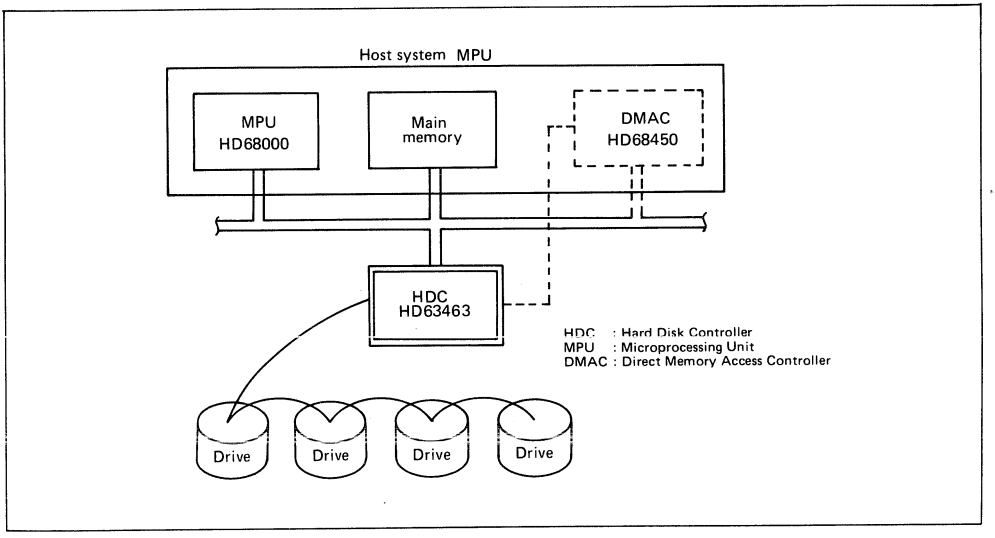


Figure 2 System Configuration Example

SIGNAL LINES

The input/output signal lines of the HDC are shown in figure 1 which covers both ST506 and SMD drive interface.

Each signal is described in the following tables and descriptions.

Host Interface

Category	Signal	I/O
Clock, Reset	CLK	I
	$\overline{RES}$	I
DMA Control (HD68450 Compatible)	$\overline{DREQ}$	O
	$\overline{DACK}$	I
	$\overline{DONE}$	I
Interrupt Request	$\overline{IRQ}$	O
Bus Control (HD68000 Compatible)	$\overline{CS}$	I
	RS	I
	R/$\overline{W}$	I
	$\overline{DTACK}$	O
Data Bus (HD68000 Compatible)	$D_0 - D_{15}$	I/O

CLK – Clock signal from the host system.

$\overline{RES}$ – Reset signal from the host system.

$\overline{DREQ}$ – Asserted when a DMA data transfer is requested to the DMAC. Receiving this signal, the DMAC obtains the bus mastership from the MPU.

$\overline{DACK}$ – Transfer acknowledge signal from the DMAC. Receiving this signal, the HDC transfers data through the host bus in the DMA mode. When $\overline{RES}$ signal is at "0", HDC data bus configuration change from 16 bits to 8 bits when $\overline{DACK}$ = 0.

$\overline{DONE}$ – Receiving this signal from the DMAC, the DMA data transfer through the host bus stops immediately.

$\overline{IRQ}$ – Interrupt request signal sent to the MPU (open drain output).

$\overline{CS}$ – Chip select signal generated by decoding address, address strobe, and data strobe of the host.

RS – Register select signal of the HDC. It selects registers when set to "0", data buffers when set to "1".

R/$\overline{W}$ – Signal that indicates the data transfer direction.

$\overline{DTACK}$ – Acknowledge signal that indicates the end of data transfer in the host bus. The host waits until the HDC asserts this signal to terminate the transfer.

D_0–D_{15} – 16-bit bi-directional data bus. When used as an 8-bit data bus, D_8–D_{15} must be open.

ST506 Interface

Category	Signal	I/O
Select Signal	SEEK	O
Control Output	LCT/DIR	O
	LATE/STEP	O
	EARLY/RGATE	O
	WGATE	O
	SYNC	O
	HSEL0–HSEL2	O
	USEL0–USEL1	O
Control Input	READY	I
	WFLT	I
	SCP	I
	IDX/TRK0	I
	USELD	I
Drive Clock	RCLK	I
	WCLK	I
Drive Data	RWDATA	I/O

SEEK – Used to decode multiplexed signals. SEEK signal remains high during the head positioning operation of the HDC.

LCT/DIR – When SEEK is at "1", this signal indicates the head direction: the head moves toward the spindle if the LCT/DIR signal is at "1". When SEEK is at "0", write current is reduced if this signal is at "1".

LATE/STEP – When SEEK is at "1", this signal serves as step pulses output for head positioning. When SEEK is at "0", this signal requests write precompensation (LATE).

EARLY/RGATE – When the WGATE signal is at "1", this signal requires write precompensation (EARLY). Otherwise, it serves as a read gate signal that requests reading data from the drive.

WGATE – Write gate signal that requests writing data to the drive.

SYNC – Signal to select the loop gain of the external data separator. SYNC is at "1" when RGATE is at "1" and one byte of $00 is detected in the disk data. SYNC is at "0" when RGATE is at "0".

HSEL0–HSEL2 – 3-bit signal that selects up to eight heads in the drive.

USEL0- USEL1 – 2-bit signal that selects one of four drives.

READY – Signal indicating that the selected drive is ready.

WFLT – Signal indicating that the drive has detected a fault which may cause a write error.

SCP – Signal indicating that head positioning (seek operation) has been completed in the drive.

IDX/TRK0 – When SEEK is at "1", this signal indicates that the head in the drive is positioned at the outermost track (track 0). When SEEK is at "0", this signal serves as an index signal that indicates the beginning of a track.

USELD – Response signal from the drive indicating that the drive is selected.

RCLK – Disk read clock from the external data separator. Its frequency is twice the serial transfer rate.

WCLK – Disk write clock from the external oscillator. Its frequency is twice the serial transfer rate.

RWDATA – Disk read/write serial data is input/output as modified frequency modulation code. This pin is normally in read state.

SMD Interface

Category	Signal	I/O
Drive Bus Control	BUSL/$\overline{H}$	O
	BUSR/$\overline{W}$	O
Drive Bus	BUS_0/BUS_5 – BUS_4/BUS_9	I/O
Tag	TAG5	O
	TAG3	O
	TAG2	O
	TAG1	O
	UTAG	O
Control Input	IDX	I
	SEC	I
	USELD	I
	SKEND	I
Drive Clock	RCLK	I
	WCLK	I
Drive Data	RWDATA	I/O

BUSL/$\overline{H}$ – When this signal is at high, lower 5 bits of 10-bit drive bus are being transferred.

BUSR/$\overline{W}$ – When this signal is at high, BUS_0/BUS_5–BUS_4/BUS_9 are in input state.

BUS_0/BUS_5 – BUS_4/BUS_9 – 5-bit bi-directional bus that is used to control the drive. When the data is output from 10-bit drive bus, the high-order 5 bits are output first and then the low-order 5 bits. When the data is input to the bus, higher 3 bits of the 8-bit status are fetched first, then the lower 5 bits.

TAG5 – Together with TAG2, used as a status input select signal.

TAG3 – Tag signal indicating that the drive bus contains information such as disk read/write instruction.

TAG2 – Tag signal indicating that the drive bus contains the address for head selection. When drive status is read from the drive bus, TAG2 and TAG5 are decoded to select the status.

TAG1 – Tag signal indicating that the drive bus contains the destination cylinder address.

UTAG – Tag signal indicating that the drive bus contains a 3-bit drive number.

IDX – Index signal indicating the beginning of a track.

SEC – Signal indicating the beginning of a sector.

USELD – Response signal from the drive indicating that the drive is selected.

SKEND – Signal that is generated when the servo circuit in the disk drive terminates seek operation and the head is placed on the track.

RCLK – Disk read clock from the drive. Its frequency is the same as the serial data transfer rate.

WCLK – Disk write clock from the drive. Its frequency is the same as the serial data transfer rate.

RWDATA – Disk read/write serial data that is input/output as Non-Return to Zero code.

HOST INTERFACE

The HDC can be directly connected to the HD68000 (MPU) and the HD68450 (DMAC), so that the HDC data is transferred asynchronously with the host system. The HDC data bus is 16-bit wide, in addition, an 8-bit configuration is available by asserting the $\overline{DACK}$ signal externally during reset. The minimum access time that is required for communication between the HDC and the MPU, or between the HDC and the DMAC is listed in Table 1 (wait cycles are not included).

Table 1 Host Interface Minimum Access Time

Transfer Direction \ Data Bus	8-Bit Data Bus (cycles)	16-Bit Data Bus (cycles)
MPU read (HDC to MPU)	3	4
MPU write (MPU to HDC)	3	3
DMA write (memory to HDC)	3	3
DMA read (HDC to memory)	3	4

DRIVE INTERFACE

The HDC can interface with two different types of drives. DIF mode of the Operation Mode register 0 (OM0) selects the drive interface. ST506 interface is selected when DIF is at "0", and SMD interface when DIF is at "1". The external circuits required for HDC drive interface vary according to which interface is used. Figures 3 and 4 show the interface circuits which connect ST506 device and SMD device respectively.

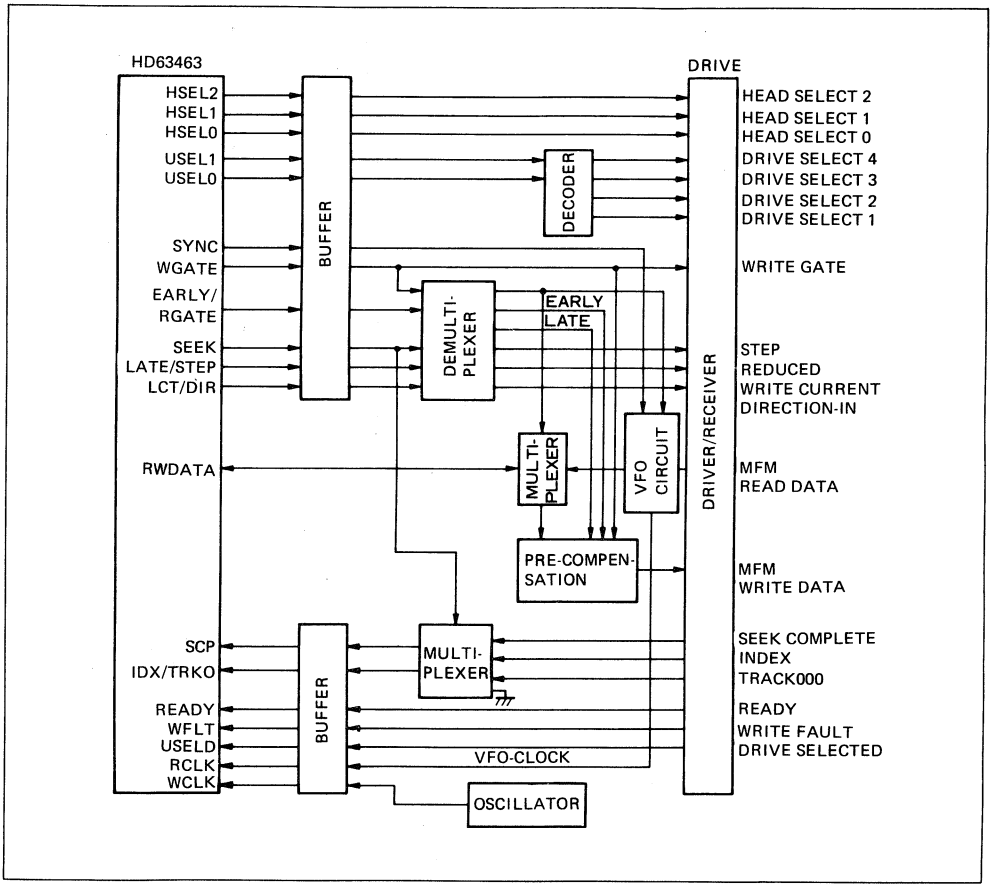


Figure 3 ST506 Interface Circuit

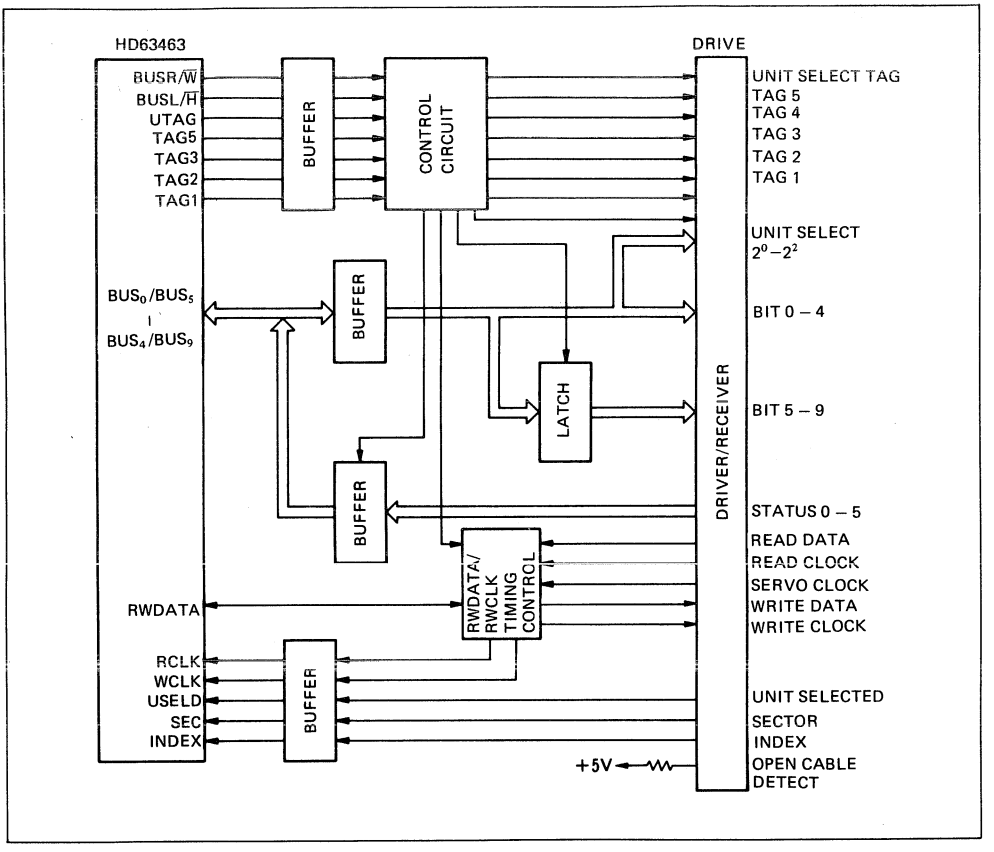


Figure 4 SMD Interface Circuit

SOFTWARE INTERFACE

The HDC is furnished with 22 commands, which are classified into 6 categories; specification, head positioning, disk access, data transfer, drive check, and others.

Table 2 List of Commands

Category	Command	Mnemonic
Specifications	Specify	SPC
Head Positiong	Recalibrate	RCLB
	Seek	SEK
Disk Access	Read Data	RD
	Read Erroneous Data	RED
	Read ID	RID
	Read ID Skew (Note 1)	RIS
	Find ID	FID
	Check Data	CKD
	Compare Data	CMPD
	Write Data	WD
	Write Format	WFM
	Write Format Skew (Note 1)	WFS
Data Transfer	Memory to Buffer	MTB
	Buffer to Memory	BTM
	Open Buffer Write	OPBW
	Open Buffer Read	OPBR
Drive Check	Polling	POL
	Check Drive	CKV
Others	Abort	ABT
	Check ECC	CKE
	Polling Disable	POD
	Recall	RCAL
	Test	TST

(Note 1) Valid only for the hard sector. Disabled for the soft sector.

Specify – Specifies the HDC's operation mode, data transfer mode, etc.

Recalibrate – Moves the drive head to the outermost track (track 0).

Seek – Moves the drive head onto a track specified by the Next Cylinder Address.

Read Data – Reads the data of specified sectors and stores it in the data buffer.

Read Erroneous Data – Reads disk data and stores it in the data buffer no matter a CRC error occurs or not in ID area.

Read ID – Reads ID areas from specified number of sectors.

Read ID Skew – Reads ID area of a sector formatted by Write Format Skew command.

Find ID – Reads ID areas and stores the data in data buffers. ID area containing a CRC error is skipped reading, and the subsequent ID area without any CRC error is searched for.

Check Data – Checks if there is any ECC or CRC error in DATA area of specified sectors. No data is transferred to data buffers or to the main memory while checking.

Compare Data – Compares the data in data buffers and the data read from specified sectors.

Write Data – Writes the data stored in data buffers into DATA area of specified sectors.

Write Format – For the hard sector, formats a specified number of sectors starting with a specified physical sector address. For the soft sector, formats a track.

Write Format Skew – Formats a sector specified by a physical sector address by skewing ID area by 64 bytes.

Memory to Buffer – Transfers data from the main memory to the data buffer by DMA transfer.

Buffer to Memory – Transfers data stored in the data buffer to the main memory by DMA transfer.

Open Buffer Write – Provides initialization of pointer to write data into the data buffer starting from an address specified by Pointer Offset. The data buffer is written in the PIO mode after the command execution ends.

Open Buffer Read – Provides initialization to read the data stored in the data buffer from an address specified by Pointer Offset. The data buffer is read in the PIO mode after the command execution ends.

Polling – Monitors drive status including seek end.

Check Drive – Sets result parameters indicating status of a specified drive to Parameter Block.

Abort – Stops all operations being executed by the HDC.

Check ECC – For ECC errors occurred during RD and RED command execution, reports result parameters indicating addresses and patterns of erroneous data.

Polling Disable – Stops Polling command execution.

Recall – Clears all bits of the status register and sets a buffer pointer to the start address of parameter block so that command parameters can be accepted.

Test – Makes the output pins of the HDC's drive interface three-stated.

Table 3 Command Code, Interrupt Request, and DMA Data Transfer

Command Name	Command Code		Interrupt Factor Bits			DMA Transfer	
	Binary	HEX	CED	SED	DER	DTM = 0	DTM = 1
Specify	1110 1000	E8					
Recalibrate	1100 1000	C8	○	○	○		
Seek	1100 0000	C0	○	○	○		
Read Data	0100 0000	40	○	○	○		○
Read Erroneous Data	0111 0000	70	○	○	○		○
Read ID	0110 0000	60	○	○	○		○
Read ID Skew	0110 1000	68					
Find ID	0110 0001	61	○	○	○		○
Check Data	0100 1000	48	○	○	○		
Compare Data	1000 1000	88	○	○	○		○
Write Data	1000 0111	87	○	○	○		○
Write Format	1010 0011	A3	○	○	○		○
Write Format Skew	1010 1011	AB					
Memory to Buffer	1001 0000	90	○			○	○
Buffer to Memory	0101 0000	50	○			○	○
Open Buffer Read	0011 0000	30					
Open Buffer Write	0011 1000	38					
Polling	0001 0000	10		○	○		
Check Drive	0010 1000	28			○		
Abort	1111 ****	F0-FF	○				
Check ECC	0010 0000	20					
Test	1110 0000	E0					
Polling Disable	0001 1000	18		○	○		
Recall	0000 1000	08					
Inhibited	1101 ****	D0-DF					

DMA: Direct Memory Access
DTM: Data Transfer Mode
*: don't care

○: Set at the end of command execution.

○: DMA transfer is performed.

PROGRAMMING MODEL

Figure 5 shows the internal configuration of the HDC and a programming model. The HDC internally provides an 8-bit STR (Status register), an 8-bit CMR (Command register), a 16-byte PB (Parameter Block) and two 256-byte data buffers (DBUF0 and DBUF1). The data can be written to/read from PB, DBUF0 and DBUF1 by externally accessing DTR (Data Transfer register). Their address are specified by a pointer, and is incremented for each access. Internal processors set pointer value, or select one of PB, DBUF0 and DBUF1 to be connected to DTR. These internal processors are initialized by writing a command from the MPU to CMR. The result of command execution is reflected in the STR.

At the beginning of the command execution, internal processors read command parameters in PB written by the MPU and determine the command operation mode. At the end of the command execution, the MPU reads result parameters in PB written by internal processors.

When the HDC writes data to a disk, the host system sends disk write data to DBUF, then internal processors write the contents of DBUF into the disk. When the HDC reads data from a disk, internal processors read the contents of the disk and stores them into DBUF, then the host system reads data from DBUF. The MPU can access STR, CMR, and DTR while the DMAC can access only DTR in the single addressing mode.

When used in 8-bit mode, the HDC requires 2-byte address space. One byte (RS (Resister Select signal) = 0) is an 8-bit read only STR or an 8-bit write only CMR. Another byte (RS = 1) is an 8-bit DTR.

When used in a 16-bit mode, the HDC requires 2-word address space. One word (RS = 0) consists of an 8-bit CMR and an 8-bit read only STR. Another word (RS = 1) serves as a 16-bit DTR.

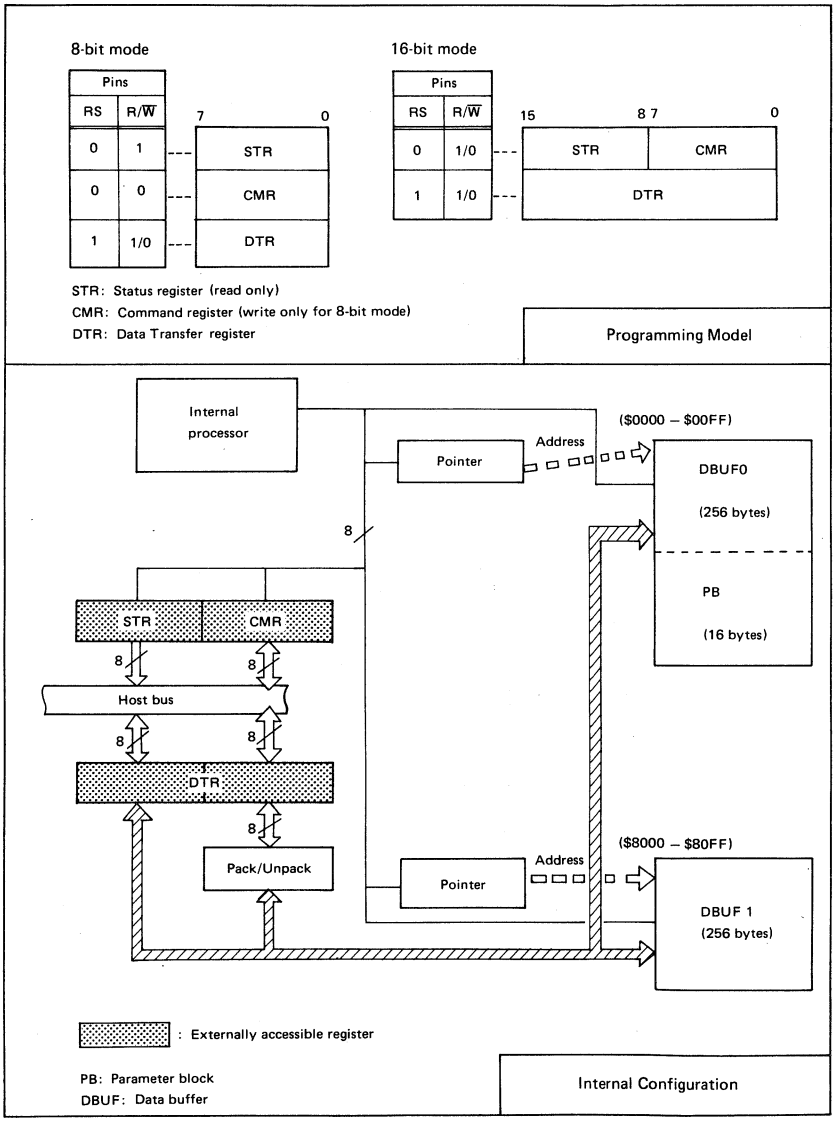


Figure 5 Internal Configuration and Programming Model

When the HDC is either in idle state or command execution end state, the MPU can access PB by accessing DTR. While the HDC is executing a command (during data transfer), DBUF0 or DBUF1 can be accessed by accessing DTR. Before accessing DBUF0 or DBUF1, the MPU must issue a command to open the buffer.

STATUS REGISTER

The bit configuration of the Status register is shown in the figure below, and each bit is described in Table 4.

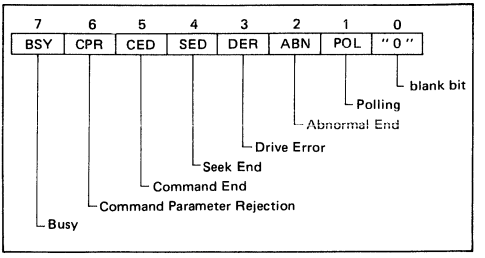


Table 4 Status Register Bit Description

Bit	Abbr.	Bit Name	Set "1" Condition	Reset "0" Condition	Interrupt Source Bit	Description
7	BSY	Busy	Command acknowledged	Command execution end (except for POL command)		While HDC is executing a command, BSY bit is set to "1".
6	CPR	Command Parameter Rejection	Command execution	RCAL command received		With this bit reset to "0", command parameters can be written.
5	CED	Command End	Command execution end	RCAL command received	○	Set to "1" when command shown in table 3 ends. When this bit is set, HDC asserts $\overline{IRQ}$ signal.
4	SED	Seek End	Drive seek end detected	RCAL command received	○	If detecting drive seek end during execution of command shown in table 3, HDC sets "1" in this bit at the end of command execution.
3	DER	Drive Error	Drive error detected	RCAL command received	○	If detecting drive error during execution of command shown in table 3, HDC sets "1" in this bit at the end of command execution.
2	ABN	Abnormal End	Error detected	RCAL command received		If acknowledging errors such as illegal command, drive faults, data over/under run, the HDC sets "1" to ABN at the end of command execution. The SSB contains the error code.
1	POL	Polling	POL command received	POD command received, seek operation end detected, drive error detected		Set to "1" during execution of POL command.
0						Blank bit, always set to "0".

○: An interrupt is generated when this bit is set.

HDC CONTROL PROCEDURE

The MPU's procedure to control the HDC is shown in figure 6. To control the HDC, the MPU must read STR of the HDC. The MPU may issue command parameters to PB in the HDC only when both BSY and CPR bits are cleared.

This enables the HDC to change its status from idle state to command wait state. Although a data buffer pointer does not indicate the start address of PB under command wait state, STR has the same contents as in the idle state. It is impossible to distinguish these two internal HDC states externally.

After this, the MPU issues a command. The HDC executes a command after setting BSY bit to "1". At the end of command execution, result parameters are stored in PB, the CPR bit is set to "1", and BSY bit is cleared. Under this condition, the MPU reads result parameters from PB. Issuing Recall command after this enables the HDC state to change from command execution end state to idle state.

Some commands do not require either or both of the command parameter and result parameter. For some commands, the CED bit, SED bit, or DER bit is set to "1", which enables the HDC to generate an interrupt request to the MPU.

In the DMA (direct memory access) mode, data transfer takes place between the main memory and the HDC when a disk access command is received. For this reason, the MPU must initialize the DMAC before issuing a disk access command to the HDC. Data such as system memory address and number of transfer words are written into the DMAC register.

When the MPU writes data into internal control register in the DMAC, the DMAC state changes from the idle state to transfer request wait state. Upon reception of a transfer request signal ($\overline{DREQ}$) from the HDC, the DMAC transfers data to/from the HDC and system memory until specified number of words are transferred. The DMAC may generate an interrupt request to the MPU when the transfer is completed.

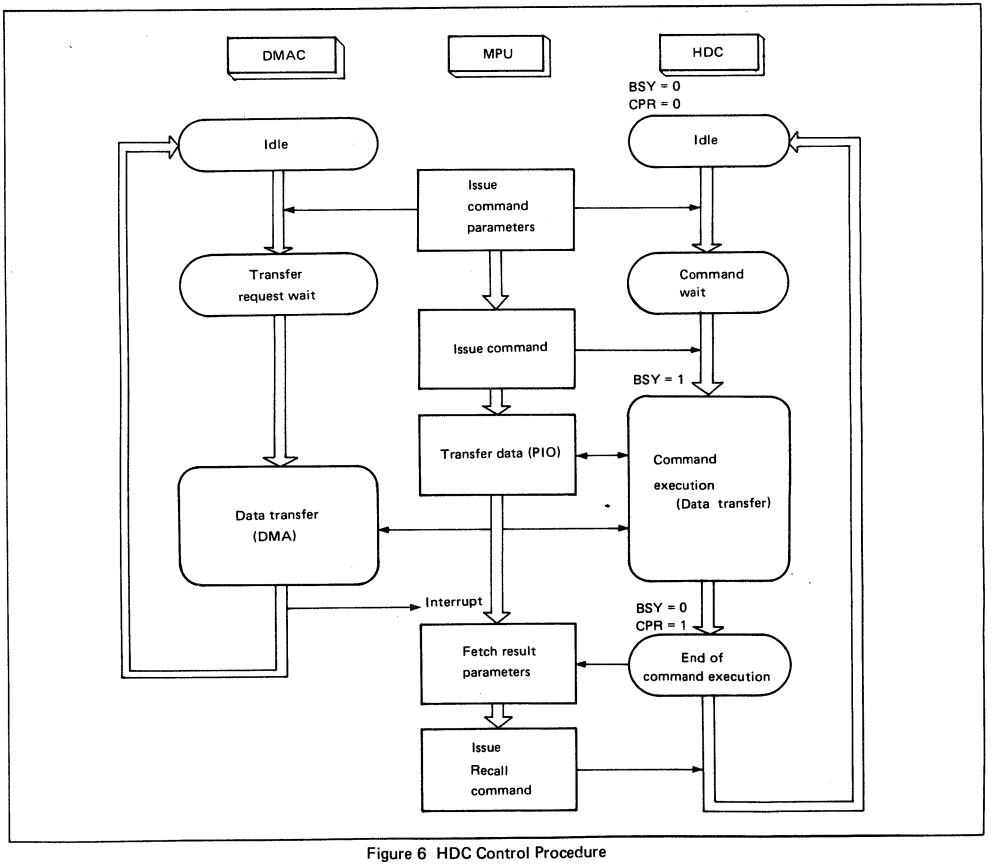


Figure 6 HDC Control Procedure

COMMAND PARAMETERS

Command parameters are listed in Table 5. Command parameters used by the HDC to control ST506 type hard disk drive are listed in the upper row of each command, and those for the SMD type in the lower row.

Table 5 Command Parameter (byte organization)

Commands	Parameters (Upper row: ST506 / Lower row: SMD)
Specify	OM0 OM1 OM2 CUL TO/NCH NCL NH NS SH/RL GPL1 GPL2 GPL3 LCCH LCCL PCCH PCCL OM0 OM1 OM2 CUL TO/NCH NCL NH NS SH/RL GPL1 GPL2 RGTLT
Recalibrate	US $00 US $00
Seek	US $00 NCAH NCAL US $00 NCAH NCAL
Read Data	US PHA LCAH LCAL LHA LSA SCNTH SCNTL US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Read Erroneous Data	US PHA SCNTH SCNTL US PHA $00 PSA SCNTH SCNTL
Read ID Read ID Skew (Note 1)	US PHA $00 OFFSET $00 SCNTL US PHA $00 PSA $00 SCNTL
Find ID	US PHA $00 OFFSET $00 SCNTL US PHA $00 PSA $00 SCNTL
Check Data	US PHA LCAH LCAL LHA LSA SCNTH SCNTL US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Compare Data	US PHA LCAH LCAL LHA LSA SCNTH SCNTL US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Write Data	US PHA LCAH LCAL LHA LSA SCNTH SCNTL US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Write Format Write Format Skew (Note 1)	US PHA SCNTH SCNTL US PHA $00 PSA SCNTH SCNTL
Memory to Buffer	POFFH POFFL POFFH POFFL
Buffer to Memory	POFFH POFFL POFFH POFFL
Open Buffer Read	POFFH POFFL POFFH POFFL
Open Buffer Write	POFFH POFFL POFFH POFFL
Polling	None
Check Drive	US $00 US $00
Abort	None
Check ECC	None
Test	None
Polling Disable	None
Recall	None

(Note 1) Read ID Skew and Write Format Skew are valid only for SMD interface.

SPECIFY COMMAND PARAMETERS

Parameters of SPC command may be used to specify the HDC operation mode and the disk format. Parameters are listed in table 6. Contents of these parameters are different according to which type of drive is used: either ST506 or SMD. Each parameter is described in tables 7 and 8. Table 7 lists parameters which are specified by a bit, and table 8 lists parameters which are specified by 3–16 bits.

The HDC supports soft sector format (in ST506 interface) and hard sector format (in SMD interface) which are shown in figure 7.

Table 6 Specify Command Parameter Organization

	Bit 7	6	5	4	3	2	1	0
OM0	SECT	MOD	DIF	PADP	ECD	CRCP	CRCI	ACOR
OM1	DTM	BRST	CEDM	SEDM	DERM	0	AMEX	PSK
OM2	SL (ST506)							
	CUL							
	TO						NCH	
	NCL							
	NH							
	NS							
	SH					RL		
	GPL1							
	GPL2							
	GPL3							
	LCC High (LCCH)							
	LCC Low (LCCL)							
	PCC High (PCCH)							
	PCC Low (PCCL)							

	(SMD)							
OM2	0	0	0	0	SOFM	SOFP	STBL	STBE

Table 7 Specify Command Parameters (a)

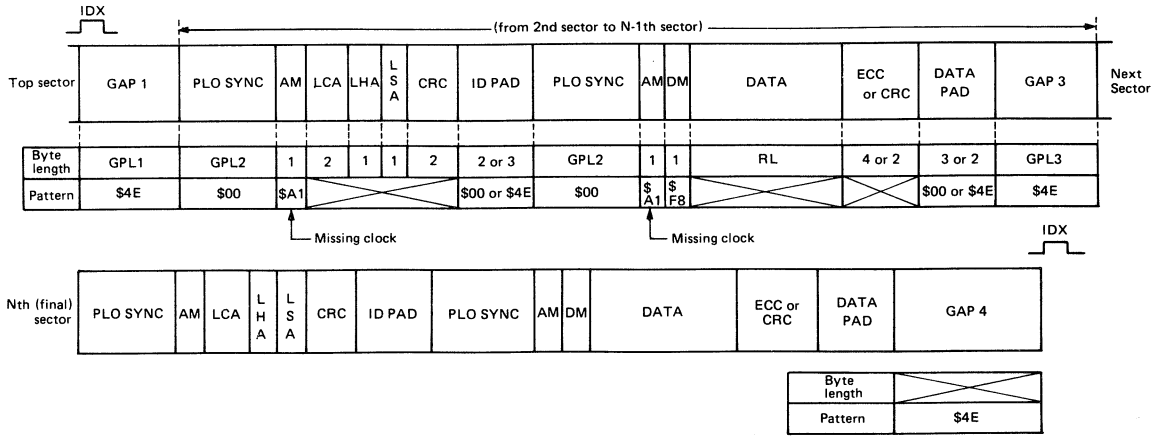
Abbreviation	Name	0	1	ST506	SMD
SECT	Sector Organization	Soft Sector	Hard Sector	0	1
MOD	Data Modulation	MFM	NRZ	0	1
DIF	Drive Interface	ST506	SMD	0	1
PADP	PAD Pattern	$00	$4E	*	0
ECD	Error Check Code	CRC	ECC	*	*
CRCP	CRC Polynomial	$X^{16} + 1$	$X^{16} + X^{12} + X^5 + 1$	*	*
CRCI	CRC Initial Value	$0000	$FFFF	*	*
ACOR	Automatic Correction	Disabled	Enabled	*	*
DTM	Data Transfer Mode	PIO	DMA	*	*
BRST	DMA Burst Mode	Cycle Steal	Burst	*	*
CEDM	Command End Mask	Unmasked	Masked	*	*
SEDM	Seek End Mask	Unmasked	Masked	*	*
DERM	Drive Error Mask	Unmasked	Masked	*	*
AMEX	Address Mark Exclude	Included	Not Included	*	*
PSK	Parallel Seek	Normal	Parallel	*	1
SOFM	Servo Offset Minus	Normal	Minus	None	*
SOFP	Servo Offset Plus	Normal	Plus	None	*
STBL	Strobe Late	Normal	Late	None	*
STBE	Strobe Early	Normal	Early	None	*

* Either 0 or 1

Table 8 Specify Command Parameters (b)

Abbreviation	Name	ST506	SMD
SL	Step Pulse Low	8 bits	None
CUL	Connecting Unit List	4 bits	8 bits
TO	Read/Write Time-over	6 bits	6 bits
NC	Number of Cylinders	10 bits	10 bits
NH	Number of Heads	3 bits	5 bits
NS	Number of Sectors	8 bits	8 bits
SH	Step Pulse High	5 bits	None
RL	Record Length	3 bits	3 bits
GPL1	Gap Length 1 (8 bits)	GAP1	HEAD SCAT
GPL2	Gap Length 2 (8 bits)	PLO SYNC	PLO SYNC
GPL3	Gap Length 3 (8 bits)	GAP3	RGATE Latency
LCC	Low Current Cylinder	16 bits	None
PCC	Precompensation Cylinder	16 bits	None

Soft Sector Format Supported by HDC



Hard Sector Format Supported by HDC

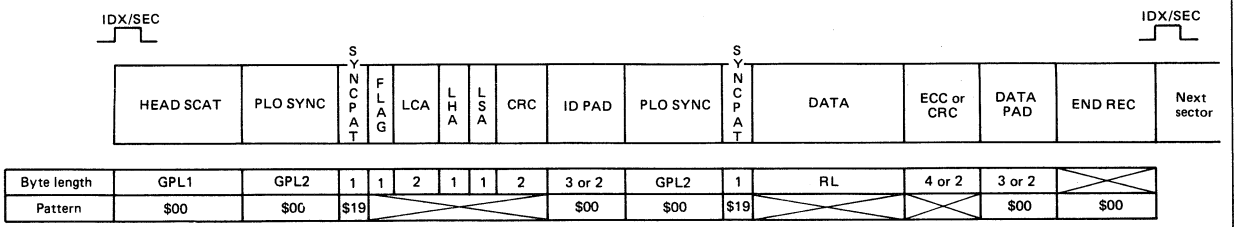


Figure 7 Disk Format

OM0 (Operation Mode 0)

(1) SECT (Sector Format) bit

This bit specifies the format of the drive to be connected to the HDC. There are two drive formats available: hard sector and soft sector.

SECT = 1: Hard Sector Format
SECT = 0: Soft Sector Format

(2) MOD (Modulation) bit

This bit specifies modulation mode for data written to/read from the drive.

MOD = 1: NRZ (Non Return to Zero)
MOD = 0: MEM (Modified FM)

(3) DIF (Drive Interface) bit

This bit specifies the type of drive interface: either ST506 or SMD. The pin function of the HDC changes according to the interface type.

DIF = 1: SMD Interface
DIF = 0: ST506 Interface

In SMD interface, the HDC performs seek instruction, head specification, drive status check, etc to the drive through 5-bit bi-directional buffer BUS_0/BUS_5—BUS_4/BUS_9.

In ST506 interface, the HDC makes the drive perform seek operation by issuing step pulses.

(4) PADP (PAD Pattern) bit

This bit specifies the data pattern of PAD area that follows ID and DATA areas. The value of the PADP bit gives the data pattern of PAD area that is written into the drive by WFM or WD command execution.

	Hard Sector	Soft Sector
PADP = 1	Prohibited	$4E
PADP = 0	$00	$00

(5) ECD (Error Check Code) bit

This bit specifies the error check code which is added to the end of the DATA area. CRC code is always specified for the ID area regardless of ECD bit.

ECD = 1: ECC (Error Correction Code)
ECD = 0: CRC (Cyclic Redundancy Check Code)

ECC enables error detection and correction. A 4-byte ECC code is added to the end of DATA area. A generation polynominal G(x) of ECC is as follows (the initial value is fixed to "00").

$$G(x) = (x^{21} + 1)(x^{11} + x^2 + 1)$$
$$= x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$$

CRC enables error detection, but not error correction. A 2-byte CRC code is added to the end of DATA area. A generation polynominal G(x) of CRC is specified by the CRCP bit.

(6) CRCP (CRC Polynominal) bit

This bit determines the polynominal G(x) that generates CRC of ID and DATA areas when ECD = 0.

CRCP = 1: $G(x) = x^{16} + x^{12} + x^5 + 1$
CRCP = 0: $G(x) = x^{16} + 1$

(7) CRCI (CRC Initial) bit

This bit sets the initial value of CRC.

CRCI = 1: Initial value = $FFFF
CRCI = 0: Initial value = $0000

(8) ACOR (Automatic Correction) bit

This bit selects whether or not the HDC will automatically correct an error detected in DATA area during RD command execution.

ACOR = 1: Automatic correction is performed.
ACOR = 0: Automatic correction is not performed.

Automatic correction mode is valid when ECC is specified as the error check code of DATA area and the sector length is 256 bytes (RL = $01, ECD = 1). For any other cases specify "0" to the ACOR bit.

OM1 (Operation Mode 1)

(1) DTM (Data Transfer Mode) bit

This bit is used to specify data transfer operation between the HDC and the main memory during the execution of the following commands:

RD	RED	RID
RIS	FID	WD
CMPD	WFM	WFS

These commands normally perform transfer between drive and memory via HDC data buffers. However, it is possible to cease transfer between the HDC and memory during these command execution by utilizing DTM bit.

DTM = 1: DMA mode
DTM = 0: PIO mode

In DMA mode, the HDC performs transfer between drive and memory via HDC data buffer. In this case, DMA transfer is performed between the HDC and memory, and transfer mode is specified by BRST bit.

In PIO mode, the HDC performs transfer between drive and the HDC. In this case, transfer between the HDC and main

memory must be supported by the host system using one of four buffer access commands of the HDC: MTB, BTM, OPBR, and OPBW.

(2) BRST (DMA Burst) bit
This bit specifies DMA transfer mode of buffer access commands and drive access commands which perform transfer between the HDC and the main memory.

BRST = 1: Burst mode
BRST = 0: Cycle Steal mode

(3) CEDM, SEDM, DERM bits
CEDM (Command End Mask), SEDM (Seek End Mask), and DERM (Drive Error Mask) bits specify whether the $\overline{IRQ}$ signal is to be asserted or not. CEDM, SEDM, and DERM correspond to CED (Command End), SED (Seek End), and DER (Drive Error) bits in STR (Status register).

1: $\overline{IRQ}$ is masked (not asserted).
0: $\overline{IRQ}$ is not masked (asserted).

Mask bit	Corresponding bits in STR	
CEDM	CED	bit 5
SEDM	SED	bit 4
DERM	DER	bit 3

(4) AMEX (Address Mark Excluded) bit
This bit specifies whether or not the byte-synchronization pattern marking the beginning of ID area or DATA area (AM in soft sector, SYNCPAT in hard sector) is to be included in the CRC or ECC error detection span. The AMEX bit affects the byte length of ID PAD area and DATA PAD area.

	AM or SYNCPAT	PAD Length
AMEX = 1	Excluded	2 bytes
AMEX = 0	Included	3 bytes

(5) PSK (Parallel Seek) bit
This bit specifies seek operation mode, and is valid only in ST506 interface (in SMD interface, PSK must be fixed to "1"). The HDC specifies step pulse issue timing by utilizing the value of OM2, SH, and PSK bits.

PSK = 0: Normal Seek mode
PSK = 1: Parallel Seek mode

In Normal Seek mode, the HDC issues step pulses in long cycle (0.1–32 ms). SEK and RCLB command execution ends when the HDC issues step pulses and then detects seek end.

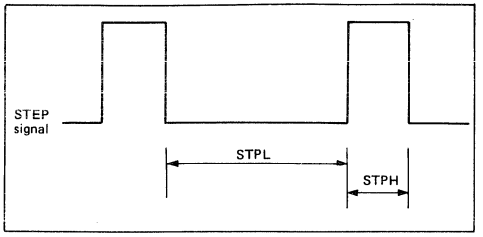
In Parallel Seek mode, the HDC issues step pulses in short cycle (0.5–115 μs). SEK and RCLB command execution ends when the HDC issues step pulses. Since the HDC does not check the seek end, parallel seek operation in multiple drives is realized by issuing SEK or RCLB command to these drives. Seek end is to be checked by using POL command.

OM2 (Operation Mode 2)
This 8-bit register specifies step pulse low width in ST506 interface, and specifies drive control output signal during disk read command execution in SMD interface.

In ST506 interface, OM2 indicates SL which specifies step pulse low width (STPL: Step Pulse Low). Low-speed seek mode (Normal Seek mode) is selected when PSK = 0, and high-speed seek mode (Parallel Seek mode) is selected when PSK = 1. Highest seek speed is realized when PSK = 1 and SL = $FF. The relation between step pulse low width and SL is shown in the following table (see Step Pulse High/Record Length register to specify step pulse high width).

7	6	5	4	3	2	1	0
Step Pulse Low (SL)							

Seek Mode	SL	STPL (step pulse low)
Normal seek (PSK = 0)	SL = $00	STPL = 988 CLK
	$01 ≦ SL ≦ $FE (1) (254)	STPL = (SL − 1) x 1280 + 2364 CLK (2364 CLK ≦ STPL ≦ 326204 CLK)
	SL = $FF	Disabled
Parallel seek (PSK = 1)	SL = $00	STPL = 27CLK
	$01 ≦ SL ≦ $FE (1) (254)	STPL = SL x 6 + 28 CLK (34CLK ≦ STPL ≦ 1152 CLK)
	SL = $FF	STPL = 5CLK



In SMD interface, OM2 specifies drive control output signal from the HDC during data read command execution. In data write command (all the commands that assert WGATE signal) and SEK, RCLB command execution, outputs of drive control signals are low regardless of the contents of OM2. Bits 4–7 in OM2 are to be set to "0".

SOFM bit: With SOFM = 1, the drive head is offset from the normal position away from the spindle.
SOFP bit: With SOFP = 1, the drive head is offset from the normal position towards the spindle.
STBL bit: With STBL = 1, the data from the drive PLO data separator is strobed later than usual.
STBE bit: With STBE = 1, the data from the drive PLO data separator is strobed earlier than usual.

7	6	5	4	3	2	1	0
0	0	0	0	SOFM	SOFP	STBL	STBE

Strobe Early
Strobe Late
Servo Offset Plus
Servo Offset Minus

CUL (Connecting Unit List)
This register stores bit-map information indicating which drive is connected to the HDC.

In ST506 interface, bits 0–3 correspond to drives 0–3 respectively. To connect a drive, write "1" into the corresponding bit (up to 4 drives can be connected).

7	6	5	4	3	2	1	0
0	0	0	0				

Drive Unit 0
Drive Unit 1
Drive Unit 2
Drive Unit 3

In SMD interface, bits 0–7 correspond to drives 0–7 respectively. To connect a drive, write "1" into the corresponding bit (up to 8 drives can be connected).

7	6	5	4	3	2	1	0

Drive Unit 0
Drive Unit 1
Drive Unit 2
Drive Unit 3
Drive Unit 4
Drive Unit 5
Drive Unit 6
Drive Unit 7

TO/NCH, NCL (Read/Write Time Over, Number of Cylinders High/Low)
NCH and NCL registers specify the number of cylinders in disk drive, and time-over during disk access command execution.

(1) TO (Read/Write Time Over)
The high-order 6 bits in TO/NCH are used to assign the ID search time: time-over (t_{over}). According to the value of TO, the HDC sets time-over period as follows.
$01 ≦ TO ≦ $3F (TO = $00 is prohibited.)
$TO \times 8 \times 10^4$ CLK ≦ t_{over} ≦ $(TO + 1) \times 8 \times 10^4$ CLK

(2) NC (Number of Cylinders)
The low-order 2 bits of TO/NCH and 8 bits of NCL specify the number of cylinders (NC). NC is 1023 at a maximum. Its value is number of cylinders minus 1.

The HDC uses NC to issue NC + 10 step pulses during RCLB command execution (ST506 interface), or to check whether or not the command parameter NCA (Next Cylinder Address) exceeds NC during SEK command execution.

15	14	13	12	11	10	9	8
Read/Write Time Over						NCH	

Number of Cylinders High

7	6	5	4	3	2	1	0
Number of Cylinders Low							

NH (Number of Heads)
This register indicates the number of heads. Its value is to be number of drive heads minus 1.

In disk access command execution, the HDC checks whether or not PHA (Physical Head Address) specified by command parameters exceeds NH. When PHA exceeds NH, the HDC sets IPH (Invalid Physical Head Address) to result parameter SSB (Sense Status Byte) and abnormally terminates the execution.

To select a head during multiple track operation in disk access command execution, the HDC checks whether PHA exceeds NH or not. When PHA exceeds NH, the HDC sets IPH to SSB and abnormally terminates the execution.

7	6	5	4	3	2	1	0
Number of Heads							

In ST506 interface, up to 8 heads can be selected ($00 ≦ NH ≦ $07). Bits 3–7 must be fixed to "0".

7	6	5	4	3	2	1	0
0	0	0	0	0	2^2	2^1	2^0

In SMD interface, up to 32 heads can be selected ($00 ≦ NH ≦ $1F). Bits 5–7 must be fixed to "0".

7	6	5	4	3	2	1	0
0	0	0	2^4	2^3	2^2	2^1	2^0

NS (Number of Sectors)
This register indicates the number of sectors. Its value is number of sectors/track minus 1 ($00 ≦ NS ≦ $FE).

In data read/write command execution, the HDC checks whether LSA (Logical Sector Address) exceeds NS or not.

In multiple sector operation in data read/write command execution, the HDC checks whether LSA exceeds NS or not each time LSA is incremented after one sector operation. If LSA exceeds NS, the HDC sets "0" to LSA, increments LHA and PHA, and compares NH and PHA. If NH exceeds PHA, the HDC executes multiple track operation. If PHA exceeds NH, the HDC sets IPH (Invalid Physical Head Address) to result parameter SSB and abnormally terminates the execution.

7	6	5	4	3	2	1	0
Number of Sectors							

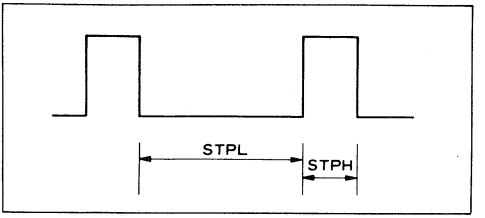
SH/RL (Step Pulse High/Record Length)

7	6	5	4	3	2	1	0
Step Pulse High (SH)					Record Length (RL)		

(1) SH (Step Pulse High)
The high-order 5-bit SH/RL indicates step pulse high width (STPH: Step Pulse High) in ST506 interface.

STPH is fixed to 2CLK in highest speed seek mode (PSK = 1 and SL = $FF). Otherwise, SH sets STPH regardless of the PSK bit. The relation between STPH and SH is shown in the following table. SH is ignored when maximum speed seek mode is selected in ST506 interface.

In SMD interface, the high-order 5 bits are to be fixed to "0".



SH	STPH (step pulse high)
SH = * * : don't care	STPH = 2 CLK (Note 1)
SH = $00	STPH = 3 CLK
$01 ≦ SH ≦ $1F (1) (31)	STPH = SH x 3 + 1 CLK (4 CLK ≦ STPH ≦ 94 CLK)

(Note 1) Highest-speed seek mode (PSK = 1, SL = $FF)

(2) RL (Record Length)
The low-order 3-bit SH/RL indicates record length per sector.

RL			Record Length
Bit 2	Bit 1	Bit 0	
0	0	0	Inhibited
0	0	1	256 bytes
0	1	0	512 bytes
0	1	1	1024 bytes
1	0	0	2048 bytes
1	0	1	4096 bytes
1	1	0	Inhibited
1	1	1	Inhibited

GPL1, 2 (Gap Length 1, 2)
These registers specify the length of gap and SYNC area in the sector during WD and WFM command execution.

GPL1 specifies the length of gap areas (GAP1 in soft sector, HEAD SCAT in hard sector) that follow an index or a sector pulse by byte. It is used for WFM command execution. These areas are formatted 6 bytes longer than the value set to GPL1 during the command execution. [$00 ≦ GPL1 ≦ $FF]

7	6	5	4	3	2	1	0
Gap Length 1							

GPL2 specifies the length of SYNC area located at the beginning of ID and DATA areas by byte. It is used for WD and WFM commands. This area is formatted 3 bytes longer than the value set to GPL2 during the command execution. [$08 ≦ GPL2 ≦ $FF]

7	6	5	4	3	2	1	0
Gap Length 2							

GPL3/RGTLT (Gap Length 3, Read Gate Latency)

GPL3/RGTLT specifies the length of GAP3 for the soft sector and read gate latency delay for the hard sector by byte.

GPL3 specifies the length of GAP3 located at the end of a sector in soft sector format by byte. It is used for WFM command. This area is formatted 3 bytes longer than the value set to GPL3. [$09 ≦ GPL3 ≦ $FF]

7	6	5	4	3	2	1	0
Gap Length 3							

RGTLT specifies the time period between the detection of an index or a sector pulse and the assertion of RGATE in unit of byte. It is used for disk read commands. RGATE is asserted 5 bytes later than the value set to RGTLT. RGTLT must be set to assert RGATE at the beginning of or before PLO SYNC area in the ID field. During RIS command execution, 64 bytes are added to the amount of latency automatically. [$00 ≦ RGTLT ≦ $FF]

7	6	5	4	3	2	1	0
RGATE Latency							

LCCH, LCCL (Low Current Cylinder High/Low)

For the inner cylinders of the drive, it is necessary to reduce write current during WFM and WD command execution. These registers specify address of the outermost cylinder from where write current is reduced. This is valid only in ST506 interface. When a disk write command is executed to any cylinder whose address is equal to or greater than LCC, the HDC asserts the LCT pin to high. [$0000 ≦ LCC ≦ NC (Number of Cylinders)]

15	14	13	12	11	10	9	8
Low Current Cylinder High							

7	6	5	4	3	2	1	0
Low Current Cylinder Low							

PCC (Precompensation Cylinder)

This register specifies the address of the outermost cylinder from where compensation of the bit data timing is required. This is valid only in ST506 interface. When a disk write command is executed to any cylinder whose address is equal to or greater than PCC, either EARLY or LATE signal is generated in accordance with the bit data timing. [$0000 ≦ PCC ≦ NC]

15	14	13	12	11	10	9	8
Pre-compensation Cylinder High							

7	6	5	4	3	2	1	0
Pre-compensation Cylinder Low							

OTHER COMMAND PARAMETERS

The following describes command parameters other than SPC command parameters in alphabetical order.

(1) FLAG

This parameter is used to specify the FLAG byte of ID area of a hard sector that the HDC will access. If the FLAG given by the command parameter does not match the FLAG read from ID area of the disk, the HDC will not access the sector.

(2) LCA (Logical Cylinder Address)

This parameter is used to specify the logical cylinder address of ID area (16 bits: the high-order 8 bits for LCAH and the low-order 8 bits for LCAL) of a sector that the HDC will access. If LCA given by the command parameter does not match LCA read from ID area, the HDC will not access the sector. In soft sector format, it is prohibited to specify $F8 to the high-order 8 bits (LCAH).

(3) LHA (Logical Head Address)

LHA is used to specify the logical head address of ID area of a sector that the HDC will access. If LHA given by the command parameter does not match the LHA read from ID area, the HDC will not access that sector. In multiple track operation, LHA is automatically incremented by one. Since LHA is logical, it may exceed the number specified by the parameter NH (number of heads).

(4) LSA (Logical Sector Address)

LSA is used to specify the logical sector address of ID area that the HDC will access. If LSA given by the command parameter does not match LSA read from ID area, the HDC will not access the sector. In multiple sector operation, LSA is automatically incremented by one. Since LSA is compared with the control register NS (number of sectors) for switching of heads, the LSA must not exceed the NS.

(5) NCA (Next Cylinder Address)

This parameter is used to specify the physical address (10 bits) of a cylinder to which the head will move when a SEK command is issued. The outermost cylinder address is $0000. The high-order 8 bits of NCA are used for NCAH and the low-order 8 bits for NCAL. The high-order 6 bits of NCAH must be fixed to "0". If NCA exceeds NC, com-

mand execution abnormally terminates.

(6) OFFSET
OFFSET specifies how many sectors to be skipped reading after an index pulse. Then the HDC reads ID fields, and stores them into the data buffer.

(7) PHA (Physical Head Address)
The MPU specifies PHA when issuing a disk access command. Unlike LHA, PHA is physical, and the bit status of PHA is directly output as HSEL signals. The high-order 5 bits of PHA must be fixed to "0" for ST506 interface, and the high-order 3 bits for SMD interface. In multiple track operation, PHA is automatically incremented by one within the HDC if another head switching is required. If PHA exceeds the value given by NH, the command execution will abnormally terminate.

(8) POFF (Pointer Offset)
The MPU specifies a transfer start address (16 bits) when issuing a command for accessing the data buffer. The MSB of the high-order 8 bits (POFFH) selects one of two data buffers, and the remaining 7 bits must be fixed to "0". The low-order 8 bits (POFFL) specifies a transfer start address of the selected data buffer (256 bytes). For the 16-bit data bus, POFF is limited to an even address only.

(9) PSA (Physical Sector Address)
This parameter is used to specify a physical address of a hard sector at which the execution of RID, RIS, FID, WFM, or WFS starts. If PSA is $00, the sector following an index pulse is specified.

(10) SCNT (Sector Count)
This parameter is used to specify the number of sectors (16 bits) that the HDC will continuously access in a disk access command execution. Upper 8 bits are SCNTH, and lower 8 bits are SCNTL. Up to 1024 sectors are specified in ST506 interface (128 sectors x 8 heads), and up to 8160 sectors are specifiable in SMD interface (255 sectors x 32 heads). For commands relating to the ID (RID and WFM), they perform no multiple track operation. In addition, maximum number of sectors that can be formatted at a time by WFM command is 128 for soft sector, and 102 for hard sector.

(11) US (Unit Select)
The MPU specifies the address (8 bits) of a target drive when issuing a head positioning, disk access or drive check command. The contents of US are directly output from USEL signals. The high-order 6 bits of US must be fixed to "0" for ST506 interface, and the high-order 5 bits for SMD interface. US is the high-order 8 bits of a 16-bit word, and the low-order 8 bits of the word are PHA or $00. It is not necessary to issue $00 to the low-order 8 bits when CKV or RCLB command is issued.

RESULT PARAMETERS

Result parameters are listed in Table 9. In this table, result parameters used by the HDC to control ST506 type hard disk drive are found in the upper row of each command, and those for SMD type in the lower row.

Table 9 Result Parameters (Byte-organized)

Command	Parameter (Upper row: ST506 / Lower row: SMD)
Recalibrate	$00 SSB US VUL $00 SSB US VUL
Specify	($00 SSB) ($00 SSB)
Seek	$00 SSB US VUL $00 SSB US VUL
Read Data	$00 SSB US PHA LCAH LCAL LHA LSA SCNTH SCNTL $00 SSB US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Read Erroneous Data	$00 SSB US PHA SCNTH SCNTL $00 SSB US PHA $00 PSA SCNTH SCNTL
Read ID Read ID Skew (Note 1)	$00 SSB US PHA $00 SCNTL $00 SSB US PHA $00 PSA $00 SCNTL
Find ID	$00 SSB US PHA $00 SCNTL $00 SSB US PHA $00 PSA $00 SCNTL
Check Data	$00 SSB US PHA LCAH LCAL LHA LSA SCNTH SCNTL $00 SSB US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Compare Data	$00 SSB US PHA LCAH LCAL LHA LSA SCNTH SCNTL $00 SSB US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Write Data	$00 SSB US PHA LCAH LCAL LHA LSA SCNTH SCNTL $00 SSB US PHA $00 FLAG LCAH LCAL LHA LSA SCNTH SCNTL
Write Format Write Format Skew (Note 1)	$00 SSB US PHA SCNTH SCNTL $00 SSB US PHA $00 PSA SCNTH SCNTL
Memory to Buffer	($00 SSB) ($00 SSB)
Buffer to Memory	($00 SSB) ($00 SSB)
Open Buffer Read	($00 SSB) ($00 SSB)
Open Buffer Write	($00 SSB) ($00 SSB)
Polling	$00 SSB US VUL $00 SSB US VUL
Check Drive	$00 SSB US $00 DST0 $00 $00 SSB US $00 DST0 DST1 DST2 DST3
Abort	$00 SSB $00 SSB
Check ECC	$00 SSB EA0 EA1 EP0 EP1 EP2 $00 $00 SSB EA0 EA1 EP0 EP1 EP2 $00
Test	($00 SSB) ($00 SSB)
Polling Disable	($00 SSB US VUL) ($00 SSB US VUL)
Recall	($00 SSB US VUL) ($00 SSB US VUL)

(Note 1) Read ID Skew and Write Format Skew are valid only for SMD.
(Note 2) Parenthesized parameters are reported when a command is issued under the illegal condition.

DST (Drive Status)

Table 10 Drive List (DST)

Bit		7	6	5	4	3	2	1	0
ST506	DST0	READY	SCP	TRK0	0	WFLT	0	0	0
SMD	DST0	*	*	*	WPRT	FLT	SKERR	OCYL	URDY
	DST1	*	*	SELER	WERR3	WERR2	WERR1	SERR2	SERR1
	DST2	*	*	SAD32	SAD16	SAD8	SAD 4	SAD 2	SAD 1
	DST3	*	*	DTP32	DTP16	DTP8	DTP4	DTP2	DTP1

*: Depends on the state of BUS_1/BUS_6 – BUS_4/BUS_9.

Each bit of DST indicates drive interface input signal level. DST0 (1 byte) is reported in ST506 interface, and DST0–3 (4 bytes) are reported in SMD interface.

In ST506 interface, the WFLT bit in DST0 indicates the signal level of WFLT pin. Even if WFLT signal is momentarily asserted, the internal latch memorizes this and reflects its state on WFLT bit. When WFLT signal is negated, the latch read operation by the HDC clears this latch.

In SMD interface, the HDC reads 8 bits by 4 words of the drive status signal which is selected by signals TAG2 and TAG5.

TAG2	TAG5	Status
0	0	DST0
0	1	DST1
1	0	DST2
1	1	DST3

Following (1) through (5) are read during CKV command execution and checked during disk access command execution. DST1 through DST3 are referred to during CKV command execution.

Status that each bit in DST1–3 indicates may vary according to the drive connected to the HDC. Following descriptions indicate DST bit function when the HDC is connected to a Hitachi 8″ disk drive, DK-812S.

(1) URDY (Unit Ready)
This bit indicates that a selected drive is in ready state.

(2) OCYL (On Cylinder)
This bit indicates that a head is positioned correctly on a track.

(3) SKERR (Seek Error)
This bit indicates that errors have been detected in a drive during seek operation.

(4) FLT (Fault)
This bit indicates that errors relevant to disk access have been detected in the drive. Result parameter DST1 indicates what type of error has occurred. See (6) through (11) for DST bits indicating error status.

(5) WPRT (Write Protected)
This bit indicates that a selected drive is write protected.

(6) SERR1 (Status Error 1)

(7) SERR2 (Status Error 2)

(8) WERR1 (Write Error 1)

(9) WERR2 (Write Error 2)

(10) WERR3 (Write Error 3)

(11) SELER (Select Error)

(12) SAD1–32 (Sector Address)

(13) DTP1–32 (Drive Type)

EA (Error Address)
Reports the start address (16 bits) of a byte from where the burst error that is detected during CKE command execution exists. The high-order 8 bits are EA0, and the low-order 8 bits are EA1. As the HDC corrects up to 11 bits of burst error, the MPU corrects contiguous 3 bytes starting from a byte specified by EA. EA = $0000 indicates a start address of sector data.

EP (Error Pattern)
Reports EP0, EP1, and EP2 as the pattern required for error correction as a result of CKE command execution. The MPU exclusive-OR 3-byte data containing errors with EP0, EP1, and EP2.

FLAG (Flag)
Reports the same value as FLAG specified by command parameters.

LCA (Logical Cylinder Address)
Reports the same value as LCA specified by command parameters.

LHA (Logical Head Address)
Bit organization of LHA is the same as that of the command parameter LHA. In multiple track operation, LHA is incremented by one each time access to one track ends.

LSA (Logical Sector Address)
Bit organization of LSA is the same as that of the command parameter LSA. In multiple sector operation, LSA is incremented by one each time access to one sector ends.

PHA (Physical Head Address)
Bit organization of PHA is the same as that of the command parameter PHA. In multiple track operation, PHA is incremented by one each time access to one track ends.

PSA (Physical Sector Address)
Bit organization of PSA is the same as that of the command parameter PSA. In multiple sector operation, PSA is incremented by one each time access to one sector ends.

SCNT (Sector Count)
Bit organization of SCNT is the same as that of the command parameter SCNT. In multiple sector operation, SCNT is decremented by one each time access to one sector ends. When SCNT reaches "0", command execution normally terminates.

SSB (Sense Status Byte)
This is the area where 8-bit error code is set ($00 is set for normal termination). There are 25 error codes which notify what kind of error has occurred during the command execution (see tables 11–14).

US (Unit Select)
Reports the same value as US specified by command parameters.

VUL (Valid Unit List)
VUL is a bit-mapped list which gives the address of a drive that is ready to accept a head positioning or a disk access command. Its bit organization is the same as that of CUL. This bit is set when seek operation in the drive is terminated, or when SPC command is executed. This bit is reset when seek operation starts, when drive error occurs, or when the bit in CUL corresponding to the drive is not set to "1".

Table 11 Error Codes Relevant to Host Interface

Mnemonic	Name	Error Code	Contents
ABT	Command Aborted	04	ABT command has been accepted.
IVC	Invalid Command	08	An invalid command has been accepted.
PER	Parameter Error	0C	The command parameter has not been stored in an appropriate area in PB.
NIN	Not Initialized	10	Head positioning, disk access, and drive check commands have been accepted, before SPC command is executed.
RTS	Rejected Test	14	The TST command is received after SPC command has been received.

Table 12 Error Codes Relevant to Drives

Mnemonic	Name	Error Code	Contents
NUS	No USELD	18	USELD signal for a selected drive has not been returned.
WFL	Write Fault	1C	WFLT signal (ST506 interface) or FLT signal (SMD interface) has been detected.
NRY	Not Ready	20	READY signal has been negated.

Table 13 Error Codes Relevant to Head Positioning Commands

Mnemonic	Name	Error Code	Contents
NSC	No SCP	24	SCP signal (ST506 interface) or the SKEND signal (SMD interface) has not been returned in a certain period.
ISE	In Seek	28	SEK, or a disk access command has been issued for a drive in seek operation.
INC	Invalid NCA	2C	NCA (Next Cylinder Address) greater than NC (number of cylinders) has been specified.
ISR	Invalid Step Rate	30	The highest-speed seek has been specified in the normal seek mode.
SKE	Seek Error	34	SEK or a disk access command has been issued to a drive which is in seek error state (SMD only).

Table 14 Error Codes Relevant to Disk Read/Write Commands

Mnemonic	Name	Error Code	Contents
OVR	Over Run	38	A transfer between the main memory and data buffers has not caught up with a transfer between a drive and data buffers.
IPH	Invalid PHA	3C	PHA (Physical Head Address) greater than NH (Number of Heads) has been specified.
DEE	DATA Field ECC Error	40	A data error has been detected by ECC (Error Correction Code).
DCE	DATA Field CRC Error	44	A CRC (Cyclic Redundancy Check Code) error has occurred in DATA area.
ECR	Error Corrected	48	An ECC error detected in DATA area has been automatically corrected.
DFE	DATA Field Fatal Error	4C	A fatal ECC error has occurred in DATA area.
NDA	No DATA AM	60	The address mark in DATA area has not been detected.
NHT	Not Hit	50	In CMPD command execution, data from the host and disk data have not coincided with each other.
ICE	ID Field CRC Error	54	A CRC error in ID area has been detected in RID command execution in SMD interface.
TOV	Time Over	58	ID has not been found in the period specified by TO (Time Over).
NIA	No ID AM	5C	The ID area that begins with improper address mark has been detected.
NWR	Not Writable	64	WD command has been issued to a drive where the write protect signal is asserted (SMD interface)

CONTROL SEQUENCE FOR ST506 TYPE DRIVE

DISK READ

The ID search timing for RD or WD command execution is shown in figure 27. (a) is the timing where AM is found. SYNC signal is negated 4-bit period (on the basis of disk data) after CRC pattern of ID area is completed. After reading CRC, the HDC switches the clock in the satellite processor from RCLK to WCLK and then negates SYNC signal.

RCLK and WCLK clock signals are independent each other. To remove the hazard during switching, the switching signal and the clock signal must be synchronized. Therefore, SYNC is normally negated 4-bit period after reading CRC to switch the clock in the satellite processor from RCLK to WCLK.

RGATE signal is usually negated 4-bit period after SYNC signal is negated, and then asserted again one to two-byte period later to read SYNC area preceding DATA area. RGATE is asserted for 1-byte period when the AMEX bit is set to "1" during SPC command execution, and for 2-byte period when set to "0".

When AM is not found as shown in (b), the HDC searches for AM again by negating both SYNC and RGATE signals. RGATE signal is usually negated 4-bit period after SYNC signal is negated, and is negated for 2-byte period.

As the MFM is specified during SPC command execution, the frequency of clock signals synchronizing with disk data (such as RCLK, WCLK) is doubled compared to the data transfer rate. Therefore, "4-bit period" or "1-byte period" description is formally expressed as "8 WCLK cycles" or "16 WCLK cycles" respectively.

After reading DATA area and ECC or CRC area by RD command execution, RGATE and SYNC signals are negated in the same timing as they are negated after reading ID CRC area (see figure 27 (a)).

DISK WRITE

The timing of WGATE signal for WD command execution is shown in figure 28. The HDC negates RGATE signal after reading ID area. Then WGATE signal is asserted 1 or 2-byte period after RGATE is negated (2-byte when AMEX specified by SPC command is at "0", 1-byte when AMEX is at "1"). WGATE signal is negated immediately after PAD of DATA field ends.

The relation between IDX signal and WGATE signal during WFM command execution is shown in figure 29. WGATE signal rises almost simultaneously with IDX signal (refer to electrical characteristics), and falls 3-byte or 4-byte period after IDX signal rises. The condition of EARLY and LATE signal generation is shown in figure 8.

HEAD POSITIONING

The relation between DIR, STEP, and SEEK signals is shown in figure 30. The unit is the number of CLK cycles (t_{cyc}).

When 8 MHz clock signal is supplied to CLK, STEP signal is output at least 33.8 μs after DIR signal becomes valid.

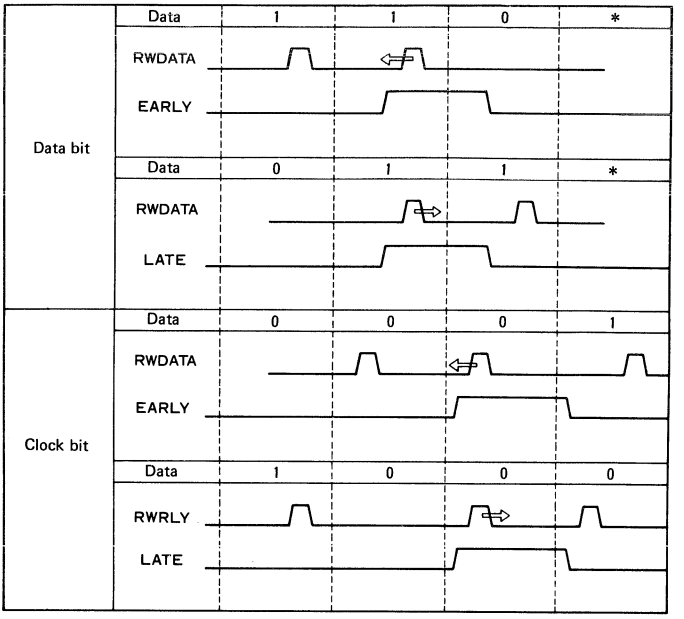


Figure 8 Write Precompensation

CONTROL SEQUENCE FOR SMD TYPE DRIVE

DRIVE SELECTION, STATUS CHECK, FAULT CLEAR

The HDC performs drive selection, status check, and Fault Clear, for all disk control command execution. Figure 35 shows the drive selection timing. The drive receives $BUS_0/BUS_5 - BUS_4/BUS_9$ from the HDC and latches them using UTAG signal. If the drive judges that its own drive number is specified, it returns USELD signal within 9 CLK after the detection of UTAG signal. Figure 36 shows the drive status check sequence. The HDC changes the direction of $BUS_0/BUS_5 - BUS_4/BUS_9$ before reading the status. Then the HDC sets BUSL/$\overline{H}$ signal to high, therefore, the external circuit of the HDC can supply drive status signal to the HDC during this period. At this time, BUSL/$\overline{H}$ is in high, and lower 5 bits are input to the HDC.

The HDC resets FLT after reading the drive status which includes Fault, and the timing is shown in figure 37. To set the high-order 5 bits of BUS outputs to low, the HDC sets $BUS_0/BUS_5 - BUS_4/BUS_9$ to low, and asserts TAG3 signal with maintaining BUSL/$\overline{H}$ in low. In external circuits of the HDC, $BUS_0/BUS_5 - BUS_4/BUS_9$ is latched by using TAG3 signal as a strobe signal. If BUSL/$\overline{H}$ is in low, external circuits must be used not to supply TAG3 signal of the HDC to the drive. Then, the HDC outputs the low-order 5-bit information to $BUS_0/BUS_5 - BUS_4/BUS_9$, sets BUSL/$\overline{H}$ signal to high, and asserts TAG3 signal. The external circuits provide the drive with above mentioned 5-bit latch outputs, the low-order 5-bit outputs on $BUS_0/BUS_5 - BUS_4/BUS_9$, and TAG3. In Fault Clear, BUSL/$\overline{H}$ signal is in high, and only BUS_4/BUS_9 is in high.

Head selection is performed by disk access commands. Figure 40 shows the head selection timing. Upper 5 bits are in low, and the head address is supplied from the low-order 5 bits of BUS. At this time, TAG2 signal is used as a strobe signal.

Further, in the execution of disk access command group, the HDC asserts TAG3 and generates RGATE or WGATE signal. Figures 41, 42 and 43 show the total sequence. When TAG3 is asserted, the high-order 5 bits of BUS output Strobe Early/Late and RTZ (it is not used for disk access). Then, the HDC outputs the low-order 5 bits. Servo offset is specified in figure 42. When TAG3 is asserted along with BUS_2/BUS_7 or BUS_3/BUS_8, servo offset is performed in the drive. Therefore, the head is moved and the HDC waits until SKEND signal is returned from the drive. Then, the HDC asserts BUS_1/BUS_6 and supplies RGATE signal to the drive to perform the read operation.

Figure 43 shows assert/negate timing of RGATE and WGATE signals which correspond to the disk format. During disk access command or ID read command execution, RGATE signal is

asserted after a time period corresponding to byte count of disk data has elapsed since IDX or SEC signal is detected. After reading CRC, the HDC itself switches the clock to WCLK signal, then negates RGATE signal with a typical delay time equivalent to 8 bits of disk data.

To read the data field, the HDC asserts RGATE again with a dwell time of 1–2 bytes period. RGATE is negated for 1-byte period when AMEX bit is set to "1" during SPC command execution, and 2-byte period when AMEX bit is set to "0". The HDC negates RGATE signal 8-bit period after reading CRC or ECC in data field.

To write the DATA field, the HDC reads ID area and asserts WGATE signal 1–2 bytes period after RGATE signal is negated. WGATE signal is to be negated when DATA PAD ends. During WFM command execution, WGATE signal rises in the same timing as IDX signal, and is negated 3–4 bytes period after IDX or SEC signal is detected.

Figure 38 shows the execution timing of RCLB command. RTZ instruction is supplied to the drive through BUS_1/BUS_6 and TAG3. Figure 39 shows the execution timing of SEK command. 10-bit cylinder address is output through $BUS_0/BUS_5-BUS_4/BUS_9$, 5 bits at a time. Strobe signal is TAG1 at this time.

Figures 44, 45, 46 and 47 shows the execution timing of CKV command. The HDC reads 8-bit drive status through $BUS_0/BUS_5-BUS_4/BUS_9$, 3 bits first and then 5 bits. Then the HDC reads status four times by switching TAG2 and TAG5 signals. Switching order is: [TAG2 = 0, TAG5 = 1], [TAG2 = 0, TAG5 = 1], [TAG2 = 1, TAG5 = 0], [TAG2 = 1, TAG5 = 1].

COMMON CONTROL

The control which is common to both ST506 and SMD interfaces is described in this section.

AUTOMATIC CORRECTION

In SPC command execution, the HDC operates in automatic correction mode if the host sets both ECD and ACOR bits in OM0 to "1". If a sector with correctable errors is detected, the erroneous data is corrected in data buffers. Automatic correction is normally performed only when the sector length is 256 bytes. Specification of the automatic correction mode is prohibited when the sector length is longer than 512 bytes because it causes the erroneous operation of the HDC.

If DTM (Data Transfer Mode) bit in OM0 is set to "1" as well as ECD and ACOR bits during SPC command execution, the HDC transfers the corrected data to the main memory in DMA mode after the automatic correction. Then, the command execution abnormally terminates. When DTM = 0, the command execution abnormally terminates after the automatic correction and data transfer is not performed. If the HDC finds the data uncorrectable, the command execution abnormally terminates without data transfer regardless of the state of DTM bit.

CORRECTION BY HOST

The host corrects erroneous data detected during RD command execution when it sets ECD and ACOR bits in OM0 to "1" and "0" respectively. When ECD bit is set to "1", the host corrects erroneous data detected during RED command execution if necessary, regardless of the status of ACOR bit. The command execution abnormally terminates when erroneous data is detected during any command execution. Then $40 is set to SSB when an error is correctable, $4C when not correctable.

When DTM = 1, the HDC sends 1-sector data including an error during RD or RED command execution and then abnormally terminates the command execution. After confirming that $40 is set to SSB, the host issues CKE command to the HDC.

When DTM = 0, the HDC abnormally terminates the command execution after 1-sector data including an error is stored in the data buffer during RD or RED command execution. After confirming that $40 is set to SSB, the host issues BTM command to the HDC after DMAC's initialization, or, issues OPBR command and reads data buffers using move and load instructions and then stores buffer data to the main memory. Then, the host issues CKE command to the HDC.

Receiving CKE command, the HDC calculates an error address (EA) and an error pattern (EP), and then sends result parameters to the host. The erroneous data exists in three contiguous bytes of the corresponding sector in main memory. EA indicates start address of this 3-byte area ($0000 indicates a start address of sector data). The host exclusive-OR the 3-byte area and EP to correct erroneous data.

The host judges CKE command execution end from status change of BSY bit from "1" to "0". When SSB is $4C, CKE command issue is prohibited as it causes the erroneous operation of the HDC. Even if errors are reported to be correctable (SSB = $40) during RD or RED command execution and the host issues CKE command, these errors may turn out to be not correctable after CKE command execution.

DMA DATA TRANSFER

In DMA data transfer, the HDC selects one of two modes: Burst mode and Cycle Steal mode. DMA transfer mode is specified by BRST (burst) bit which is a command parameter of SPC command.

In Burst mode (BRST = 1), the HDC maintains $\overline{\text{DREQ}}$ signal at low level until data transfer is terminated. $\overline{\text{DREQ}}$ signal is negated when $\overline{\text{DONE}}$ signal is input synchronously with $\overline{\text{DACK}}$ signal, or when DMA transfer of data in 256-byte internal data buffer is finished.

In Cycle Steal mode (BRST = 0), the HDC asserts $\overline{\text{DREQ}}$ signal until $\overline{\text{DACK}}$ signal is asserted. The HDC negates $\overline{\text{DREQ}}$ signal when $\overline{\text{DACK}}$ signal assertion is detected. $\overline{\text{DREQ}}$ signal will be reasserted if $\overline{\text{DACK}}$ is negated and the HDC has the transfer request. The DMA transfer conditions of Cycle Steal mode are the same as those of Burst mode.

DATA TRANSFER IN HOST INTERFACE

DMA Data Transfer in Disk Access

DMA data transfer mode, either Burst mode or Cycle Steal mode, is selected by BRST bit specified by SPC command. Figure 9 shows DMA data transfer sequence during RD and RED command execution. For 256-byte sector, (a) shows the case that the host computer reads the disk data from data buffers (DBUF0 and DBUF1) by DMA at a high speed. The capacity of two data buffers is 256 bytes for each.

If data buffers are not provided, most of high-speed host bus is occupied by transferring drive data during low-speed reading of drive data.

Internal data buffers can separate high-speed host bus timing and low-speed drive data timing, which effectively shorten drive data transfer time in host bus. Therefore, host system throughput is notably improved. The data transfer from data buffers to the main memory is performed only when the HDC is reading ID area or DATA area of the disk, but is exceptional when data in the last sector is transferred to the main memory during the multiple sector operation.

Figure 9 (b) shows the low-speed DMA transfer of the host in 256-byte sector organization. According to the figure, DBUF0 receives data of the sector 1, and DBUF1 receives that of the sector i+1. While DBUF1 is receiving the data of sector i+1, the data transfer from DBUF0 to the main memory cannot be finished because the host cannot operate promptly. Therefore, being unable to receive the data of i+2, DBUF0 waits until the disk makes one rotation (all data of DBUF0 is sent to the main manner, no data overrun occurs even if operation speed of the host is slow. Therefore, an interleave format is not required.

Figure 9 (c) indicates the sequence in 512-byte sector organization. Capacity of buffers is 256 bytes for each, and each buffer stores disk data and transfers the data to the main memory alternately. Therefore, buffers effectively operates in toggle fashion even if sector length exceeds 256 bytes, and host system throughput is improved. If operation speed of the host is too slow, data overrun may occur because data buffer cannot be emptied to receive disk data. The data transfer from data buffer to main memory must be terminated while the HDC is accessing disk data in ID or DATA area.

If the HDC receives $\overline{\text{DONE}}$ signal from the DMAC during RD or RED command execution, the HDC immediately terminates DMA data transfer. Disk reading operation continues until the HDC finishes reading the sector which has been read when $\overline{\text{DONE}}$ signal is applied.

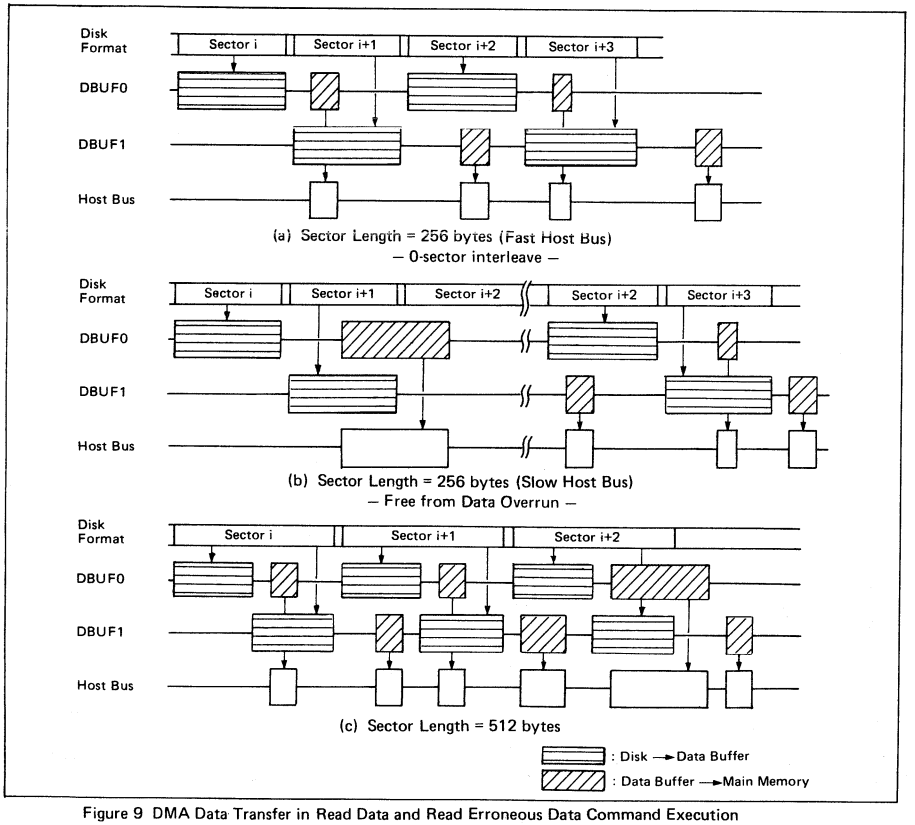


Figure 9 DMA Data Transfer in Read Data and Read Erroneous Data Command Execution

DMA data transfer during WD and CMPD command execution is shown in figure 10. This figure differs from figure 9 (a) in data transfer direction, DMA transfer order, and access method of first and last sectors. In figure 10, the host is fast and sector length is 256 bytes. When the host is slow and sector length is 256 bytes, or when sector length is 512 bytes or more, data transfer sequence is the same as figure 9.

When the HDC receives $\overline{\text{DONE}}$ signal from the DMAC during WD command execution, the HDC immediately terminates DMA data transfer. Then all data stored in DBUF0 and DBUF1 are written to DATA area of the sector. If there is any room in DATA area after writing buffer data, the old data in buffers is written to DATA area. After DATA area is filled with buffer data, command execution terminates.

When the HDC receives $\overline{\text{DONE}}$ signal from the DMAC during CMPD command execution, the HDC immediately terminates DMA data transfer. However, the data of the sector which has been accessed when $\overline{\text{DONE}}$ is received, is used for comparison with disk data, further, the reading operation continues until reading of the sector is finished. Therefore, $50 (Not Hit) is set to SSB in most cases when reading of the sector is finished, and then the command execution abnormally terminates.

DMA data transfer during RID or FID command execution is performed as follows (see figure 11). When DBUF0 is filled with ID information, DBUF1 receives the succeeding ID information. DMA data transfer is not performed unless all the ID information is stored in data buffer. After DBUF0 with/without DBUF1 finishes accepting ID information from specified number of sectors, data are sent to the main memory by DMA. DMA data transfer continues until 512-byte transfer is finished.

DMA data transfer can be stopped when the DMAC sends $\overline{\text{DONE}}$ to the HDC. Therefore, the host can store only the necessary ID information to the main memory by setting the number of ID areas to be read, to the DMAC.

DMA data transfer during WFM command execution is shown in figure 12. The HDC starts formatting operation when both DBUF0 and DBUF1 are filled with ID information from the host. The HDC writes data buffer data to the ID area of a specified sector, and writes fixed pattern to other area such as DATA area. When DBUF0 becomes empty during formatting operation, DBUF1 becomes the source in turn. When the DMAC issues $\overline{\text{DONE}}$ signal to the HDC, the HDC stops data transfer to data buffers and starts formatting. Therefore, the host can write only the necessary ID information to data buffer by setting data of how many ID areas to be transferred, to the DMAC.

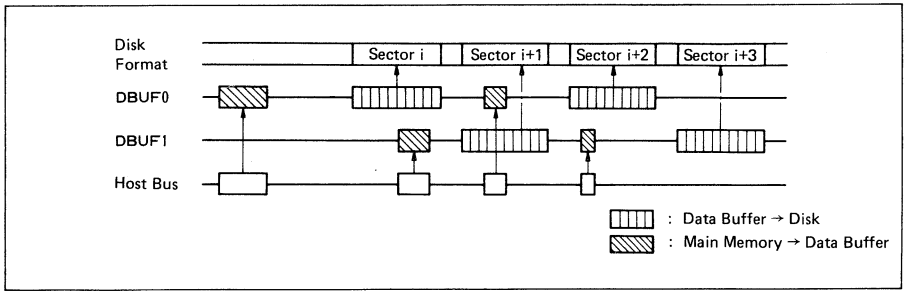


Figure 10 DMA Data Transfer in Write Data, Compare Data Command Execution (Sector Length = 256 bytes)

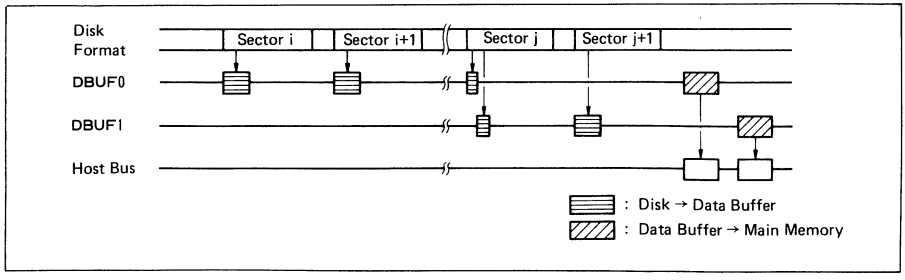


Figure 11 DMA Transfer in Read ID, Find ID Command Execution

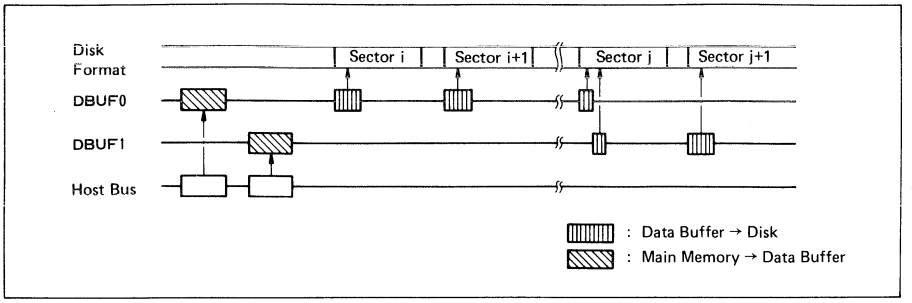


Figure 12 DMA Data Transfer in Write Format Command Execution

DMA Data Transfer by Data Transfer Commands

Accepting data transfer commands, the HDC can perform DMA data transfer between the main memory and data buffers without disk access. Either Burst mode or Cycle Steal mode is selected by the BRST bit of SPC command parameter. There are two commands available, BTM and MTB.

Selection of either DBUF0 or DBUF1, and access start address of each buffer (address 0 to 250 are specifiable), are specified by POFF (Pointer Offset). POFF is set to the data buffer pointer by command execution.

Data buffer pointer is incremented each time the DMAC accesses data buffer (+2 for 16-bit bus mode, +1 for 8-bit bus mode). Data buffer data is not guaranteed if data buffer pointer exceeds address 255. Receiving $\overline{\text{DONE}}$ signal from the DMAC, the command execution immediately terminates normally, and the CED bit in STR is set to "1". Receiving above data transfer commands, the HDC requests transfer by issuing $\overline{\text{DREQ}}$ signal to the DMAC within 150 CLK cycles.

Data Buffer Access by PIO

The host MPU can access data buffers by move or load/store instruction (Programmed I/O). In this case, the host issues OPBR or OPBW command prior to PIO access. Receiving these commands, the HDC sets BSY bit in STR to "1". Then the HDC sets data buffer pointer, sets BSY bit to "0", and terminates the command execution. It takes up to 100 CLK cycles from the command reception to BSY bit clear. Before issuing above commands, POFF must be specified by command parameters. POFF specifies either DBUF0 or DBUF1 to be accessed, and access start address (specifiable range is address 0 to 255).

The host issues move instruction to the HDC after confirming that BSY = 0. Data buffer pointer is incremented each time the HDC receives move instruction (+2 for 16-bit bus mode, +1 for 8-bit bus mode). If the pointer exceeds address 255 during data transfer in PIO mode, the buffer data is not guaranteed. The host must issue RCAL command to close the buffer.

Notes on Data Buffer

Item \ Sector Length (Byte)	256	512	1024	2048	4096
High Speed DMA (0-sector interleave)	○	○	○	○	○
PIO	○	○			
Low Speed DMA (free from overrun)	○				
Automatic Correction	○				

○ : Provided

Others

Recall command – After the host issues RCAL command, the HDC finishes the operation within up to 40 CLK cycles and clears all bits in STR.

Test command – After the host issues TST command, the HDC makes drive output pins floated within 60 CLK cycles. To cancel this state, $\overline{\text{RES}}$ signal is to be externally supplied.

Specify command – After the host issues SPC command, the HDC makes the drive interface pins fitted for either ST506 or SMD, and clears BSY bit within 250 cycles.

Abort command – After the host issues ABT command, the HDC negates all drive output pins within up to 180 CLK cycles, terminates all operation within 300 CLK cycles, and clears BSY bit. Receiving this command, the HDC clears all internal flip-flops, but the value of the control register which has been set by SPC command still remains.

Reset – Reset is not a command, but after receiving $\overline{\text{RES}}$ signal, the HDC terminates initialization within up to 150 CLK cycles and clears BSY bit.

LIMITATION ON USE

SPECIFY COMMAND

Sometimes, when the SPECIFY command is issued, the HDC may erroneously assert the WGATE signal depending on the result of the previous command execution. There are two cases in which the HDC asserts the WGATE signal. One is after the RD, RED, CMPD, or CKD command execution with the result status $40, $44, or $4C (ECC or CRC error occured). The other is after the WFM command execution.

The WGATE signal assertion occurs 13μsec (CLK = 8 MHz) after the issuance of the SPECIFY command and is 1 (disk data) byte time long. To prevent such a WGATE assertion, just before issuing the SPECIFY command always issue the ABORT command.

Note: The HDC will not assert WGATE when any of the commands in Table A is issued with the indicated result status after the execution of the RD, RED, CMPD, CKD, or WFM command.

Table A

Commands	Result Status
ABT	SSB = $04
WD	SSB = $00, $60
RD	SSB = $00, $60
RED	SSB = $00, $60
CKD	SSB = $00, $60
CMPD	SSB = $00, $50, $60

POLLING DISABLE COMMAND

Sometimes, the HDC may not accept the POLLING DISABLE command during the execution of the POLLING command.

This problem can be fixed by issuing the POLLING DISABLE command twice. The interval between the two POLLING DISABLE commands should be greater than 25 CLK and less than 100 CLK periods.

TIMINGS OF THE WGATE AND HSEL0 SIGNALS IN THE ST506

The negate timings of the WGATE and HSEL0 signals during the WRITE FORMAT command execution in the ST506 interface mode are shown in Fig. A. HSEL0 is negated before WGATE is negated when 10WCLK is greater than 7CLK. This causes some HDD's assert the WRITE FAULT signal.

Even if some other head is selected by premature negation of the HSEL0 signal and some spurious data is written, the data is only written in the early part of the GAP1 field, immediately following the index. This should not cause a problem since any VFO should still be able to sync to the PLO SYNC field. However, if a shown in Fig. B will eliminate the problem.

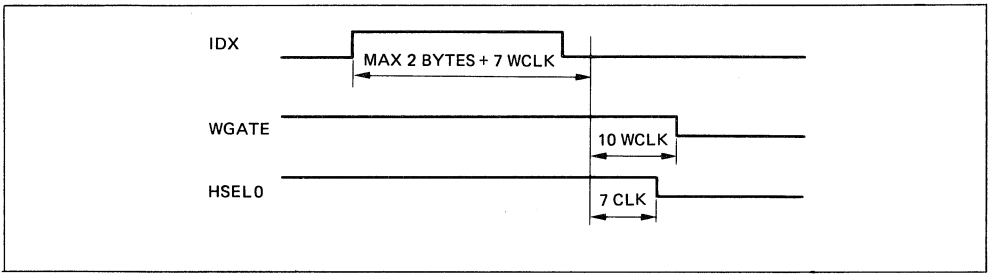


Figure A Timings of WGATE and HSEL0 Signals

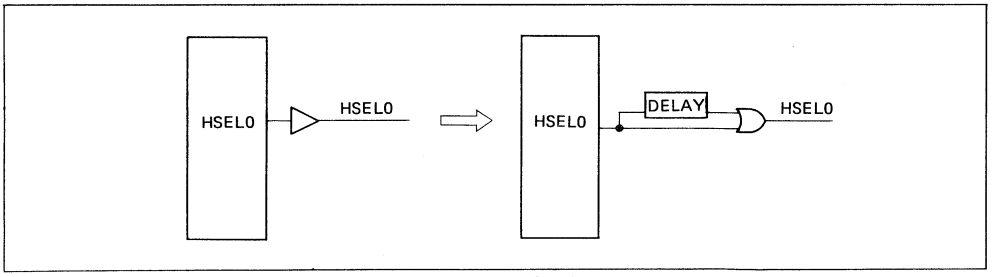


Figure B Typical Circuit

NOTES ON WRITE SPLICES IN THE ST506

Careful consideration should be taken when the HDC is used with a disk where a write splice has been included: the HDC cannot read the designated sector due to the presence of "$00" or "$FF" or "AM" (Address mark: $A1) in the GAP3 field.

This is detailed for two cases: when a "$00" or "$FF" is generated and when an "AM" (Address mark: $A1) is generated, as follows.

(1) When a "$00" or "$FF" Occurs in the GAP3 Field by a Write Splice

(a) Phenomenon

Figure C shows the HDC operation timing in SYNC searching state. When "$00 or $FF" (zero pattern) occurs in the GAP3 field by a write splice, the HDC mistakenly regards the "$00 or $FF" as SYNC and asserts the SYNC signal. The HDC then negates the RGATE and SYNC signals by detecting a not-zero pattern (data other than zero pattern) following the write splice, since a not-zero pattern is normally input following a write splice. After this, the HDC asserts the RGATE signal again to return to normal SYNC searching and "AM" detecting operations. The above results in a relatively great loss of time.

In addition, as you can see from Figure C, HDC requires a period of 12.5 bytes + write splice width (max) + VF0 synchronization time to detect "AM" of the following sector. Consequently, the HDC may not be able to read the next sector depending on the GAP3 length, SYNC length, write splice width, and VF0 synchronization time. (VF0 synchronization time in this case is defined as the period from RGATE assertion to correct RCLK and read data input.)

(b) Countermeasure

In the user system, first check whether or not the following condition is satisfied.

Condition: GAP3 length + SYNC length − 12.5 bytes > Write splice width (max.) + VF0 synchronization time

If the above condition is not satisfied, GAP3 length and SYNC length must be extended.

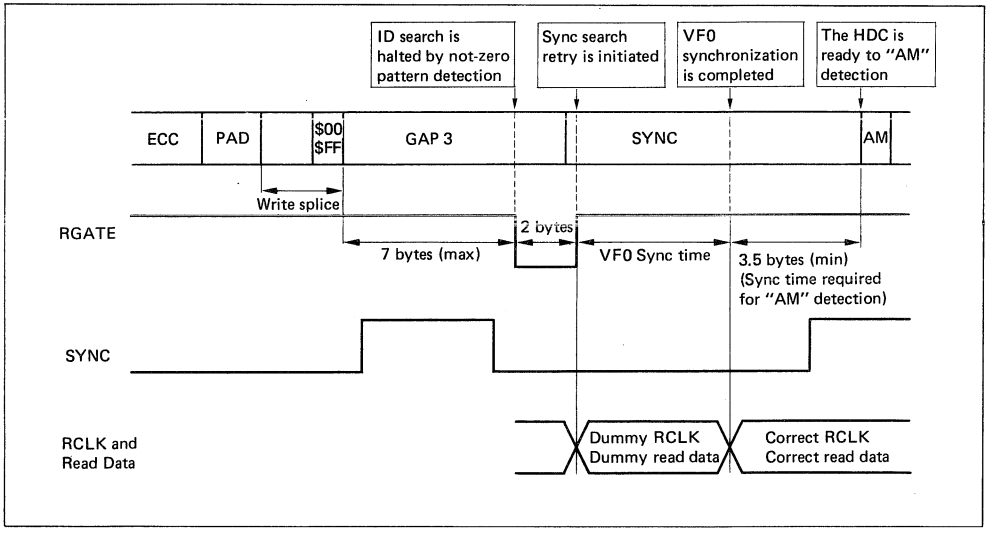


Figure C HDC Operation Timing in SYNC Search State When a "$00" or "$FF" Occurs by Write Splice

(2) When a Dummy "AM" Occurs in the GAP3 Field by a Write Splice

(a) Phenomenon

When "$00 or $FF" is included in the ECC or PAD field, the HDC regards the "$00 or $FF" as SYNC and mistakenly recognizes the following dummy "AM" caused by a write splice as "AM". The HDC then handles the data string following the dummy "AM" as an ID. This erroneous ID causes a CRC error or ID mismatch. The HDC is then forced to execute corresponding error processing. As a result, the HDC cannot read the next sector since the HDC ignores the "AM" for the next sector when performing ID error or ID mismatch processing (Figure D).

The reason for the above bug is described below. The HDC recognizes SYNC field by detecting a 1-byte zero pattern. After a 1-byte zero pattern detection, the HDC searches for an "AM" or a not-zero pattern. If the HDC detects an "AM" before a not-zero pattern, the HDC handles data following the "AM" as an ID. On the other hand, if the HDC detects a not-zero pattern before an "AM", the HDC enters SYNC pattern search by re-asserting the RGATE signal following the RGATE and SYNC signal negation. In addition, the HDC exhibits "don't care" for a 1.5 bytes period after SYNC pattern detection. Moreover, if an "AM" pattern resides within a 1.5 to 3 byte period after SYNC pattern detection, the HDC detects the "AM" pattern regardless of data residing between the zero pattern and the "AM" pattern. Accordingly, if the HDC regards the zero pattern residing in ECC or PAD as a SYNC pattern and if the "AM" pattern caused by a write splice resides 1.5 to 3 bytes after the SYNC pattern, the HDC regards the erroneous "AM" pattern as a correct "AM" pattern as shown in Figure E.

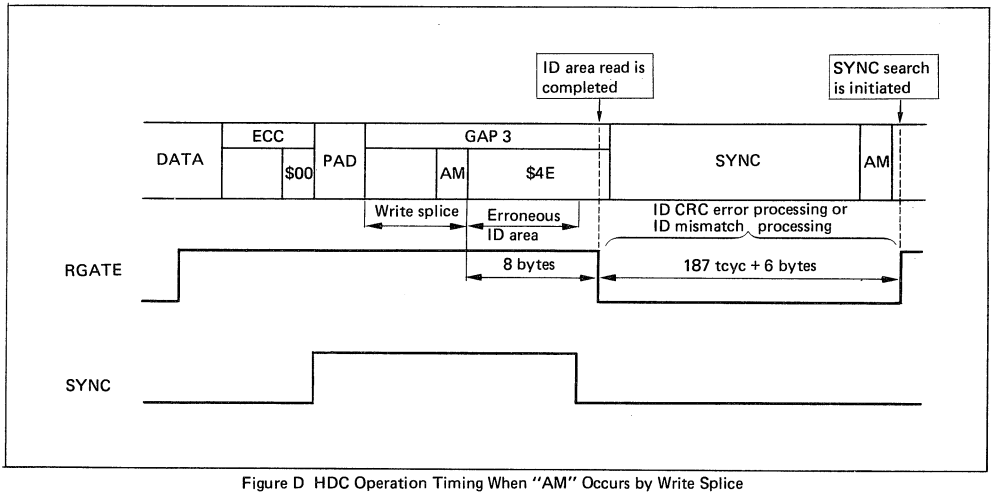


Figure D HDC Operation Timing When "AM" Occurs by Write Splice

(b) Countermeasures
One of the following countermeasures must be taken to prevent the problem.

① Writing "$4E" for three bytes

The SPC command parameter must be specified as shown below:
- OM0 PADP bit = "1"
- OM1 AMEX bit = "0"

after which "$4E" should be written to three bytes to form PAD.

Figure E shows the relationship between the number of "$4E" bytes and the "AM" detection area length. As shown in Figure E, by writing "$4E" to form PAD, the "AM" detection area length can be reduced to prevent erroneous "AM" detection.

However, note that a sector formatted before the above countermeasure cannot be accessed since the ECC or CRC data in the sector changes after the above countermeasure.

② Delaying WGATE negation timing

WGATE negation timing must be delayed according to Table B during which dummy data other than "$00", "$FF", and "AM" should be input to the drive. This effectively prevents "AM" pattern generation within the "AM" detection area. However, note that following condition must be satisfied before performing the above countermeasure.

Condition: GAP3 length + SYNC length - 12.5 bytes
> write splice width (max) + VF0 synchronization time + WGATE delay

Table B WGATE Delay

PAD Pattern	PAD Length	WGATE Delay
$4E	2 bytes	At least 2.5 bytes
	3 bytes	At least 1.5 bytes
$00	2 bytes	At least 4.5 bytes
	3 bytes	

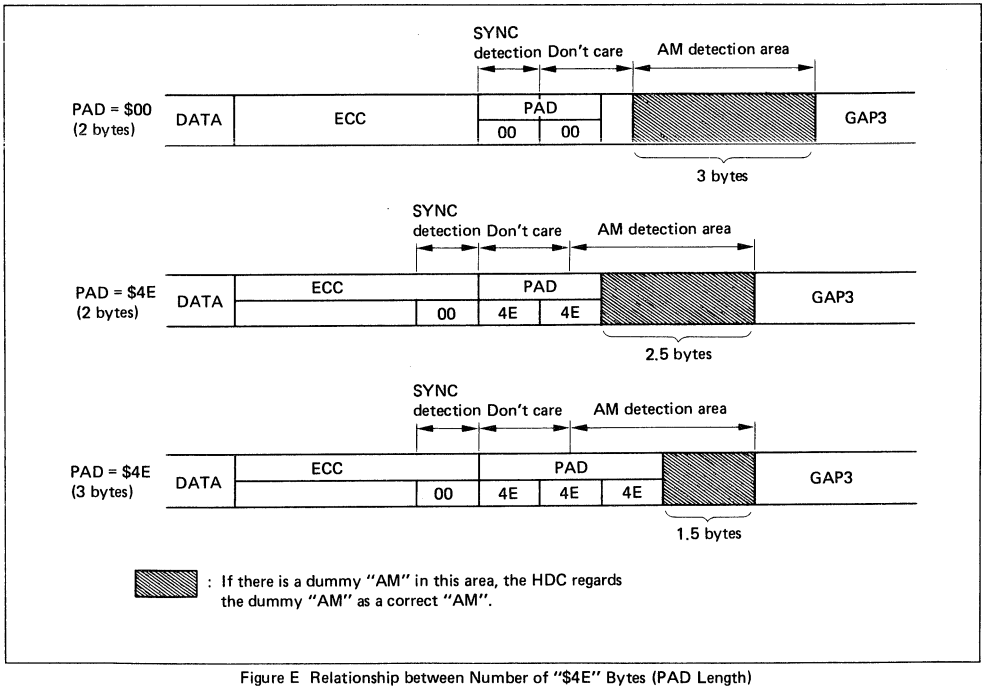


Figure E Relationship between Number of "$4E" Bytes (PAD Length) and "AM" Detection Area Length

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} *1	−0.3 − +7.0	V
Input Voltage	V_{in} *1	−0.3 − V_{CC} + 0.3	V
Output Current per Pin	$\|Io\|$ *2	5	mA
Total Output Current	$\|\Sigma Io\|$ *3	80	mA
Operating Temperature	T_{opr}	0 − +70	°C
Storage Temperature	T_{stg}	−55 − +150	°C

*1 This value is in reference to V_{ss} = 0V.

*2 The allowable output current is the maximum current that may be drawn from, or flow out to, one output terminal or one input/output common terminal.

*3 The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.

(Note) Using an LSI beyond its maximum ratings may result in its permanent destruction. LSI's should usually be used under recommended operating conditions. Exceeding any of these conditions may adversely affect its reliability.

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}*	4.75	5.0	5.25	V
Input Low Level Voltage	V_{IL}*	0	–	0.8	V
Input High Level Voltage	V_{IH}*	2.2	–	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

* This value is in reference to V_{SS} = 0V.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, Ta = 0 – 70°C, unless otherwise noted)

Item			Symbol	HD63463-8 min	HD63463-8 max	Unit	Test Condition
Input High Level Voltage	All Inputs		V_{IH}	2.2	V_{CC}	V	
Input Low Level Voltage	All Inputs		V_{IL}	–0.3	0.8	V	
Input Leak Current	R / $\overline{W}$, $\overline{CS}$, RS, $\overline{RES}$, $\overline{DACK}$, CLK, $\overline{DONE}$		I_{IN}	–2.5	2.5	μA	V_{in} = 0–V_{CC}
	ST506	SMD					
	IDX/ TRKO SCP USELD WCLK RCLK	IDX SEC USELD WCLK RCLK					
Three State (Off State) Input Current	RWDATA $\overline{SYNC}$*1 WGATE*2 EARLY/ RGATE*1 LATE/ STEP*1 WFLT LCT/DIR*1 READY	RWDATA $\overline{SKEND}$ BUS_0/BUS_5 BUS_1 BUS_6 BUS_2/BUS_7 BUS_3/BUS_8 BUS_4/BUS_9 $BUSL/\overline{H}$*1	I_{TSI}	–10	10	μA	V_{in} = 0.4–V_{CC}
	$D_0 - D_{15}$						
Output High Level Voltage	All Outputs		V_{OH}	V_{CC}–1.0	–	V	I_{OH} = –400 μA
Output Low Level Voltage			V_{OL}	–	0.5	V	I_{OL} = 2.2 mA
Output Leak Current (Off State)	$\overline{IRQ}$		I_{LOH}	–	10	μA	V_{OH} = V_{CC}

(to be continued)

*1 These signals are defined when HDC is in Test mode or when drive interface is not specified. Otherwise, these signals are not defined since these are switched to output signals.

*2 This signal is defined when HDS is in test mode, otherwise this signal is not defined.

Item			Symbol	HD63463-8		Unit	Test Condition
				min	max		
Signal Capacity	$\overline{RES}$ $\overline{DONE}$ RS R / $\overline{W}$ $\overline{CS}$ $\overline{DACK}$ $D_0 - D_{15}$ CLK $\overline{IRQ}$		C_{pin}	–	17	pF	V_{in} = 0 V Ta = 25°C f = 1.0 MHz
	ST506	SMD					
	RWDATA WCLK RCLK – – – WFLT – IDX/ TRK0 SCP USELD READY	RWDATA WCLK RCLK SKEND BUS_0/BUS_5 BUS_1/BUS_6 BUS_2/BUS_7 BUS_3/BUS_8 BUS_4/BUS_9 IDX SEC USELD –						
Current Consumption			I_{CC}	–	80	mA	• Data bus in read/ write operation • Command execution in progress

AC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = 0 – 70°C, unless otherwise noted.)

Clock Timing

No.	Item	Symbol	HD63463-8		Unit	Test Condition
			min	max		
1	Clock Cycle time	tCYC	125	500	ns	See Figure 15
2	Clock Low Level Pulse Width	tPWCL	55	250	ns	
3	Clock High Level Pulse Width	tPWCH	55	250	ns	
4	Clock Rise Time	tCR	–	10	ns	
5	Clock Fall Time	tCF	–	10	ns	
6	Write Clock Cycle time	tWCYC	50	250	ns	
7	Write Clock Low Level Pulse Width	tPWCL	20	115	ns	
8	Write Clock High Level Pulse Width	tWCH	20	115	ns	
9	Write Clock Rise Time	tWCR	–	10	ns	
10	Write Clock Fall Time	tWCF	–	10	ns	
11	Read Clock Cycle Time	tRCYC	50	250	ns	
12	Read Clock Low Level Pulse Width	tRCL	20	115	ns	
13	Read Clock High Level Pulse Width	tRCH	20	115	ns	
14	Read Clock Rise Time	tRCR	–	10	ns	
15	Read Clock Fall Time	tRCF	–	10	ns	

Data Bus Configuration and $\overline{IRQ}$

No.	Item	Symbol	HD63463-8		Unit	Test Condition
			min	max		
21	$\overline{RES}$ Input Pulse Width	tRES	10	–	tcyc	See Figure 16
22	$\overline{DACK}$ Setup Time for $\overline{RES}$	tDACKSR	100	–	ns	
23	$\overline{DACK}$ Hold Time For $\overline{RES}$	tDACKHR	0	50	ns	
24	$\overline{IRQ}$ Delay Time 1	tIRD1	–	150	ns	See Figure 17
26	$\overline{RES}$ Rise Time	tRESR	–	10	μs	See Figure 16

MPU Interface

No.	Item	Symbol	HD63463-8		Unit	Test Condition
			min	max		
31	R / $\overline{W}$ Setup Time for $\overline{CS}$ Assert	tRWS	50	–	ns	
32	R / $\overline{W}$ Hold Time	tRWH	0	–	ns	
33	RS Setup Time for $\overline{CS}$ Assert	tRSS	50	–	ns	
34	RS Hold Time	tRSH	0	–	ns	
35	$\overline{CS}$ Setup Time	tCSS	40	–	ns	
36	$\overline{CS}$ Negate Hold Time	tCSNH	40	–	ns	
37	$\overline{CS}$ Negate Width	tCSNW	80	–	ns	
38	Write Data Setup Time	tWDS	40	–	ns	See Figures 18 and 19
39	Write Data Hold Time	tWDH	10	–	ns	
40	$\overline{DTACK}$ Delay Time	tDTKZL	–	80	ns	
41	$\overline{DTACK}$ Hold Time	tDTKLH	–	80	ns	
43	Data Bus 3 State Recovery Time	tDBR	0	–	ns	
44	Read Data Access Time	tRDAC	–	70	ns	
45	Read Data Hold Time	tRDH	10	–	ns	
46	$\overline{CS}$ Fall Time	tCSF	–	1	tcyc	
47	$\overline{CS}$ Rise Time	tCSR	–	1	tcyc	

DMA Interface

No.	Item	Symbol	HD634638-8		Unit	Test Condition
			min	max		
50	$\overline{DREQ}$ Assert Delay Time 1	tDRAD1	–	80	ns	
51	$\overline{DREQ}$ Negate Delay Time 1 (Cycle Steal Mode)	tDRND1	–	80	ns	
52	$\overline{DREQ}$ Assert Delay Time 2 (Cycle Steal Mode)	tDRAD2	–	80	ns	
53	$\overline{DREQ}$ Negate Delay Time 2	tDRND2	–	80	ns	
54	$\overline{DREQ}$ Negate Delay Time 3 ($\overline{DONE}$ Assert)	tDRND3	–	80	ns	
55	DMA R /$\overline{W}$ Setup Time	tDRWS	50	–	ns	See Figures 20 and 21
56	DMA R / $\overline{W}$ Hold Time	tDRWH	0	–	ns	
57	$\overline{DACK}$ Setup Time	tDACKS	40	–	ns	
58	$\overline{DACK}$ Negate Hold Time	tDACKHN	40	–	ns	
59	$\overline{DACK}$ Negate Width	tDAKNW	80	–	ns	
60	DMA Write Data Setup Time	tDWDS	40	–	ns	
61	DMA Write Data Hold Time	tDWDH	10	–	ns	
62	DMA $\overline{DTACK}$ Delay Time	tDDTZL	–	80	ns	
63	DMA $\overline{DTACK}$ Hold Time	tDDTLH	–	60	ns	

(to be continued)

No.	Item	Symbol	HD63463-8		Unit	Test Condition
			min	max		
65	$\overline{\text{DONE}}$ Input Pulse Width	tPWDN	1.5	–	tcyc	See Figures 20 and 21
66	DMA Data Bus 3 State Recovery Time	tDDBR	0	–	ns	
67	DMA Read Data Access Time	tDRDAC	–	70	ns	
68	DMA Read Data Hold Time	tDRDH	10	–	ns	
69	$\overline{\text{DACK}}$ Fall Time	tDACKF	–	1	tcyc	
70	$\overline{\text{DACK}}$ Rise Time	tDACKR	–	1	tcyc	

ST506 Interface

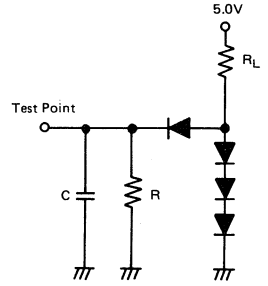
No.	Item	Symbol	HD63463-8		Unit	Test Condition
			min	max		
110	USELD Setup Time (for USEL)	tUSLDS	–	5	tcyc	See Figure 22
111	WGATE Delay Time for Index	tWGTIDX	–	100	ns	See Figure 23
112	WFLT Pulse Width	tWFLT	2	–	tcyc	
113	Index Pulse Width	tIDXW	8tcyc 24twcyc	– –	–	(Note 1) See Figure 23
114	WGATE Delay Time	tWGTD	–	125	ns	See Figure 24
116	Write Data Delay Time	tWDD	–	125	ns	
118	LATE / EARLY Delay Time	tELD	–	125	ns	
120	LATE / EARLY Setup Time (for Write Data)	tWDS	0	–	ns	
121	RGATE Delay Time	tRGTD	–	125	ns	See Figure 25
123	SYNC Delay Time	tSYND	–	125	ns	
125	Read Data Setup Time	tRDS	15	–	ns	
126	Read Data Hold Time	tRDH	15	–	ns	
127	USELD-DIR Time	tUS-DIR	70	–	tcyc	See Figure 26
128	STEP-USEL Time	tSTPUS	80	–	tcyc	
129	DIR-STEP Time	tDIRSTP	270	–	tcyc	
130	STP-DIR Time	tSTPDIR	80	–	tcyc	
131	SEEK-USEL Time	tSEKUS	1	–	tcyc	
132	SCP Wait Time	tSCP	–	1.0×10^7	tcyc	

(Note 1) The index pulse width must satisfy min 8 tcyc and min 24 twcyc.

SMD Interface

No.	Item	Symbol	HD63463-8		Unit	Test Condition
			min	max		
150	Index Pulse Width	tIDXW	8tcyc 12twcyc	50tcyc	—	(Note 2) See Figure 32
151	USELD Setup Time	tUSLDS	—	7	tcyc	See Figure 31
152	Sector Pulse Width	tPWSET	8tcyc 12twcyc	50tcyc	—	(Note 2) See Figure 32
153	WGATE Delay Time for SEC / IDX	tWGTSEC	—	125	ns	See Figure 32
156	REGATE Delay Time	tRGTD	—	125	ns	See Figure 33
158	Read Data Setup Time	tRDS	15	—	ns	
159	Read Data Hold Time	tRDH	15	—	ns	
165	WGATE Delay Time	tWGTD	—	125	ns	See Figure 34
169	Write Data Delay Time	tWDD	—	125	ns	

(Note 2) The index sector pulse width must satisfy min 8 tcyc and min 12 twcyc.



Signal		Load Condition
$D_0 - D_{15}$ $\overline{DTACK}$ $\overline{DREQ}$ RWDATA		RL = 1.8 kΩ C = 40 pF
ST506	SMD	
SYNC	–	R = 10 kΩ
WGATE	BUS_0/BUS_5	
EARLY/ RGATE	BUS_1/BUS_6	
LATE/ STEP	BUS_2/BUS_7	All diodes are
–	BUS_3/BUS_8	1S2074 Ⓗ 's or
LCT/DIR	BUS_4/BUS_9	the equivalent.
USEL0	TAG1	
USEL1	TAG2	
HSEL0	TAG3	
HSEL1	UTAG	
HSEL2	TAG5	
SEEK	BUSR/$\overline{W}$	
–	BUSL/$\overline{H}$	

Figure 13 Test Load Circuit A

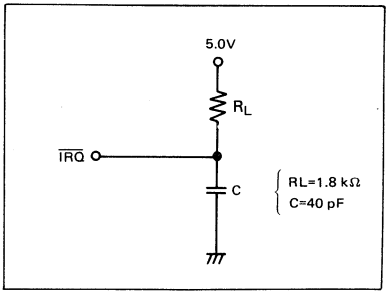


Figure 14 Test Load Circuit B

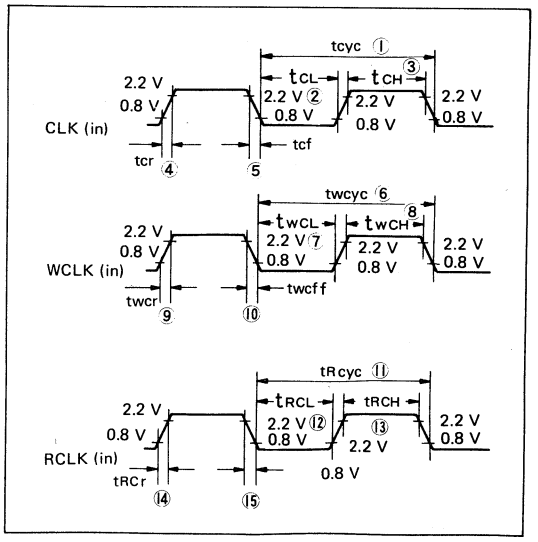


Figure 15 CLOCK

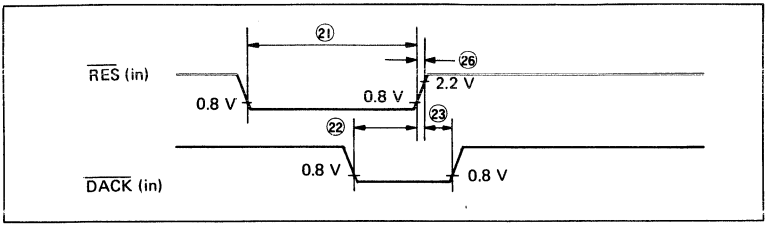


Figure 16 RES – DACK Input Timing (Data Bus Width Selection)

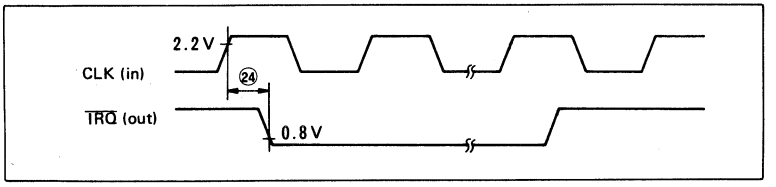
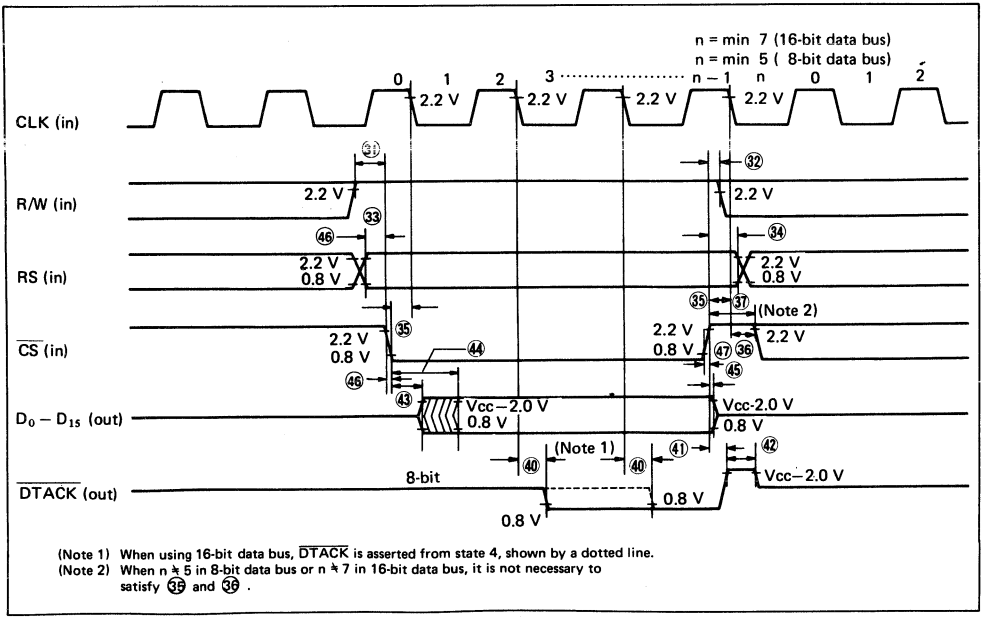


Figure 17 IRQ Output Timing



(Note 1) When using 16-bit data bus, DTACK is asserted from state 4, shown by a dotted line.
(Note 2) When n ≠ 5 in 8-bit data bus or n ≠ 7 in 16-bit data bus, it is not necessary to satisfy ㉟ and ㊱ .

Figure 18 MPU Read Cycle
HDC → MPU

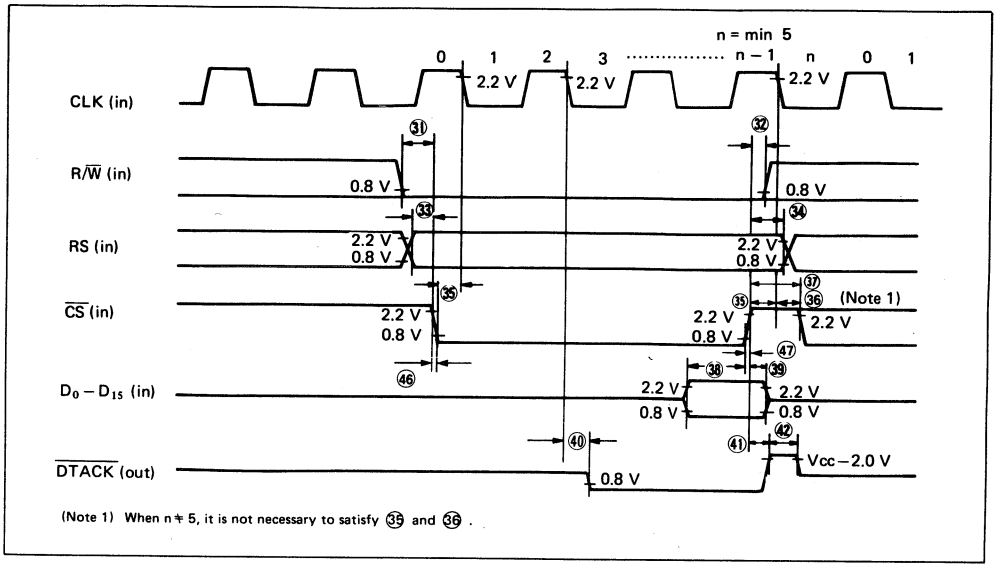
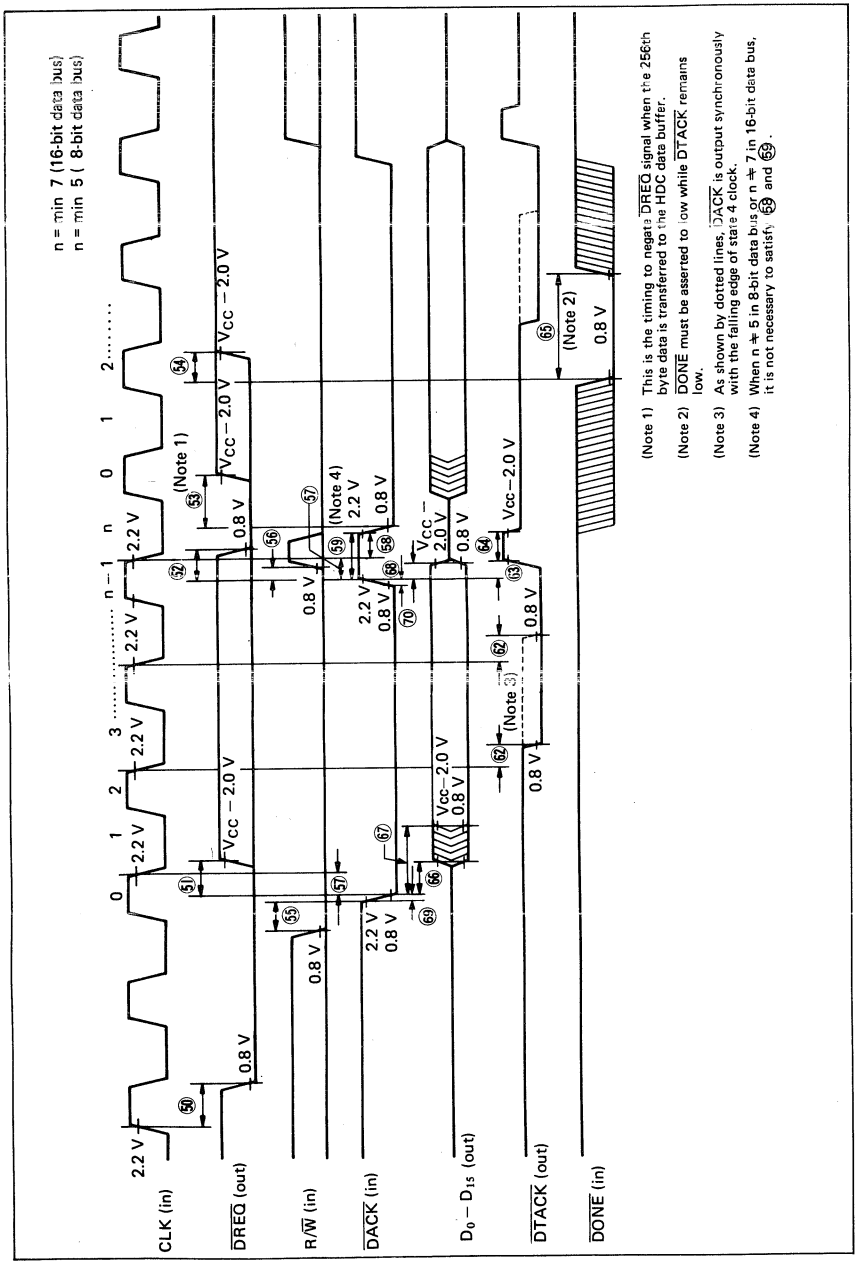


Figure 19 MPU Write Cycle
MPU → HDC
(8 or 16-bit data bus)



(Note 1) This is the timing to negate DREQ signal when the 256th byte data is transferred to the HDC data buffer.

(Note 2) DONE must be asserted to low while DTACK remains low.

(Note 3) As shown by dotted lines, DACK is output synchronously with the falling edge of state 4 clock.

(Note 4) When n ≠ 5 in 8-bit data bus or n ≠ 7 in 16-bit data bus, it is not necessary to satisfy (59) and (69).

Figure 20 DMA Read Cycle
HDC → Memory

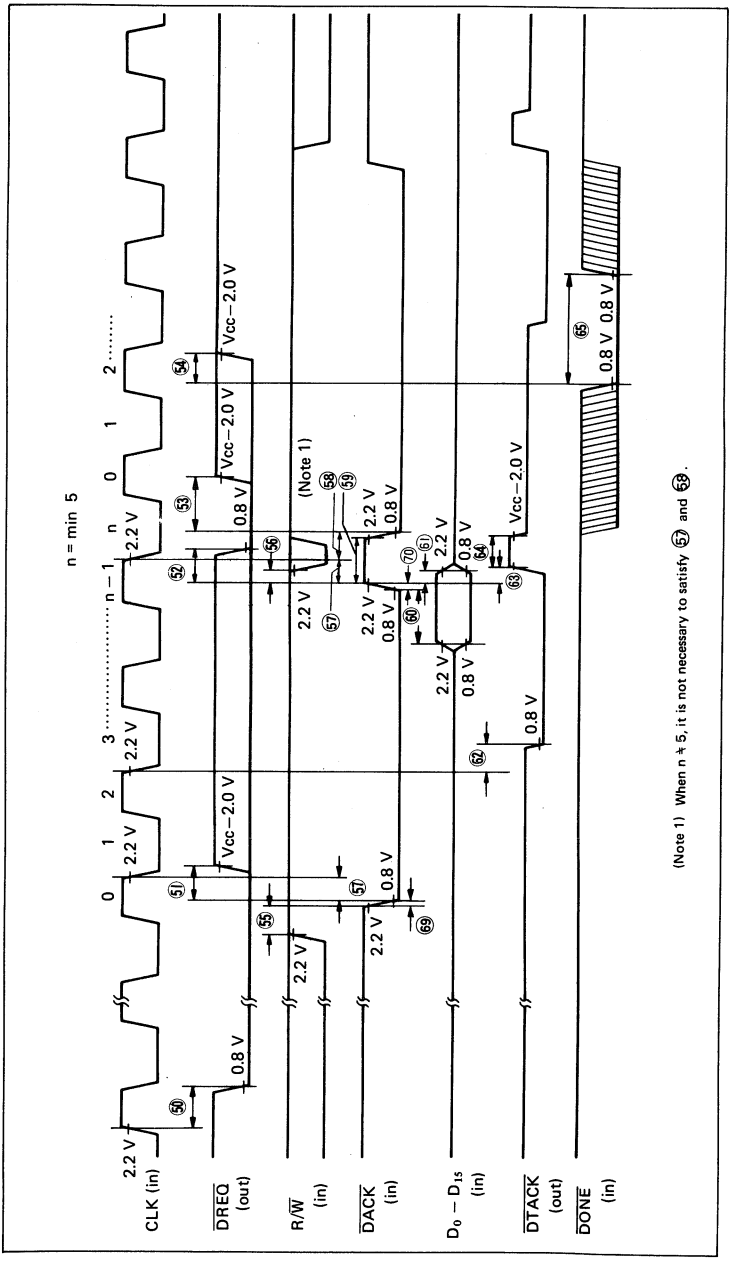


Figure 21 DMA Write Cycle
Memory → HDC

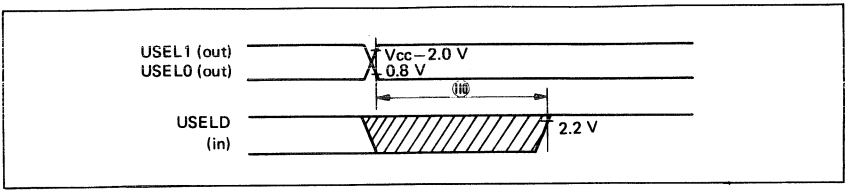
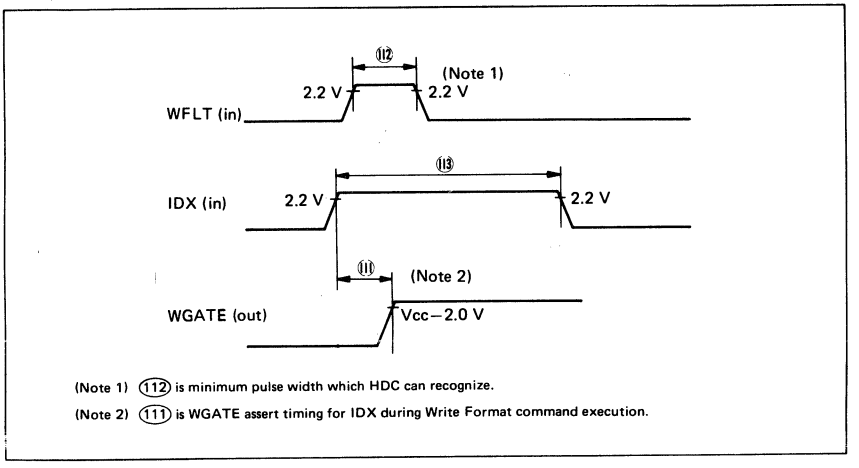


Figure 22 USEL, USELD Timing (ST506)



(Note 1) (12) is minimum pulse width which HDC can recognize.

(Note 2) (11) is WGATE assert timing for IDX during Write Format command execution.

Figure 23 WFLT, IDX, WGATE Timing (ST506)

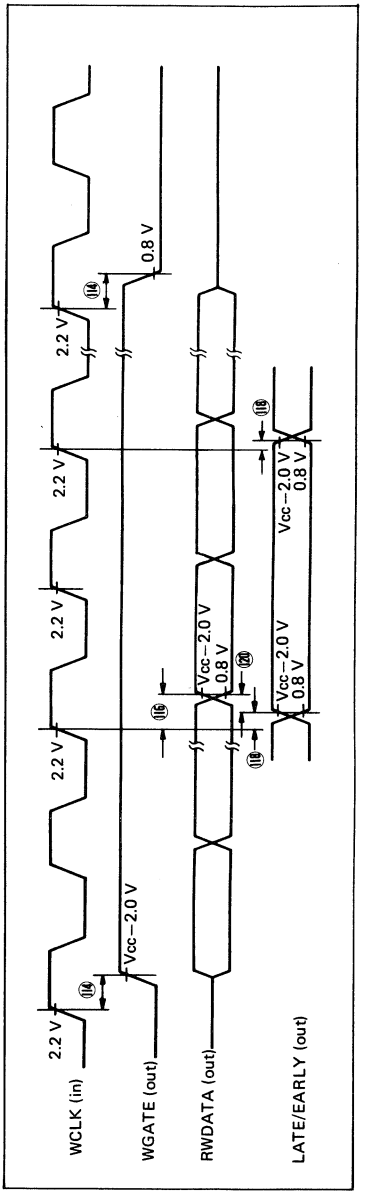


Figure 24 Write Operation (ST506)

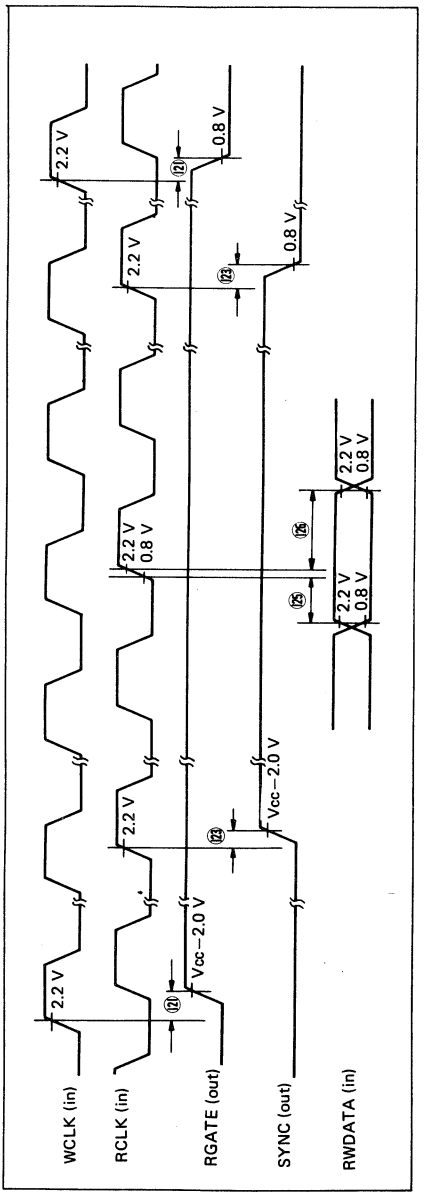


Figure 25 Read Operation (ST506)

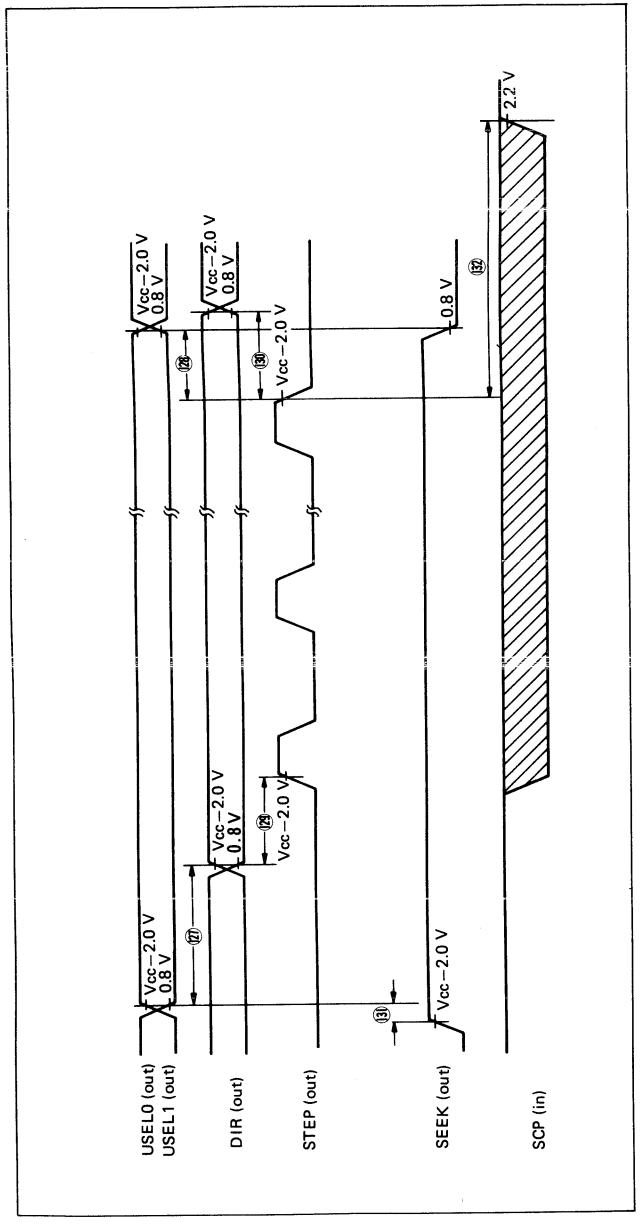


Figure 26 Head Positioning Operation (ST506)

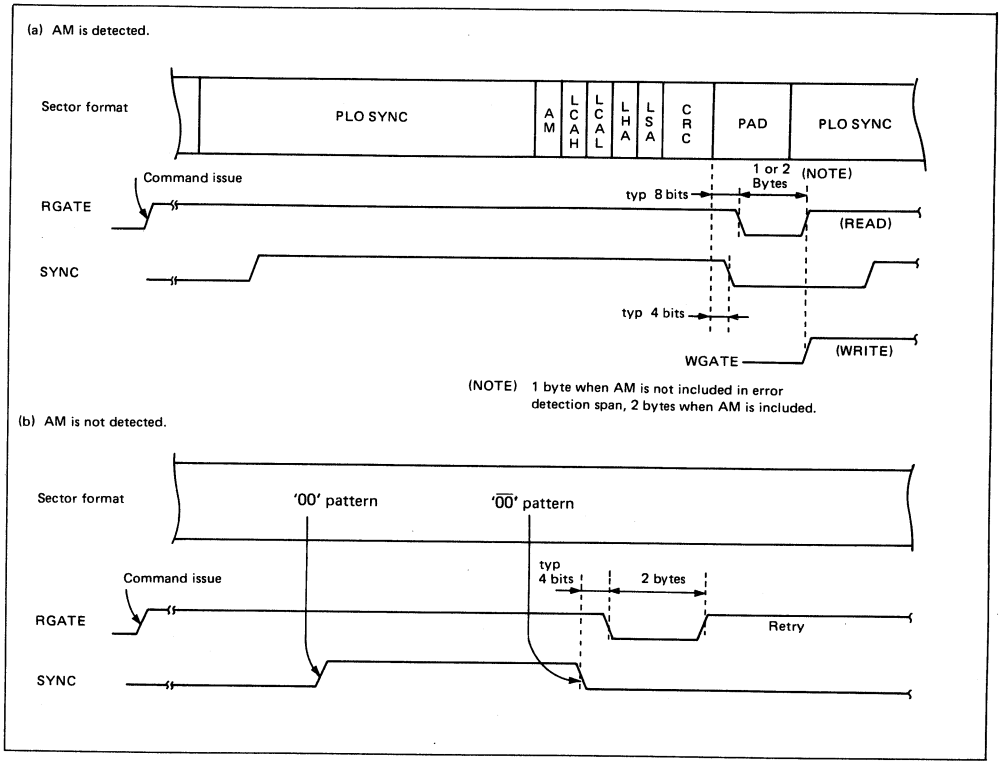


Figure 27 ID Search Timing Chart (ST506)

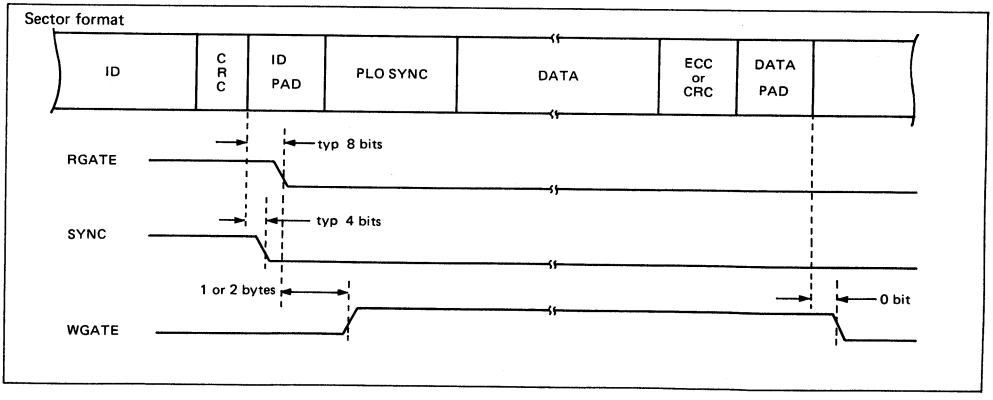


Figure 28 Write Data Timing (ST506)

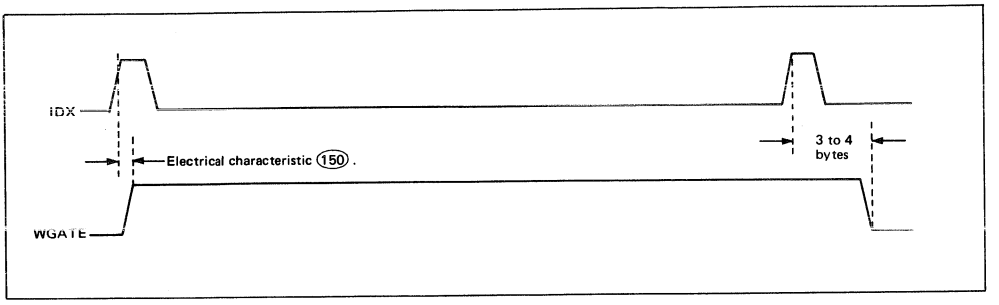


Figure 29 Write Format Timing (ST506)

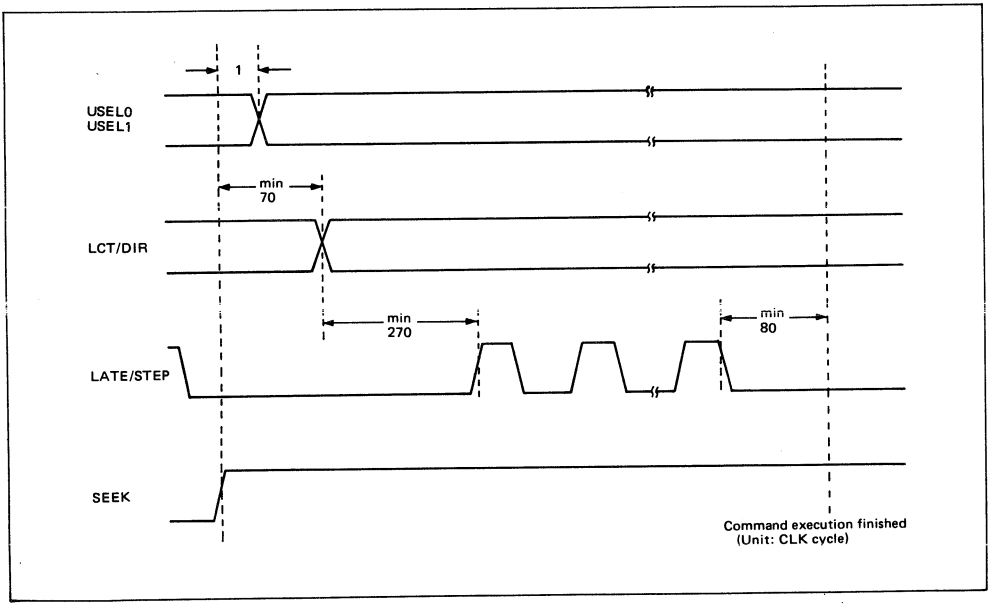


Figure 30 Seek, Recalibrate Command Execution Timing (ST506)

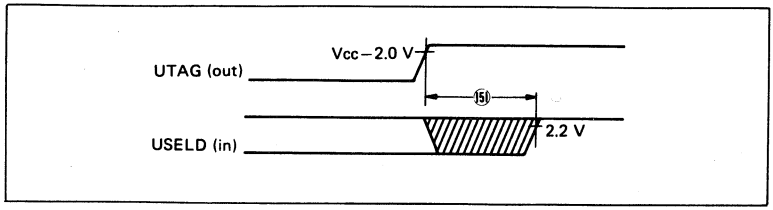


Figure 31 UTAG, USELD Timing (SMD)

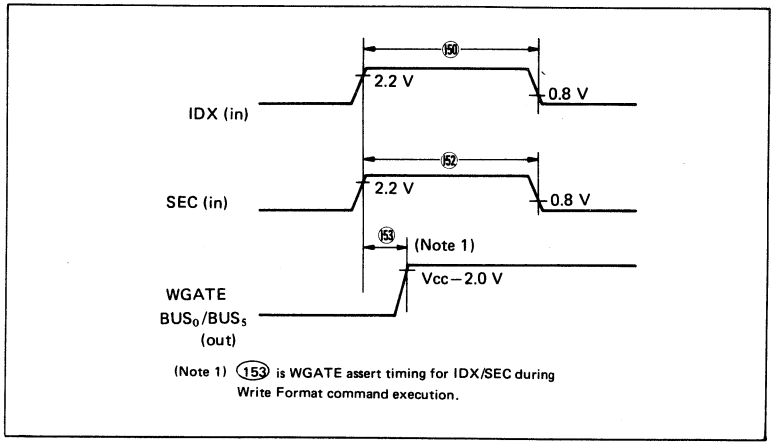


Figure 32 IDX/SEC, WGATE Timing (SMD)

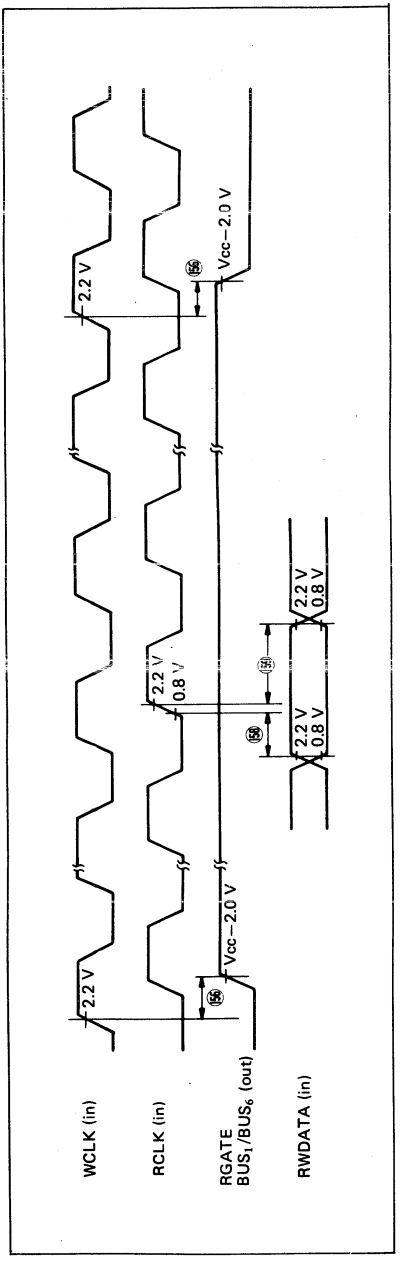


Figure 33 Read Operation (SMD)

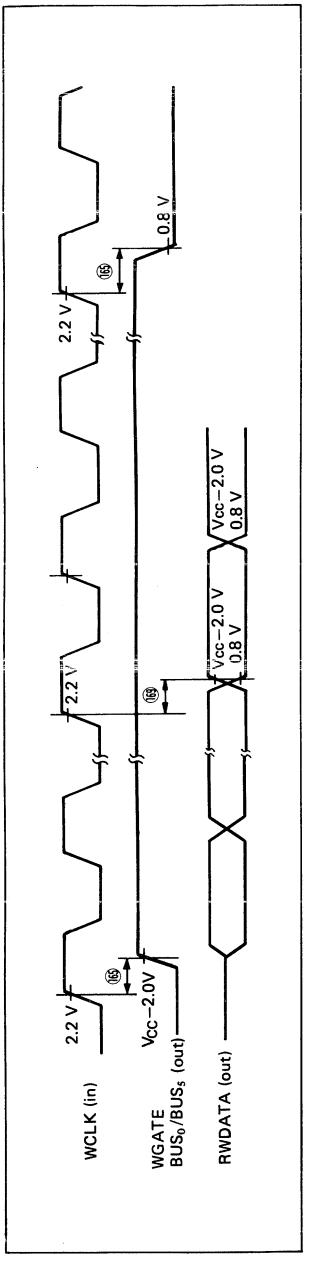


Figure 34 Write Operation (SMD)

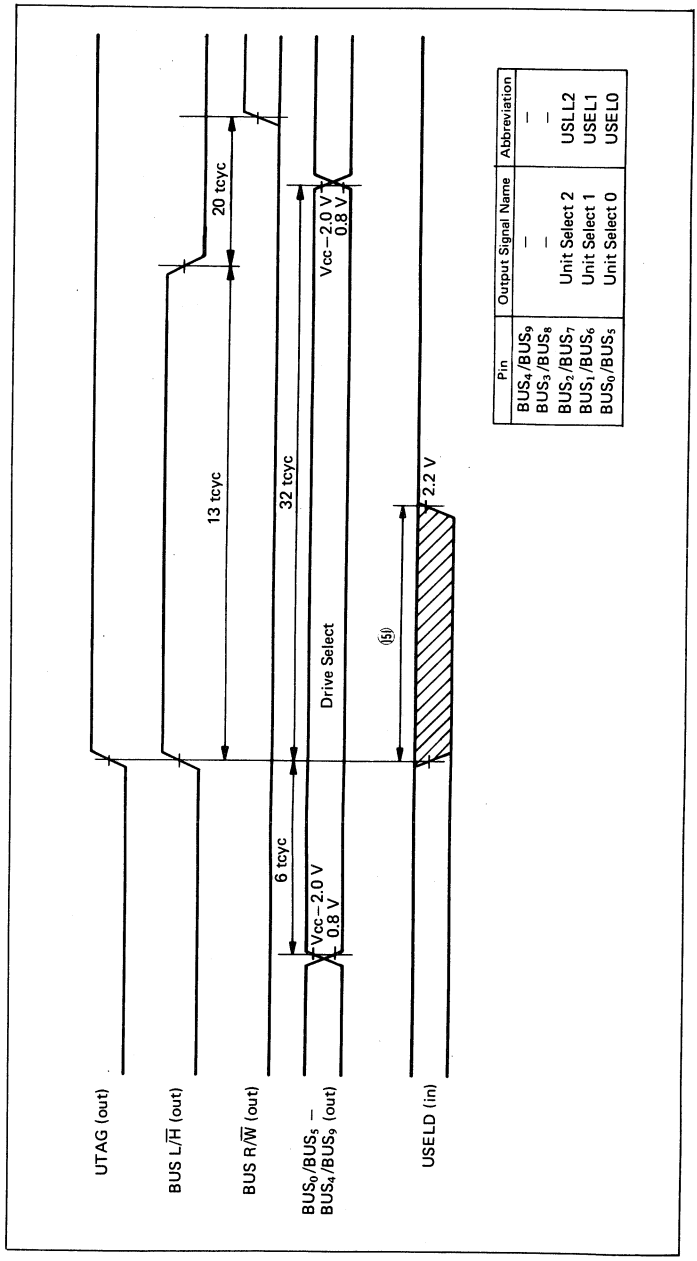


Figure 35 Drive Select Operation (SMD)

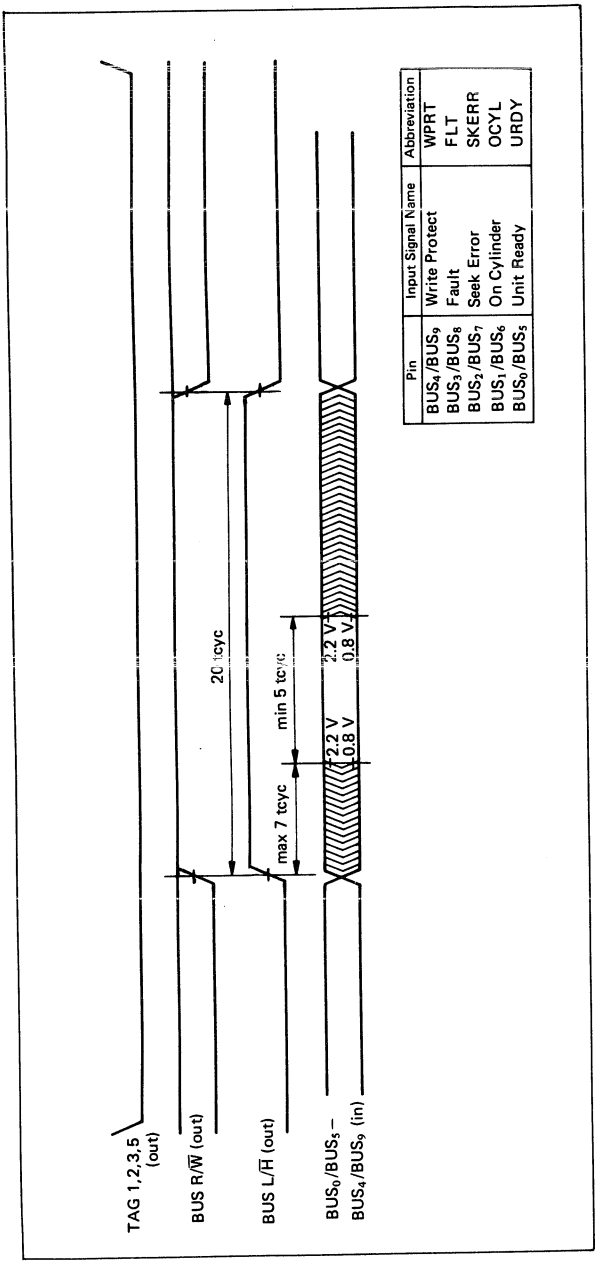
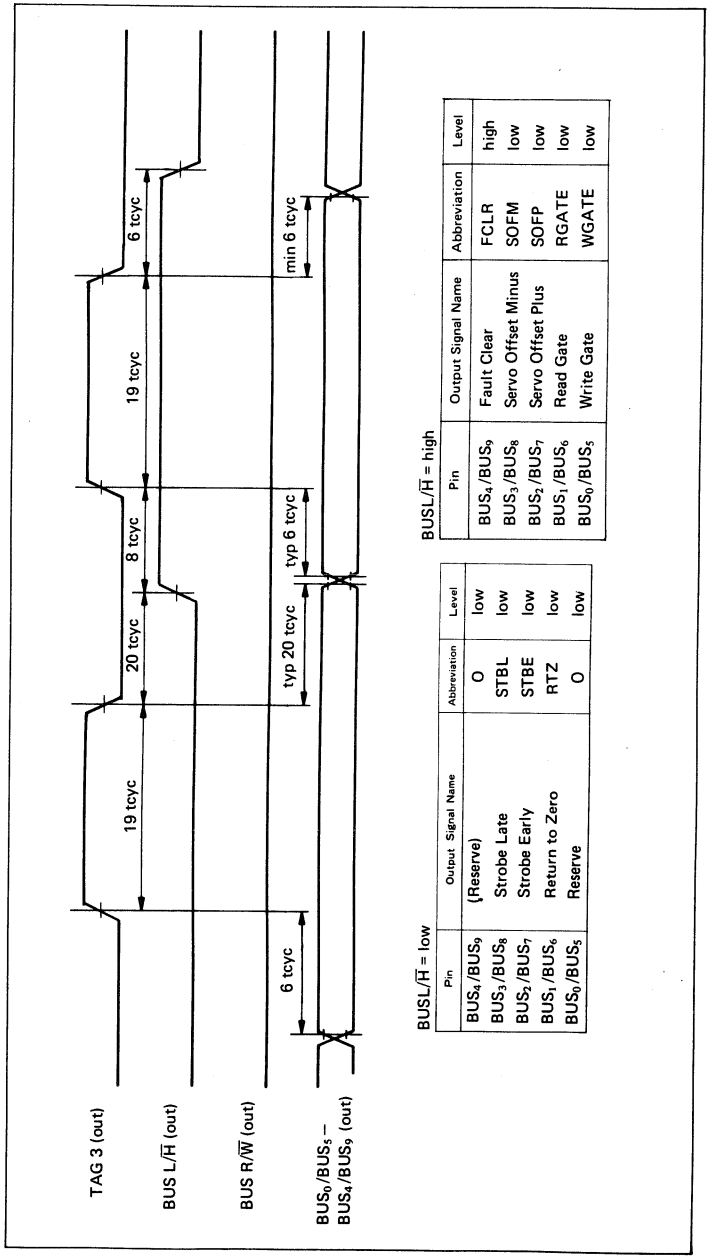


Figure 36 Drive Check Operation (SMD)



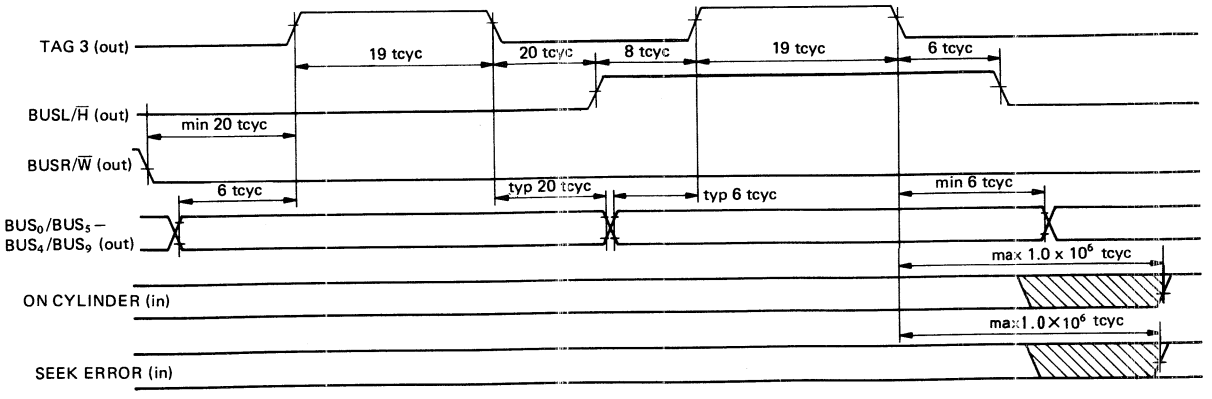
BUSL/$\overline{H}$ = low

Pin	Output Signal Name	Abbreviation	Level
BUS_4/BUS_9	(Reserve)	O	low
BUS_3/BUS_8	Strobe Late	STBL	low
BUS_2/BUS_7	Strobe Early	STBE	low
BUS_1/BUS_6	Return to Zero	RTZ	low
BUS_0/BUS_5	Reserve	O	low

BUSL/$\overline{H}$ = high

Pin	Output Signal Name	Abbreviation	Level
BUS_4/BUS_9	Fault Clear	FCLR	high
BUS_3/BUS_8	Servo Offset Minus	SOFM	low
BUS_2/BUS_7	Servo Offset Plus	SOFP	low
BUS_1/BUS_6	Read Gate	RGATE	low
BUS_0/BUS_5	Write Gate	WGATE	low

Figure 37 Fault Clear Operation (SMD)



BUSL/$\overline{H}$ = low

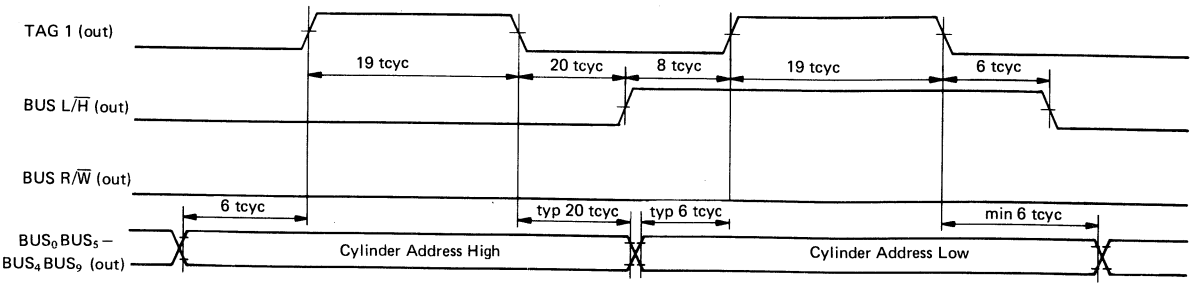
Pin	Output Signal Name	Abbreviation	Level
BUS_4/BUS_9	Reserve	O	low
BUS_3/BUS_8	Strobe Late	STBL	low
BUS_2/BUS_7	Strobe Early	STBE	low
BUS_1/BUS_6	Return to Zero	RTZ	high
BUS_0/BUS_5	Reserve	O	low

BUSL/$\overline{H}$ = high

Pin	Output Signal Name	Abbreviation	Level
BUS_4/BUS_9	Fault Clear	FCLR	low
BUS_3/BUS_8	Servo Offset Minus	SOFM	low
BUS_2/BUS_7	Servo Offset Plus	SOFP	low
BUS_1/BUS_6	Read Gate	RGATE	low
BUS_0/BUS_5	Write Gate	WGATE	low

(Note) On Cylinder and Seek Error are checked by Polling command.

Figure 38 Recalibrate Command Execution Timing (SMD)



BUSL/H = low

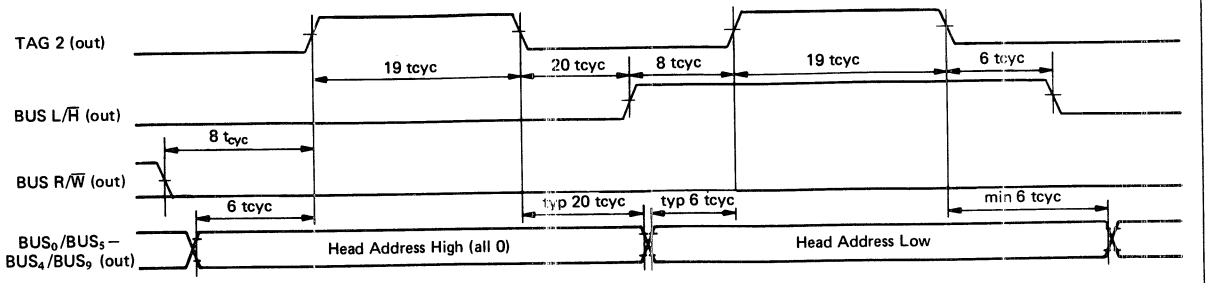
Pin	Output Signal Name	Abbreviation
BUS$_4$/BUS$_9$	Cylinder Address 9	CAD 9
BUS$_3$/BUS$_8$	Cylinder Address 8	CAD 8
BUS$_2$/BUS$_7$	Cylinder Address 7	CAD 7
BUS$_1$/BUS$_6$	Cylinder Address 6	CAD 6
BUS$_0$/BUS$_5$	Cylinder Address 5	CAD 5

BUSL/H = high

Pin	Output Signal Name	Abbreviation
BUS$_4$/BUS$_9$	Cylinder Address 4	CAD 4
BUS$_3$/BUS$_8$	Cylinder Address 3	CAD 3
BUS$_2$/BUS$_7$	Cylinder Address 2	CAD 2
BUS$_1$/BUS$_6$	Cylinder Address 1	CAD 1
BUS$_0$/BUS$_5$	Cylinder Address 0	CAD 0

(Note) After outputting the cylinder address, the minimum wait time until On Cylinder and Seek Error are returned from the drive is equivalent to that of Recalibrate operation.

Figure 39 Seek Command Execution Timing (SMD)



BUSL/H = low

Pin	Output Signal Name	Abbreviation
BUS_4/BUS_9	Head Address 9	HAD 9
BUS_3/BUS_8	Head Address 8	HAD 8
BUS_2/BUS_7	Head Address 7	HAD 7
BUS_1/BUS_6	Head Address 6	HAD 6
BUS_0/BUS_5	Head Address 5	HAD 5

BUSL/H = high

Pin	Output Signal Name	Abbreviation
BUS_4/BUS_9	Head Address 4	HAD 4
BUS_3/BUS_8	Head Address 3	HAD 3
BUS_2/BUS_7	Head Address 2	HAD 2
BUS_1/BUS_6	Head Address 1	HAD 1
BUS_0/BUS_5	Head Address 0	HAD 0

(Note) Head Address 5 – 9 are fixed at low level.

Figure 40 Head Selection Operation (SMD)

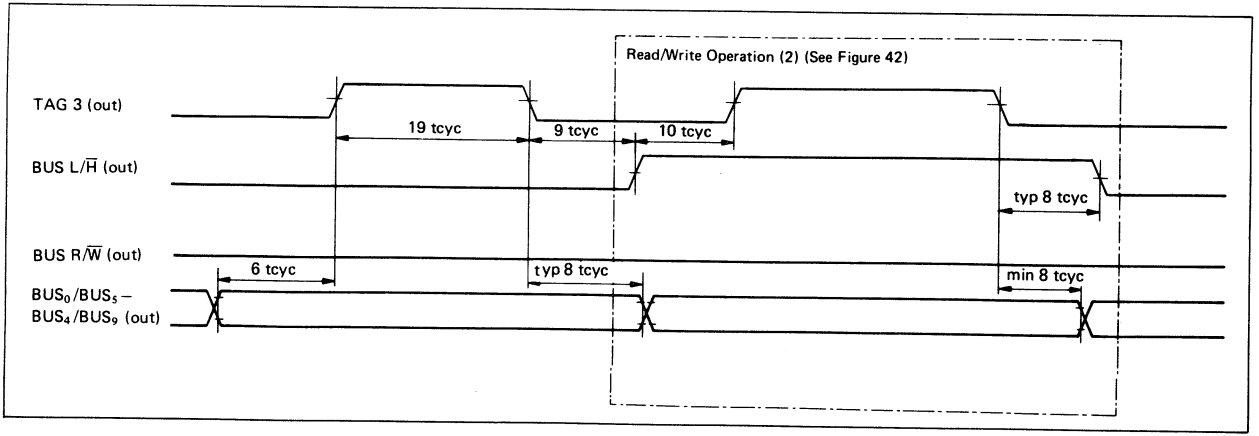


Figure 41 Read/Write Operation (1) (SMD)

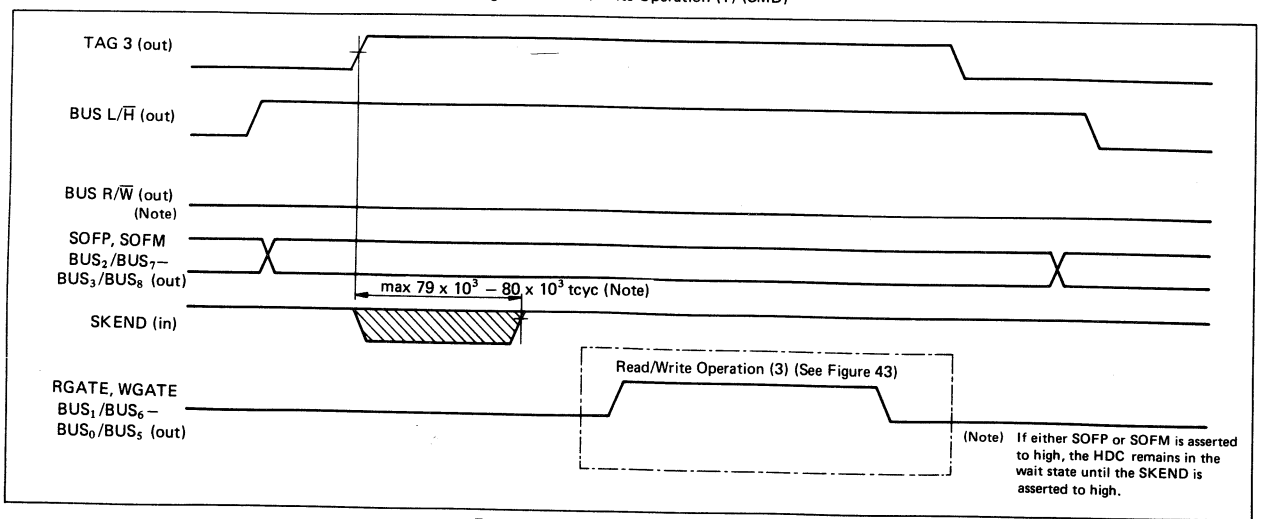


Figure 42 Read/Write Operation (2) (SMD)

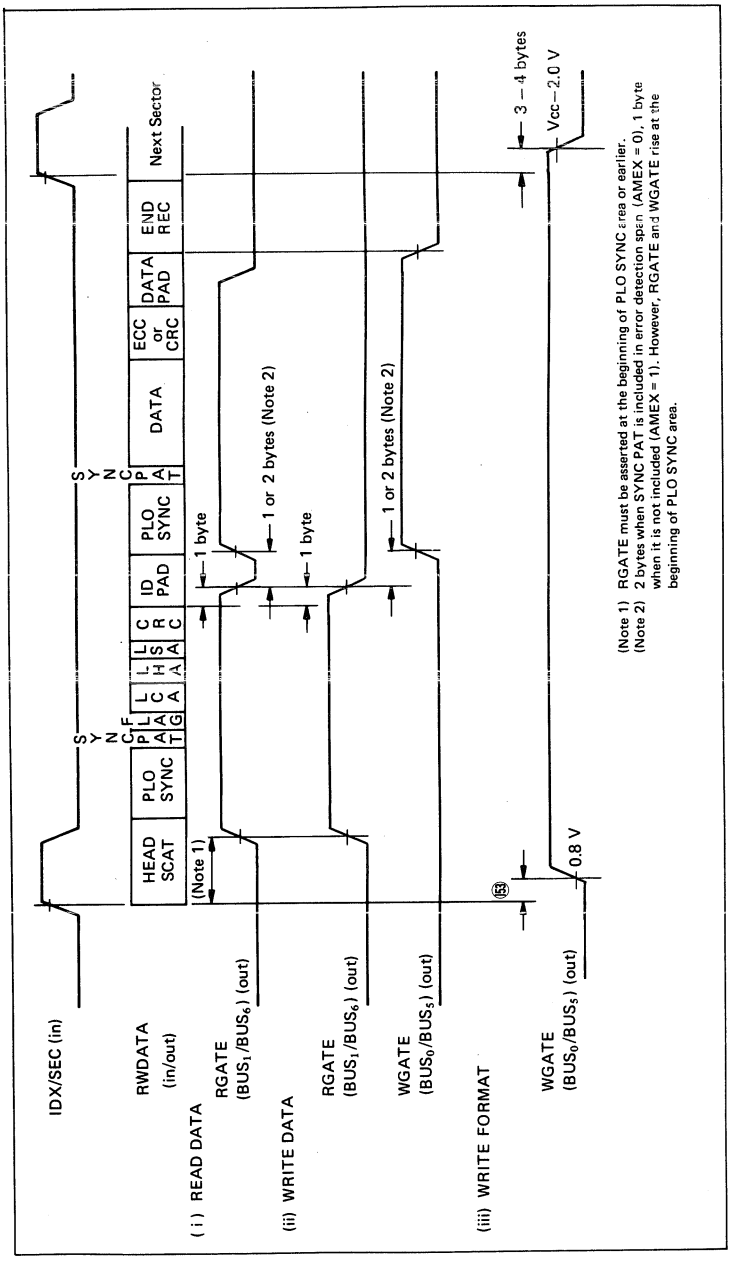
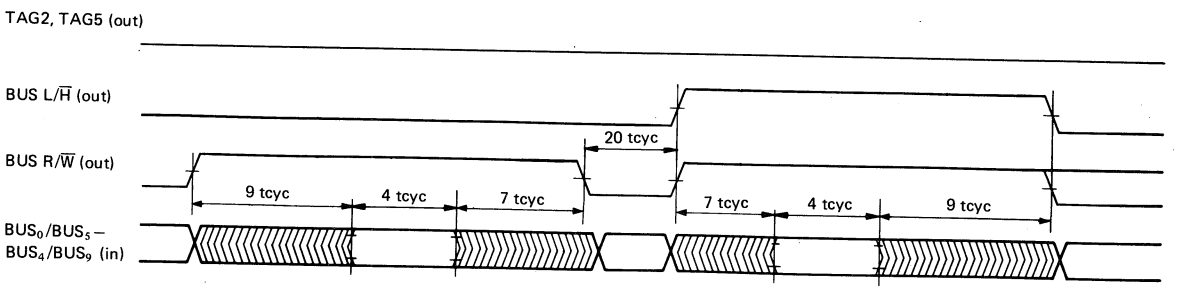


Figure 43 Read/Write Operation (3) (SMD)



BUSL/H = low

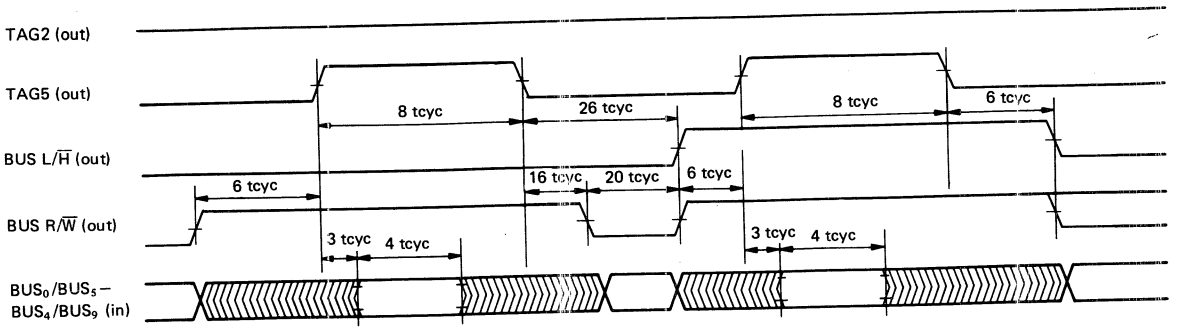
Pin	Input Signal Name	Abbreviation
BUS_4/BUS_9	—	—
BUS_3/BUS_8	—	—
BUS_2/BUS_7	*	*
BUS_1/BUS_6	*	*
BUS_0/BUS_5	*	*

BUSL/H = high

Pin	Input Signal Name	Abbreviation
BUS_4/BUS_9	Write Protected	WPRT
BUS_3/BUS_8	Fault	FLT
BUS_2/BUS_7	Seek Error	SKERR
BUS_1/BUS_6	On Cylinder	OCYL
BUS_0/BUS_5	Unit Ready	URDY

(Note 1) Names of signals which are read from a drive when the HDC is connected to the DK812S (Hitachi).
(Note 2) User Area

Figure 44 Sense Drive Operation (1) (SMD)



BUSL/H = low

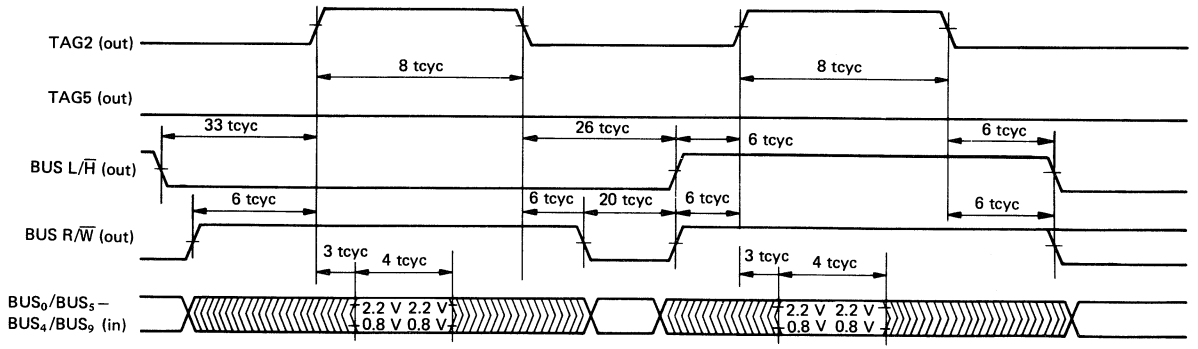
Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	–	–
BUS_3/BUS_8	–	–
BUS_2/BUS_7	* (Note 2)	*
BUS_1/BUS_6	*	*
BUS_0/BUS_5	SELECT ERROR	SELER

BUSL/H = high

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	Write Error 3	WERR3
BUS_3/BUS_8	Write Error 2	WERR2
BUS_2/BUS_7	Write Error 1	WERR1
BUS_1/BUS_6	Status Error 2	SERR2
BUS_0/BUS_5	Status Error 1	SERR1

(Note 1) Names of signals which are read from a drive when the HDC is connected to the DK812S (Hitachi).
(Note 2) User Area

Figure 45 Check Drive Status (2) (SMD)



BUSL/H̄ = low

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	–	–
BUS_3/BUS_8	–	–
BUS_2/BUS_7	* (Note 2)	*
BUS_1/BUS_6	* (Note 2)	*
BUS_0/BUS_5	Sector Address 32	SAD32

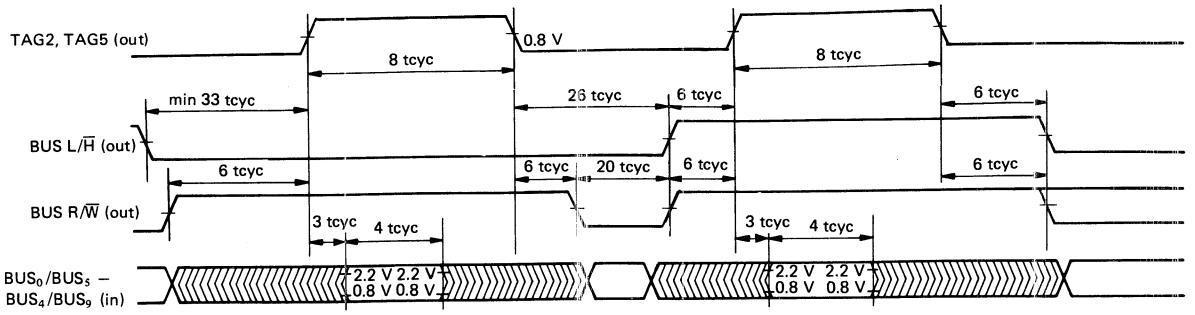
BUSL/H̄ = high

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	Sector Address 16	SAD16
BUS_3/BUS_8	Sector Address 8	SAD8
BUS_2/BUS_7	Sector Address 4	SAD4
BUS_1/BUS_6	Sector Address 2	SAD2
BUS_0/BUS_5	Sector Address 1	SAD1

(Note 1) Names of signals which are read from a drive when the HDC is connected to the DK812S (Hitachi).

(Note 2) User area

Figure 46 Check Drive Status (3) (SMD)



BUSL/$\overline{H}$ = low

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	—	—
BUS_3/BUS_8	—	—
BUS_2/BUS_7	* (Note 2)	*
BUS_1/BUS_6	* (Note 2)	*
BUS_0/BUS_5	Device Type 32	DTP32

BUSL/$\overline{H}$ = high

Pin	Input Signal Name (Note 1)	Abbreviation
BUS_4/BUS_9	Device Type 16	DTP16
BUS_3/BUS_8	Device Type 8	DTP8
BUS_2/BUS_7	Device Type 4	DTP4
BUS_1/BUS_6	Device Type 2	DTP2
BUS_0/BUS_5	Device Type 1	DTP1

(Note 1) Names of signals which are read from a drive when the HDC is connected to the DK812S (Hitachi).

(Note 2) User Area

Figure 47 Check Drive Status (4) (SMD)

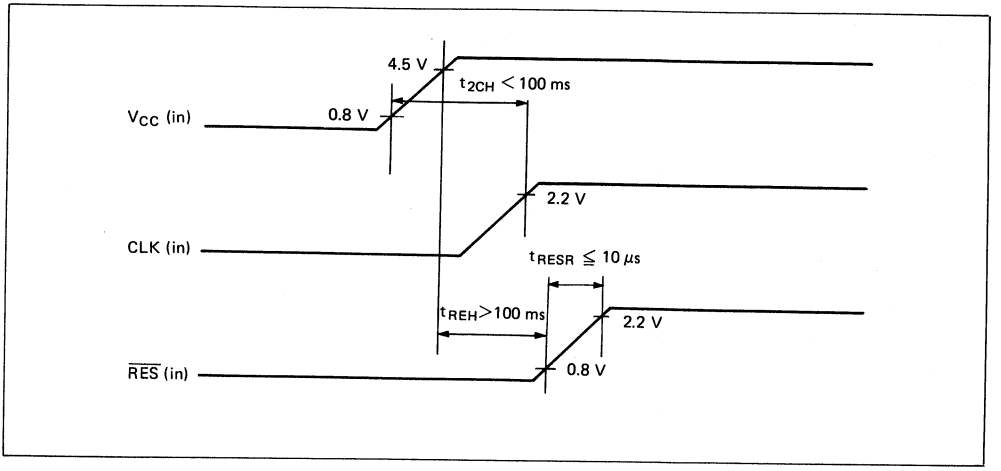


Figure 48 Timing Requirement during Power-On.

Refer to user's manual (No. 680-1-33A) and application note (No. 680-3-06A) for detail of this product.

Preliminary

HD64950S

File Data Processor (FDP)

Description

The HD64950S file data processor (FDP) is a hard disk controller LSI produced by 1.5-µm CMOS processing and designed to interface with a 16-bit microprocessing unit (MPU).

The FDP is placed between the host system and a disk drive unit to provide serial-to-parallel and parallel-to-serial data conversion, error checking, and automatic correction of data transferred to and from the disk drive unit.

This FDP provides separate controller section that functions as a file manager (FM: general-purpose microcomputer such as the H8/532, microprocessor-controlled high performance level, various disk drive interfaces, user-specific programmable data processing, compatibility with various standard buses, and expansibility.

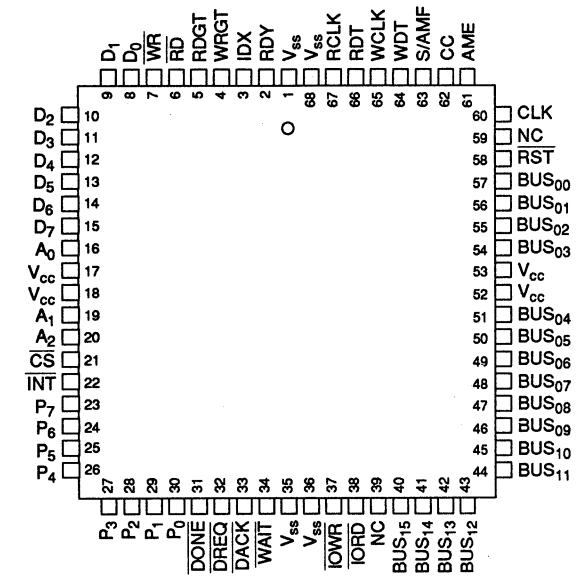
Features

- Versatility
  - Selectable data bus width:
    16-bit or 8-bit data bus (Only the 8-bit data bus is available in master mode.)
  - Selectable operation mode:
    Master mode or slave mode
  - Selectable DMA transfer mode:
    Burst transfer mode or cycle steal transfer mode
- High-speed transfer
  - Simultaneous data transfer between host systems and between hard disk drives
  - HDD transfer rate:
    Maximum 15 Mbits/s
  - Host transfer rate:
    Maximum 6 Mbytes/s (on 16-bit data bus)
    Maximum 4 Mbytes/s (on 8-bit data bus)
  - Multi-sector processing by controller available
  - Retry processing available
- Built-in data buffer
  - The FDP's data buffer consists of two 608-byte static memories (used as two 544-byte memories during DMA transfer).
- Error correction function
  - Selectable ECC polynominal (any)
  - Selectable ECC data length (4, 6, or 7 bytes)
- Highly flexible operation
  - Operations by combinations of 32 format commands
  - Wide sector length range (4 to 1088 bytes)
  - Free format
- Low power dissipation
  - CMOS circuit configuration reduces power dissipation (typically 200 mW)

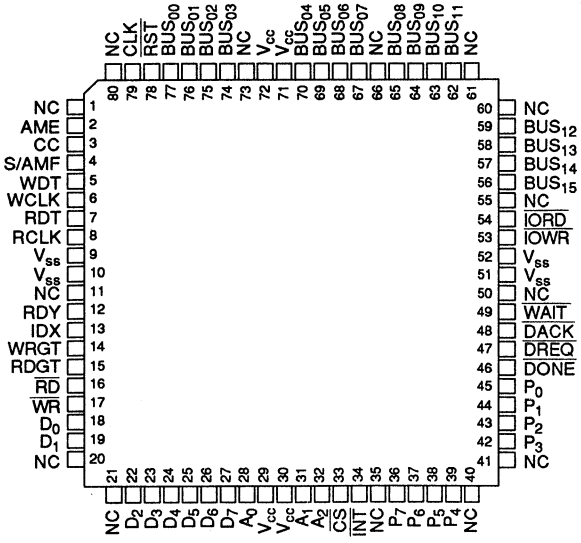
Ordering Information

Product Name	Package
HD64950SCP	68-pin PLCC (CP-68)
HD64950SFP	80-pin flat plastic package (FP-80A)

Pin Arrangement



(CP-68)



(FP-80A)
(Top View)

Pin Description

Class.	Pin No. (PLCC)	Symbol	Pin Name	Type	Function
Supply voltage, clock, reset	17, 18, 52, 53	V_{cc}		—	+5 V supply
	1, 35, 36, 68	V_{ss}		—	Ground (connected to the GND pin)
	60	CLK		Input	Inputs system clock
	58	$\overline{RST}$	Reset	Input	Resets the internal status of the FDP
File manager interface	6	$\overline{RD}$	Read	Input	Controls read operations: the FDP outputs data while this signal is asserted
	7	$\overline{WR}$	Write	Input	Controls write operations: the FDP fetches data at the rising edge of this signal
	21	$\overline{CS}$	Chip select	Input	Enables the file manager to access the FDP: the file manager reads/writes to the selected register in the FDP while $\overline{CS}$ is low
	16, 19, 20	A_0–A_2	$ADDRESS_0$–$ADDRESS_2$	Input	Direct register address lines for file manager access
	8–15	D_0–D_7	$DATABUS_0$–$DATABUS_7$	Input/output	Data lines between file manager and FDP
	22	$\overline{INT}$	Interrupt	Output (open drain)	Informs the file manager of the end of a command (open-drain output)

A_2	A_1	A_0	Register
0	0	0	AR
0	0	1	DTR
0	1	0	CEND
0	1	1	CMR
1	0	0	BUF0
1	0	1	BUF1

Pin Description (cont)

Class.	Pin No. (PLCC)	Symbol	Pin Name	Type	Function
Port	23–30	P_7–P_0	$PORT_7$–$PORT_0$	Input/ output	8-bit I/O port whose direction (input or output) is determined by the data direction register (DDR)
Drive interface	5	RDGT	Read gate	Output	Shows that data can be read from the disk drive
	4	WRGT	Write gate	Output	Shows that data can be written to the disk drive
	3	IDX	Index	Input	Inputs a track start signal
	2	RDY	Ready	Input	Shows that the disk drive is ready
	63	S/AMF	Sector, address mark found	Input	Indicates the start of a sector (inputs a sector pulse in hard sector mode or an address mark found signal in soft sector mode)
	67	RCLK	Read clock, reference clock	Input	Inputs disk read/write clock from the disk drive (the same frequency as the serial data transfer rate)
	66	RDT	Read data	Input	Inputs serial data from the disk drive (in NRZ code)
	65	WCLK	Write clock	Output	Outputs disk write clock to the disk drive (the same frequency as RCLK)
	64	WDT	Write data	Output	Contains serial data to be written to the disk (NRZ code is output to the disk drive in synchronism with WCLK)
	62	CC	Command complete	Input	Indicates that the disk drive is ready to receive a command
	61	AME	Address mark enable	Output	Instructs the ESDI disk drive to read or write an address mark

Pin Description

FDP in Slave Mode (MST bit of MDR 1 is 0)

Class.	Pin No.	Symbol	Pin Name	Type	Function
Host interface (slave mode)	32	$\overline{DREQ}$	DMA request	Output	Asserted when the FDP requests the DMAC to transfer data
	33	$\overline{DACK}$	DMA acknowledge	Input	Inputs data transfer timing during a DMA transfer: the FDP is enabled to read or write when this signal is low
	31	$\overline{DONE}$	Done	Input	Indicates the completion of DMA transfer
	37	$\overline{IOWR}$	I/O write	Input	Controls writing to the data buffer: the FDP fetches data at the rising edge of this signal
	38	$\overline{IORD}$	I/O read	Input	Controls reading from the data buffer: the FDP outputs data while this signal is asserted
	48–51, 54–57	BUS_{00}–BUS_{07}	BUS_{00}–BUS_{07}	Input/ output	Bi-directional data bus between host and data buffer (in both 16-and 8-bit modes)
	40–47	BUS_{08}–BUS_{15}	BUS_{08}–BUS_{15}	Input/ output	Bi-directional data bus (16-bit mode (B8 = 0) only)

B8 (MDR1)	Bus mode	BUS_{00}–BUS_{07}
1	8-bit mode	Data buffer
0	16-bit mode	Data buffer (Low byte)

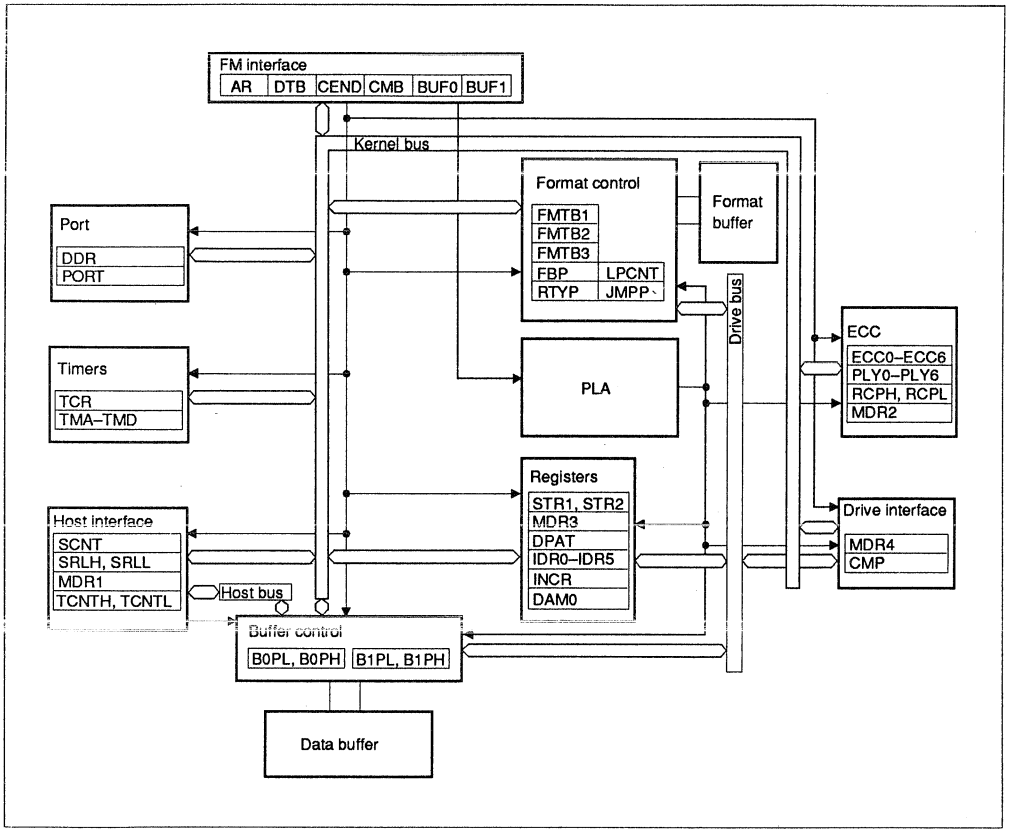
B8 (MDR2)	Bus mode	BUS_{08}–BUS_{15}
1	8-bit mode	Any (must be pulled up)
0	16-bit mode	Data buffer (High byte)

Pin Description

FDP in Master Mode (MST bit of MDR 1 is 1)

Class.	Pin No.	Symbol	Pin Name	Type	Function
Host interface (master mode)	32	$\overline{\text{DREQ}}$	DMA request	Input	Requests the FDP for a DMA transfer
	33	$\overline{\text{DACK}}$	DMA acknowledge	Output	Outputs data-transfer timing during a DMA transfer: the FDP sets this signal low before starting a read or write cycle
	31	$\overline{\text{DONE}}$	Done	Input	Indicates the end of a DMA transfer
	37	$\overline{\text{IOWR}}$	I/O write	Output	Indicates that the FDP is executing a write cycle: the FDP outputs data while this signal is asserted
	38	$\overline{\text{IORD}}$	I/O read	Output	Indicates that the FDP is executing a read cycle: the FDP fetches data at the rising edge of this signal
	34	$\overline{\text{WAIT}}$	Wait	Input	Requests the FDP to prolong the access cycle: the $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ signals are not negated while this signal is low
	48–51, 54–57	BUS_{00}–BUS_{07}	BUS_{00}–BUS_{07}	Input/ output	Bi-directional data bus (used to carry data buffer data during a DMA transfer)
	40–47	BUS_{08}–BUS_{15}	BUS_{08}–BUS_{15}	Input/ output	Not used in master mode (must be pulled up)

Block Diagram



The components shown in the block diagram are described below.

FM Interface: Sets data in the indirect registers, data buffer, and format buffer, based on data set in the direct registers by the FM. Decodes a direct command and displays that command's execution status.

Host Interface: Generates signals for data transfer and controls data transfer between host and data buffer.

Format Buffer: Stores format commands.

Format Control: Automatically writes into the format buffer any data that is set in indirect registers FMTB1, FMTB2, and FMTB3. Reads the data in the format buffer at the reception of a START command, and outputs its code to the PLA.

PLA: Controls the disk drive interface, ECC, registers, and formats according to format commands, at the reception of a START command.

Drive Interface: Reads, writes, or compares disk data under PLA control, then performs serial-to-parallel or parallel-to-serial data conversion.

ECC: Generates and performs ECC and CRC checks, and calculates ECC correction patterns.

Register: Stores data and mode information required to access the disk drive.

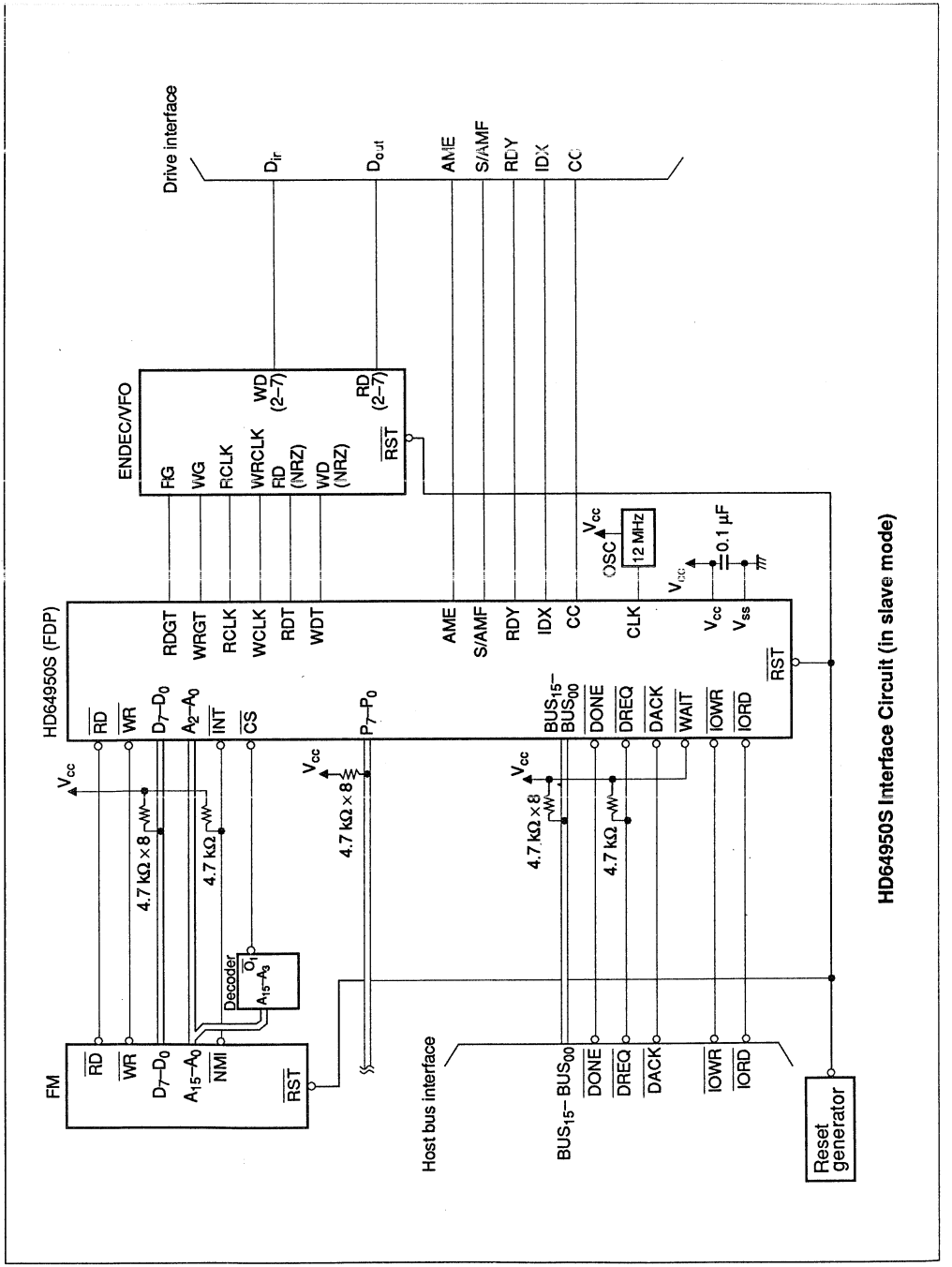
Data Buffer: Stores data transferred between disk drive and host. Also used as external RAM for the file manager.

Buffer Control: Switches buffers during command execution to prevent conflicts with accesses from disk drive and host.

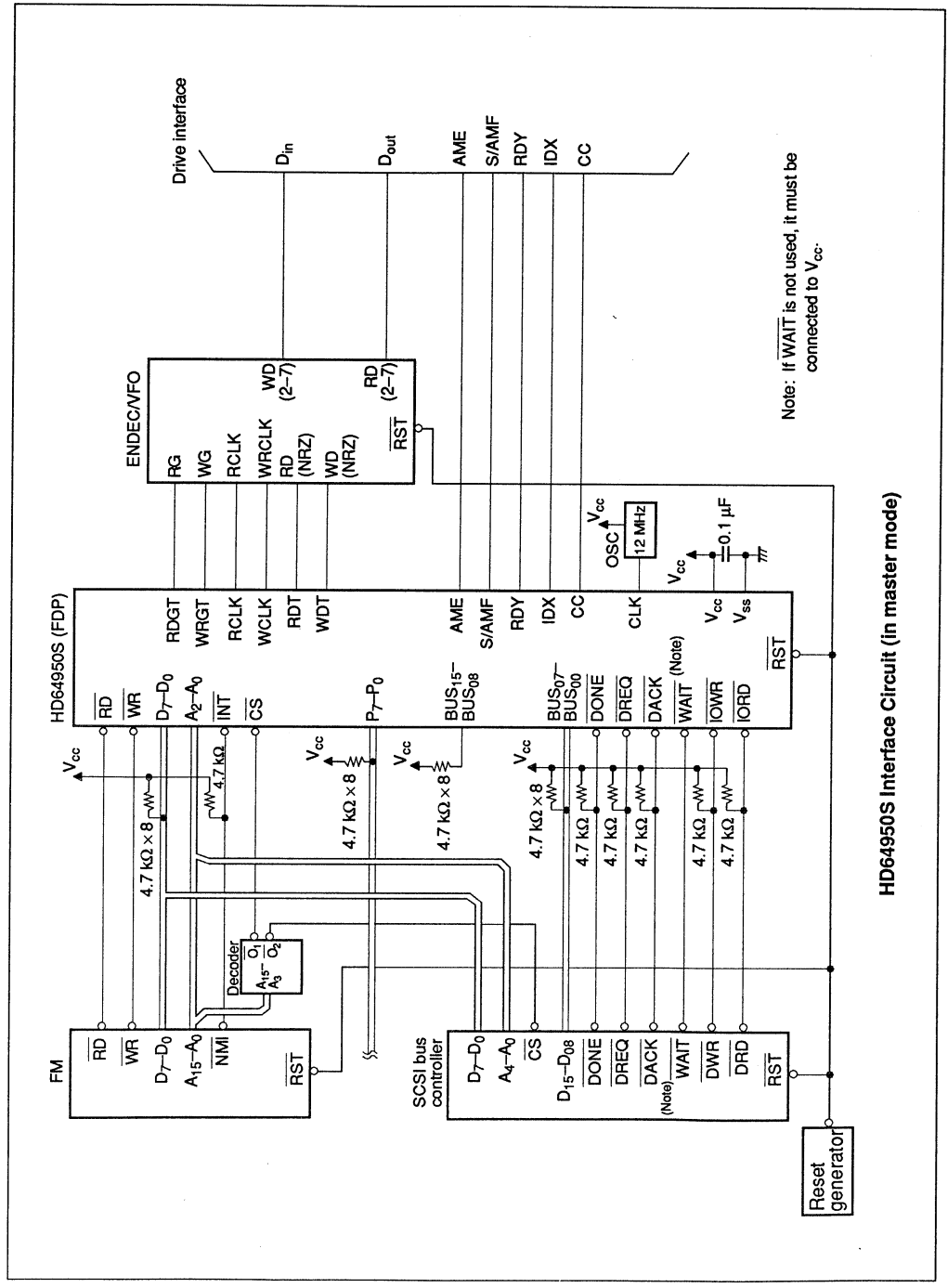
Timers: One timer monitors the number of retries and another monitors the index pulse input. Two additional general-purpose timers are available.

Port: I/O data port

Circuit Diagrams



HD64950S Interface Circuit (in slave mode)



HD64950S Interface Circuit (in master mode)

System Configuration

Figure 1 shows the configuration of a servo drive system containing the HD64950S FDP and controlled by software, and figure 2 shows the bus configurations when the FDP is in slave mode and master mode. In this example, the FM (file manager) is a general-purpose MPU (microprocessing unit) containing software to control the FDP, host bus controller, and drive.

After receiving a command over the host bus, the FM first decodes it to determine if any FDP processing (e.g., read/write of data) is required. If it is required, the FM starts the FDP and issues a command to it to begin the processing. Data is then transferred through the FDP and the host bus controller without FM intervention.

If an ECC error occurs during data read from the drive, the FDP informs the FM. If correction is required, the FM sets the FDP accordingly and issues STECC commands to correct the contents of the data buffer. The FDP supports multi-sector processing, during which time the FM can perform drive control such as servo processing set by software.

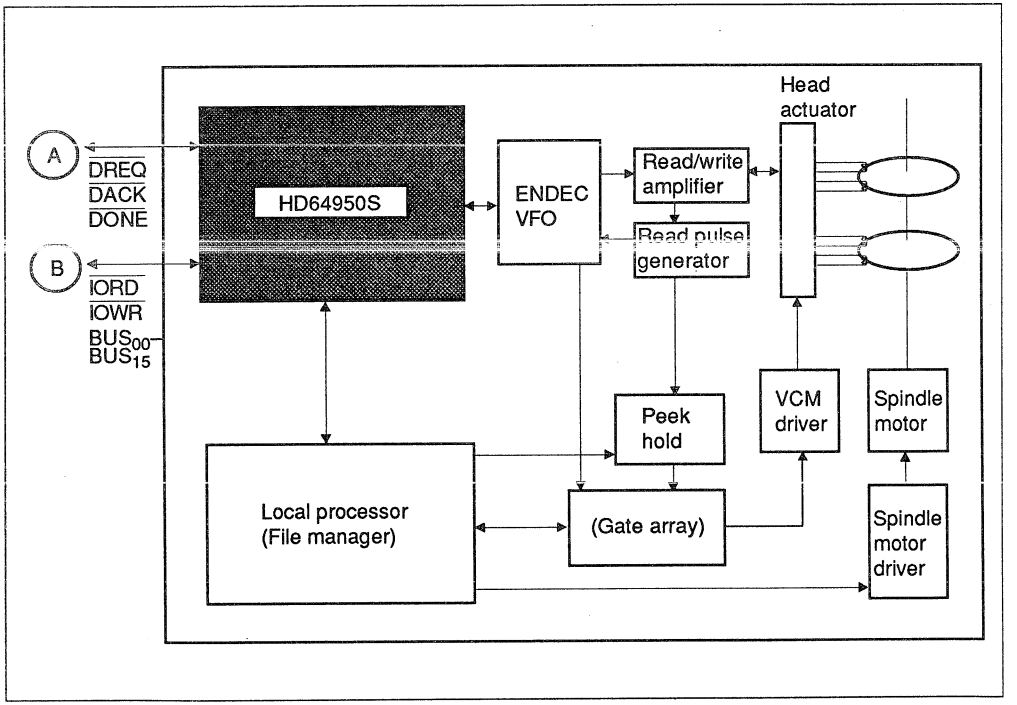


Figure 1 Servo Drive System

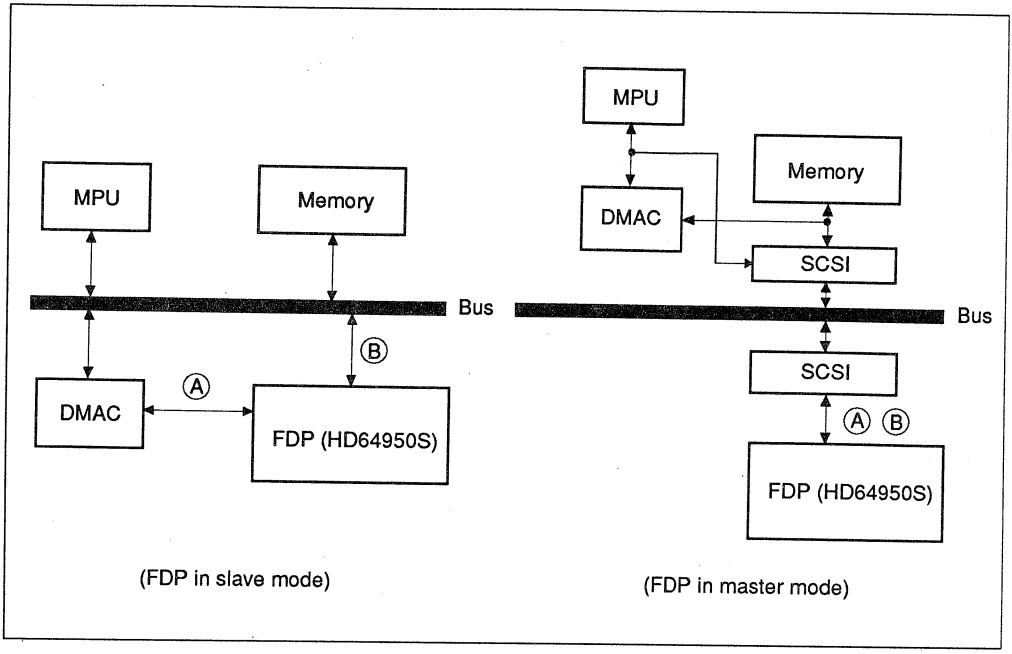


Figure 2 Bus Configurations

FDP Operating Procedure

To operate the FDP, the following preparation is necessary:

1. Set the indirect registers according to the required operation mode, using the direct registers of the file manager interface. Refer to the Registers section for details of direct and indirect registers and their settings.

   During write-formatting or write to the drive without host transfer, data must be stored in the data buffer.

2. Store format commands for the required operation mode in the format buffer. Refer to the Commands section for details of format commands and their storage in the format buffer.

   Note: When format buffer storage is completed, set the desired start address in the indirect register FBP (format buffer pointer).

   When a command other than the START command is issued, it is not necessary to store a format command in the format buffer.

3. Write an ABORT command, then write an FDP start command (START, LOAD, STORE, or STECC) in the direct register CMR (command register).

When these preparations are complete, the FDP will run according to the initialized values and commands. The operating status of the FDP is displayed in the direct register CEND. Determine the completion of an FDP operation by the contents of direct register CEND or by the $\overline{\text{INT}}$ (interrupt) signal.

Registers

The FDP has two kinds of register: direct registers which the file manager (FM) accesses directly with signals A_0 to A_2 and indirect registers which the FM accesses by means of direct registers AR (specifying the address of an indirect register) and DTR (containing data to be written to or read from the indirect register). Direct registers are listed in table 1 and indirect registers are listed in table 2. Refer to the Interface Functions section for details of register settings.

Table 1 Direct Registers

Symbol	Name	Description
AR	Address register	Specifies the address of an indirect register to be read or written
DTR	Data register	Data port used to access a specified indirect register: stores data to be written in a specified indirect register (write operation) or the contents of indirect register AR (read operation)
CMR	Command register	Stores a direct command (START, STECC, LOAD, STORE, or ABORT) for FDP start
CEND	Command end	Stores the operating status of the FDP and operation results (read-only register)
BUF0	Buffer 0	Data port for data buffer 0
BUF1	Buffer 1	Data port for data buffer 1

Table 2 Indirect Registers

Symbol	Name	Description
TCNTH, TCNTL	Transfer counter	Counts the number of bytes sent during DMA transfer (read-only register that loads the value of SRLL and SRLH and decrements them at each transfer)
MDR1–MDR4	Mode register 1 to mode register 4	Specifies the FDP operation mode (host, drive, timer, ECC, etc.)
IDR0–IDR5	ID register 0 to ID register 5	Specifies byte sync patterns and ID field information
DAM0	Data byte sync pattern	Specifies a data byte sync pattern
INCR	Increment register	Specifies automatic incrementation from IDR0 to IDR5
PORT	Data port	General-purpose I/O register
DDR	Data direction register	Specifies input or output for each port bit

Table 2 Indirect Registers (cont)

Symbol	Name	Description
FMTB1, FMTB2, FMTB3	Format buffer 1 to format buffer 3	Stores a format command which specifies the disk format
FBP	Format buffer pointer	Specifies the address of the format buffer to be accessed
RTYP	Retry pointer	Specifies an FBP value for retry (read-only register)
JMPP	Jump pointer	Specifies an FBP value for jumping (read-only register)
LPCNT	Loop counter	Specifies the number of jumps for the format buffer
TCR	Timer control register	Specifies operating periods for the three internal timers (TMA, TMC, and TMD)
RCPH, RCPL	Read correction pointer	Specifies bit location for ECC correction (read-only register)
SRLH, SRLL	Sector length	Specifies the sector data field length
B0PH, B0PL	Buffer 0 pointer	Specifies the address of a unit which read/writes to buffer 0
B1PH, B1PL	Buffer 1 pointer	Specifies the address of a unit which read/writes to buffer 1
ECC0–ECC6	ECC register 0 to ECC register 6	ECC generation/check registers which specify an ECC correction pattern (read-only registers)
PLY0–PLY6	Polynominal 0 to polynominal 6	Specify ECC polynominal
TMA	Timer A	General-purpose timer
TMB	Timer B	Timer for controlling the number of retries
TMC	Timer C	Watch dog timer for IDX pulse
TMD	Timer D	General-purpose timer
STR1, STR2	Status 1, status 2	Indicate the cause of FDP abnormal termination and the status of the disk drive
CMP	Comparator	Compares byte sync patterns and indicates the result (read-only register)
DPAT	Data pattern	Specifies data to be written in data fields (for formatting)
SCNT	Sector counter	Specifies the total number of sectors to be transferred to or from the host

Table 3 Direct Register Addresses and Structures

Address (A_0–A_2)	Register Name	R/W	Data Bits							
			7	6	5	4	3	2	1	0
$00	AR	R/W								
$01	DTR	R/W								
$02	CEND	R	BSY	ERR	HBSY	INT	BFACS		BUSINT	
$03	CMR	R/W						C2	C1	C0
$04	BUF0	R/W								
$05	BUF1	R/W								

Note: ▨ : Expansion bit (set to 0 in writing. Only 0 is read in reading.)

Bit Description

BSY (Busy): Shows that disk drive is being accessed, or error correction processing is being executed. BSY is set when a START or STECC command is stored in the CMR, and is reset when command execution is completed.

ERR (Error): Set when the operation is terminated by an error; reset when data is written in the CMR.

HBSY (Host Busy): Shows that data is being accessed from the host. HBSY is set during a data transfer between the FDP and the host, and is reset when all data has been transferred.

INT (Interrupt): Set by an interrupt caused by the normal completion or abnormal termination of operation; reset when data is written into the CMR.

BFACS (Buffer Access): Shows that data is being accessed between the disk drive and data buffer. BFACS is set during while access, and is reset when all data is transferred.

BUSINT (Bus Interrupt): Shows that the bus was interrupted during data transfer from the host. BUSINT is set when $\overline{\text{DONE}}$ is input during a DMA transfer (in master mode, this bit is set even when no DMA transfer is in progress), and is reset when data is written in the CMR.

Table 4 Indirect Register Addresses and Structures

Address (AR)		Register Name	R/W	Data Bits							
7654 3210	(HEX)			7	6	5	4	3	2	1	0
0000 0000	00	IDR0	R/W								
0000 0001	01	IDR1	R/W								
0000 0010	02	IDR2	R/W								
0000 0011	03	IDR3	R/W								
0000 0100	04	IDR4	R/W								
0000 0101	05	IDR5	R/W								
0000 1000	08	INCR	R/W			IFG5	IFG4	IFG3	IFG2	IFG1	IFG0
0000 1001	09	CMP	R								
0000 1010	0A	TCNTL	R								
0000 1011	0B	TCNTH	R								
0000 1100	0C	SRLL	R/W								
0000 1101	0D	SRLH	R/W								
0001 0000	10	LPCNT	R/W								
0001 0001	11	JMPP	R								
0001 0010	12	RTYP	R								
0001 0011	13	FBP	R/W								
0001 0100	14	STR1	R/W	SNF	IBSNF	DBSNF	VER	CCE	CRFLT	FLG	
0001 0101	15	STR2	R/W	TOA	TOB	TOC	TOD	DR		CC	
0001 1000	18	TCR	R/W	TDC1	TDC0	TCC1	TCC0			TAC1	TAC0
0001 1001	19	TMA	R/W								
0001 1010	1A	TMB	R/W								
0001 1011	1B	TMC	R/W								
0001 1100	1C	TMD	R/W								
0001 1101	1D	MDR3	R/W							FLEN	
0001 1111	1F	RCPL	R								

Table 4 Indirect Register Addresses and Structures (cont)

Address (AR)		Register Name	R/W	Data Bits							
7654 3210	(HEX)			7	6	5	4	3	2	1	0
0010 0000	20	RCPH	R								
0010 0001	21	ECC0	R								
0010 0010	22	ECC1	R								
0010 0011	23	ECC2	R								
0010 0100	24	ECC3	R								
0010 0101	25	ECC4	R								
0010 0110	26	ECC5	R								
0010 0111	27	ECC6	R								
0010 1010	2A	B0PL	R/W								
0010 1011	2B	B0PH	R/W								
0010 1100	2C	B1PL	R/W								
0010 1101	2D	B1PH	R/W								
0010 1110	2E	MDR1	R/W	MST	B8	NIMK	AIMK		DMA	DMAM	DRBF
0010 1111	2F	MDR2	R/W	ECM1	ECM0	ECCI	CRCI	BSEX	ZCK2	ZCK1	ZCK0
0011 0000	30	DDR	R/W								
0011 0001	31	PORT	R/W								
0011 0010	32	PLY0	R/W								
0011 0011	33	PLY1	R/W								
0011 0100	34	PLY2	R/W								
0011 0101	35	PLY3	R/W								
0011 0110	36	PLY4	R/W								
0011 0111	37	PLY5	R/W								
0011 1000	38	PLY6	R/W								
0011 1011	3B	DPAT	R/W								
0011 1100	3C	FMTB1	R/W								

Table 4 Indirect Register Addresses and Structures (cont)

Address (AR)		Register Name	R/W	Data Bits							
7654 3210	(HEX)			7	6	5	4	3	2	1	0
0011 1101	3D	FMTB2	R/W								
0011 1110	3E	FMTB3	R/W								
0011 1111	3F	DAM0	R/W								
0100 0100	44	MDR4	R/W				HS		BURST	BFM	
0100 0101	45	SCNT	R/W								

Notes: 1. ▨: Expansion bit (set to 0 in writing. Only 0 is read in reading.)
2. Only 0 can be written in indirect registers STR1 and STR2.

Bit Description

IFG0–IFG5: Specifies the register (IDR0 to IDR5) to be incremented. For example, IDR0 is incremented after the execution of format command IDINC if IFG0 is set to 1.

SNF (Sector Not Found): Set if no sector is found after the specified number of rotations.

IBSNF (ID Byte Sync Pattern Not Found): Set if the byte sync pattern of the ID field does not match.

DBSNF (Data Byte Sync Pattern Not Found): Set if the byte sync pattern of the data field does not match.

VER (Verify Error): Set if an unmatch error is detected by verify/comparison processing.

CCE (Check Code Error): Set if a CRC/ECC error occurs.

CRFLT (Correction Fault): Set if no ECC error correction pattern or pattern location is detected.

FLG (Flag Error): Set if flags do not match (but CRC/ECC is operating correctly).

TOA–TOD (Timer Overflow A to D): Set if the corresponding timer (TMA to TMD) overflows.

DR (Drive Ready): Set while the RDY signal is input.

CC (Command Complete): Set while the CC signal is input

TAC0/1, TCC0/1, TDC0/1: Specify the decrementation clock cycles of timers TMA, TMC, and TMD. Cycles are determined to be fractions of the CLK frequency, as follows:

(Timer n Control 0/1)

TnC1	TnC0	TMn Input Clock
0	0	$1/2^7$ of source clock (CLK)
0	1	$1/2^{11}$ of source clock (CLK)
1	0	$1/2^{15}$ of source clock (CLK)
1	1	$1/2^{19}$ of source clock (CLK)

FLEN (Flag Enable): Set to 1 when flag check is enabled.

MST (Master Mode): Set to 1 when FDP is in master mode.

B8 (8-Bit Bus Mode): Set to 1 when FDP is in 8-bit host bus mode.

NIMK (Normal Interrupt Mask): Set to 1 if interrupt signals are to be masked at the completion of operation. (START (normal completion or abnormal termination) or STECC (normal completion) command)

AIMK (Abnormal Interrupt Mask): Set to 1 if interrupt signals are to be masked at the termination of operation. (START, STECC, LOAD, or STORE command)

DMA (DMA Enable Mode): Set to 1 if DMA transfer is to be enabled during command execution.

DMAM (DMA Mode): Specifies the switching mode of the data buffer. DMAM is set to 1 during format command execution.

DRBF (Drive Buffer Select): Specifies the data buffer to be used first in DMA transfer. 0 specifies that buffer 0 is used first.

ECM0/1 (ECC Mode 0/1): Specifies the ECC data length, as follows:

ECM1	ECM0	ECC Data Length
0	0	4 bytes
0	1	6 bytes
1	0	7 bytes

ECCI (ECC Initial): Specifies the initial ECC value. 0 specifies that the initial value is all zeros; 1 specifies that it is all ones.

CRCI (CRC Initial): Specifies the initial CRC value. 0 specifies that the initial value is all zeros; 1 specifies that it is all ones.

BSEX (Byte Sync Pattern Excluded): Set to 0 if no byte sync pattern is to be included in the ECC/CRC operation.

ZCK0/1/2 (Zero Check 0/1/2): Specifies the maximum correctable burst error length, as follows:

ZCK2	ZCK1	ZCK0	Max Correctable Burst Error Length
0	0	0	16 bits
0	0	1	11 bits
0	1	0	10 bits
0	1	1	9 bits
1	0	0	8 bits
1	0	1	7 bits
1	1	0	6 bits
1	1	1	5 bits

HS (Hard Sector): Specifies the drive interface mode. 0 specifies soft sector mode; 1 specifies hard sector mode.

BURST (Burst Mode): Specifies the transfer mode. 0 specifies cycle steal mode; 1 specifies burst mode.

BFM (Buffer Mode): Specifies the data buffer mode. 0 specifies that two data buffers are used, 1 specifies that one is used.

Direct Registers

The direct registers are described below.

Address Register (AR)

Bit Configuration

AR Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$00
	Indirect register address									

Function

The AR latches the address of the indirect register to be accessed by the DTR.

Note: Do not specify an address which is not assigned to an indirect register.

Data Register (DTR)

Bit Configuration

DTR Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	Any	$01
Contents of specified indirect register										

Function

The DTR acts as a data port for accessing an indirect register. It stores data which is to be written to or has been read from the indirect register specified by the AR.

Command End (CEND)

Bit Configuration

CEND Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R	00	$02
BSY	ERR	HBSY	INT	BFACS		BUSINT				

Bit Description

BSY (Busy): Is high (1) when a START or STECC command is being executed, to indicate that accessible registers are limited. Refer to the File Manager Interface section for further details.

ERR (Error): Goes high (1) when a command is terminated abnormally or a timer overflows. ERR goes high under any of the following conditions:

- When an error occurs and the SNF, IBSNF, DBSNF, VER, CCE, CRFLT, or FLG bit of status register 1 (STR1) goes high.
- When a timer overflows and the TOA, TOB, TOC, or TOD bit of status register 2 (STR2) goes high.
- When $\overline{\text{DONE}}$ is input during a DMA transfer and the DMA transfer is aborted.
- When the FDP is in master mode, ERR is set whenever $\overline{\text{DONE}}$ is input

To reset ERR to low, clear the high bits in STR1 or STR2 and issue a direct command.

HBSY (Host Busy): Goes high (1) when DMA transfer is performed, to indicate that accessible registers are limited. Refer to the File Manager Interface section for further details. HBSY goes high (1) under any of the following conditions:

- When a LOAD or STORE command is issued while the DMA bit of MDR1 is 1.
- When a DMAW command is executed while the DMA bit of MDR1 is 1.
- When a WIDB, WDTB, RIDB, RDTB, or VDTB command is executed while the DMA bit of MDR1 is 1, and data transfer between the data buffer and disk drive has started or verification of data has started.

HBSY is reset under any of the following conditions:

- When the specified amount of data (SRLH/SRLL × SCNT) has been transferred.

  Note: HBSY is reset within 1.5 CLK after $\overline{\text{IOWR}}$ or $\overline{\text{IORD}}$ of the last data transfer is asserted. Therefore, the HBSY bit may be reset while $\overline{\text{IOWR}}$ or $\overline{\text{IORD}}$ is still asserted.

- When $\overline{\text{DONE}}$ is asserted.
- When a disk access error (which sets the SNF, IBSNF, DBSNF, VER, CCE, or FLG bit of STR1, or the TOB or TOC bit of STR2) occurs.
- When the ABORT command is issued.

INT (Interrupt): Indicates an interrupt caused by the completion of command execution. Interrupts can be masked in different ways at normal completion and abnormal termination by the NIMK and AIMK bits of MDR1.

- INT set by completion of command execution INT is set when START, STECC command execution is completed.
- INT set by abnormal termination of command execution INT is set when START, STECC, LOAD, or STORE command execution is terminated abnormally by an error which sets the ERR bit of CEND.

INT is cleared when another command is issued.

BFACS (Buffer Access): Set to 1 during data transfer between data buffer and drive, or during data verification. BFACS is set only during execution of the WIDB, WDTB, RIDB, or VDTB command.

BUSINT (Bus Interrupt): Set to 1 when DMA transfer between host and data buffer is terminated by $\overline{\text{DONE}}$ input, except when $\overline{\text{DONE}}$ is asserted during the transfer of the last of the specified amount of data (set by SRLL/SRLH × SCNT) when the FDP is in slave mode (when the MST bit of MDR1 is 0).
When the FDP is in master mode, BUSINT is set whenever $\overline{\text{DONE}}$ is input.

BUSINT is cleared when another command is issued.

Command Register (CMR)

Bit Configuration

CMR Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$03
					C2	C1	C0			

Function

The CMR enables direct command activation by specifying the command code of the START, STECC, LOAD, or STORE command for execution. The specified direct command can be issued only when both the BSY and HBSY bits of CEND are low (0).

To abort the execution of the specified direct command, issue the ABORT command. (The ABORT command can be issued regardless of the BSY and HBSY values.) The direct commands codes are listed below. For details on direct command functions, refer to the Direct Commands section.

Command	Command Code
START	$01
STECC	$02
LOAD	$04
STORE	$06
ABORT	$00

Notes: 1. Do not use any other command codes.
2. Make sure that the contents of status registers STR1 and STR2 are cleared before writing a command (except the ABORT command) code to the CMR.

Buffer Registers 0 and 1 (BUF0, BUF1)

Bit Configuration

BUF0 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$04
Buffer 0 data										

BUF1 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$05
Buffer 1 data										

Function

BUF0 and BUF1 act as data ports. They access data from the data buffer address specified by the buffer pointer.

Note: Always set the buffer pointer before accessing the buffer.

Indirect Registers

The main indirect registers are described below.

Status Register 1 (STR1)

Bit Configuration

STR Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$14
SNF	IBSNF	DBSNF	VER	CCE	CRFLT	FLG				

Function

STR1 indicates the result of a command's execution. If a command is terminated because of an error, the appropriate data bit of STR1 is set to 1. However, if retry succeeds, no data bits are set.

The set bits can be reset to 0 by the FM writing 0 to them. Conditions for setting the data bits in STR1 vary with commands. Refer to the Commands section for details.

Note: Under some conditions, set bits may be reset to 0 by writing 1 to them.

Bit Description

SNF (Sector not found)

Set When	Commands
No sector is detected • IDX and SCT are not input • ID byte sync pattern is not detected	WPUIS, RIDB, WABSC, RIDS, WTISA, VID
The buffer cannot be accessed by the disk drive. (Either the IBSNF or DBSNF bit is also high)	WIDB, WDTB, RIDB, RDTB, VDTB

IBSNF (ID Byte Sync Pattern Not Found)

Set When	Commands
ID byte sync pattern is not detected	RIDB, RIDS, VID
The buffer cannot be accessed by the disk drive (both the SNF and DBSNF bits are also high)	WIDB, WDTB, RIDB, RDTB, VDTB

DBSNF (Data Byte Sync Pattern Not Found)

Set When	Commands
Data byte sync pattern is not detected	RDTB, RDTS, VDTB
The buffer cannot be accessed by the disk drive (both the SNF and IBSNF bits are also high)	WIDB, WDTB, RIDB, RDTB, VDTB

VER (Verify Error)

Set When	Commands
Drive data does not match the contents of the buffer or the IDR	VID, VDTB

CCE (Check Code Error)

Set When	Commands
A CRC or ECC error occurs	CCRC, CECC, VCRC, VECC, VCRCR, VECCR, VCRCW, VECCW

CRFLT (Correction Fault)

Set When	Commands
No ECC error correction pattern was obtained	STECC

FLG (Flag Error)

Set When	Commands
The flag bytes do not match (but no CRC or ECC error has occurred)	VCRC, VECC, VCRCR, VECCR, VCRCW, VECCW

Status Register 2 (STR2)

Bit Configuration

STR2 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00[Note]	$15
TOA	TOB	TOC	TOD	DR		CC				

Note: The DR and CC bits are set by inputs from the FDP's pins.

Function

STR2 indicates the status of timers and input pins.

Bit Description

TOA, TOB, TOC, and TOD (Timer Overflows A, B, C, and D): Set when the corresponding timer (TMA, TMB, TMC, and TMD) overflows. The set bits can be reset by the FM writing 0 to them, but in some cases they may be reset by writing 1 to them. .

DR (Drive Ready) and CC (Command Complete): Indicate the status of the RDY and CC pins, as follows:

RDY Pin	DR (STR2)
Low	0
High	1

CC Pin	CC (STR2)
Low	0
High	1

Mode Register 1 (MDR1)

Bit Configuration

MDR1 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$2E
MST	B8	NIMK	AIMK		DMA	DMAM	DRBF			

Function

MDR1 controls data transfers and interrupts.

Bit Description

MST (Master Mode): Specifies the mode of the FDP.

- MST = 0: The FDP functions as a slave and the DMAC controls the DMA transfer.
- MST = 1: The FDP functions as the master, controlling the DMA transfer. Only bus lines BUS_{00} to BUS_{07} are used (8-bit data bus); bus lines BUS_{08} to BUS_{15} should be pulled up.

Refer to the Host Interface section for further details of master details of master and slave modes.

B8 (8-Bit Bus Mode): Specifies the width of the host interface bus. When the FDP is in master mode, B8 must always be 1 (8-bit data bus). When the FDP is in slave mode, B8 specifies the width of the host interface bus.

- B8 = 0: 16-bit data bus
- B8 = 1: 8-bit data bus (Only bus lines BUS_{00} to BUS_{07} are used; bus lines BUS_{08} to BUS_{15} should be pulled up.)

NIMK (Normal Interrupt Mask): Specifies whether interrupts are to be masked at the completion of a command. Setting this bit affects the INT bit of the CEND register and the $\overline{INT}$ signal.

- NIMK = 0

  Interrupts are not masked at the completion of a command. If the execution of START command is completed, the FDP sets the INT bit of the CEND register and asserts the $\overline{INT}$ signal. If the execution of a STECC command is completed, the FDP sets the INT bit of the CEND register and asserts the $\overline{INT}$ signal.

- NIMK = 1

  Interrupts are masked at the completion of a command. The FDP dose not set the INT bit of CEND and does not assert the $\overline{INT}$ signal, even when the execution of the START command completed. The FDP does not set the INT bit of CEND and does not assert the $\overline{INT}$ signal, even when the execution of the STECC command is completed.

AIMK (Abnormal Interrupt Mask): Specifies whether interrupts are to be masked at the abnormal termination of a command. Setting this bit affects the INT bit of CEND and the $\overline{INT}$ signal.

- AIMK = 0

  Interrupts are not masked at the abnormal termination of a command. If an error which would set the ERR bit of CEND is detected during the execution of a START, STECC, LOAD, or STORE command, the FDP sets the INT bit of CEND and asserts the $\overline{INT}$ signal.

- AIMK = 1

  Interrupts are masked at the abnormal termination of a command. The FDP does not set the INT bit of CEND and does not assert the $\overline{INT}$ signal, even when an error which would set the ERR bit of the CEND register is detected during the execution of the START, STECC, LOAD, or STORE command.

DMA (DMA Enable Mode): Specifies whether the FDP can start DMA transfer during the execution of a command. Set DMA to 1 to enable DMA transfers to and from the host.

- DMA = 0: Disables DMA transfer, even when a command which starts DMA transfer is executed.
- DMA = 1: Enables DMA transfer for commands which request DMA transfer.

Commands which request DMA transfer are:
- Format commands such as DMAW, WIDB, WDTB, RTDB, and VDTB
- LOAD and STORE commands

DMAM (DMA Mode): Specifies the data buffer switching mode.

- DMAM = 0

  Data buffers are switched each time one sector is transferred. In this mode, the BFM bit of MDR4 must be specified as follows, according to sector size:

  BFM = 0: Sector size of 4 to 544 bytes
  BFM = 1: Sector size of 545 to 1088 bytes

- DMAM = 1

  Data buffers are switched when address 543 is accessed. This switch has no connection with the value of the BFM bit of MDR4.

If two or more format commands that access buffers are executed, each access begins at the address after the address accessed by the preceding command.

Note: DMAM = 1 is valid only for the execution of a format command. In this mode, the DMA bit of MDR1 must be 0.

Refer to the Data Transfer Function section for more details.

DRBF (Drive Buffer Select): Selects the data buffer to be used first for DMA transfer.

- DRBF = 0: BUF0 is used first.
- DRBF = 1: BUF1 is used first.

DRBF is valid as soon as it is set, but it only indicates the data buffer to be used first; not the buffer currently being used.

Mode Register 2 (MDR2)

Bit Configuration

MDR2 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$2F
ECM1	ECM0	ECCI	CRCI	BSEX	ZCK2	ZCK1	ZCK0			

Function

MDR2 specifies details relating to ECC/CRC.

Bit Description

ECM1 and ECM0 (ECC Modes 1 and 0): Specify the ECC byte length to be used in the execution of an ECC format command or STECC command, as follows:

ECM1	ECM0	Number of ECC Bytes
0	0	4
0	1	6
1	0	7
1	1	Reserved

ECCI (ECC Initial): Specifies the initial ECC value to be used by an ECC-initializing format command.

- ECCI = 0: The initial ECC value is all zeros.
- ECCI = 1: The initial ECC value is all ones.

CRCI (CRC Initial): Specifies the initial CRC value to be used by a CRC-initializing format command.

- CRCI = 0: The initial CRC value is all zeros.
- CRCI = 1: The initial CRC value is all ones.

BSEX (Byte Sync Pattern Excluded): Specifies whether a format command that performs an ECC or CRC operation includes a byte sync pattern.

- BSEX = 0: A byte sync pattern is included in the ECC or CRC operation.
- BSEX = 1: No byte sync pattern is included in the ECC or CRC operation.

ZCK2, ZCK1, and ZCK0 (Zero Checks 2, 1, and 0): Specify the maximum length of burst error that can be corrected during the calculation of an ECC error correction pattern by the STECC command.

ZCK2	ZCK1	ZCK0	Maximum Correctable Burst Error Length
0	0	0	16 bits
0	0	1	11 bits
0	1	0	10 bits
0	1	1	9 bits
1	0	0	8 bits
1	0	1	7 bits
1	1	0	6 bits
1	1	1	5 bits

Refer to the Error Checking and Correction Function section for details of ECC and CRC operations.

Mode Register 3 (MDR3)

Bit Configuration

MDR3 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$1D
						FLEN				

Function

MDR3 specifies details relating to disk formatting.

Bit Description

FLEN (Flag Enable): Indicates if flag comparison is required with the VID command.

- FLEN = 1

  The contents of IDR5 are checked as a flag byte during the execution of a VID command. If only the flag bytes do not match (but all other information matches and no ECC/CRC error occurs), the FDP sets the FLG bit of STR1 and the ERR bit of CEND and completes the START command execution.

  A verification ECC/CRC command that checks for flag byte errors must be executed after a CRC/ECC check, so the VID command must be followed by a VCRC, VCRCR, VCRCW, VECC, VECCR, or VECCW command.

- FLEN = 0: No flag comparison is performed

Mode Register 4 (MDR4)

Bit Configuration

MDR4 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$44
			HS		BURST	BFM				

Function

MDR4 specifies the type of disk drive and other details relating to data transfer.

Bit Description

HS (Hard Sector): Specifies the type of disk drive and affects the sequence of WAFSA and WTISA commands.

- HS = 0: Soft sector mode
- HS = 1: Hard sector mode

BURST (Burst Mode): Specifies the DMA transfer mode when the FDP is in slave mode. The DMA transfer mode in FDP master mode is always burst mode.

- BURST = 0 (cycle steal mode)

  In this mode, the FDP negates $\overline{\text{DREQ}}$ when $\overline{\text{DACK}}$ is asserted in response to the assertion of $\overline{\text{DREQ}}$. The FDP continues to negate $\overline{\text{DREQ}}$ while $\overline{\text{DACK}}$ is asserted, and it continues to assert $\overline{\text{DREQ}}$ until the DMA transfer is completed (all sectors are transferred) or aborted ($\overline{\text{DONE}}$ is input, ABORT command is issued, or drive error occurs).

- BURST = 1 (burst mode)

  In this mode, the FDP continues to assert $\overline{\text{DREQ}}$ until a DMA transfer is completed (all sectors are transferred) or aborted ($\overline{\text{DONE}}$ is input, ABORT command is issued, or drive error occurs), or until buffers are switched.

BFM (Buffer Mode): Specifies the mode of the data buffer during DMA transfer. BFM must be specified when DMAM = 0 and DMA = 1.

- BFM = 0: Sector length is 4 to 544 bytes (two-data-buffer mode)
- BFM = 1: Sector length is 545 to 1088 bytes (one-data-buffer mode)

Format Buffer Pointer (FBP)

Bit Configuration

FBP Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	00	$13
			Format buffer pointer							

Function

The FBP holds the format buffer address accessed by the FM or the START command's start address. It is updated by any of the following causes:

- When the START command is not being executed (BSY = 0) and:
  - The FM writes to the FBP,
  - The FM reads the 3 bytes of FMTB1 to FBTB3 (in any order), Note or
  - The FMN writes the 3 bytes of FMTB1 to FBTB3 (in any order). Note

  Note: The FBP is incremented automatically.
- When the START command is being executed (BSY = 1) and:
  - The contents of JMPP are loaded at the end of the execution of a format command specifying JMP,
  - The contents of RTYP are loaded into the FBP when a retry occurs during the execution of a format command specifying JRSR or RTY, or
  - The FBP is incremented when any other format command is completed.

Format Buffer Registers 1, 2, and 3 (FMTB1, FMTB2, and FMTB3)

Bit Configuration

FMTB1 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	Any	$3C
Format buffer data										

FMTB2 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	Any	$3D
Format buffer data										

FMTB3 Data Bits								R/W	Initial Value	Address
7	6	5	4	3	2	1	0	R/W	Any	$3E
Format buffer data										

Function

FMTB1, FMTB2, and FMTB3 act as a port through which the FM accesses the format buffer. The format buffer pointer (FBP) must be set before these registers are accessed.

Writing to the Format Buffer: The FM sets data indirect registers FMTB1, FMTB2, and FMTB3 before writing the data to the format buffer, then increments the FBP.

Reading from the Format Buffer: When the FBP is set, data is loaded from the format buffer to the format buffer registers (FMTB1, FMTB2, and FMTB3). The FM reads the 3 bytes of the contents of the format buffer registers, then increments the FBP.

In both read and write, the monitoring of access to the format buffers (FMTB1 to FMTB3) is cleared when a value is specified in the FBP. If the FBP value is specified again after data has been read from or written to FMTB1 and FMTB2, that data must be read from or written to FMTB1, FMTB2, and FMTB3 again. Otherwise, the format buffer cannot be accessed.

The FM can access FMTB1, FMTB2, and FMTB3 in any order.

Commands

The FDP supports direct commands, format commands, and supplementary commands.

A direct command starts or ends FDP operations and must be written in the command register (CMR) for its execution.

A format command controls disk formatting. Format commands are set in the format buffer by indirect registers FMTB1, FMTB2, and FMTB3, and are started by a START command.

A supplementary command controls jumps and retrys.

Direct Commands

When a command code is written in the command register (CMR), the FDP executes the corresponding direct command. Before a direct command is issued, the command's operating conditions must be specified in the relevant registers.

Except for the ABORT command, direct commands can be issued only when both the BSY and HBSY bits of CEND are 0. (The ABORT command can be issued at any time.)

Only START, STECC, LOAD, STORE, and ABORT commands can be written in the CMR. These direct commands are listed in table 5 and further details are given below.

Table 5 Direct Commands

Direct Command Name	Command Code								Function
	7	6	5	4	3	2	1	0	
START						0	0	1	Starts the execution of the format commands stored in the format buffer. The START command ends when an END command is read from the format buffer or if the START command is terminated abnormally.
STECC						0	1	0	Obtains the error correction pattern and the error bit location from the error syndrome left in the ECC registers after an ECC error. The STECC command does not correct errors.
LOAD						1	0	0	Transfers data from data buffer to the host (DMA transfer).
STORE						1	1	0	Transfers data from the host to the data buffer (DMA transfer).
ABORT						0	0	0	Stops the execution of the four direct commands listed above.

START (Start)

Function

The START command executes a series of format commands stored in the format buffer registers FMTB1, FMTB2, and FMTB3, starting from the command at the address specified by the FBP to the END command. During data transfer, the FDP sets bit 7 (BSY) of CEND while it is processing drive data and bit 5 (HBSY) while it is performing DMA transfer.

Registers Available

FMTB1, FBTB2, FMTB3, LPCNT, FBP, and registers required for the execution of the specified format commands.

STECC (Start ECC)

Function

The STECC command obtains the ECC correction pattern and error bit locations. (Refer to the Error Correction Function section for details of ECC correction patterns and error bit locations.) If the FDP fails to obtain the correction pattern and bit locations, it sets the CRFLT bit of STR1.

The FDP sets bit 7 (BSY) of CEND while this command is executing.

Registers Available

PLY0, PLY1, PLY2, PLY3, PLY4, PLY5, PLY6

LOAD (Load from Buffer)

Function

The LOAD command transfers data from the internal data buffer to the host (DMA transfer), provided that all the following conditions are satisfied:

- The transfer start data buffer is specified by DRBF (MDR1).
- The transfer start address is specified by B0PL/B0PH or B1PL/B1PH.
- The byte length to be transferred is specified by SRLL/SRLH.
- The number of sectors to be transferred is specified by SCNT.

The FDP sets bit 5 (HBSY) of CEND while this command is executing.

Registers Available

B0PH, B0PL, B1PH, B1PL, SRLH, SRLL, SCNT

STORE (Store to Buffer)

Function

The STORE command transfers data from the host to the internal data buffer (DMA transfer), provided that all the following conditions are satisfied:

- The transfer start data buffer is specified by DRBF (MDR1).
- The transfer start address is specified by B0PL/B0PH or B1PL/B1PH.
- The number of sectors to be transferred is specified by SRLL/SRLH.
- The number of transfers is specified by SCNT.

The FDP sets bit 5 (HBSY) of CEND while this command is executing.

Registers Available

B0PH, B0PL, B1PH, B1PL, SRLH, SRLL, SCNT

ABORT (Abort)

Function

The ABORT command terminates the currently executing command.

Format Commands

Format commands must be stored in the format buffer before they can be executed. Once stored, format commands can be executed repeatedly until the commands in the format buffer are updated.

The FDP interprets 3-byte format commands. A format command consists of a command, supplementary command (sup CMD), byte length, and pattern. The functions of these components of the format command are given in table 6.

Table 6 Functions of Format Command Components

Item	Function
Command	Specifies how the disk drive interface is controlled
Supplementary Command	Controls the execution of the command (e.g., it sets jump and/or retry)
Byte length	Specifies the length of the command in bytes (some commands specify the length of execution after a specific condition is satisfied, such as after IDX/SCT is input)
Pattern	Specifies the data pattern to be output by the current or the next command

When the START command is issued, the FDP interprets and executes the command at the address specified by the format buffer pointer (FBP). When command execution is completed, the FBP is incremented unless a jump or retry is specified. The FDP then interprets and executes the command at the next address specified by the FBP. In this way, the FDP interprets and executes commands in sequence until the END command is executed or an error occurs.

To control jumps and retrys the format buffer pointer (FBP), jump pointer (JMPP), and retry pointer (RTYP) can be set by the supplementary command. Refer to the Supplementary Commands section for details.

Format commands can be classify into three types: type A, type B, and type C.

Type A Command

FMTB	Bits							
	7	6	5	4	3	2	1	0
1	Command					Sup CMD		
2	Pattern							
3	Byte length							

- Type A commands write predetermined data and ECC or CRC data.
- Byte length specifies the number of bytes (4 to 255 bytes) to be written. Do not specify a value of less than 4 in this field.

Type B Command

FMTB	Bits							
	7	6	5	4	3	2	1	0
1	Command					Sup CMD		
2						Byte length (high)		
3	Byte length (low)							

- Type B commands write, read, and verify data in ID fields and data fields.
- Byte length specifies the number of bytes (4 to 2047 bytes) to be processed. Do not specify a value of less then 4 in this field.

Type C Command

FMTB	Bits							
	7	6	5	4	3	2	1	0
1	Command					Sup CMD		
2	0	0	0	0	0	0	0	0
3	Byte length							

- Type C commands wait for the IDX/SCT signal, read ECC and CRC data, and execute DMA transfer.
- Byte length specifies the number of bytes (4 to 255 bytes) to be processed. Do not specify a value of less than 4 in this field.

Table 8 Format Command Functions

Mnemonic	Command Code	Function
WIDB	10111	Writes the byte sync pattern set in IDR0 and the predetermined ID information set in the data buffer
WDTB	11000	Writes the byte sync pattern set in DAM0 and the predetermined data set in the data buffer
WDTP	11001	Writes the byte sync pattern set in DAM0 and the data pattern set in DPAT
WCRC	00100	Writes 2-byte-long CRC data
WECC	00101	Writes ECC data of the length (in bytes) set in MDR2
WPTN	00001	Writes the value set in FMTB2
WSP	00110	Negates one byte of the WRGT signal, then writes the value set in FMTB2 (used to write a write splice and the following sync field)
WPUIS	00010	Writes the value set in FMTB2 until the FDP receives the IDX or SCT signal
WPAI	00011	Writes the value set in FMTB2, after the FDP receives the IDX signal
WABSC	00111	Writes the value set in FMTB2 until the FDP receives the SCT signal (valid in hard sector mode only)
WAFSA	01000	• Writes the value set in FMTB2, after the FDP receives the SCT signal (valid in hard sector mode only) • Outputs the AME signal, and writes the value set in FMTB2 (valid in soft sector mode only)
RIDB	11010	Compares a byte sync pattern with the one stored in IDR0, and sets ID information in the buffer if the patterns match
RIDS	11011	Compares a byte sync pattern with the one stored in IDR0, and skips ID information if the patterns match
RDTB	11100	Compares a byte sync pattern with the one stored in DAM0, and sets data in the buffer if the patterns match
RDTS	11101	Compares a byte sync pattern with the one stored in DAM0, and skips data if the patterns match
CCRC	01100	Performs a CRC check
CECC	10000	Performs an ECC check
VID	01011	Compares a byte sync pattern and ID information with values set in ID registers IDR0 to IDRn

Table 8 Format Command Functions (cont)

Mnemonic	Command Code	Function
VDTB	10100 ▨	Compares a byte sync pattern with the one stored in DAM0, and compares data with the contents of the buffer if the patterns match
VCRC	01101 ▨	Compares the last two bytes in the ID or data field, and performs a CRC check and a flag check
VCRCR	01110 ▨	Compares the last two bytes in the ID or data field, performs a CRC check and a flag check, and asserts the RDGT signal from CRC data
VCRCW	01111 ▨	Compares the last two bytes in the ID or data field, performs a CRC check and a flag check, negates the RDGT signal and asserts the WRGT signal at the end of CRC data
VECC	10001 ▨	Compares the last two bytes in the ID or data field, and performs an ECC check and a flag check
VECCR	10010 ▨	Compares the last two bytes in the ID or data field, performs an ECC check and a flag check, and asserts the RDGT signal from ECC data
VECCW	10011 ▨	Compares the last two bytes in the ID or data field, performs an ECC check and a flag check, and negates the RDGT signal and asserts the WRGT signal at the end of ECC data
WAITI	10101 ▨	Waits until the FDP receives the IDX signal
WTISA	10110 ▨	• Waits until the FDP receives the IDX or SCT signal (valid only in hard sector mode) • Asserts the AME signal and waits until the FDP receives the AMF signal (valid only in soft sector mode)
SKIP	11110 ▨	Waits
SKIRG	01001 ▨	Asserts the RDGT signal and waits
DMAW	01010 ▨	Starts DMA transfer of data from the host to the buffer
IDINC	11111 ▨	Increments the value (ID field) of the ID register (IDR0 to IDR5) specified by INCR
END	00000 ▨	Terminates the processing of format commands, and waits for the input of a direct command

Note: ▨: Position of supplementary command

Supplementary Commands

Supplementary commands (Sup CMDs) set the jump and/or retry pointer(s) and execute jump and/or retry operation(s). These commands are listed in table 9.

Table 9 Supplementary Commands (Sup CMDs)

Mnemonic	Bits 2 1 0	Function
NOP	0 0 0	Does nothing
JPS	0 0 1	Sets the jump pointer (JMPP)
RPS	0 1 0	Sets the retry pointer (RTYP)
JRS	0 1 1	Sets the jump pointer and retry pointer
JRSR	1 0 0	Sets the jump pointer and retry pointer, and retries
JMP	1 0 1	Jumps
RTY	1 1 0	Retries
NOP	1 1 1	Does Nothing

Jump Pointer (JMPP) Setting: The FDP sets the value of the FBP into the JMPP during the current command execution.

Retry Pointer (RTYP) Setting: The FDP sets the value of the FBP into the RTYP during the current command execution.

Jump: If the value in the loop counter (LPCNT) is not 0, the FDP sets the JMPP value into the FBP to cause a jump corresponding to that value. The LPCNT is decremented after its value is checked.

Retry: If data does not match during the execution of a verify command, the FDP sets the RTYP value into the FBP to cause a jump corresponding to that value.

The JMPP specifies the start address of a series of format commands set in an execution loop to process two or more sectors. To set a jump address in the JMPP, JPS, JRS, or JRSR must be specified in the supplementary command field of each format command. JMP must be set in the supplementary command field of the last format command of the loop.

The LPCNT specifies the number of repetitions of the loop set by JMPP. (This value must be set by the FM in advance.)

The RTYP specifies the start address of the execution loop to be restarted at the detection of a sector pulse after ID data does not match. To set an address in the RTYP, RPS, JRS, and JRSR must be specified in the supplementary command field of the format command.

To set the FBP at the start loop address pointed to by the RTYP, RTY or JRSR must be specified in the supplementary command field of the format command to be retried.

The processing specified by a supplementary command is jump processing and/or retry processing.

Supplementary commands for jump processing are Jump Pointer Set (JPS) which sets a jump destination address and Jump (JMP) which jumps at normal termination to the address specified by the jump pointer (JMPP).

Supplementary commands for retry processing are Retry Pointer Set (RPS) which sets a retry destination address and Retry (RTY) which jumps to the address specified by the retry pointer (RTYP) if an error occurs.

Other supplementary commands combine the above command functions.

For example, the first processing in the reading of or writing to a sector is the verification (by the VID command) of the ID field. In multi-sector processing, this verification must be performed for each sector, and, if data in the ID field does not match, the operation must be retried. The supplementary command JRSR (which sets the JMPP and RTYP and enables retry) simplifies the retry.

Similarly, the first processing in hard sector mode is to wait for a sector pulse (by the WTISA command). This process is performed for each sector. If ID data does not match in the succeeding ID verification, the operation must be restarted from the wait process. In such a case, the supplementary command JRS (which sets JMPP and RTYP) simplifies the process.

Example 1: Loop processing

```
                                    LPCNT = N

              Address
                 n        CMD
JMPP  ←          n + 1    CMD (JPS, JRS, JRSR)
                                .
                                .
                 m        CMD (JMP)
```

If any one of JPS, JRS, and JRSR is specified in the supplementary command field of the format command at address n + 1, the FDP sets address n + 1 in the JMPP. If the format command at address m has JMP specified in its supplementary command field, the FDP jumps to the specified address (n + 1) every time it encounters that command, until the LPCNT reaches 0. The LPCNT is decremented by each jump. In this example, N + 1 loops from address n + 1 to address m are performed.

Example 2: Retry processing

```
              Address
                 n        CMD
RTYP  ←          n + 1    CMD (RPS, JRS, JRSR)
                          CMD (RTY)
                                .
                                .
                 m        CMD
```

If any one of RPS, JRS, and JRSR is specified in the supplementary command field of the format command at address n + 1, the FDP sets address n + 1 in the RTYP.

If a retry is instructed (after an error occurs during a format command that has RTY or JSRS specified in its supplementary command field), the contents of the RTYP are loaded into the FBP, and processing resumes from the address specified by the RTYP.

Interface Functions

Drive Interface

The status of the HS bit of the indirect register MDR4 is determined by the interface specification of the disk drive (hard sector mode or soft sector mode), as follows:

HS = 1 for hard sector mode
HS = 0 for soft sector mode

File Manager Interface

The FDP has two types of register: direct registers which the file manager can directly access and indirect registers which the file manager accesses via the direct registers. (Refer to the Block Diagram.)

Accessing Direct Registers: There are six direct registers: address register (AR), data register (DTR), command end register (CEND), command register (CMR), and buffer register 0 and 1 (BUF0 and BUF1). CEND is a read-only register but the other five registers can be read from and written to.

- Accessing AR, DTR, CEND, and CMR

  Set the address of the target direct register in signals A_2 to A_0, and assert $\overline{CS}$ and $\overline{WR}$ to write to the register or asserts $\overline{CS}$ and $\overline{RD}$ to read from the register. The register stores data at the rising edge of $\overline{WR}$ (write), or outputs data when $\overline{RD}$ is asserted (read).

- Accessing BUF0 and BUF1

  Set the address of the target direct register (BUF0 or BUF1) in signals A_2 to A_0, and assert $\overline{CS}$ and $\overline{WR}$ to write to the register or assert $\overline{CS}$ and $\overline{RD}$ to read from the register. In addition, the register address for buffer pointers (B0PL/B0PH and B1PL/B1PH) must be specified before the register is accessed. Refer to the next section for details on setting indirect registers B0PL/B0PH and B1PL/B1PH.

The addresses of the direct registers are listed in table 10.

Table 10 Direct Register Address

A2	A1	A0	Register	R/W	Remarks
0	0	0	AR	R/W	
0	0	1	DTR	R/W	
0	1	0	CEND	R	
0	1	1	CMR	R/W	
1	0	0	BUF0	R/W	Set the address of this register in the buffer pointer before accessing it, and increment the value of the buffer pointer afteraccessing it
1	0	1	BUF1	R/W	Set the address of this register in the buffer pointer before accessing it, and increment the value of the buffer pointer after accessing it

Accessing Indirect Registers: Write the target indirect register address in the address register (AR). Set the data to be written to or read from the indirect register in the data register (DTR).

The AR retains the specified address so that the file manager can repeatedly access the specified indirect register until the AR is updated.

Refer to the Indirect Registers section for further details.

Register Access Conditions: During some FDP operating states, the file manager may not be able to access some of the registers. Operating states and corresponding inaccessable registers are listed in table 11.

Table 11 Register Access States

FDP Operation	Registers Not Accessable by the File Manager
No operation	None
LOAD or STORE command	B0PL, B0PH, B1PL, B1PH, MDR1, MDR4, BUF0, BUF1, SCNT, SRLH, SRLL, TCNTH, TCNTL
START command	Direct registers except CMR and CEND, and all indirect registers
STECC command	MDR2, ECC0–ECC6, PLY0–PLY6, RCPH, RCPL

Host Interface

The FDP can operate in two modes: master mode (MST bit of MDR1 is 1) in which the FDP has the bus right and slave mode (MST bit of MDR1 is 0) in which the MPU or DMAC has the bus right.

Asynchronous data transfer, with a minimum of 4 access cycles in 16-bit mode or 3 access cycles in 8-bit mode, is enabled in both modes.

Slave Mode: In slave mode (MST = 0), FDP pins relating to the host interface (pins 31, 32, 33, 34, 37, and 38) have the functions listed in table 12.

Table 12 Pin Functions in Slave Mode

Pin No.	Type	Pin Name	Remarks
32	Output	$\overline{\text{DREQ}}$	
33	Input	$\overline{\text{DACK}}$	
38	Input	$\overline{\text{IORD}}$	
37	Input	$\overline{\text{IOWR}}$	
31	Input	$\overline{\text{DONE}}$	
34	Input	$\overline{\text{WAIT}}$	Not used (must be pulled up)

- DMA transfer
  - DMA write (host to FDP)

    When a DMA write transfer is requested, the FDP asserts the $\overline{\text{DREQ}}$ signal. When $\overline{\text{DACK}}$ and $\overline{\text{IOWR}}$ are then asserted in this state, the FDP receives data from the host at the rising edge of the $\overline{\text{IOWR}}$ signal.

  - DMA read (FDP to host)

    When a DMA read transfer is requested, the FDP asserts the $\overline{\text{DREQ}}$ signal. When $\overline{\text{DACK}}$ and $\overline{\text{IORD}}$ are then asserted in this state, the FDP outputs data to the host.

  - DMA transfer modes

    Two DMA transfer modes are available: burst mode and cycle steal mode. The DMA transfer mode is indicated by the BURST bit of MDR4, as follows

    BURST bit = 0: Cycle steal mode
    BURST bit = 1: Burst mode

    Burst mode: The FDP asserts the $\overline{\text{DREQ}}$ signal until the DMA transfer is completed (all data sectors are transferred), aborted ($\overline{\text{DONE}}$ is input, the ABORT command is issued, or a drive error occurs), or the buffer is switched. $\overline{\text{DREQ}}$ is temporarily negated when data of one sector has been transferred or after 544 bytes have been transferred if the sector is more than 544 bytes long (figure 3).

    Cycle steal mode: When it receives $\overline{\text{DACK}}$ after asserting $\overline{\text{DREQ}}$, the FDP negates $\overline{\text{DREQ}}$ while $\overline{\text{DACK}}$ is asserted. While $\overline{\text{DACK}}$ is not asserted, the FDP asserts $\overline{\text{DREQ}}$ until the DMA transfer is completed (all sectors are transferred) or aborted ($\overline{\text{DONE}}$ is input, ABORT command is issued, or a drive error occurs).

– Data bus

Two data buses can be selected: 8-bit data bus and 16-bit data bus. The data bus width is indicated by the B8 bit of MDR1, as follows:

B8 bit = 0: 16-bit data bus (16-bit mode)
B8 bit = 1: 8-bit data bus (8-bit mode)

In 16-bit mode, BUS_{00} to BUS_{07} are the most significant byte and BUS_{08} to BUS_{15} are the least significant byte. In 8-bit mode, only BUS_{00} to BUS_{07} are used so BUS_{08} to BUS_{15} must be pulled up.

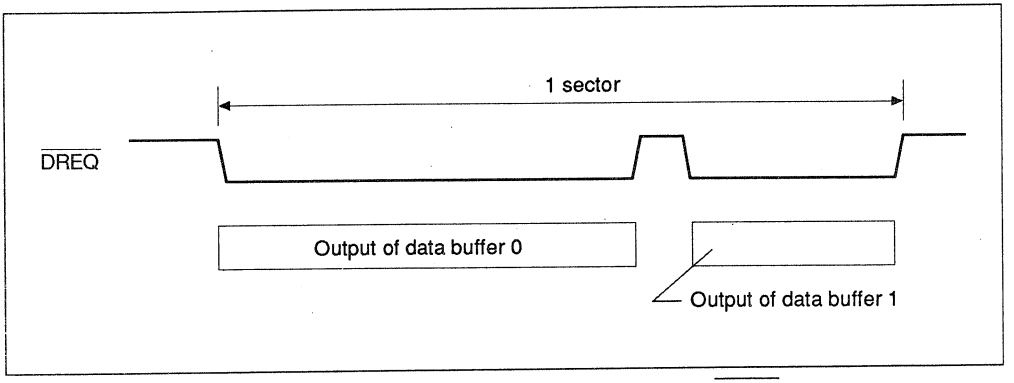


Figure 3 Data Buffer Switching and Negation of $\overline{DREQ}$

Master Mode: In master mode: (MST = 1), the FDP pins relating to the host interface (pins 31, 32, 33, 34, 37, and 38) have the functions listed in table 13.

Table 13 Pin Functions in Master Mode

Pin No.	Type	Pin Name	Remarks
32	Input	$\overline{DREQ}$	
33	Output	$\overline{DACK}$	
38	Output	$\overline{IORD}$	
37	Output	$\overline{IOWR}$	
31	Input	$\overline{DONE}$	
34	Input	$\overline{WAIT}$	

- DMA transfer

  - DMA read (FDP to host)

    When a DMA write transfer is requested, the FDP waits until the $\overline{\text{DREQ}}$ signal is asserted, then it asserts $\overline{\text{DACK}}$ and $\overline{\text{IOWR}}$ and begins to transfer data. (The FDP outputs data at the falling edge of $\overline{\text{IOWR}}$.) If $\overline{\text{DREQ}}$ is asserted and $\overline{\text{WAIT}}$ is negated, the FDP transfers data for two asserted cycles and one negated cycle of $\overline{\text{IOWR}}$. If the transfer rate of the host is too slow to complete the transfer during these cycles, $\overline{\text{WAIT}}$ must be asserted or $\overline{\text{DREQ}}$ negated. The FDP does not negate $\overline{\text{IOWR}}$ while $\overline{\text{WAIT}}$ is asserted, and it does not assert $\overline{\text{IOWR}}$ while $\overline{\text{DREQ}}$ is negated.

  - DMA write (host to FDP)

    When a DMA read transfer is requested, the FDP waits until the $\overline{\text{DREQ}}$ signal is asserted, then it asserts $\overline{\text{DACK}}$ and $\overline{\text{IORD}}$ and begins to transfer data. (The FDP fetches data at the rising edge of $\overline{\text{IORD}}$.) If $\overline{\text{DREQ}}$ is asserted and $\overline{\text{WAIT}}$ is negated, the FDP transfers data for two asserted cycles and one negated cycle of $\overline{\text{IORD}}$. If the transfer rate of the host is too slow to complete the transfer during these cycles, $\overline{\text{WAIT}}$ must be asserted or $\overline{\text{DREQ}}$ negated.

  - DMA transfer mode

    In master mode, only burst mode is available. The FDP asserts the $\overline{\text{DACK}}$ signal until DMA transfer is aborted or completed. The FDP negates the $\overline{\text{DACK}}$ signal under any of the following conditions:
    - All data sectors are transferred.
    - $\overline{\text{DONE}}$ is input.
    - ABORT command is issued.

    Note: If DMA transfer is aborted because of a drive error, $\overline{\text{DACK}}$ will not be negated. Therefore, an ABORT command must be issued from the FM. (The setting and resetting of CEND bits are the same as those in slave mode.)

  - Data bus

    In master mode, only the 8-bit data bus (BUS_{00} to BUS_{07}) is used. The remaining data bus lines (BUS_{08} to BUS_{15}) must be pulled up.

Notes:
1. Assert $\overline{\text{DONE}}$ only during a DMA transfer. In master mode, the FDP accepts $\overline{\text{DONE}}$ and sets the BUSINT bit of CEND to 1.
2. If $\overline{\text{DONE}}$ is input when the last data of each sector is transferred, that sector's data may be written to the drive, depending on the input timing of $\overline{\text{DONE}}$.
3. $\overline{\text{WAIT}}$ is ignored while $\overline{\text{DONE}}$ is input.
4. If $\overline{\text{DONE}}$ is input during a DMA transfer (except as described in note 2), the transfer ($\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, and data AC characteristics) cannot be guaranteed.
5. If a sector is 545 bytes or longer, the negation width of $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ increases while data buffers are switched, as shown in figure 4.

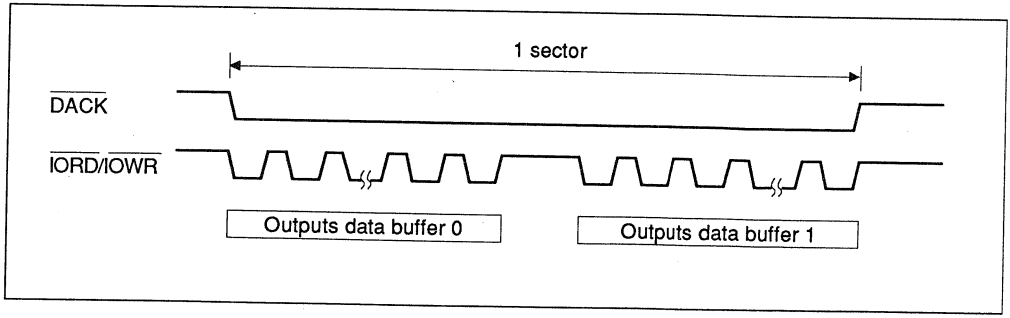


Figure 4 Negation of $\overline{\text{IORD}}$/$\overline{\text{IOWR}}$

Data Transfer Function

Various data transfer modes are available, depending on the settings of registers. All data transfers are DMA transfers.

Data Transfer Modes

The bits shown in tables 14 and 15 must be set to suit the mode selected for data transfer.

Table 14 Host Interface Mode Settings

Register	Bit	Value	Mode
MDR1	MST	0	FDP slave mode
		1	FDP master mode
	B8	0	16-bit data bus
		1	8-bit data bus
	DMA	0	A DMA transfer is not performed when a command is issued
		1	A DMA transfer is performed when a command is issued
MDR4	BURST	0	Cycle steal mode
		1	Burst mode

Note: The B8 and BURST bits are valid only when MST = 0.

Table 15 Data Buffer Mode Settings

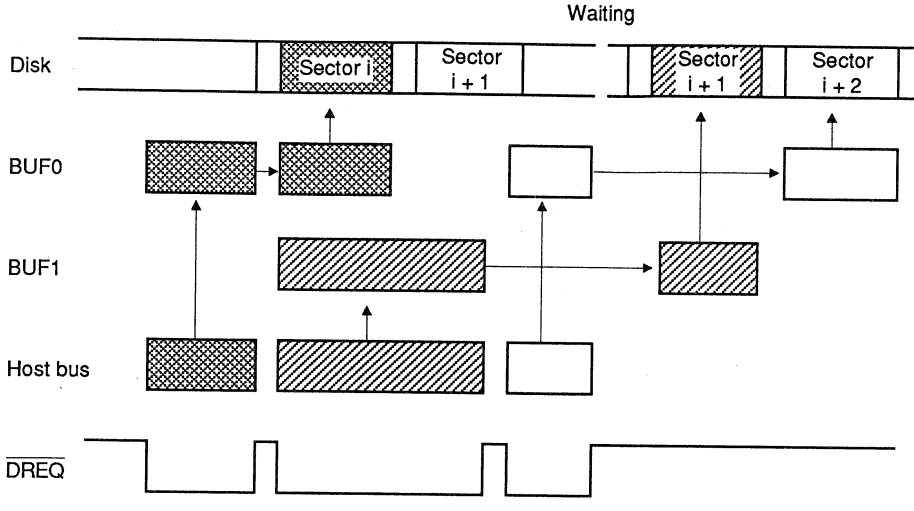
Register	Bit	Value	Mode
MDR1	DRBF	0	Starts DMA transfer from data buffer 0 (BUF0)
		1	Starts DMA transfer from data buffer 1 (BUF1)
	DMAM	0	Changes data buffers for each sector
		1	Does not change data buffers for each sector
MDR4	BFM	0	Two-buffer mode (one sector is 4 to 544 bytes long)
		1	One-buffer mode (one sector is 545 to 1088 bytes long)

Notes: 1. The DMAM = 1 setting is valid only in write format mode. (The DMA bit must be 0 in write format mode.)
2. BFM is valid only when DMAM = 0.

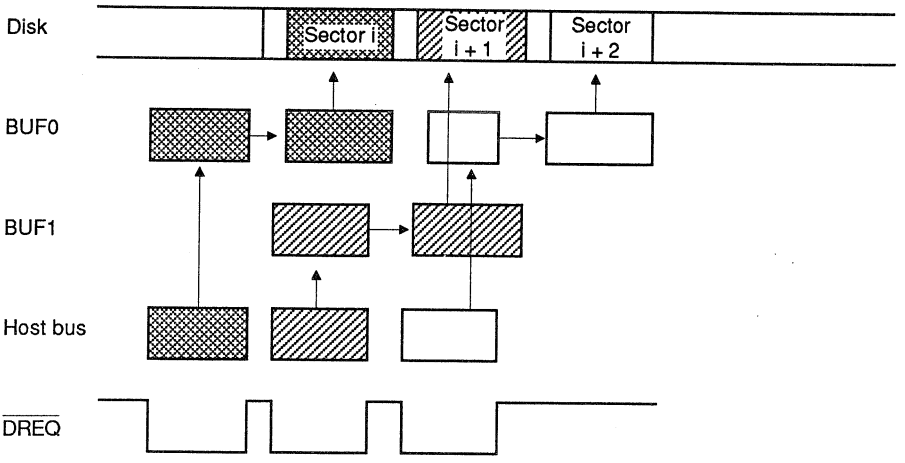
- Data transfer when DMAM=0

For a DMA transfer in this mode, the data buffer receives one sector of data from disk, for example, and transfers it to the host. Since the data buffers (BUF0 and BUF1) hold a maximum of 1088 bytes (544 bytes each), each sector must be no more than 1088 bytes long.

If the sector length is no more than 543 bytes, multi-sector processing without interleaving is possible. The writing of data to disk by DMA transfer in this case is shown in figure 5 and the reading of data from disk is shown in figure 6.

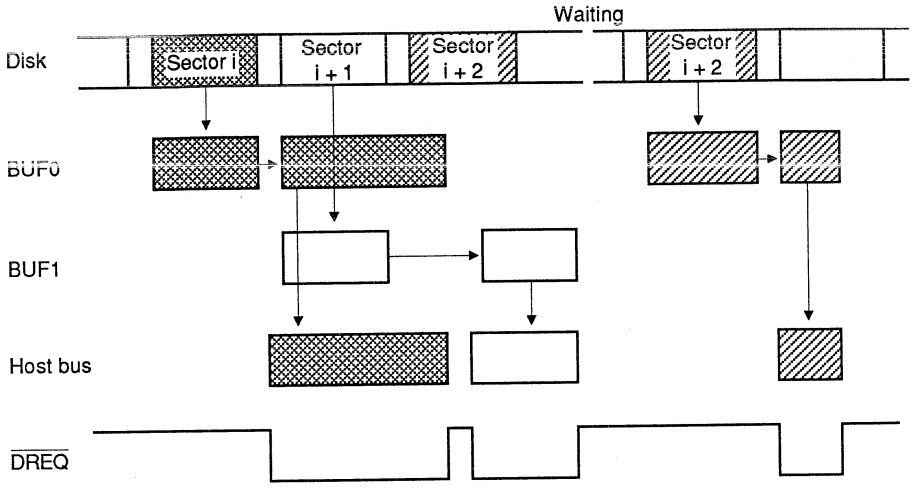


(a) Slow Host Transfer Rate

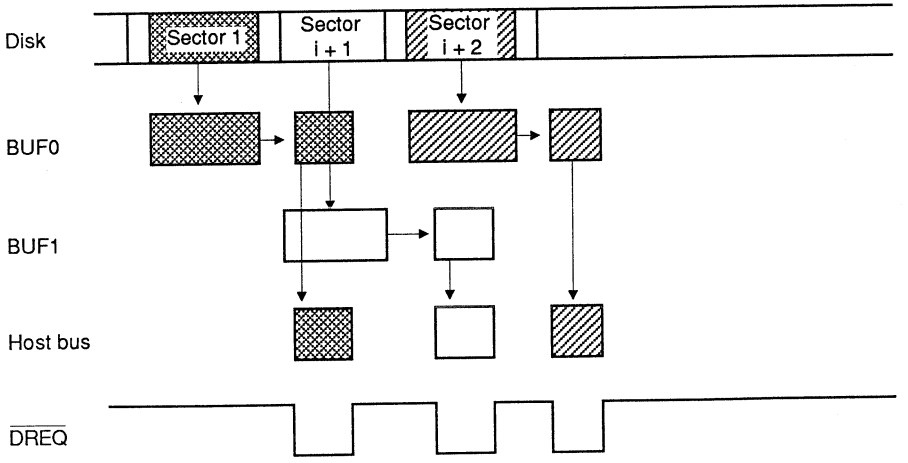


(b) Fast Host Transfer Rate

Figure 5 DMA Write (up to 543 bytes/sector) Started by DMAW Command



(a) Slow Host Transfer Rate



(b) Fast Host Transfer Rate

Figure 6 DMA Read (up to 543 bytes/sector)

- Data transfer when DMAM = 1

  In this mode, data buffers are switched when address 543 is accessed. The next address is accessed by the next format command (Figure 7).

  Use this transfer method for write formatting when DMA = 0.

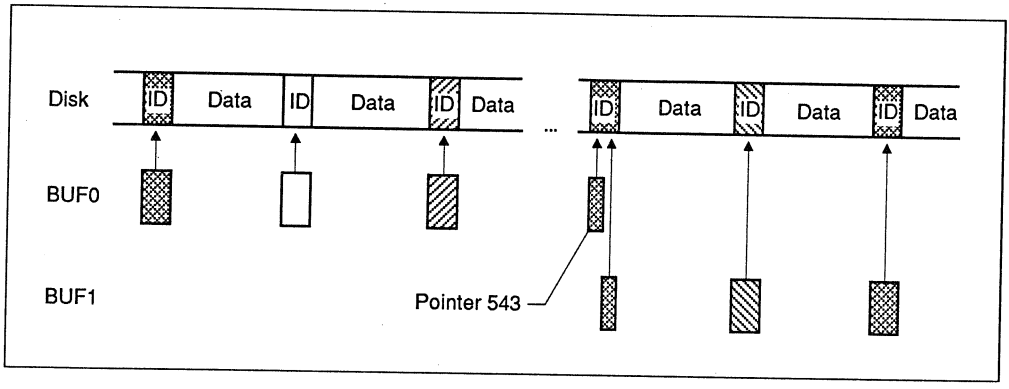


Figure 7 Write Formatting

Data Transfer

Start of DMA Transfer: The FDP starts DMA transfer between the data buffer and the host when a LOAD or STORE command is issued or when a WIDB, WDTB, RIDB, RDTB, VDTB, or DMAW command is executed while DMA = 1.

Completion of DMA Transfer: The FDP completes DMA transfer when any of the following conditions is satisfied:

- The specified amount of data (SRLL/SRLH value × SCNT value) has been transferred.
- A drive access error aborts a command.
- $\overline{\text{DONE}}$ is asserted.
- An ABORT command is issued.

Stopping DMA Transfer (to monitor the status of data buffers): When a LOAD or STORE command is executing, the FDP (in slave mode) asserts $\overline{\text{DREQ}}$ until the specified amount of data has been transferred. If data to be stored overflows the data buffers, the data stored last is valid.

Example: If the STORE command specifying DMAM = 0, SCNT = 3, and DRBF = 0 is executed, the third sector's data is stored in data buffer BUF0 and the second sector's data is stored in BUF1. The first sector's data is not stored.

If LOAD commands with the same specifications are executed, the same data is repeatedly output.

If DMA transfer is initiated by the execution of command other than STORE or LOAD, the FDP monitors the status of the data buffers to ensure that the data buffers' contents and disk data are not lost. If a data transfer between the host and data buffer overflows, the FDP negates $\overline{\text{DREQ}}$ if it is in slave mode, or asserts neither $\overline{\text{IORD}}$ nor $\overline{\text{IOWR}}$ if it is in master mode.

DMA transfer is requested by a WIDB, WDTB, RIDB, RDTB, or VDTB command, the FDP inhibits transfers between the host and the data buffers, but allows transfers between the data buffers and the disk drive. If DMA transfer is requested by a DMAW command, the FDP allows transfers between the host and the data buffers but inhibits transfers between the data buffers and the disk drive.

Error Checking and Correction Function

The FDP has two error checking and correction circuits: a detection and generation circuit for 16-bit CRC (cyclic redundancy code) and a detection, generation, and correction circuit for ECC (error checking and correction) code (max. 7-byte fire code). These codes are attached to each disk field if specified with the format commands. The characteristics of the CRC and ECC circuits are listed in tables 16 and 17.

Table 16 CRC Detection and Generation Circuit

Item	Description
Polynominal	$X^{16} + X^{12} + X^5 + 1$ (fixed)
Initial value	Either all zeros or all ones (set by the CRCI bit of MDR2)
CRC operation	Either addition or non-addition of the byte sync pattern (set by the BSEX bit of MDR2)
Format command	(Generation) WCRC (Detection) CCRC, VCRC, VCRCW, VCRCR

Table 17 ECC Detection, Generation, and Correction Circuit

Item	Description
ECC data length	4, 6, or 7 bytes (set by the ECM0 and ECM1 bits of MDR2)
Polynominal	any (set by PLY0 to PLY6)
Initial value	Either all zeros or all ones (set by the ECCI bit of MDR2)
ECC operation	Either addition or non-addition of the byte sync pattern (set by the BSEX bit of MDR2)
Format command	(Generation) WECC (Detection) CECC, VECC, VECCW, VECCR
Maximum length of correctable burst error	5, 6, 7, 8, 9, 10, 11, or 16 bits Note (Set by ZCK2, ZCK1, and ZCK0 bits of MDR2)
Correction pattern generation command	STECC (direct command)

Note: Limited by polynominal and error pattern

ECC/CRC Generation and Detection Functions

Setting of ECC Data Length and Polynominal: To use ECC codes, it is necessary to set their data length and their polynominal first.

- Setting of ECC data length

The ECC data length is specified by the ECM1 and ECM0 bits of MDR2, as follows:

ECM1	ECM0	ECC Data Length
0	0	4 bytes
0	1	6 bytes
1	0	7 bytes
1	1	(Reserved)

The relations between ECC data lengths and polynominal registers are given below.

– 4-byte mode

Bits	Plynominal Register	ECC
0–7	PLY0	ECC0
8–15	PLY1	ECC1
16–23	PLY5	ECC5
24–31	PLY6	ECC6

– 6-byte mode

Bits	Plynominal Register	ECC
0–7	PLY0	ECC0
8–15	PLY1	ECC1
16–23	PLY2	ECC2
24–31	PLY4	ECC4
32–39	PLY5	ECC5
40–47	PLY6	ECC6

– 7-byte mode

Bits	Plynominal Register	ECC
0–7	PLY0	ECC0
8–15	PLY1	ECC1
16–23	PLY2	ECC2
24–31	PLY3	ECC3
32–39	PLY4	ECC4
40–47	PLY5	ECC5
48–55	PLY6	ECC6

Note: Polynominal registers PLY0 to PLY6 not listed in the above tables need not be set.

- Setting of polynominals

The polynominals that generate ECC codes are specified by PLY0 to PLY6. The bits of each polynominal register (PLY0 to PLY6) are in a one-to-one relationship with the bits of the ECC registers (ECC0 to ECC6). The 1 bits specified in PLY0 to PLY6 are fed back, and the 0 bits are directly shifted. The least significant bit (LSB) represents the data which was shifted from the most significant bit (MSB), independently of the PLY0 value.

The examples below show typical settings of PLY0 to PLY6 for each byte mode.

– Typical polynominal for 4-byte mode

$(x^{21} + 1)(x^{11} + x^2 + 1)$
$= x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$

Exponent = 32 31 30 29 28 27 26 25 24
PLY6 = 1 0 0 0 0 0 0 0 0 = $00

Exponent = 23 22 21 20 19 18 17 16
PLY5 = 1 0 1 0 0 0 0 0 = $A0

Exponent = 15 14 13 12 11 10 9 8
PLY1 = 0 0 0 0 1 0 0 0 = $08

Exponent = 7 6 5 4 3 2 1 0
PLY0 = 0 0 0 0 0 1 0 1 = $05

– Typical polynominal for 6-byte mode

$(x^{13} + 1)(x^{35} + x^{23} + x^8 + x^2 + 1)$
$= x^{48} + x^{36} + x^{35} + x^{23} + x^{21} + x^{15} + x^{13} + x^8 + x^2 + 1$

PLY6 = $00
PLY5 = $18
PLY4 = $00
PLY2 = $A0
PLY1 = $A1
PLY0 = $05

– Typical polynominal for 7-byte mode

$(x^{22} + 1)(x^{12} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^6 + x^5 + x^4 + x^3 + x^2 + x + 1)(x^{11} + x^7 + x^6 + x + 1)(x^{11} + x^9 + x^7 + x^6 + x^5 + x + 1)$
$= x^{56} + x^{55} + x^{49} + x^{45} + x^{41} + x^{39} + x^{38} + x^{37} + x^{36} + x^{31} + x^{22} + x^{19} + x^{17} + x^{16} + x^{15} + x^{14} + x^{12} + x^{11} + x^9 + x^5 + x + 1$

PLY6 = $82
PLY5 = $22
PLY4 = $F0
PLY3 = $80
PLY2 = $4B
PLY1 = $DA
PLY0 = $23

Setting of Initial Values and Treatment of the Byte Sync Pattern: Before an CRC/ECC operation is started, the initial CRC and ECC values must be specified by the CRCI and ECCI bits of MDR2. The initial values set by the CRCI and ECCI bits are used each time a CRC/ECC initialization command is executed.

CRCI = 0: The initial CRC value is all zeros.
CRCI = 1: The initial CRC value is all ones.

ECCI = 0: The initial ECC value is all zeros.
ECCI = 1: The initial ECC value is all ones.

Specify the treatment of the byte sync pattern by the BSEX bit of MDR2, as follows:

BSEX = 0: A byte sync pattern is included in the ECC/CRC operation.
BSEX = 1: No byte sync pattern is included in the ECC/CRC operation.

Generation and Detection of ECC and CRC Codes: The FDP can generate ECC and CRC codes and detect errors if specified format commands are run after the ECC data length, polynominals, and initial values have been set. To ensure normal ECC/CRC generation and detection, the format commands must be combined as follows:

Command to initialize ECC/CRC	→	Command to execute ECC/CRC operation	→	Command to determine or output an ECC/CRC error

Repeat this combination of format commands to process two or more sectors (for multi-sector processing). Valid format commands are listed in table 18.

Table 18 ECC/CRC Generation and Detection Commands

Command	ECC/CRC Initialization	ECC/CRC Operation	ECC/CRC Error Determination/Output
WPTN	○	×	×
WPUIS	(○)	×	×
WPAI	(○)	×	×
WCRC	○	×	○
WECC	(○)	×	○
WSP	○	×	×
WASFI	(○)	×	×
WAFSA (hard sector)	(○)	×	×
WAFSA (soft sector)	○	×	×
DMAW	○	×	×
VID	○	(○)	×
CCRC	(○)	○	○
VCRC	(○)	(○)	○
VCRCR	(○)	(○)	○
VCRCW	(○)	(○)	○
CECC	(○)	○	○
VECC	(○)	(○)	○
VECCR	(○)	(○)	○
VECCW	(○)	(○)	○
VDTB	×	(○)	×
WAITI	(○)	×	×
WTISA (hard sector)	(○)	×	×
WTISA (soft sector)	(○)	×	×
WIDB	×	(○)	×
WDTB	×	(○)	×

Table 18 ECC/CRC Generation and Detection Commands (cont)

Command	ECC/CRC Initialization	ECC/CRC Operation	ECC/CRC Error Determination/Output
WDTP	×	○	×
RIDB	(○)	○	×
RIDS	○	(○)	×
RDTB	(○)	(○)	×
RDTS	○	(○)	×
IDINC	○	×	×
SKIP	○	×	×
END	×	×	×

○: Always enabled (○): Conditionally enabled. ×: Disabled

Error Correction Function

Any ECC error found in read data must be corrected. The FDP uses the error diagnosis (the contents of ECC0 to ECC6 after the ECC check) to calculate error positions and a correction pattern. Therefore, the FM must correct the data stored in the data buffers, based on the result of the FDP's calculation.

Setting of Reciprocal Polynominals: To generate a correction pattern, the FDP reverses the generation and checking operations using the error diagnosis. Therefore, it is necessary to specify a reciprocal polynominal before issuing the STECC command to obtain the correction pattern. Assuming that the original polynominal is f(x), the reciprocal polynominal can be expressed by:

$$x^n \cdot f\left(\frac{1}{x}\right)$$

The following polynominals are the reciprocals of the original typical polynominals for 4-, 6- and 7-byte modes given above:

4-byte ECC mode

$$x^{32} + x^{30} + x^{21} + x^{11} + x^9 + 1$$

6-byte ECC mode

$$x^{48} + x^{46} + x^{40} + x^{35} + x^{33} + x^{27} + x^{25} + x^{13} + x^{12} + 1$$

7-byte ECC mode

$$x^{56} + x^{55} + x^{51} + x^{47} + x^{45} + x^{44} + x^{42} + x^{41} + x^{40} + x^{39} + x^{37} + x^{34} + x^{25} + x^{20} + x^{19} + x^{18} + x^{17} + x^{15} + x^{11} + x^7 + x + 1$$

These reciprocal polynominals are set in polynominal registers PLY0 to PLY6 in the same manner as described in the previous section, and the specification of ECC data length and the relations between polynominal registers and ECC registers are also exactly the same. The values in the polynominal registers in each ECC byte mode are as follows:

4-byte ECC mode	6-byte ECC mode	7-byte ECC mode
PLY6 = $40	PLY6 = $41	PLY6 = $88
PLY5 = $20	PLY5 = $0A	PLY5 = $B7
PLY1 = $0A	PLY4 = $0A	PLY4 = $A4
PLY0 = $01	PLY2 = $00	PLY3 = $02
	PLY1 = $30	PLY2 = $1E
	PLY0 = $01	PLY1 = $88
		PLY0 = $83

Setting of Correction bit Length: Generally speaking, ECC accuracy decreases as the correction bit length increases. To avoid this deterioration, the necessary correction bit length should be specified for the FDP, using the ZCK2, ZCK1, and ZCK0 bits of MDR2.

ZCK2	ZCK1	ZCK0	Correction Bit Length
0	0	0	16 bits
0	0	1	11 bits
0	1	0	10 bits
0	1	1	9 bits
1	0	0	8 bits
1	0	1	7 bits
1	1	0	6 bits
1	1	1	5 bits

Activation by Command: Issue a STECC command after setting the reciprocal polynominal and the correction bit length. The FDP begins the operation from the error diagnosis left in ECC0 to ECC6, and stops after the specified number of operations (corresponding to the sector length), regardless of whether it has obtained a correction pattern. This operation limit is specified by the indirect register SRLH as follows:

SRLH = ****000X: $(2^{13} - 1)$ times (8191 times)
****001X: $(2^{14} - 1)$ times (16383 times)
****01XX: $(2^{15} - 1)$ times (32767 times)

If it does not obtain a correction pattern after the specified number of operations the FDP stops command execution, setting the CRFLT bit of STR1 and the ERR bit of CEND. In this case, the contents of RCPH, RCPL, and ECC0 to ECC6 are meaningless.

Correction: If it obtains a correction pattern, the FDP stops command execution without setting the CRFLT bit of STR1 and the ERR bit of CEND. In this case, the contents of RCPH and RCPL indicate the error bit position, counting from the end of all the data (including ECC codes), and ECC0 and ECC1 contain the correction pattern. The FM can now correct the buffer data from the contents of ECC0 and ECC1.

Example: Sector length = 256 bytes, ECC data length = 32 bits, number of correction bits = 11, RCPL, RCPH = 410 (decimal), ECC0 = $0A, ECC1 = $05 (figure 8)

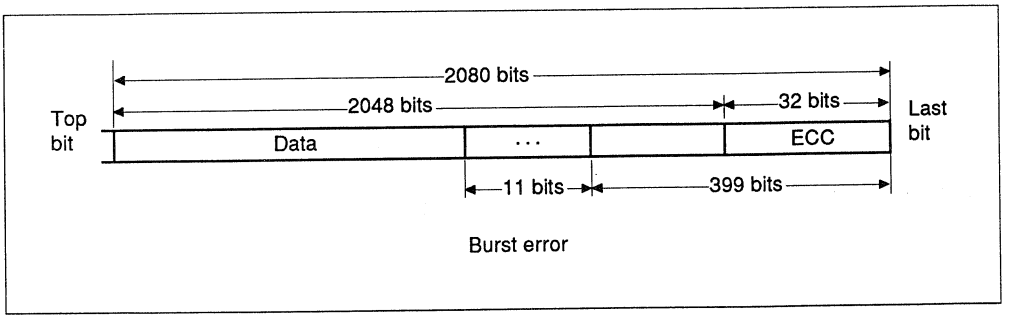


Figure 8 Burst Error Data

In this example, a burst error is detected between bit 410 and bit 400 (11 bits), counting from the last data bit. The correction pattern is represented by bits 0 to 7 of ECC0 and bits 0 to 2 of ECC1 (for 11 correction bits), as shown in figure 9.

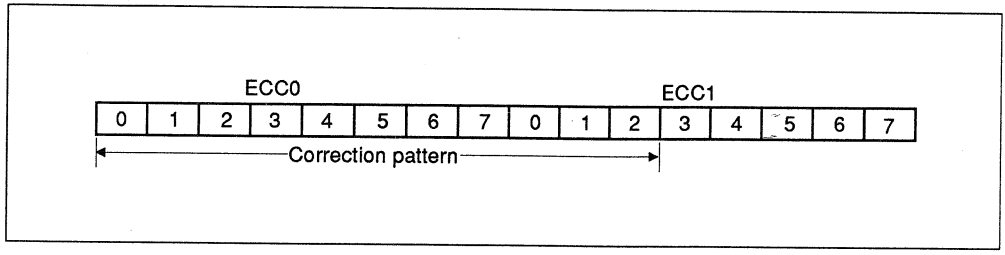


Figure 9 Correction Pattern

1 bits in the correction pattern invert the corresponding bits in drive data. 0 bits keep drive data unchanged. The following shows the one-to-one relationship of the bits of registers ECC0 and ECC1 to data bits.

ECC0 Bit 0: Bit 410
Bit 1: Bit 409
Bit 2: Bit 408
Bit 3: Bit 407
Bit 4: Bit 406
Bit 5: Bit 405
Bit 6: Bit 404
Bit 7: Bit 403
ECC1 Bit 0: Bit 402
Bit 1: Bit 401
Bit 2: Bit 400

The following is an example of error correction:

Burst error data	10100011100
Correction pattern	01010000101
Corrected data	11110011001

Operation Examples

Formatting

Conditions: Hard sector mode, 3 sectors to be formatted, ECC data 4 bytes long (figure 10)
The result of the formatting is shown in figure 11.

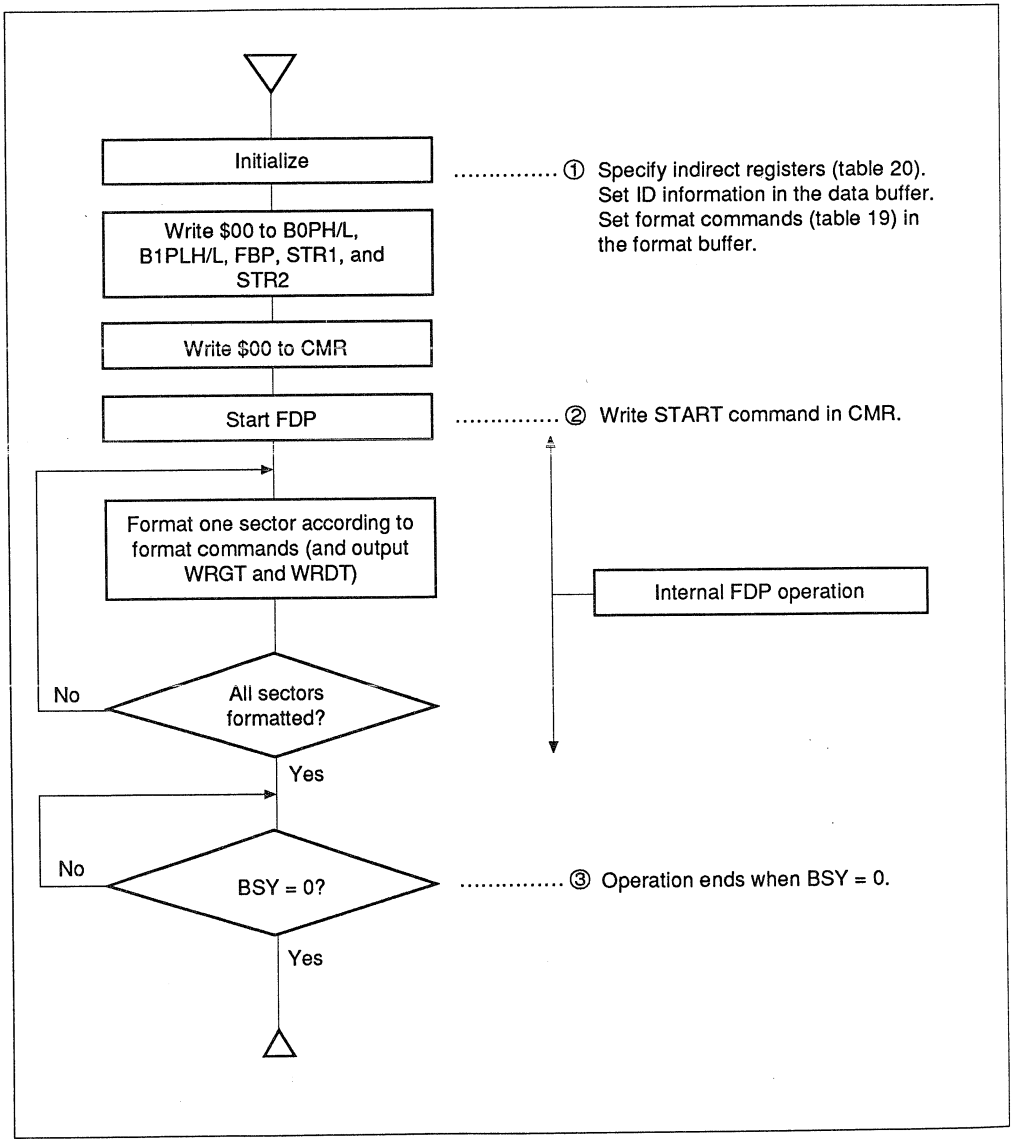


Figure 10 Formatting Flowchart

Table 19 Formatting Commands

FBP	FMTB1		FMTB2	FMTB3
00	WPAI + NOP	$18	$00	$07
01	WPTN + JRS	$0B	$00	$0B
02	WIDB + NOP	$B8	$00	$06
03	WCRC + NOP	$20	$00	$06
04	WPTN + NOP	$08	$00	$0B
05	WDTP + NOP	$C8	$02	$01
06	WECC + NOP	$28	$00	$06
07	WABSC + JMP	$3D	$00	$07
08	WPTN + NOP	$08	$00	$0B
09	WIDB + NOP	$B8	$00	$06
0A	WPTN + NOP	$08	$00	$0B
0B	WDTP + NOP	$C8	$02	$01
0C	WECC + NOP	$28	$00	$06
0D	WPUIS + NOP	$10	$00	$04
0E	END	$00	$00	$00

Table 20 Register Setting Example

Register	Setting	Register	Setting
IDR0	$A0	DAM0	$A1
TCR	$A2	DPAT	$00
LPCNT	$02	PLY0	$05
TMB	$03	PLY1	$A0
TMC	$FF	PLY2	($00)
MDR1	$32	PLY3	($00)
MDR2	$3D	PLY4	($00)
MDR3	($02)	PLY5	$A0
MDR4	$14	PLY6	$00

( ): Omittable

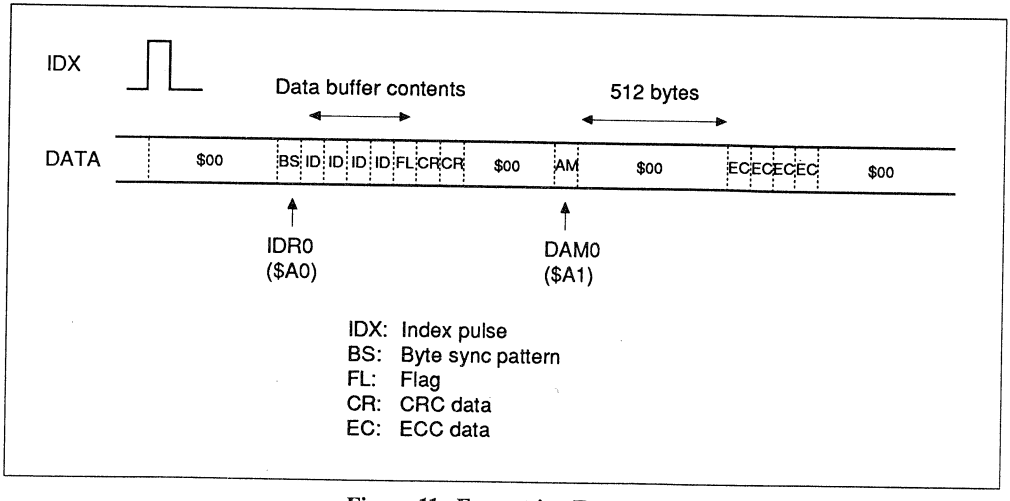


Figure 11 Formatting Example

Writing

Conditions: Hard sector mode, 3 sectors to be written, ECC data 4 bytes long (figure 12)

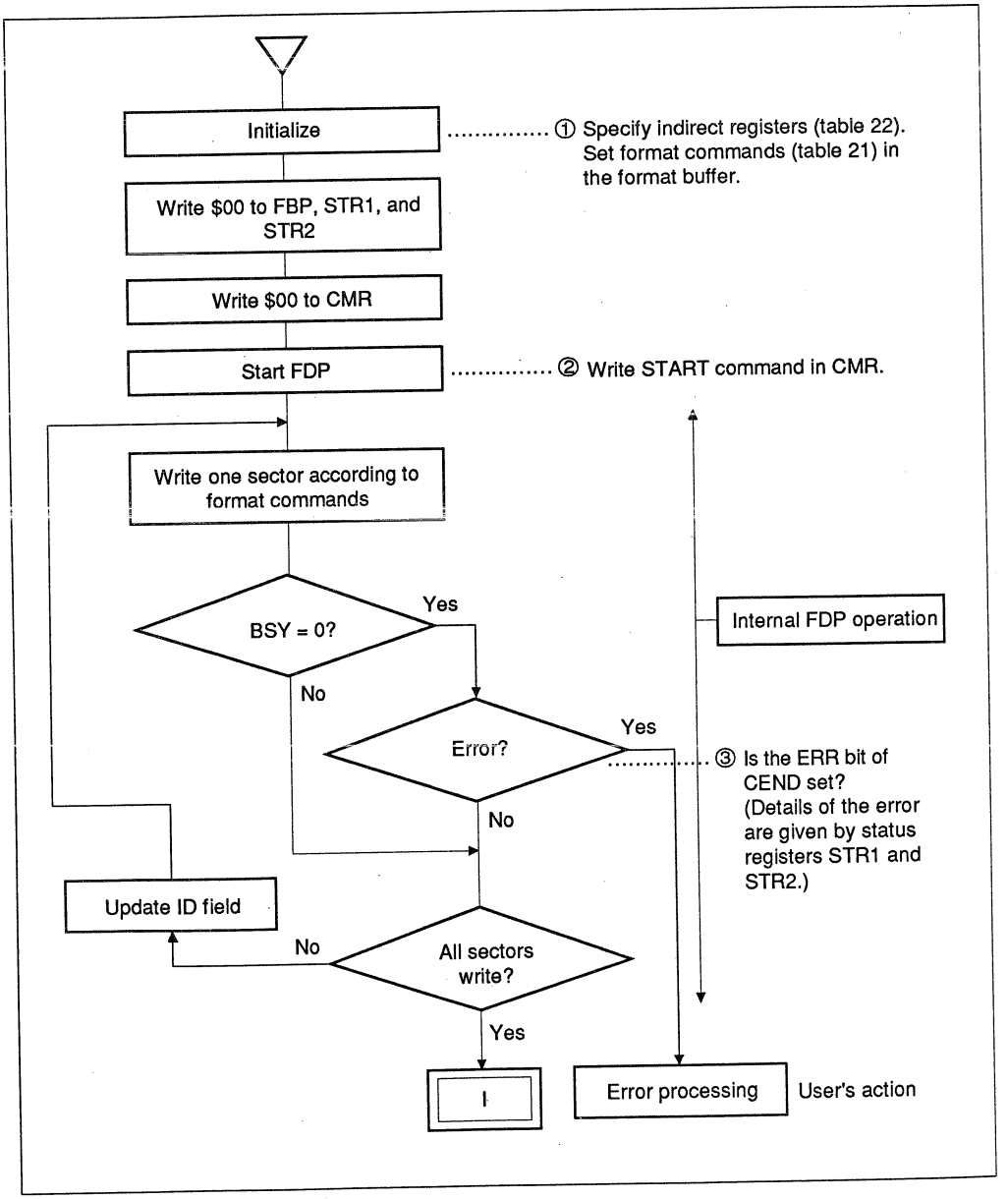


Figure 12 Write Flowchart

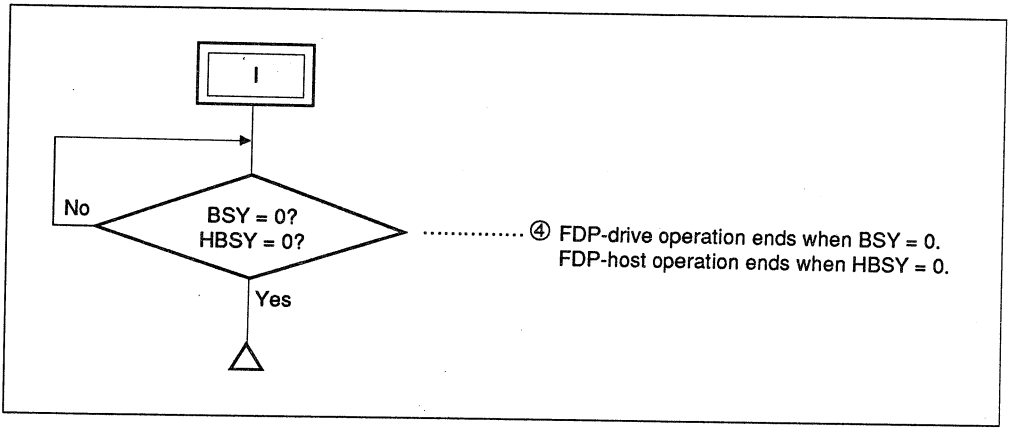


Figure 12 Write Flowchart (cont)

Table 21 Write Commands

FBP	FMTB1		FMTB2	FMTB3
00	DMAW + NOP	$50	$00	$04
01	WTISA + JRS	$B3	$00	$04
02	VID + RTY	$5E	$00	$06
03	VCRCW + RTY	$7E	$00	$0C
04	WDTB + RTY	$C6	$02	$01
05	WECC + NOP	$28	$00	$06
06	IDINC + JMP	$FD	$00	$04
07	END	$00	$00	$00
08				
09				
0A				
0B				
0C				

Table 22 Register Setting Example

Register	Setting	Register	Setting
IDR0	$A0	DAM0	$A1
IDR1	$00	B0PL	$00
IDR2	$01	B0PH	$00
IDR3	$01	B1PL	$00
IDR4	$01	B1PH	$00
IDR5	$00	SCNT	$03
TCR	$A2	PLY0	$05
SRLL	$00	PLY1	$A0
SRLH	$02	PLY2	($00)
LPCNT	$02	PLY3	($00)
TMB	$03	PLY4	($00)
TMC	$FF	PLY5	$A0
MDR1	$34	PLY6	$00
MDR2	$3D		
MDR3	$02		
MDR4	$14		

Reading

Conditions: Hard Sector mode, 3 sectors to be read, ECC data 4 bytes long

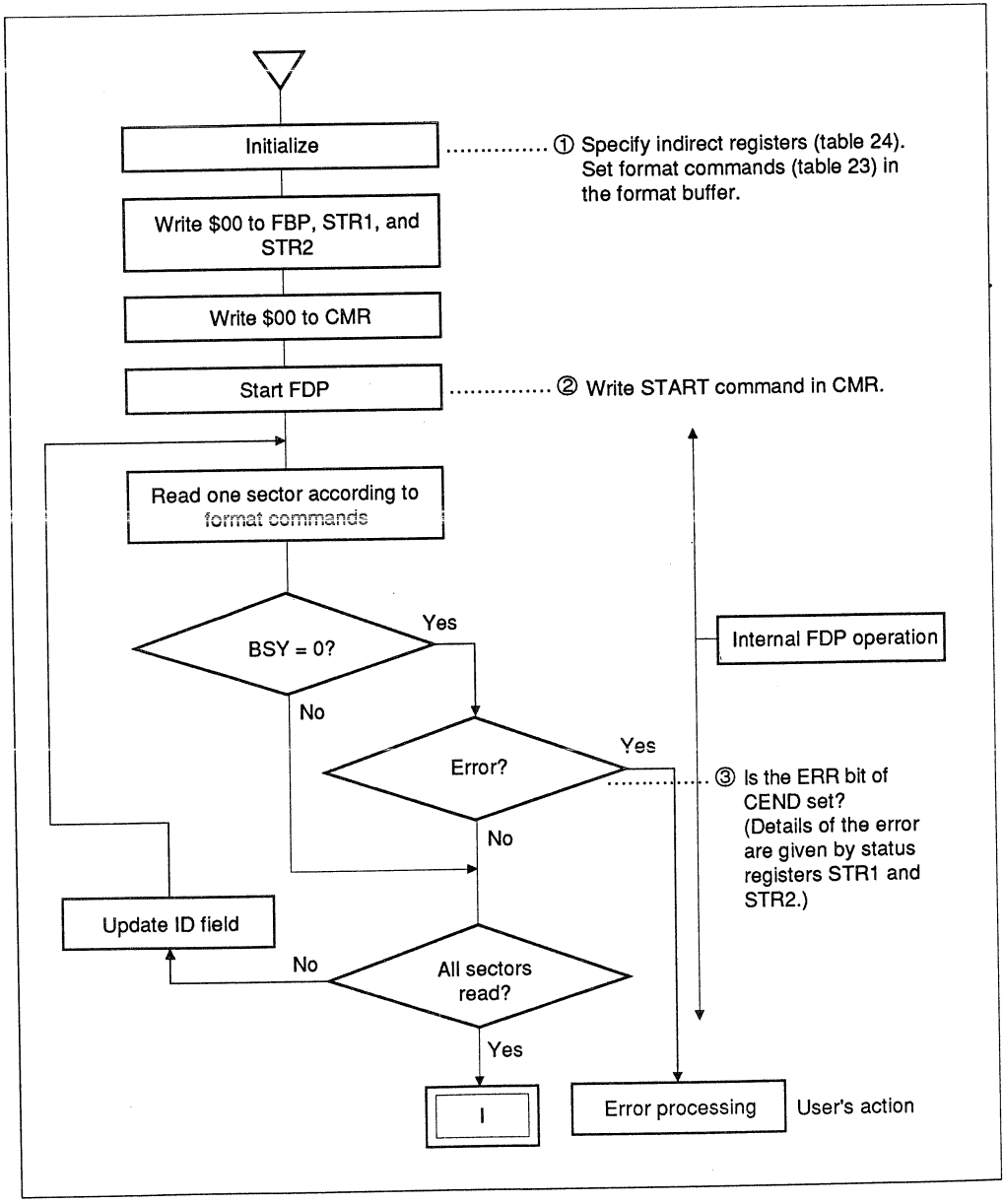


Figure 13 Read Flowchart

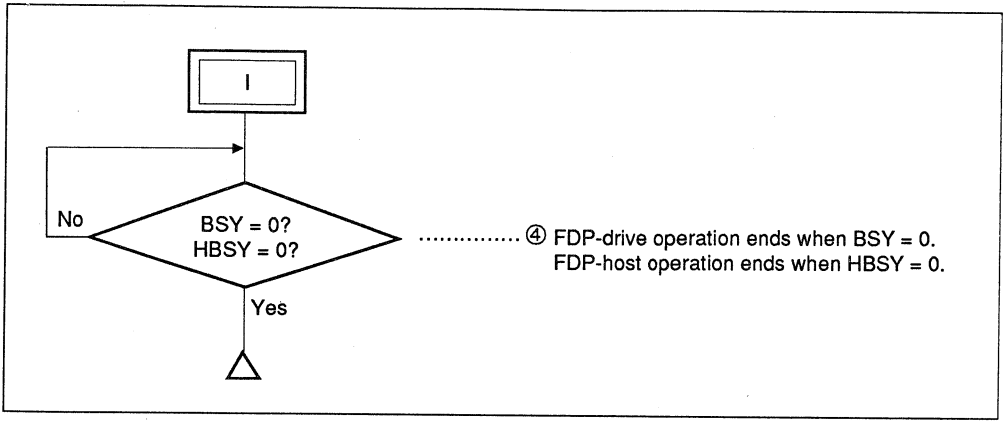


Figure 13 Read Flowchart (cont)

Table 23 Read Commands

FBP	FMTB1		FMTB2	FMTB3
00	WTISA + JRS	$B3	$00	$04
01	VID + RTY	$5E	$00	$06
02	VCRC + RTY	$6E	$00	$04
03	RDTB + RTY	$E6	$02	$02
04	CECC + NOP	$80	$00	$05
05	IDINC + JMP	$FD	$00	$04
06	END	$00	$00	$00
07				
08				
09				
0A				
0B				
0C				

Table 24 Register Setting Example

Register	Setting	Register	Setting
IDR0	$A0	DAM0	$A1
IDR1	$00	B0PL	$00
IDR2	$01	B0PH	$00
IDR3	$01	B1PL	$00
IDR4	$01	B1PH	$00
IDR5	$00	SCNT	$03
TCR	$A2	PLY0	$05
SRLL	$00	PLY1	$A0
SRLH	$02	PLY2	($00)
LPCNT	$02	PLY3	($00)
TMB	$03	PLY4	($00)
TMC	$FF	PLY5	$A0
MDR1	$34	PLY6	$00
MDR2	$3D		
MDR3	$02		
MDR4	$14		

Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note
Supply voltage	V_{cc}	–0.3 to +7.0	V	1
Input voltage	V_{in}	–0.3 to V_{cc} +0.3	V	1
Maximum output current	$\|I_o\|$	5	mA	2
Total allowable output current	$\|\Sigma I_o\|$	150	mA	3
Operating temperature	T_{opr}	0 to +70	°C	
Storage temperature	T_{stg}	–55 to +150	°C	

Notes: 1. With reference to V_{ss} = 0 V.
2. The maximum output current is the maximum current that may be drawn from, or flow out to, one output pin or one common input/output pin.
3. The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output pins or common input/output pins.
4. Using an LSI beyond its maximum ratings may result in its permanent destruction. The FDP must be used under the recommended operating conditions. Exceeding any of these conditions may adversely affect its reliability.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{cc}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.2	—	V_{cc}	V	1
Input low voltage	V_{IL}	0	—	0.8	V	1
Operating temperature	T_{opr}	0	25	70	°C	

Note: 1. With reference to V_{ss} = 0 V.

Output Timing Values

The levels at which output signal timings are measured are shown in figure 14.

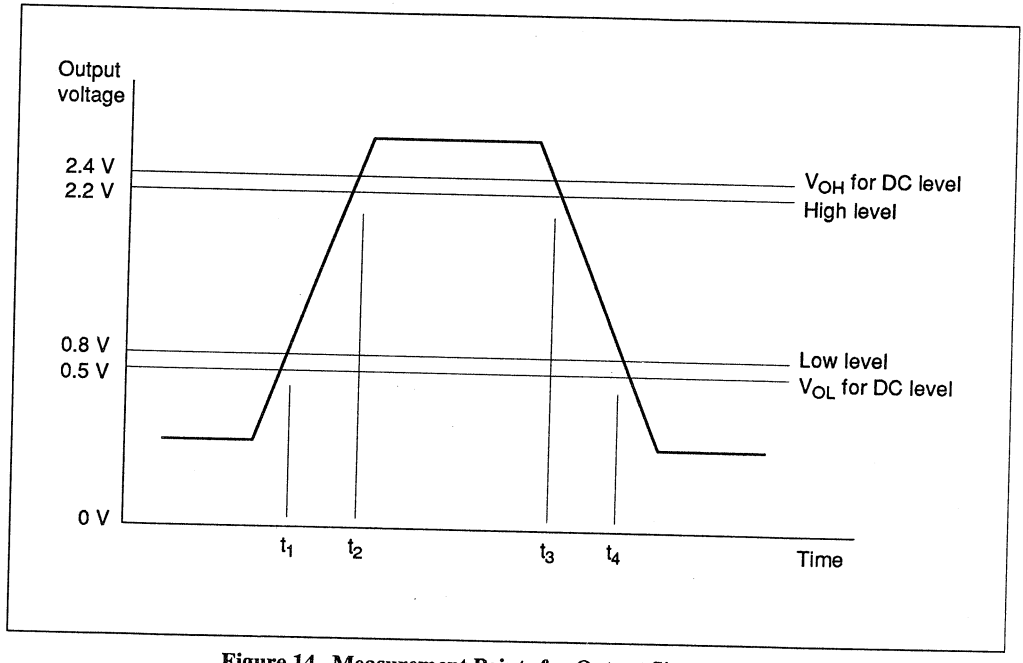


Figure 14 Measurement Points for Output Signal Timing

Electrical Characteristics

DC Characteristics (V_{cc} = 5.0 V ± 5%, V_{ss} = 0 V, Ta = 0 to + 70°C, unless otherwise specified)

Item		Symbol	Test Conditions	Limits Min	Typ	Max	Unit	Note
Supply voltage		V_{cc}		4.75	5.0	5.25	V	1
Input high voltage	All input pins	V_{IH}		2.2	—	V_{cc}	V	1
Input low voltage	All input pins	V_{IL}		–0.3	—	0.8	V	1
Output high voltage		V_{OH}	I_{OH} = –400 µA	2.4	—	—	V	1
Output low voltage		V_{OL}	I_{OL} = 1.6 mA	—	—	0.5	V	1
Input leakage current	RCLK, CC, CLK, S/AMF, RDT, RDY, $\overline{\text{DONE}}$, IDX, $\overline{\text{WAIT}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A_0–A_2, $\overline{\text{CS}}$ $\overline{\text{RST}}$	I_{in}	V_{in} = 0 V – V_{cc}	–2.5	—	2.5	µA	
3-state input current (off state)	D_0–D_7, $\overline{\text{DREQ}}$, BUS_{00}–BUS_{15}, P_0–P_7, $\overline{\text{DACK}}$ $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$	I_{TSI}	V_{in} = 0.4 V – V_{cc}	–10	—	10	µA	
Output leakage current (off state)	$\overline{\text{INT}}$	I_{LOD}	V_{OH} = V_{cc}	—	—	10	µA	
Input capacitance	All input pins	C_{in}	V_{in} = 0 V f = 1 MHz Ta = 25°C	—	—	20	pF	
Output capacitance	All output pins	C_{out}	V_{in} = 0 V f = 1 MHz Ta = 25°C	—	—	20	pF	
Current dissipation	During operation	I_{cc}	CLK = 12 MHz, RCLK = 15 MHz, V_{cc} = 5.25 V, Rated load	—	40	70	mA	

Note: 1. With reference to V_{ss}= 0 V.

AC Characteristics

Clock Cycle

Numbers in the leftmost columns of the tables on this and the following pages refer to numbers in figures 15 to 28.

No.	Item	Symbol	Min	Max	Unit	Note
1	Clock cycle time	t_{CYC}	81	250	ns	
2	Clock low level pulse width	t_{PWCL}	36	—	ns	
3	Clock high level pulse width	t_{PWCH}	36	—	ns	
4	Clock rise time	t_{CR}	—	5	ns	
5	Clock fall time	t_{CF}	—	5	ns	
6	Read clock cycle time	t_{RCYC}	66	250	ns	
7	Read clock low level pulse width	t_{RCL}	0.45	0.55	t_{RCYC}	
8	Read clock high level pulse width	t_{RCH}	0.45	0.55	t_{RCYC}	
9	Read clock rise time	t_{RCR}	—	5	ns	
10	Read clock fall time	t_{RCF}	—	5	ns	
11	Write clock cycle time	t_{WCYC}			= t_{RCYC}	
12	Write clock low level width	t_{WCL}	t_{RCL} – 10	t_{RCL} + 10	ns	
13	Write clock high level width	t_{WCH}	t_{RCH} – 10	t_{RCH} + 15	ns	
14	Write clock rise time	t_{WCR}	—	10	ns	
15	Write clock fall time	t_{WCF}	—	10	ns	
17	Read clock low level width 1	t_{RCL1}	—	400	ns	
18	Read clock high level width 1	t_{RCH1}	—	400	ns	
20	$\overline{RST}$ input pulse width	t_{RES}	30	—	t_{CYC}	
23	V_{cc} to CLK time	t_{VCT}	—	100	ms	
24	V_{cc} to $\overline{RST}$ time	t_{VRT}	100	—	ms	
25	$\overline{RST}$ rise time	t_{RRT}	—	20	ns	
26	$\overline{INT}$ delay time	t_{IDT}	—	110	ns	
27	$\overline{INT}$ release time	t_{IRT}	—	300	ns	

File Manager Interface

No.	Item		Symbol	Min	Max	Unit	Note
30	Address setup time		t_{AS1}	5	—	ns	1
31			t_{AS2}	10	—	ns	
32	Address hold time		t_{AH1}	10	—	ns	
33	$\overline{RD}$, $\overline{WR}$ pulse width	Except during TMA, TMC, or TMD read	t_{PW1}	2	—	t_{CYC}	
		During TMA, TMC, or TMD read		3	—		2
34	Read data delay time	Except during TMA, TMC, or TMD read	t_{DDR1}	—	100 ns	—	
		During TMA, TMC, or TMD read		—	1 t_{CYC} + 100 ns		2
35	Read data hold time		t_{HR1}	20	—	ns	
36	Write data setup time		t_{DSW1}	30	—	ns	
37	Write data hold time		t_{HW1}	20	—	ns	

Notes: 1. If t_{PW1} or t_{DDR1} is incremented by 1 t_{CYC}, the minimum value of t_{AS1} is −40 ns.
2. When the timers (TMA, TMB, TMC, and TMD) are being read, t_{PW1} min is 3 t_{cyc} and t_{DDR1} max is 1 t_{CYC} + 100 ns. The status of a timer is detected by reading the contents of STR2 and CEND.

Host Interface (slave mode)

No.	Item		Symbol	Min	Max	Unit	Note
40	$\overline{IORD}$, $\overline{IOWR}$ cycle time	8 bits	t_{HCYC}	3	—	t_{CYC}	
		16 bits		4	—		
41	$\overline{DACK}$ release after $\overline{IORD}$, $\overline{IOWR}$		t_{AKD}	0	—	ns	
42	$\overline{IORD}$, $\overline{IOWR}$ delay		t_{ACDS}	5	—	ns	1
43	$\overline{DREQ}$ release after $\overline{DONE}$		t_{DRQD}	0.5 t_{CYC}	1.5 t_{CYC} + 100 ns		
45	$\overline{DREQ}$ release after $\overline{DACK}$		t_{ARQD}	0.5 t_{CYC}	1.5 t_{CYC} + 100 ns		
46	$\overline{DREQ}$ release after $\overline{IORD}$, $\overline{IOWR}$		t_{CRQD1}	0.5 t_{CYC}	1.5 t_{CYC} + 100 ns		
48	$\overline{DREQ}$ release after $\overline{IORD}$, $\overline{IOWR}$ negation	8 bits	t_{CRQD2}	1.5 t_{CYC}	2.5 t_{CYC} + 100 ns		
		16 bits		2.5 t_{CYC}	3.5 t_{CYC} + 100 ns		
49	$\overline{DONE}$ low level pulse width		t_{DONE}	2	—	t_{CYC}	
50	$\overline{IORD}$, $\overline{IOWR}$ low pulse width		t_{PWL}	2 t_{CYC} − 10 ns	—		
51	$\overline{IORD}$, $\overline{IOWR}$ high level pulse width	8 bits	t_{PWH}	1 t_{CYC} − 10 ns	—		
		16 bits		2 t_{CYC} − 10 ns	—		
52	BUS_{00}-BUS_{15} read data delay time		t_{DDR2}	—	1 t_{CYC} + 70 ns		
53	BUS_{00}-BUS_{15} read data hold time		t_{HR2}	20	—	ns	
54	BUS_{00}-BUS_{15} write data setup time		t_{DSW2}	30	—	ns	
55	BUS_{00}-BUS_{15} write data hold time		t_{HW2}	20	—	ns	

Host Interface (slave mode) (cont)

No.	Item		Symbol	Min	Max	Unit	Note
56	BUS_{00}-BUS_{15} read data hold time after $\overline{IORD}$, $\overline{IOWR}$ negation	8 bits	t_{DDR3}	—	2 t_{CYC} + 70 ns		
		16 bits		—	3 t_{CYC} + 70 ns		
57	$\overline{DACK}$ response time		t_{AKR}	0	—	ns	
58	$\overline{DREQ}$ delay after $\overline{DACK}$		t_{RQDA}	0.5 t_{CYC}	1.5 t_{CYC} + 100 ns		

Note: 1. If t_{PWL} or t_{DDR2} is incremented by 1 t_{CYC}, the minimum value of t_{ACDS} is –40 ns.

Host Interface (master mode)

No.	Item	Symbol	Min	Max	Unit	Note
60	$\overline{DACK}$ delay time	t_{ACD}	0	80	ns	
61	$\overline{IORD}$, $\overline{IOWR}$ delay time	t_{RWD}	0	80	ns	
62	$\overline{DREQ}$ setup time	t_{RQS}	10	—	ns	
63	$\overline{DREQ}$ hold time	t_{RQH}	20	—	ns	
64	BUS_{00}-BUS_{07} read data setup time	t_{DSR}	60	—	ns	
65	BUS_{00}-BUS_{07} read data hold time	t_{HRM}	10	—	ns	
66	BUS_{00}-BUS_{07} write data delay time	t_{DDW}	—	50	ns	
67	BUS_{00}-BUS_{07} write data hold time	t_{HWM}	10	—	ns	
68	$\overline{WAIT}$ setup time	t_{WTS}	10	—	ns	
69	$\overline{WAIT}$ hold time	t_{WTH}	20	—	ns	
70	$\overline{DACK}$ release after $\overline{DONE}$	t_{DAKD}	2.5 t_{CYC}	3.5 t_{CYC} + 100 ns		
71	$\overline{DACK}$ release after $\overline{DREQ}$	t_{RAKD}	2.5 t_{CYC}	3.5 t_{CYC} + 100 ns		

Drive Interface

No.	Item	Symbol	Min	Max	Unit	Note
80	RDT setup time	t_{RDTS}	10	—	ns	
81	RDT hold time	t_{RDTH}	10	—	ns	
82	RDGT delay time	t_{RGTD}	0	100	ns	
83	WDT delay after WCLK	t_{WDTD}	—	15	ns	1
84	WDT hold after WCLK	t_{WDTH}	20	—	ns	
85	WRGT delay time	t_{WGTD}	0	100	ns	
86	AME delay time	t_{AMED}	0	100	ns	
87	IDX pulse width	t_{PWIDX}	2	—	t_{RCYC}	
88	S/AMF pulse width	t_{PWSA}	2	—	t_{RCYC}	
89	RDY, CC pulse width	t_{RDYCC}	2	—	t_{CYC}	
100	WDT delay after RCLK	t_{WDTD2}	—	30	ns	
101	WDT hold after RCLK	t_{WDTH2}	30	—	ns	

Note: 1. WDT setup time minimum from WCLK is 10 ns.

Port

No.	Item	Symbol	Min	Max	Unit	Note
90	P_0–P_7 $\overline{WR}$ setup time	t_{PWS}	30	—	ns	
91	P_0–P_7 write data delay time	t_{PWD}	—	100	ns	
92	P_0–P_7 read data setup time	t_{PRS}	30	—	ns	
93	P_0–P_7 read data hold time	t_{PRH}	30	—	ns	
94	P_0–P_7 $\overline{RD}$ delay time	t_{PRD}	30	—	ns	

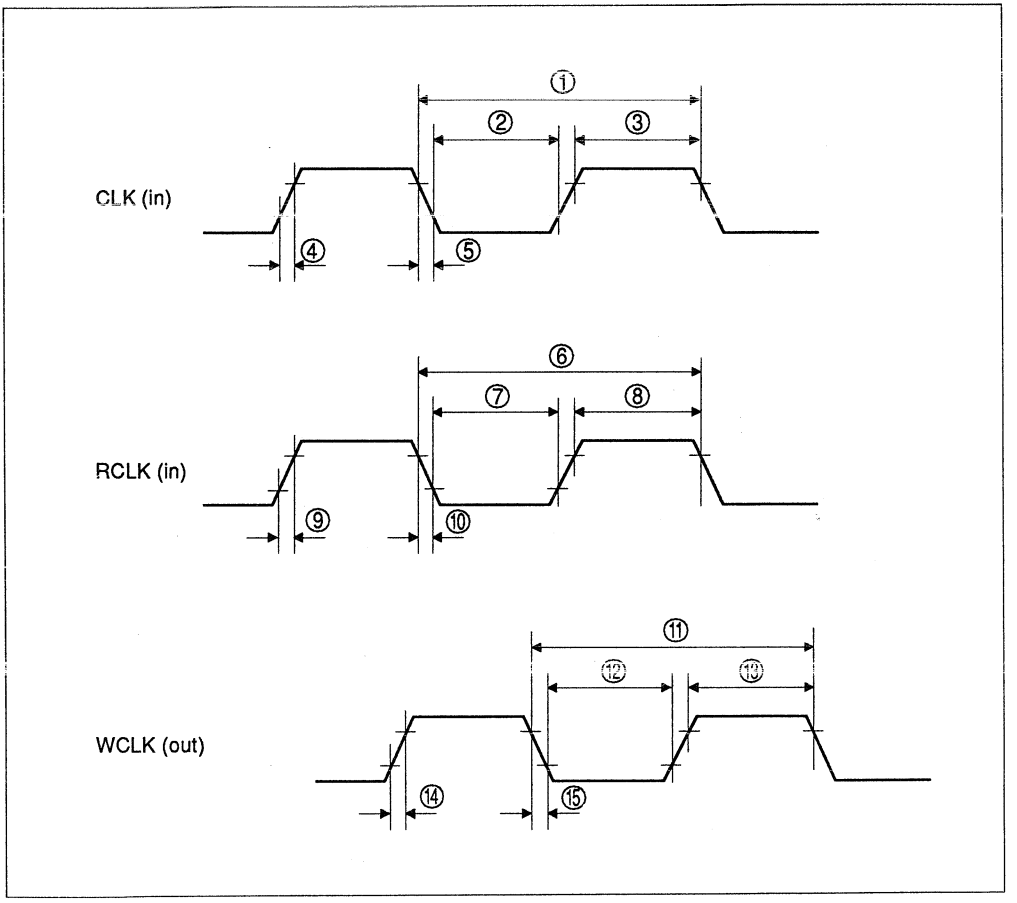


Figure 15 Clocks

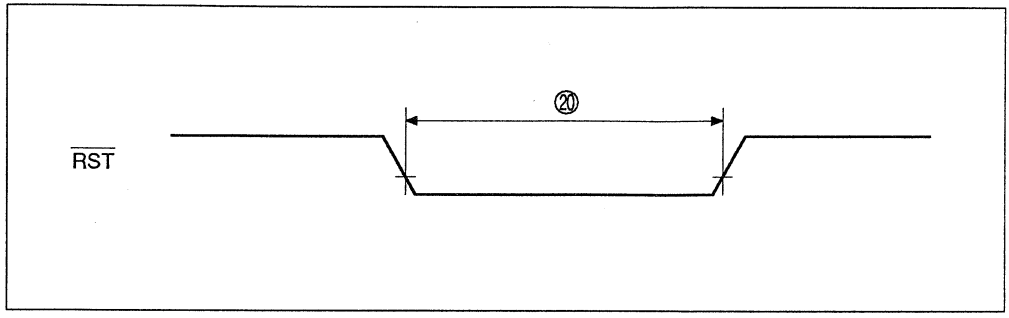


Figure 16 Reset

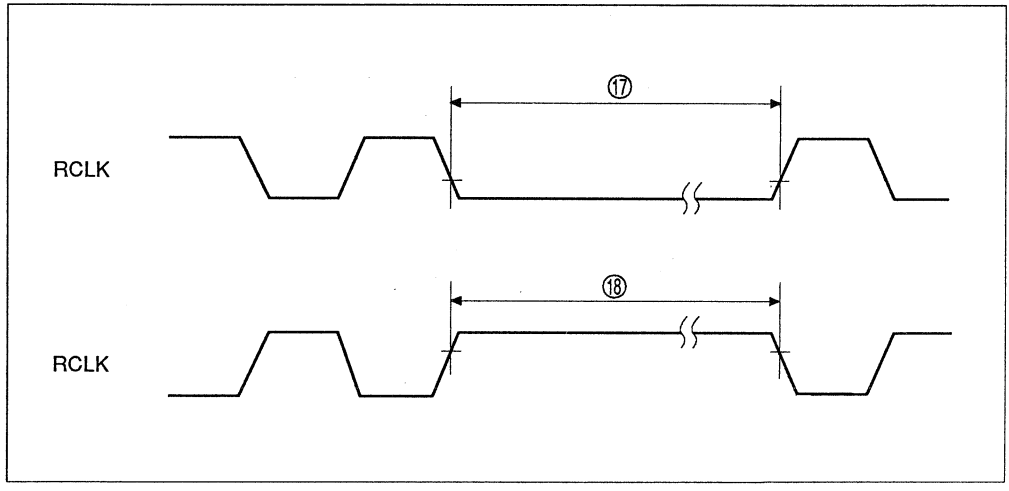


Figure 17 RCLK Waveform at Clock Switching (Non-operating)

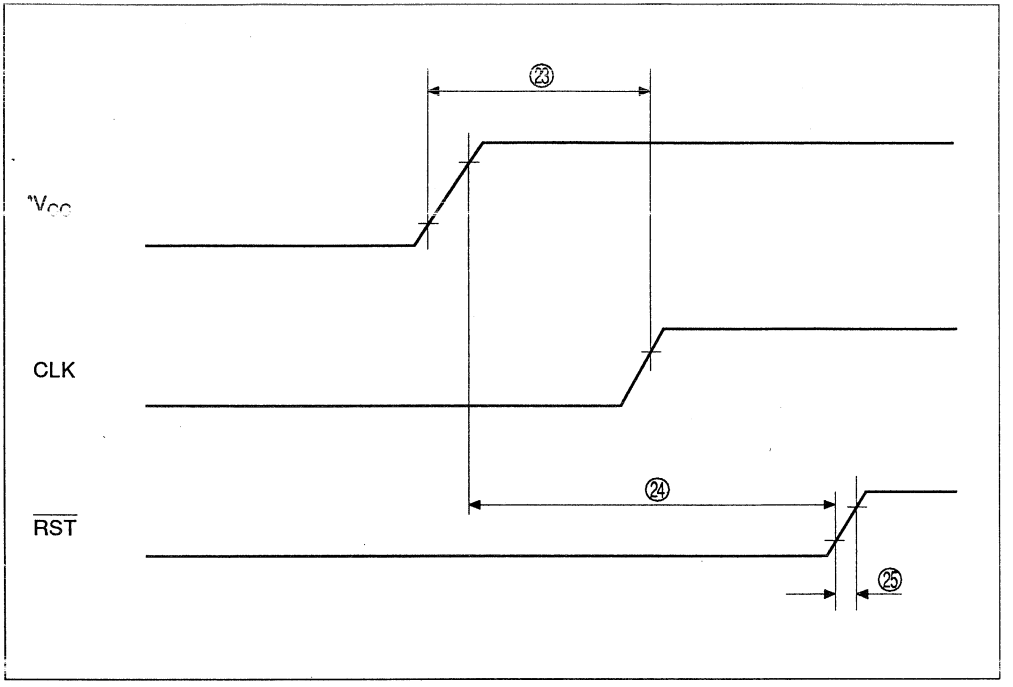


Figure 18 Power-on Timing

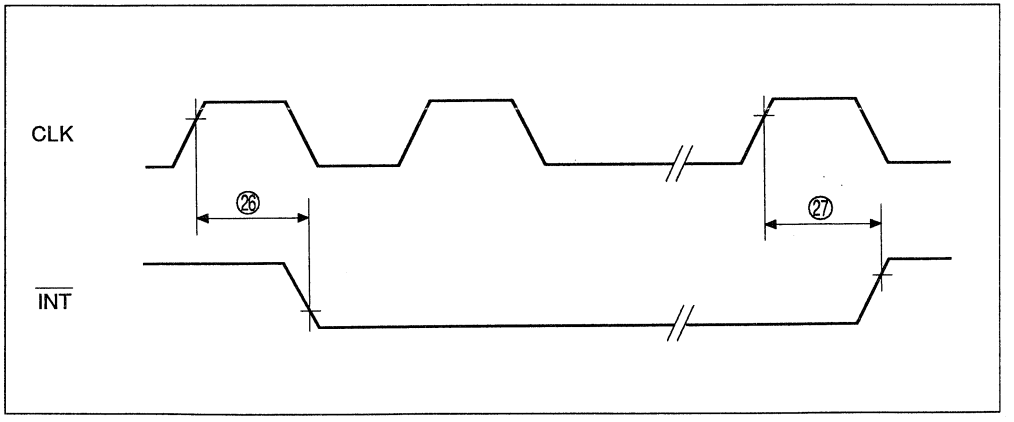
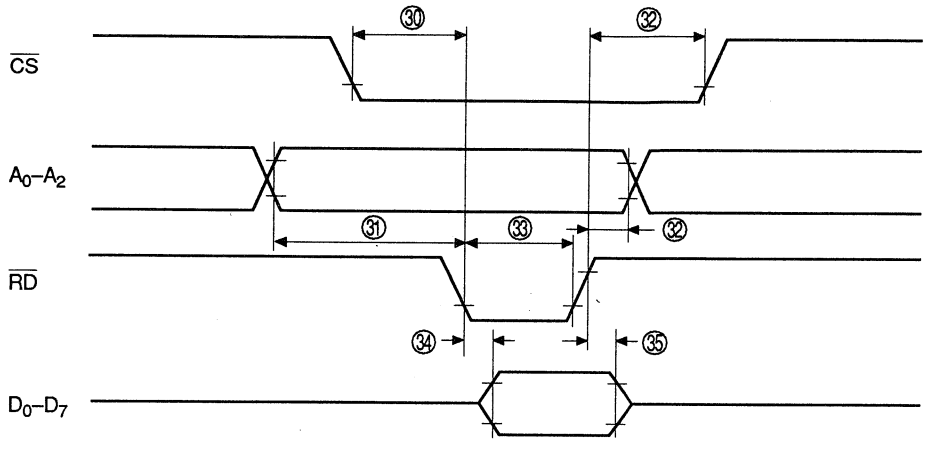
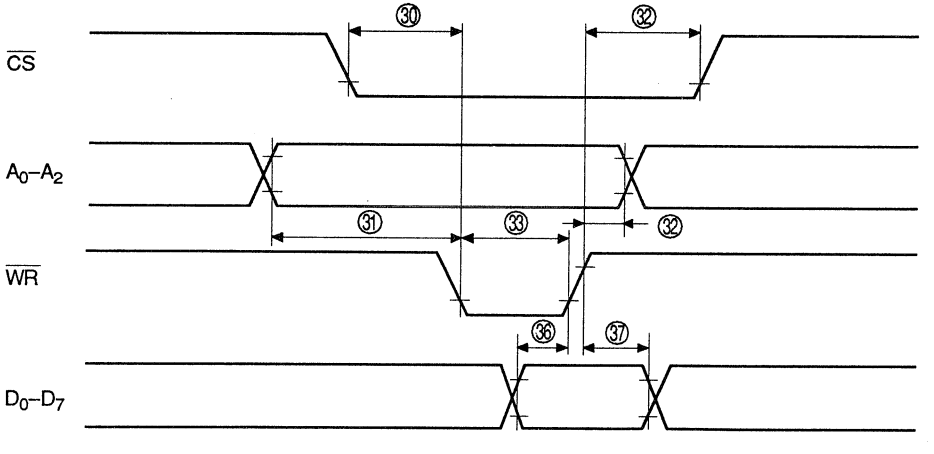


Figure 19 $\overline{\text{INT}}$ Output Timing



(a) Read Timing



(b) Write Timing

Figure 20 File Manager Interface

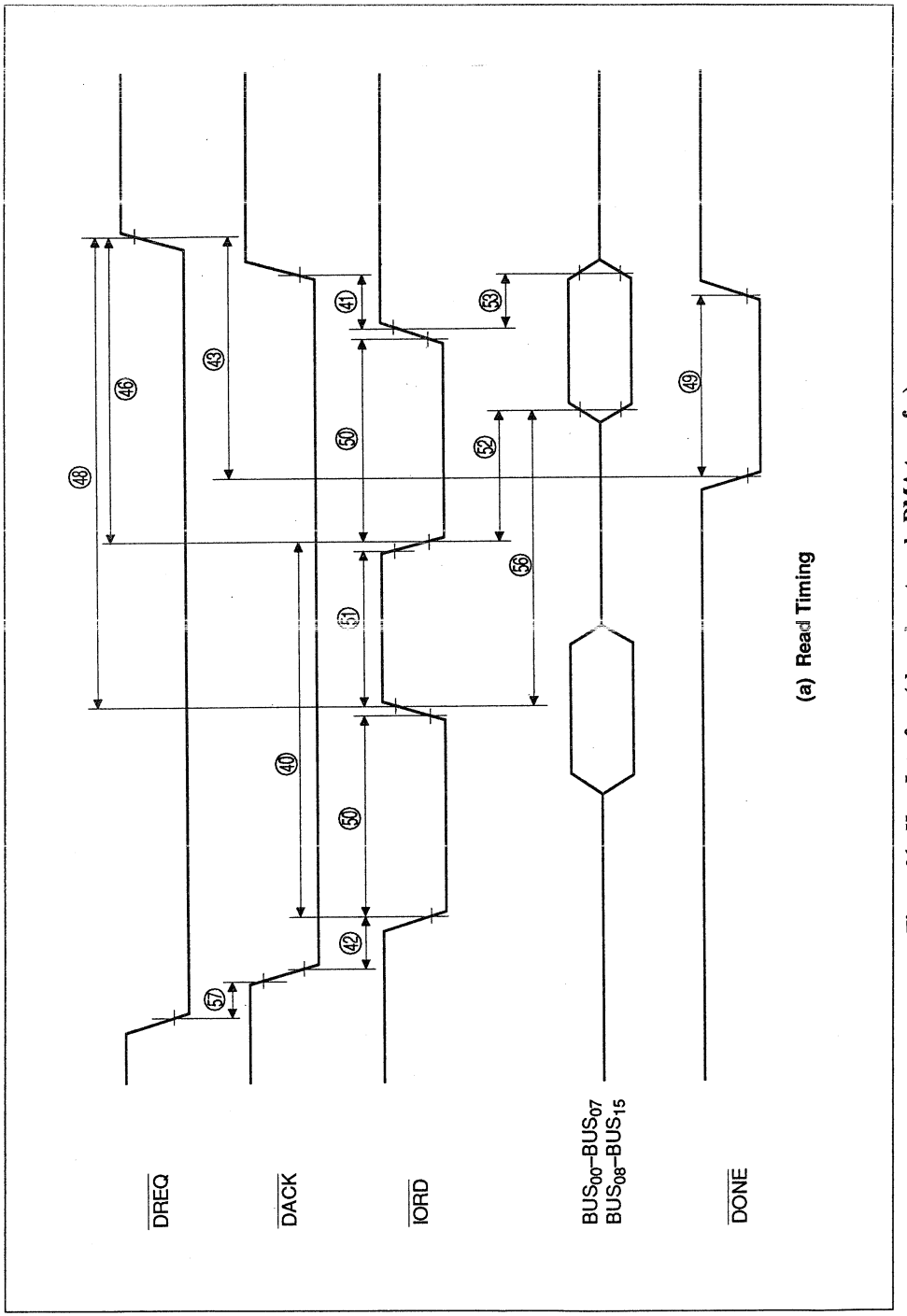
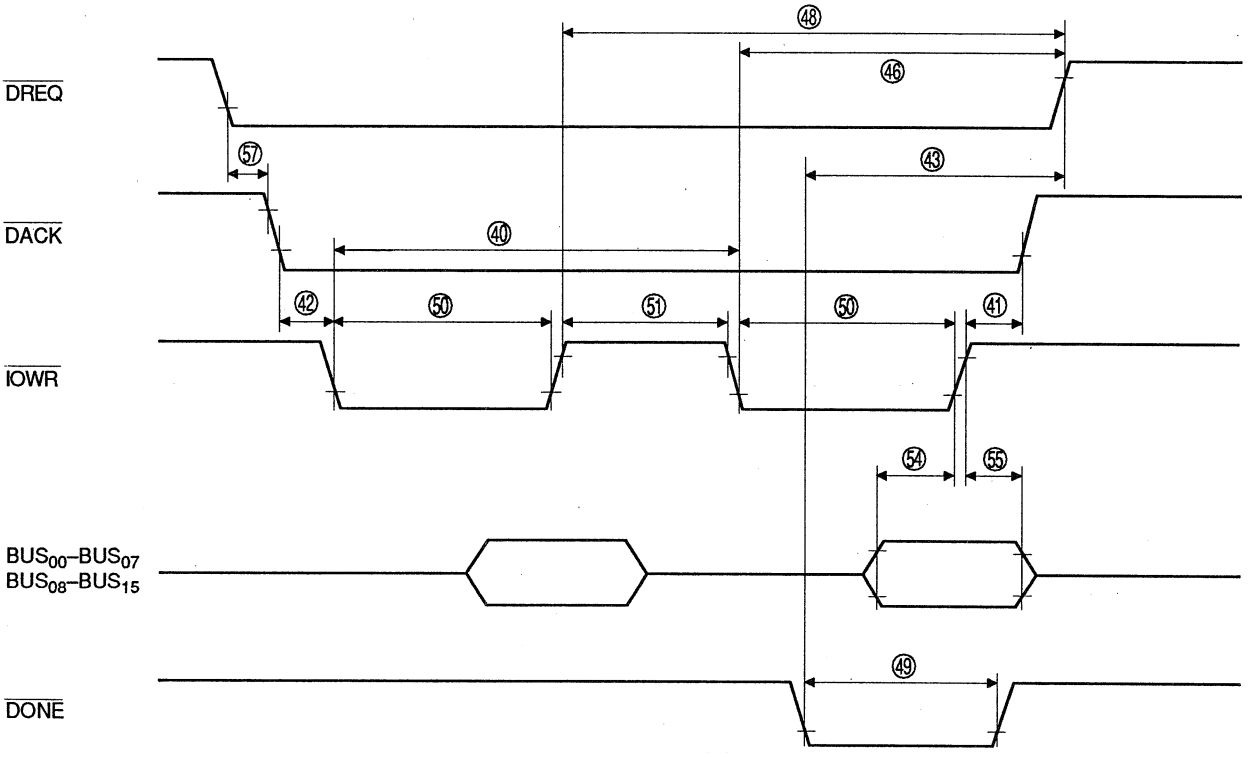


Figure 21 Host Interface (slave, burst mode DMA transfer)



(b) Write Timing

Figure 22 Host Interface (slave, burst mode DMA transfer) (cont)

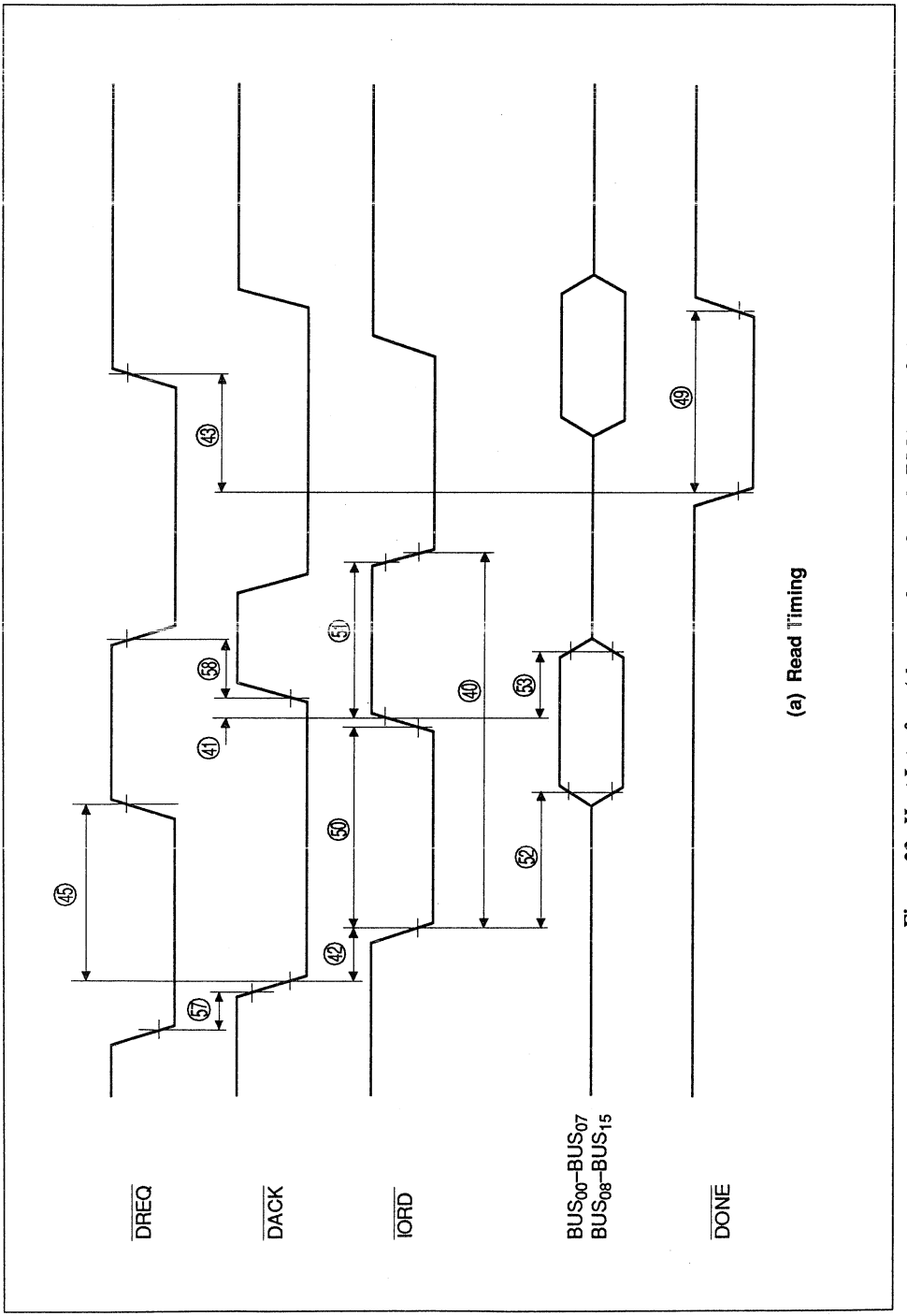


Figure 23 Host Interface (slave, cycle steal mode DMA transfer)

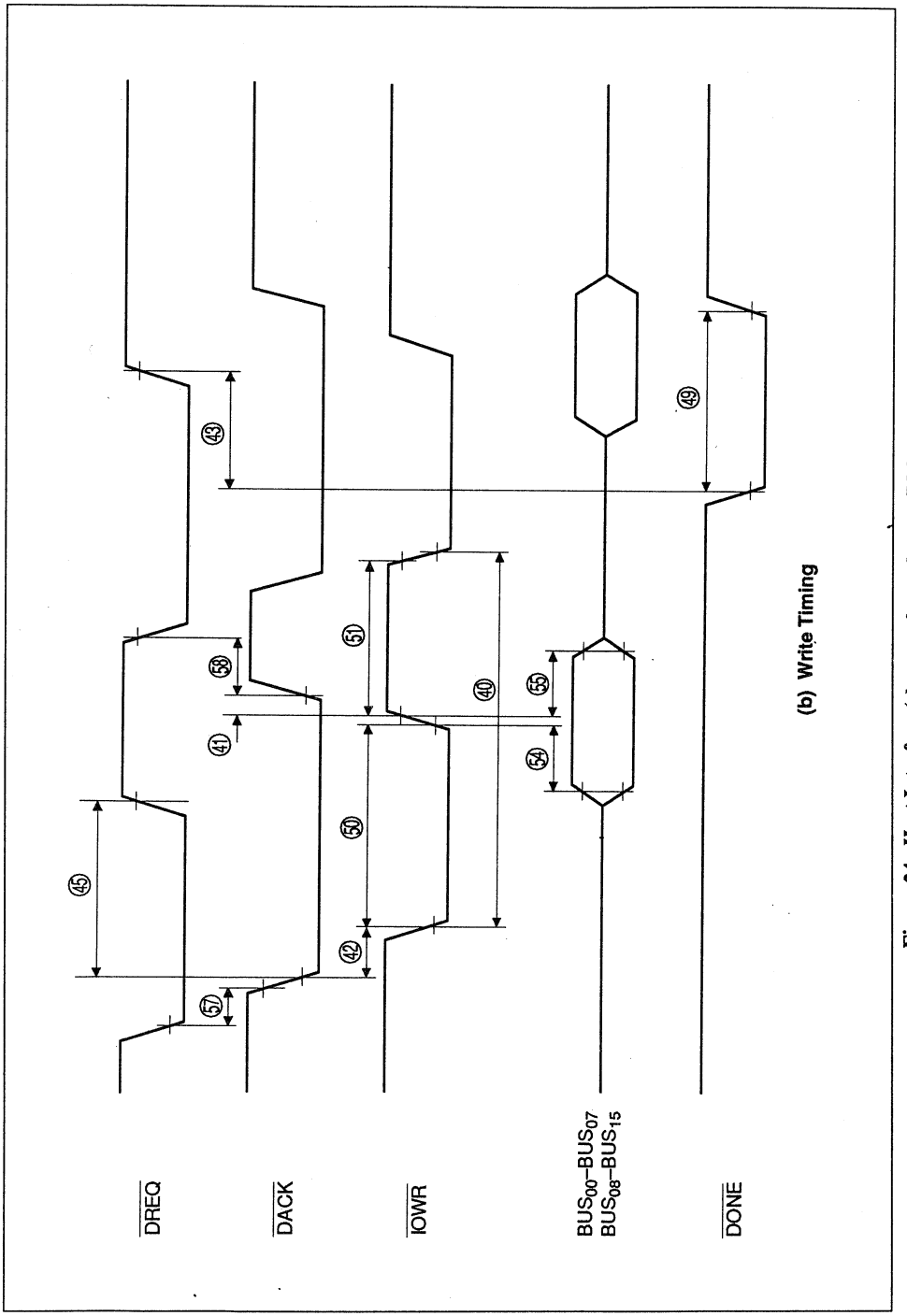


Figure 24 Host Interface (slave, cycle steal mode DMA transfer) (cont)

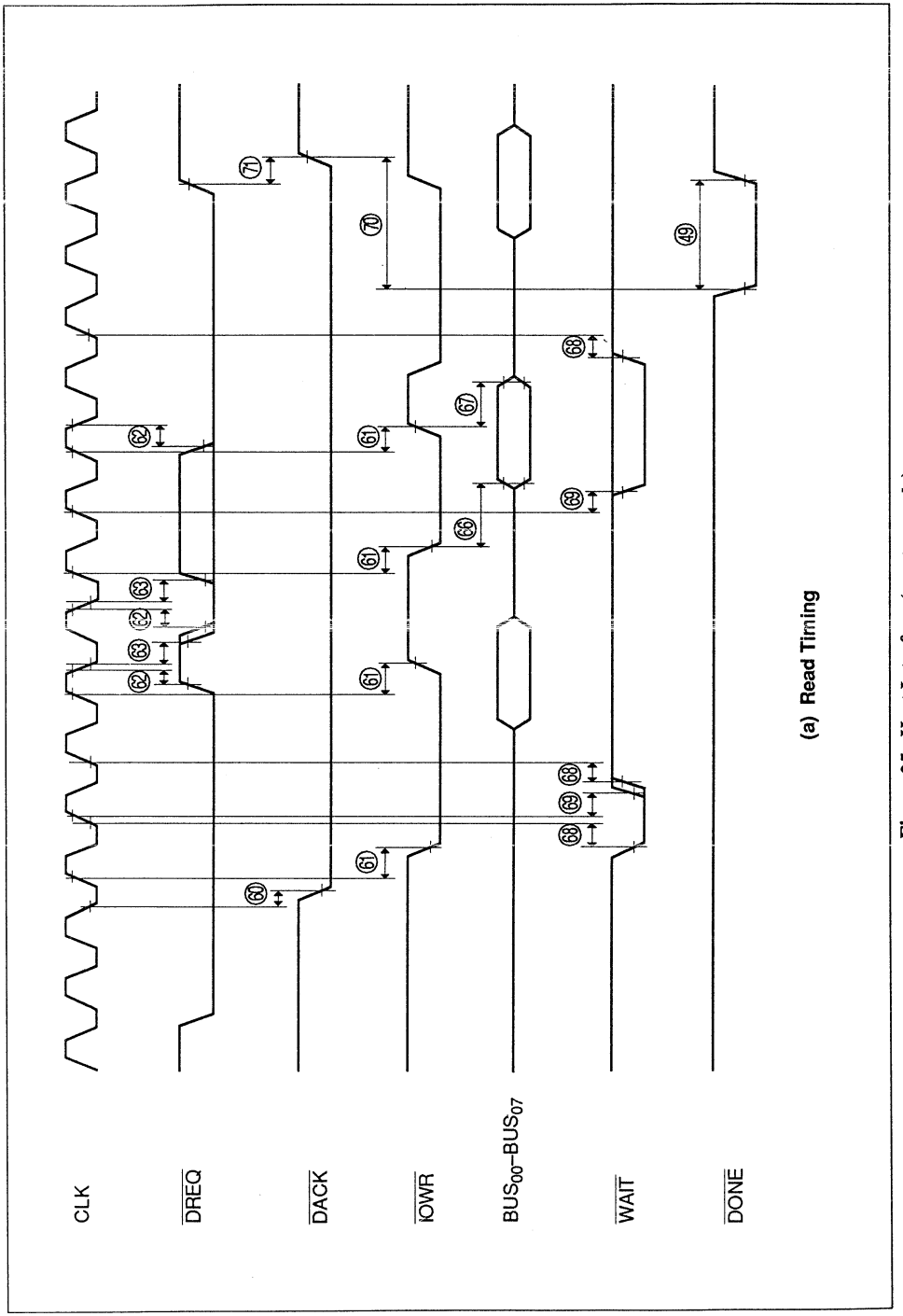
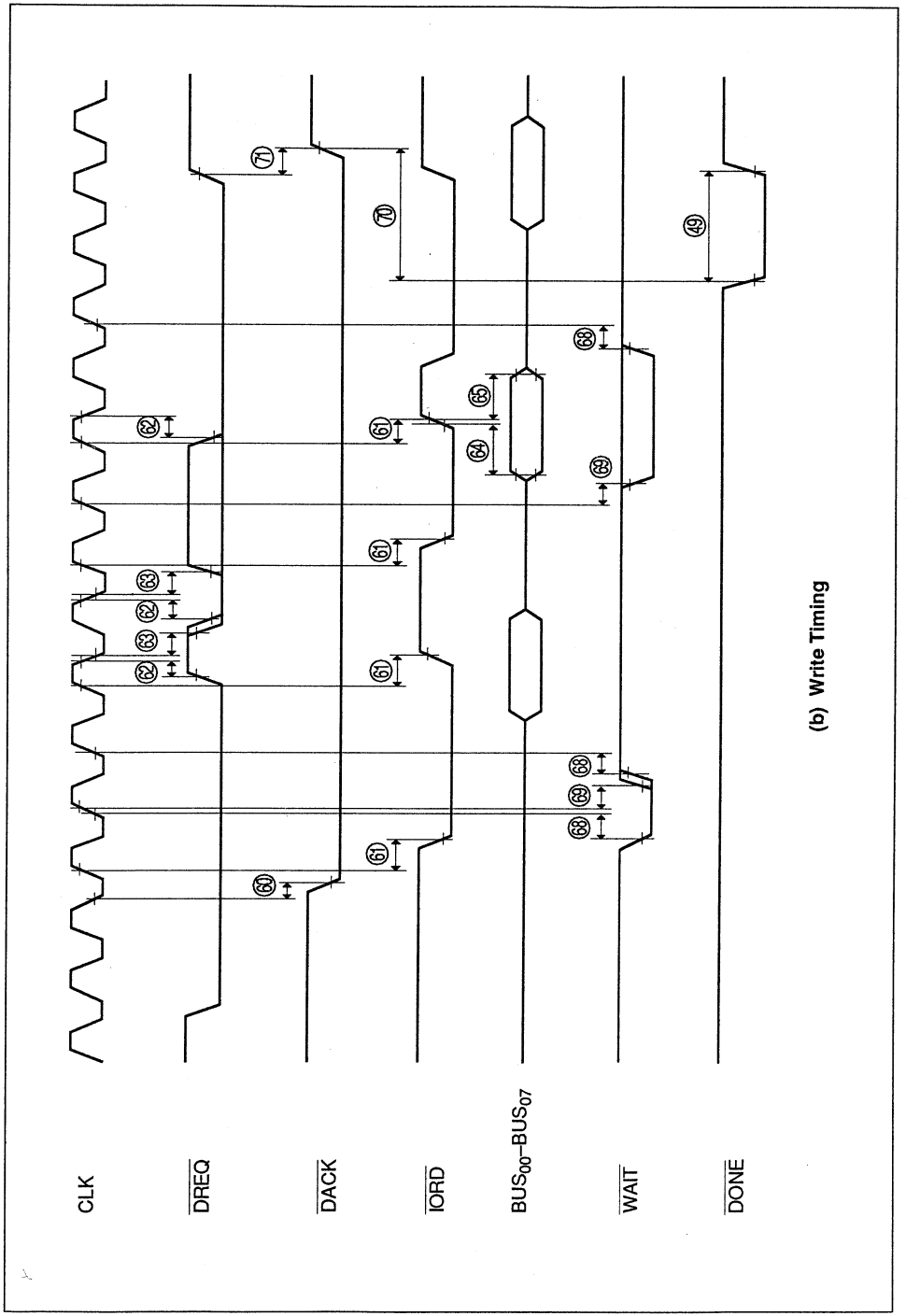


Figure 25 Host Interface (master mode)



(b) Write Timing

Figure 26 Host Interface (master mode) (cont)

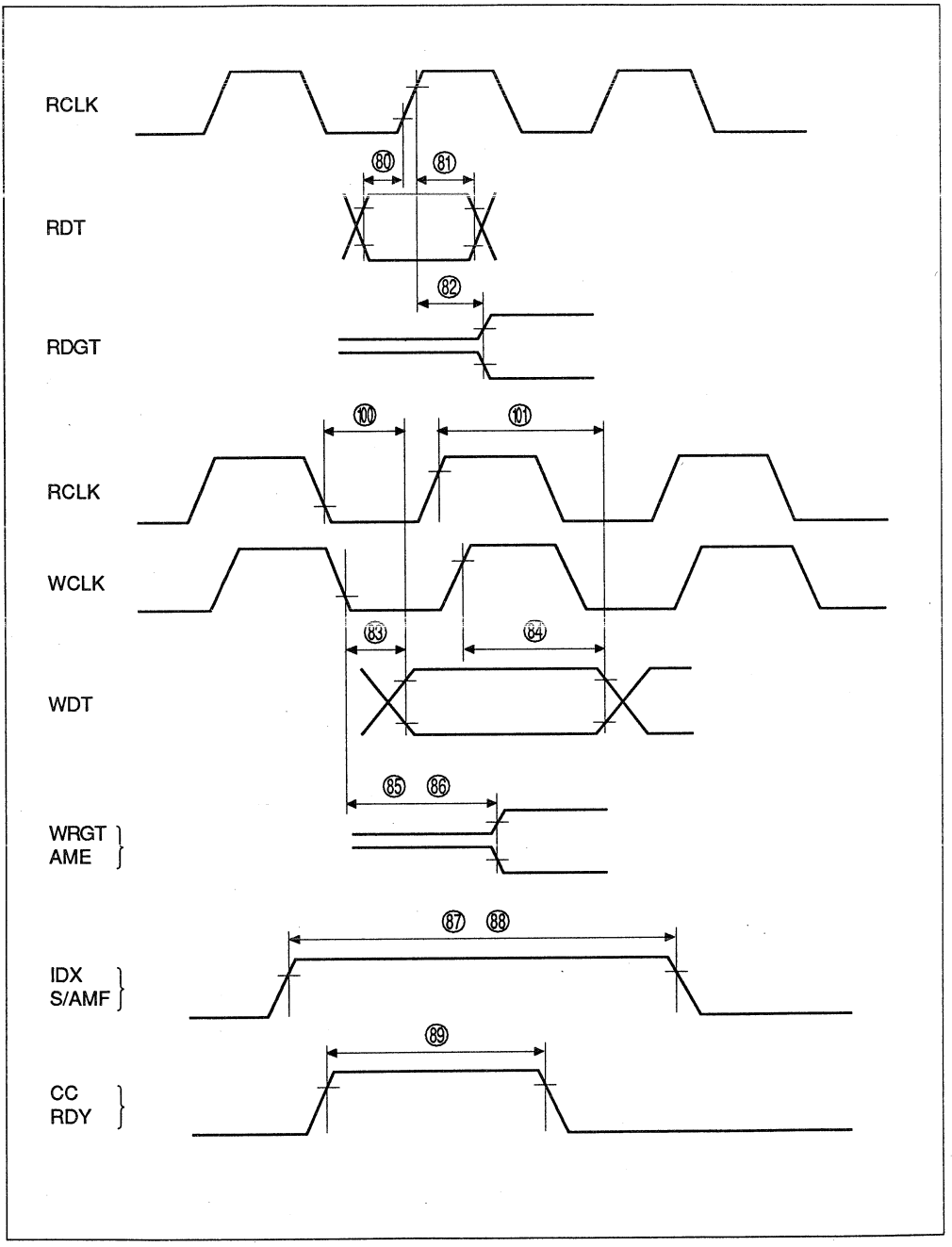


Figure 27 Drive Interface

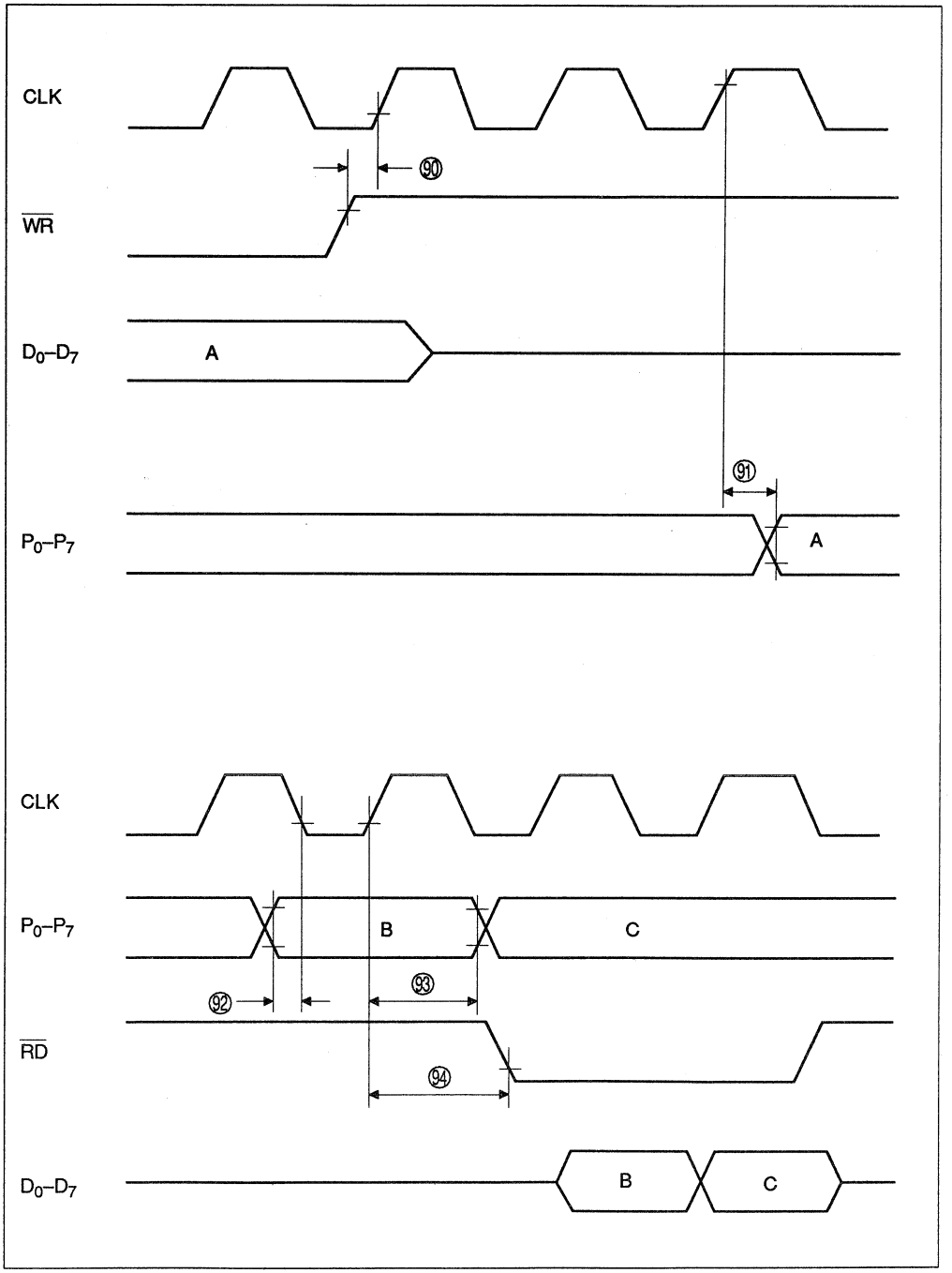


Figure 28 Ports

HD64951

SCSI Controller

The HD64951 is designed to control a high-performance peripheral interface known as SCSI (small computer system interface). This device contains a SCSI driver/receiver to facilitate SCSI bus operation.

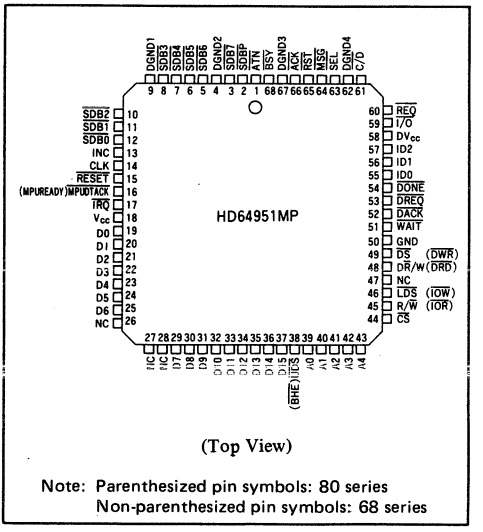
Functions

- Driver (48 mA sink) and receiver (with Schmitt-trigger inputs)
- 8/16-bit bus switching
- MPU and DMAC interface circuit
- SCSI bus interface circuit
- Auto arbitration/selection
- Auto non-arbitration/selection
- Auto single initiator/selection

Features

- Supports both initiator and target
- Transfer mode: high speed asynchronous transfer (1.3 Mbytes/s max)
- Built-in time-out detection counter (8 bits)
- Microcomputer bus: directly connectable to 6310, 68000, and 80-series MPU (both 8 and 16 bits)
- DMA function: directly connectable to FDP, HD68450, and 80-series DMAC (both 8 and 16 bits)

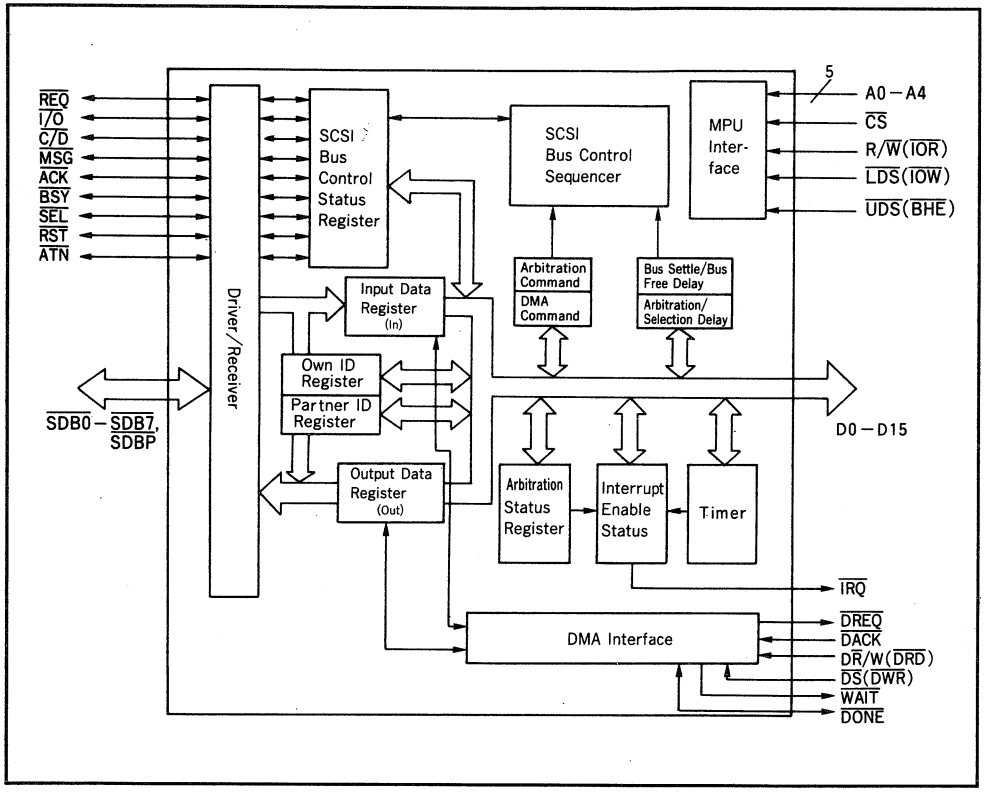
Pin Arrangement



(Top View)

Note: Parenthesized pin symbols: 80 series
Non-parenthesized pin symbols: 68 series

Block Diagram



Pin Description

The HD64951 provides two signal interfaces: the MPU/DMA and the SCSI interface signals (table 1). The HD64951 can control the bus connected to a 68- or 80-series MPU or DMAC. The SCSI bus phases can be controlled by commands received from the MPU.

Table 1. Pin Function

Interface	Pin No.	Symbol	I/O	Name	Function
MPU/DMA	19 to 25 29 30 to 37	D0 to D15 D7 D8 to D15	I/O	Data bus	The MPU/DMA interface (figure 1) enables the MPU/DMAC to access the HD64951 registers, to supply a clock signal to the HD64951, and to reset the HD64951 interface circuits. The data bus transfers data between the MPU and the HD64951. They are used in MPU or DMA mode as follows: • In MPU mode, the MPU can access the HD64951's internal registers • In DMA mode, data is transferred by DMA between the HD64951 and another peripheral or memory In 8-bit mode, use D0-D7. In 16-bit mode, use D0-D7 and D8-D15. During 8-bit DMA transfer, use D8-D15, the MPU can read all registers except the input/output data registers via D0-D7. In case of 16-bit DMA, use D0-D7 and D8-D15, can transfer each byte individually.
	39 to 43	A0 to A4	I	Address bus	The address bus inputs address signals from the MPU in either MPU or DMA mode (byte transfer mode only). It selects the HD64951's internal registers.
	44	$\overline{CS}$	I	Chip Select	$\overline{CS}$ input low enables the MPU to select the HD64951.
	45	$\overline{IOR}$	I	I/O Read	In MPU80 mode, $\overline{IOR}$ inputs the $\overline{IOR}$ or $\overline{RD}$ signal to enable the 80-series MPU to read data from the HD64951.
		R/$\overline{W}$	I	Read/Write	In MPU68 mode, the R/$\overline{W}$ input signal enables the 68-series MPU to read and write data from and to the HD64951. Set R/$\overline{W}$ high to read and low to write.
	46	$\overline{IOW}$	I	I/O Write	In MPU80 mode, $\overline{IOW}$ inputs the $\overline{IOW}$ or $\overline{WR}$ signal from the 80-series MPU to enable it to the write data to the HD64951.
		$\overline{LDS}$	I	Low Data Strobe	In MPU68 mode, the $\overline{LDS}$ signal is input from the 68-series MPU when the lower bytes of the data bus are valid during data transfer between the MPU and the HD64951.
	38	$\overline{BHE}$	I	Byte High Enable	In MPU80 mode, the $\overline{BHE}$ signal is input from the 80-series MPU when D8-D15 are valid.
		$\overline{UDS}$	I	Upper Data Strobe	In MPU68 mode, the $\overline{UDS}$ signal is input from the 68-series MPU when D8-D15 are valid.
	17	$\overline{IRQ}$	O	Interrupt Request	The interrupt request signal informs the MPU of a completed internal operation or an error. (See interrupt description.)
	53	$\overline{DREQ}$	O	DMA Request	$\overline{DREQ}$ outputs a low signal to the DMAC to request a DMA transfer. The data transfer will not begin until the HD64951 receives the acknowledge signal ($\overline{DACK}$) from the DMAC.
	52	$\overline{DACK}$	I	DMA Acknowledge	$\overline{DACK}$ inputs the acknowledge signal sent by the $\overline{DMAC}$ in response to the $\overline{DREQ}$ signal. $\overline{DACK}$ low enables data transfer to memory controlled by the DMAC or another peripheral.
	51	$\overline{WAIT}$	O	Wait	$\overline{WAIT}$ output low requests that the DMAC extend the read/write period.
	54	$\overline{DONE}$	I/O	Done	In DMA mode, $\overline{DONE}$ inputs a low level from the DMAC when the DMA transfer is complete. The $\overline{DONE}$ input is also low when a DMA transfer error occurs. At reset, the $\overline{DONE}$ input level determines whether the a 68-or 80-series MPU interface is used. $\overline{DONE}$ high selects an 80-series interface, $\overline{DONE}$ low selects a 68-series interface.

Table 1. Pin Function (Cont.)

Interface	Pin No.	Symbol	I/O	Name	Function
MPU/DMA (Cont.)	48	$\overline{DRD}$	I	DMA Read	In DMA80 mode, $\overline{DRD}$ inputs the $\overline{IORD}$ signal from the DMAC to enable it to read data from the HD64951.
		DR/$\overline{W}$	I	DMA Read/ Write	In the DMA68 mode, DR/$\overline{W}$ inputs the R/$\overline{W}$ signal from the DMAC. It is low for read and high for write.
	49	$\overline{DWR}$	I	DMA Write	In DMA80 mode, $\overline{DWR}$ inputs the $\overline{IOWR}$ signal from the DMAC to enable the DMAC to write data to the HD64951.
		$\overline{DS}$	I	Data Strobe	In DMA68 mode, the $\overline{DS}$ input timing signal enables the DMAC to read/write data from/to the HD64951.
	14	CLK	I	Clock	CLK inputs the clock to generate the internal operation timing signals (8 MHz max).
	15	$\overline{RESET}$	I	Reset	$\overline{RESET}$ input clears the HD64951's registers and halts operation for initialization.
	58	DV_{CC}	I	Driver power	DV_{CC} and DGND1-DGND4 are the power supply and ground for the output stage driver/receivers.
	9, 4 67, 62	DGND1-4	I	Driver Ground	
	18	V_{CC}	I	Power supply	V_{CC} and GND are the power supply and ground for the all circuits other than the output stage driver/receivers.
	50	GND	I	Ground	
	16	MPU READY	O	MPU Ready	In MPU80 mode, $\overline{MPU\ READY}$ requests that the MPU extend a data cycle when a high-speed MPU accesses an HD64951 internal register.
		$\overline{MPU}$ $\overline{DTACK}$	O	MPU Data Acknowledge	In MPU68 mode, MPU DTACK output active low informs the MPU of data access completion when a high-speed MPU accesses an HD64951 internal register.
	55 to 57	ID0 to ID2	I	Identification data 0-2	The ID0-ID2 outputs determine the device ID to be output on the SCSI bus during the arbitration phase.
	13	INC	I	Input clock	When the timer is driven, the value stored in the time out counter is decremented by the input clock.
SCSI					The SCSI interface (figure 2) includes 9 control signals and 9 data signals, including a parity line.
	12 to 10 8 to 5 3, 2	$\overline{SDB0}$ to $\overline{SDB2}$ $\overline{SDB3}$ to $\overline{SDB6}$ $\overline{SDB7}$ $\overline{SDBP}$	I/O	SCSI Data Bus	$\overline{SDB0}$-$\overline{SDB7}$ are the 8 data lines of the SCSI data bus; $\overline{SDBP}$ is the parity line. The SCSI bus has odd parity. Parity check is programmable. No parity check is performed during the arbitration phase.
	66	$\overline{ACK}$	I/O	Acknowledge	In initiator mode, the HD64951 outputs $\overline{ACK}$ in response to the $\overline{REQ}$ signal. In target mode, it inputs $\overline{ACK}$ from the initiator.
	60	$\overline{REQ}$	I/O	Request	In initiator mode, the HD64951 inputs $\overline{REQ}$ from the target. In target mode, it outputs $\overline{ACK}$ to the initiator.
	61	$\overline{C/D}$	I/O	Command/ DATA	In initiator mode, $\overline{C/D}$, $\overline{I/O}$ and $\overline{MSG}$ inputs detect the transfer phase and direction. In target mode, $\overline{C/D}$, $\overline{I/O}$ and $\overline{MSG}$ outputs determine transfer phase and direction. See table 2.
	59	$\overline{I/O}$	I/O	Input/Output	
	64	$\overline{MSG}$	I/O	Message	

Table 2 Transfer Phase and Direction

$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	Transfer phase	Transfer direction
Low	Low	Low	Message-in	Initiator ← Target
Low	Low	High	Message-out	Initiator → Target
High	Low	Low	Status	Initiator ← Target
High	Low	High	Command	Initiator → Target
High	High	Low	Data-in	Initiator ← Target
High	High	High	Data-out	Initiator → Target

Table 1. Pin Function (Cont.)

Interface	Pin No.	Symbol	I/O	Name	Function
MPU/DMA (Cont)	68	$\overline{BSY}$	I/O	Busy	The HD64951 sets $\overline{BSY}$ low to request to occupy the bus. $\overline{BSY}$ active low indicates that the bus is occupied.
	63	$\overline{SEL}$	I/O	Selection	In initiator mode, the HD64951 outputs $\overline{SEL}$ to the target to be selected at selection phase, or inputs $\overline{SEL}$ from the target in reselection phase. In target mode, it outputs $\overline{SEL}$ to the initiator to be selected at reselection phase, or inputs $\overline{SEL}$ from the initiator in selection phase.
	1	$\overline{ATN}$	I/O	Attention	In initiator mode, the HD64951 outputs $\overline{ATN}$ to the target, requesting the target to drive the message-out phase. In the target mode, it inputs $\overline{ATN}$ from the initiator.
	65	$\overline{RST}$	I/O	Reset	The HD64951 outputs the $\overline{RST}$ signal to reset the SCSI bus, or inputs it to detect the reset state.

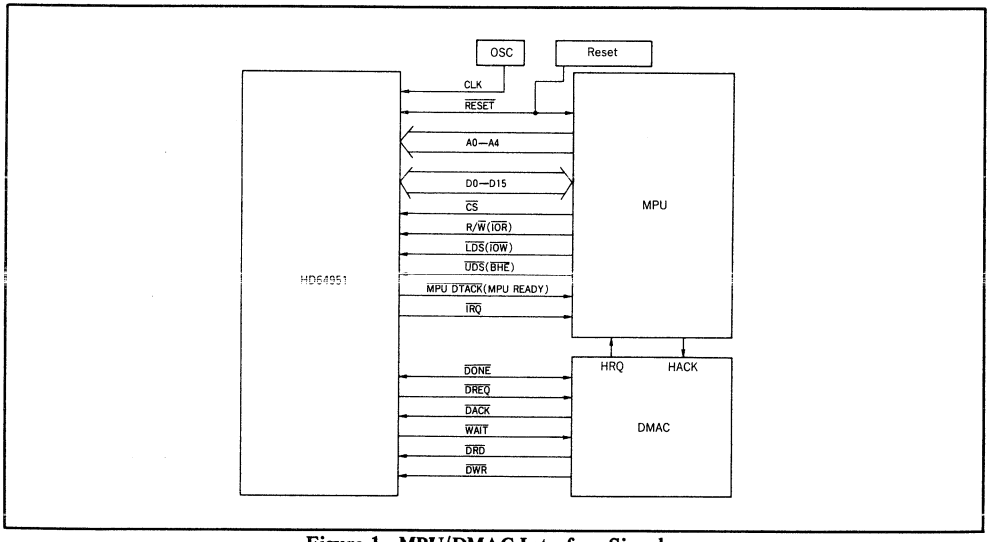


Figure 1. MPU/DMAC Interface Signals

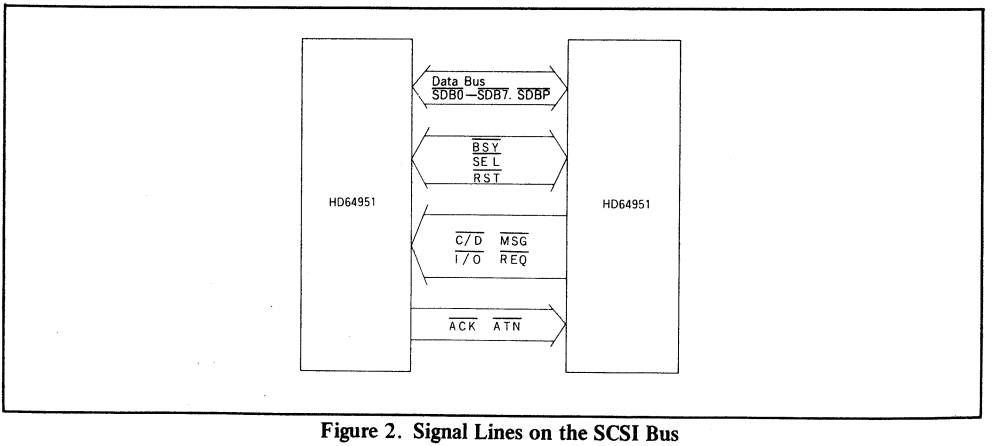


Figure 2. Signal Lines on the SCSI Bus

SCSI Bus Operation

SCSI bus operation is defined by eight bus phases as shown below. These bus phases are controlled by the bus control circuit and internal registers of the HD64951.

1. Bus free phase
2. Arbitration phase
3. Selection phase
4. Reselection phase
5. Command phase
6. Data phase
7. Status phase
8. Message phase

(5–8: Information transfer phases)

Phase 1 to 8 above are generally called bus phases. Phases 5 to 8 are called information transfer phases.

Bus Free Phase

In bus free phase the SCSI bus is not occupied by any bus devices connected to it. This phase is detected when the $\overline{BSY}$ and $\overline{SEL}$ are simultaneously held high for 400 ns or more. An operation sequence begins with this phase. Enter the bus free phase by setting the $\overline{BSY}$ and $\overline{SEL}$ simultaneously or by setting bit 3 (RST) of SCSI bus control register 2 to generate a reset condition as shown in figure 3 (see the internal register description).

The SCSI bus interface signals are all reset by a reset condition, resulting in all SCSI bus devices being disconnected from the bus as shown in figure 4.

During generating a reset condition, bit 3 of interrupt status register is set to "1" (See the internal register description).

An interrupt is issued when the bit 3 of interrupt enable register is "1" (See the internal register description).

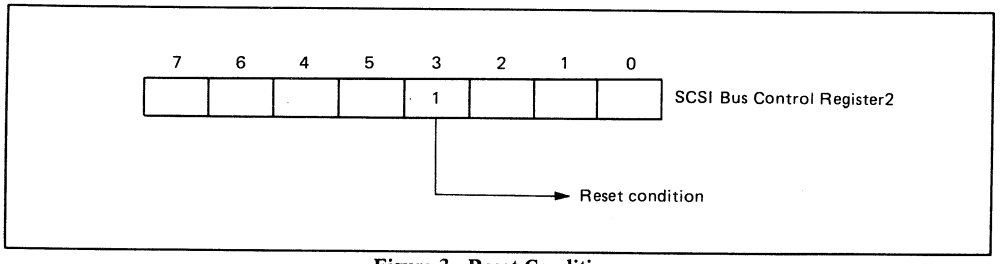


Figure 3. Reset Condition

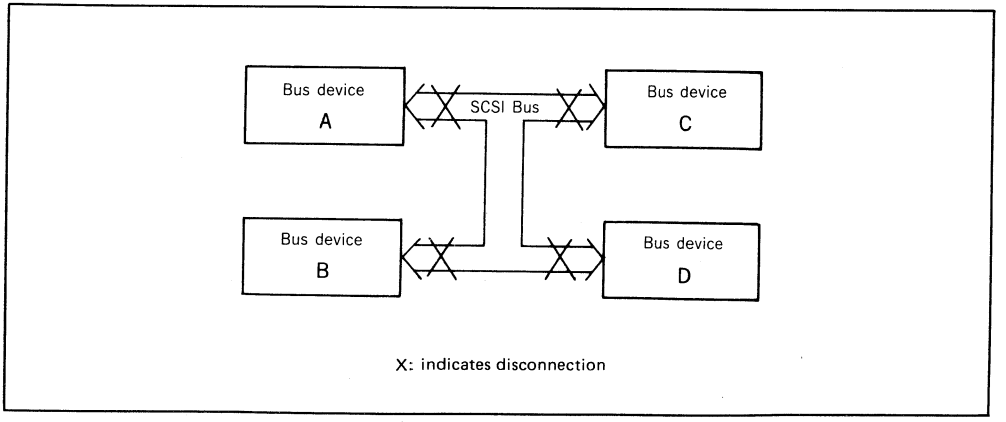


Figure 4. Bus Free Phase

Arbitration Phase

In arbitration phase, a SCSI device acquires the SCSI bus. Bus devices requiring SCSI bus acquisition set the $\overline{BSY}$ signal to low to enter the arbitration phase, and then output their own ID onto the SCSI data bus. The SCSI device with the highest number among the IDs output to the bus acquires the SCSI bus (figure 5).

Selection Phase

In selection phase, the initiator which acquired the bus in arbitration phase selects a target device to transmit/receive data to/from (figure 6). The ID of the target to be selected must be preset in the partner ID register before entering the selection phase. See register description for details.

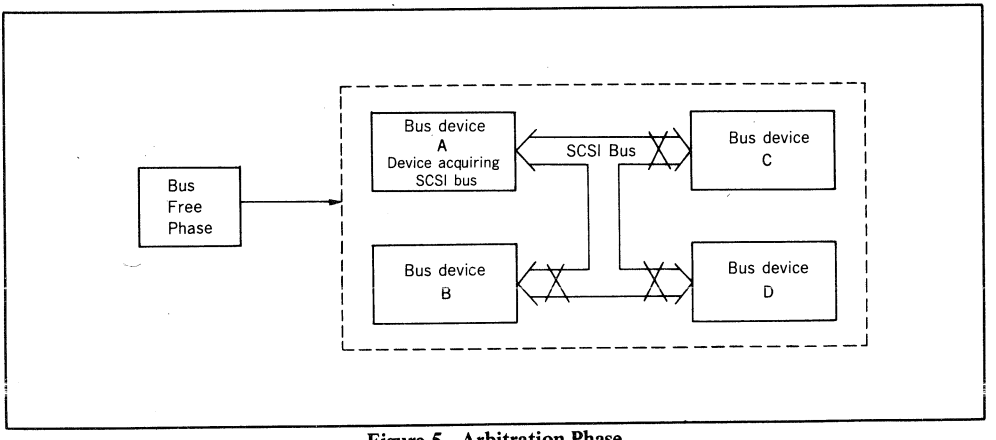


Figure 5. Arbitration Phase

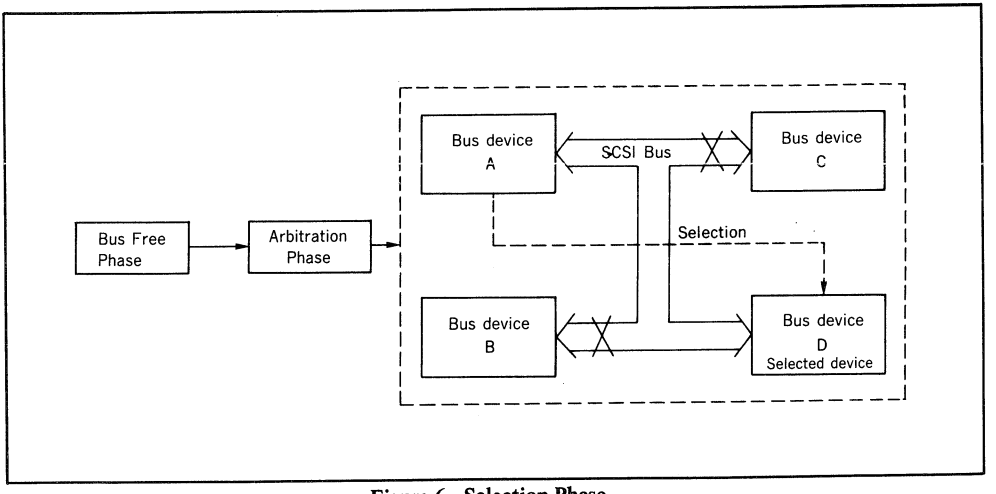


Figure 6. Selection Phase

Reselection Phase

During data transfer between the selected initiator and target, if the target has occupied the SCSI bus for a long period, it must sometimes vacate the bus. To resume the interrupted operation sequence, the target determined in the previous phase reacquires the SCSI bus and selects the previously selected initiator during the reselection phase (figure 7). This phase is performed by setting the ID of the initiator to be reselected in the target's partner ID register.

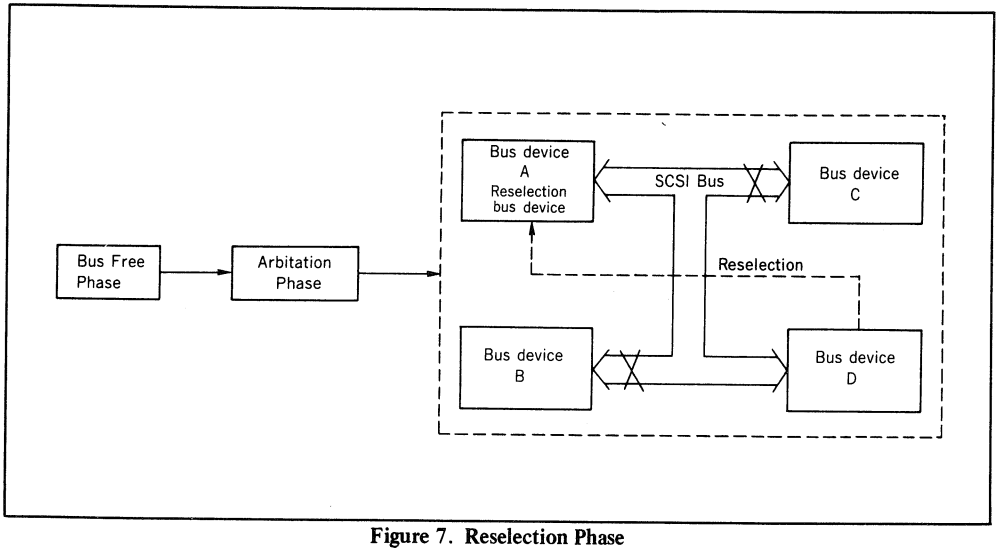


Figure 7. Reselection Phase

Information Transfer Phase

When selection or reselection phase is normally completed, the HD64951 enters the information transfer phase, the information transfer phase is catagorized into the following four phases:

Command Phase: In the command phase the initiator transfer commands to the target, which in turn determines the task to be performed with the command. The command phase can be performed by writing 0, 1, and 0 to bits 1, 2 and 3 of SCSI bus control register 1 respectively.

Data Phase: In the data phase, data is transferred between the initiator and target. Data phase has a data-in phase (transfer from the target to the initiator) and a data-out phase (transfer from the initiator to the target). Data input/output is defined with respect to the initiator; input to the initiator is the data-in phase, while output from the initiator is the data-out phase. Data-in phase is performed by writing 1, 0, and 0 to bits 1, 2, and 3 of SCSI bus control register 1, respectively. Data-out phase is performed by writing zero to all of these register bits.

Status Phase: In status phase, the target informs the initiator of status data. Status phase can be performed by writing 1, 1, and 0 to bit 1, 2, and 3 of SCSI bus control register 1, respectively.

Message Phase: In message phase, a message is transferred between the initiator and the target. Like the data phase, there are a message-in phase and a message-out phase. Message-in phase is performed by writing one to all of bits 1 to 3 of SCSI bus control register 1, while message-out phase is performed by writing 0, 1, and 1 to bits 1, 2 and 3. To realize message-out phase, an attention condition must be generated, as shown in figures 8 and 9.

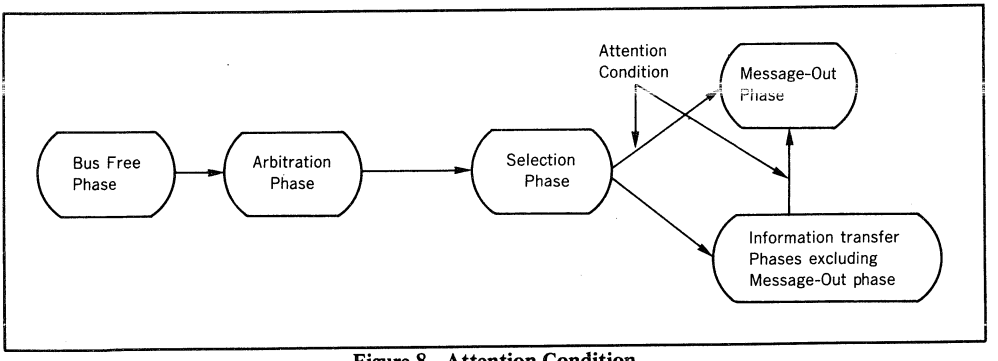


Figure 8. Attention Condition

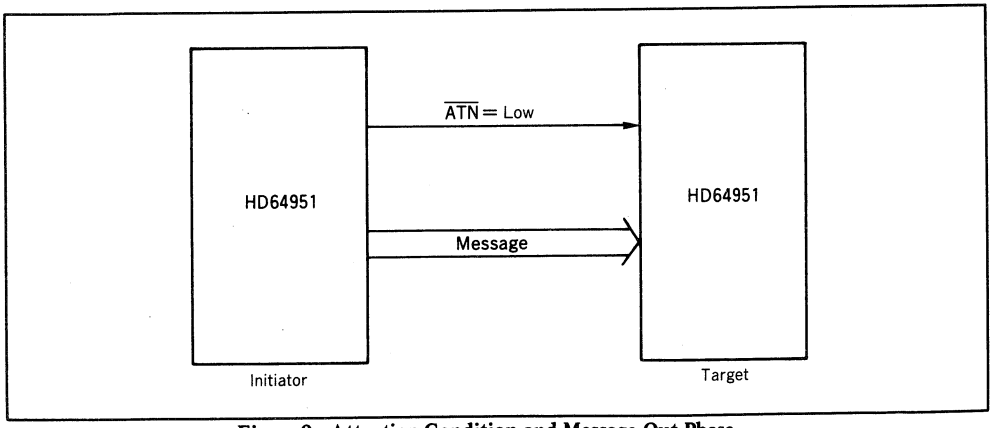


Figure 9. Attention Condition and Message-Out Phase

Internal Registers

The HD64951 contains 23 externally accessible internal registers. These registers control HD64951 internal operation and contain operation status and results.

Internal Register Selection

Internal registers include even-address and odd-address registers. The 8/16-bit MPU select these registers with the $\overline{CS}$, $\overline{UDS}$ ($\overline{BHE}$), $\overline{LDS}$, and A0 inputs (table 3).

Table 3. Register Selection, 80 Mode

$\overline{CS}$	$\overline{BHE}$	A0	D15–D8	D7 to D0
H	–	–	High impedance	High impedance
L	L	L	Inhibited	Inhibited
L	L	H	Odd-address register	High impedance
L	H	L	High impedance	Even-address register
L	H	H	High impedance	Odd-address register

Note: When an 8-bit bus is used, the $\overline{BHE}$ pin must be fixed high.

Table 4. Register Selection, 68 Mode

$\overline{CS}$	$\overline{UDS}$	$\overline{LDS}$	A0	D15–D8	D7 to D0
H	–	–	–	High impedance	High impedance
L	L	L	H	Inhibited	Inhibited
L	L	H	H	Even-address register	High impedance
L	H	L	L	High impedance	Even-address register
L	H	L	H	High impedance	Odd-address register
L	H	H	–	High impedance	High impedance

Note: When a 16-bit bus is used, the A0 pin must be fixed high.
When an 8-bit bus is used, the $\overline{UDS}$ pin must be fixed high.

Internal Register Address Allocation

Specific addresses are allocated to each of the internal registers. They are selected by five address bits A0 to A4, as shown in table 5.

Internal Register Bit Allocation

The allocation of internal register bits is shown in table 6. Bits indicated by "–" can be written as 1 or 0 although they are not defined while reading. Addresses $11 to $1F cannot be used.

Table 5. Internal Register Allocation

Address	A4	A3	A2	A1	A0	OP	Register Name	Initialized Value After Reset
$00	0	0	0	0	0	R	Input Data Register	$00
						W	Output Data Register	$00
$01	0	0	0	0	1	R	Input Data Register	$00
						W	Output Data Register	$00
$02	0	0	0	1	0	R	SCSI Bus Status Register 1	$E0
						W	SCSI Bus Control Register 1	$E0
$03	0	0	0	1	1	R	SCSI Bus Status Register 2	$E0
						W	SCSI Bus Control Register 2	$E0
$04	0	0	1	0	0	R/W	Mode Register	Note 1
$05	0	0	1	0	1	R/W	Interrupt Enable Register	$00
$06	0	0	1	1	0	R/W	Own ID Register	ID input decoded values
$07	0	0	1	1	1	R/W	Partner ID Register	$00
$08	0	1	0	0	0	R/W	Bus Settle/Bus Free Delay Register	$FF
$09	0	1	0	0	1	R/W	Arbitration/Selection Register	$FF
$0A	0	1	0	1	0	R/W	Time Out Register	$FF
$0B	0	1	0	1	1	R	Time Out Counter	$FF
						W	Time Out Control Register	$FC
$0C	0	1	1	0	0	R/W	Arbitration Command Register	$F8
$0D	0	1	1	0	1	R/W	DMA Command Register	$7C
$0E	0	1	1	1	0	R/W	Interrupt Status Register	$00 (Note 2)
$0F	0	1	1	1	1	R/W	Arbitration Status Register	$F0
$10	1	0	0	0	0	R	In-Data Status	$00
						W	Hard Reset	$00

Note: 1. Initialized value for the Mode Register is different in 68 and 80 series.

OP	68 Series	80 Series
R	$88	$08
W	$08	$08

2. Set to $20 if the bus free phase is detected after reset.

Table 6. Internal Register Bit Allocation

Address	Register Name	R/W	Register Bit 7	6	5	4	3	2	1	0
$00	Input/Output Data Register	R	SDB7	SDB6	SDB5	SDB4	SDB3	SDB2	SDB1	SDB0
		W								
$01		R	SDB7	SDB6	SDB5	SDB4	SDB3	SDB2	SDB1	SDB0
		W								
$02	SCSI Bus Status 1	R	—		WRDY	RRDY	MSG	C/D	I/O	REQ
	SCSI Bus Control 1	W	—							
$03	SCSI Bus Status 2	R	—			ATN	RST	SEL	BSY	ACK
	SCSI Bus Control 2	W	—							
$04	Mode Register	R	M68/$\overline{80}$	D68/$\overline{80}$	0	NS/$\overline{S}$	AB/$\overline{NAB}$	IDCE	PE	I/$\overline{T}$
		W	—							
$05	Interrupt Enable Register	R	END	IPC	BUFF	ATN	RST	TMO	IDE	PRTY
		W								
$06	Own ID Register	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		W								
$07	Partner ID Register	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		W								
$08	Bus Free/Bus Settle Delay Register	R	Bus Free Delay				Bus Settle Delay			
		W								
$09	Arbitration/Selection Delay Register	R	Selection Delay				Arbitration Delay			
		W								
$0A	Time Out Register	R	b7	b6	b5	b4	b3	b2	b1	b0
		W								
$0B	Time Out Counter	R	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
	Time Out Control	W	—						TCDEC	TCE
$0C	Arbitration Command Register	R	—					ATN/ NON	Resel/ Sel	CMS/ STOP
		W	—							
$0D	DMA Command Register	R	E/L	—					AUTO/ MANU	DMA/ MPU
		W		—						
$0E	Interrupt Status Register	R	END	IPC	BUFF	ATN	RST	TMO	IDE	PRTY
		W	Interrupt Test							
$0F	Arbitration Status Register	R	—				ArbNOT	S/REND	Reseld	Seld
		W	Arbitration Test							
$10	Input-Data Status	R	SDB7	SDB6	SDB5	SDB4	SDB3	SDB2	SDB1	SDB0
	Hard Reset	W	—							HRST

Operation Modes

$\overline{\text{DONE}}$ Pin Setting

There are two main HD64951 operation modes. MPU68 mode and MPU80 mode. Switching between the two modes is performed by the $\overline{\text{DONE}}$ pin input at reset; low level $\overline{\text{DONE}}$ signal selects MPU68 mode while high level $\overline{\text{DONE}}$ selects MPU80 mode.

Mode register Setting

In addition to MPU68 mode and MPU80 modes, various HD64951 operation modes include initiator mode and target mode. These operation modes can be specified by the mode register (figure 10).

- Bit 0: When the HD64951 is used as an initiator device, this bit must be set to 1 (initiator mode), and when it is used as a target, this bit must be cleared (target mode).
- Bit 1: Determined whether or not the parity bit of data on the SCSI data bus is checked.
- Bit 2: Determines whether or not an ID check is performed.
- Bit 3: Specifies arbitration mode if arbitration phase is used, and non-arbitration mode otherwise.
- Bit 4: Specifies a single initiator or non-single initiators when non-arbitration mode is specified by bit 3.
- Bit 5: Set to 0
- Bit 6: Specifies 68-series or 80-series DMA connection.
- Bit 7: Writing to this bit is inhibited. MPU68 mode or MPU80 mode status can only be read.

Each mode setting is summarized in table 7. Examples of data bus and pin connections in each mode are illustrated in figure 11 and 12.

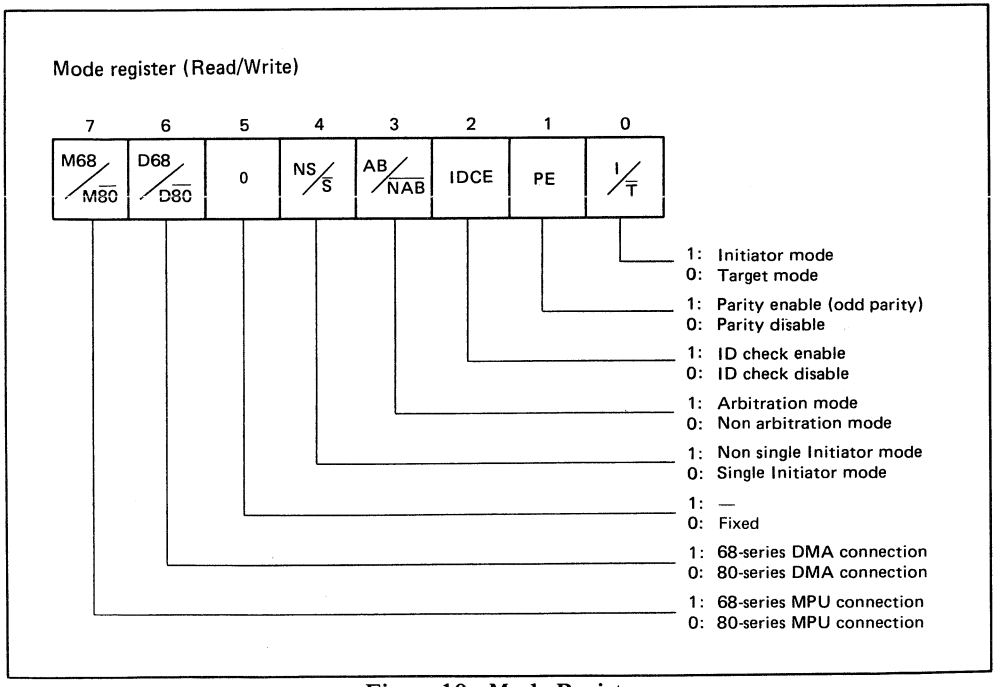


Figure 10. Mode Register

Table 7. Mode Setting

Mode	MPU/DMA 68/80 Mode Setting	Data Bus 8-or 16-Bit Mode Setting
MPU68 mode 8-bit data bus mode	Input low to $\overline{\text{DONE}}$ pin at reset	$\overline{\text{UDS}}$ = High
MPU68 mode 16-bit data bus mode		A0 = High
DMA68 mode Byte transfer mode	Write 1 to bit 6 of the mode register	Write 0 to bit 5 of the mode register
MPU80 mode 8-bit data bus mode	Input high to $\overline{\text{DONE}}$ pin at reset	$\overline{\text{BHE}}$ = High
MPU80 mode 16-bit data bus mode		No settings required (Note 1)
DMA80 mode Byte transfer mode	Write 0 to bit 6 of the mode register	Write 0 to bit 5 of the mode register
DMA80 mode Word transfer mode		Write 1 to bit 5 of the mode register

Notes: 1. See (1) 80 mode of Internal register selection, P. 9
2. MPU mode, DMA mode, and the bus width can be separately specified.

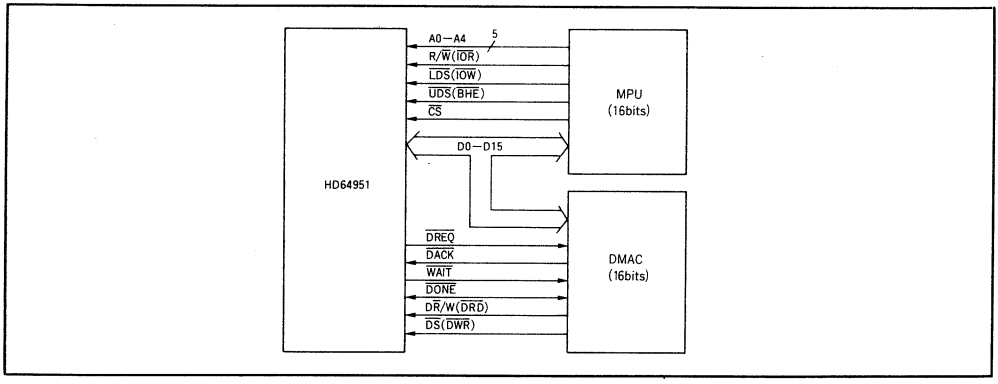


Figure 11. MPU 16-Bit Mode and DMA Byte Transfer Mode

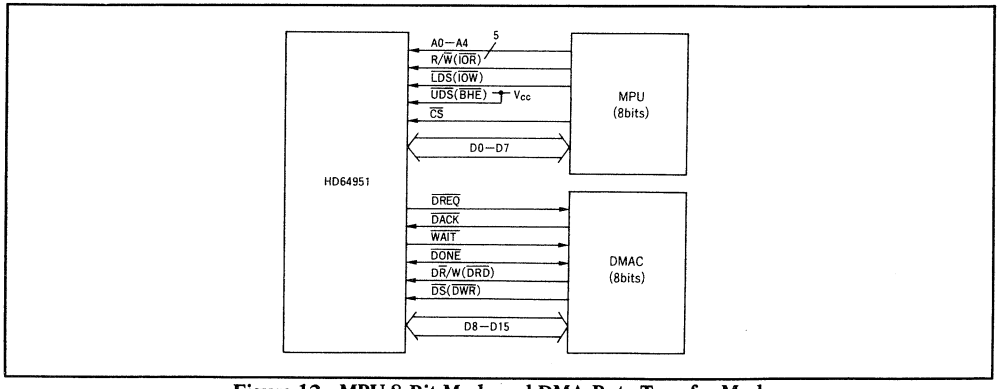


Figure 12. MPU 8-Bit Mode and DMA Byte Transfer Mode

Operational Description

The main components of the HD64951 are the SCSI bus control/status registers, the input/output data registers, own-ID/partner-ID register, the arbitration command/DMA command registers, the bus settle/bus free, delay register, arbitration/selection delay register, arbitration status register, interrupt enable/status registers, timer, and MPU interface. Functional descriptions for these registers are given below.

SCSI Bus Control/Status Registers

SCSI bus control/status registers consist of the following four 8-bit registers:

- SCSI Bus Control Register 1
- SCSI Bus Status Register 1
- SCSI Bus Control Register 2
- SCSI Bus Status Register 2

These registers can specify the SCSI bus control signals. The bus condition can be verified by reading SCSI bus status registers 1 and 2.

SCSI Bus Control Register 1: Bits 3 to 0 of SCSI bus control register 1 (figure 13) control the four SCSI bus control signals $\overline{MSG}$, $\overline{C/D}$, I/O, and $\overline{REQ}$. Bit 4 (RRDY) and bit 5 (WRDY) initialize the counters in the input/output data registers which transfer data to/from the SCSI data bus.

- Target mode: The contents of bits 0 to 3 of this register are output as SCSI bus control signals. The type of transfer phase and transfer direction are determined by the combinations of bits 1 to 3 shown in table 8.
- Initiator mode: The contents of bits 3 (MSG), 2 (C/D), and 1 (I/O) are compared with those of the corresponding target. If these signals agree with each other, a information transfer phase is performed; if not, a phase change interruput is generated, and the initiator and target respecify these three signals to perform an information transfer phase (figure 14).

Table 8. Transfer Direction and Phase

Bit 3 MSG	Bit 2 C/D	Bit 1 I/O	Transfer Phase	Transfer Direction
1	1	1	Message-in	Initiator ← Target
1	1	0	Message-out	Initiator → Target
0	1	1	Status	Initiator ← Target
0	1	0	Command	Initiator → Target
0	0	1	Data-in	Initiator ← Target
0	0	0	Data-out	Initiator → Target

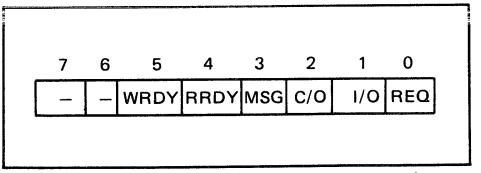


Figure 13. SCSI Bus Control Register 1

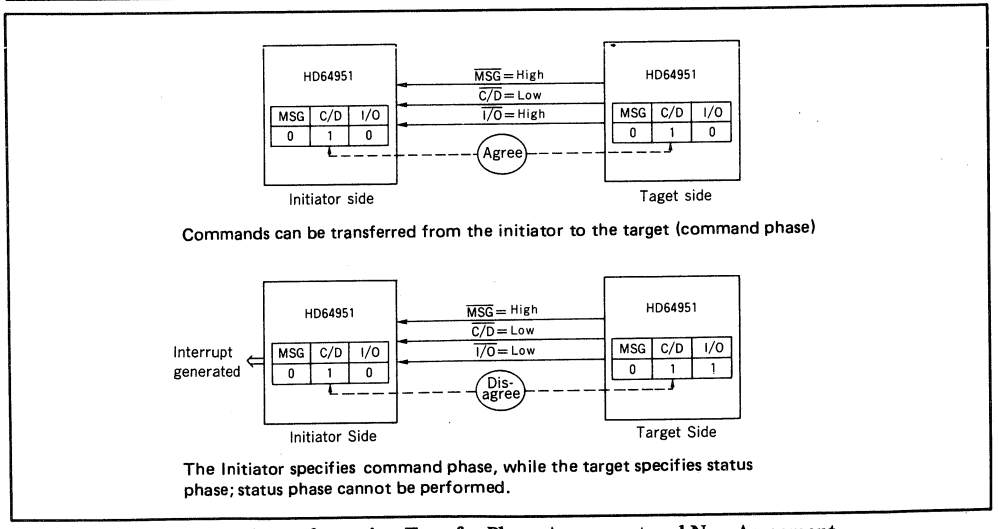


Figure 14. Information Transfer Phase Agreement and Non-Agreement

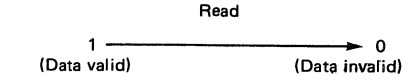
As shown in figure 14, if the initiator and target specify the same information transfer phase, the phase can be performed. However, if the specify different phases, no phase is performed and a phase change interrupt is issued.

Note: The C/D, I/O, and MSG bits stored in the target are output to the initiator via the SCSI bus. The C/D, I/O, and MSG set by the initiator are not output to the SCSI bus, but rather are written to the SCSI bus control register.

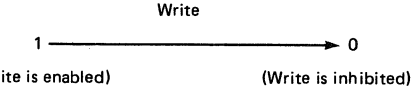
Bit 4 (RRDY) and bit 5 (WRDY) settings and the corresponding input/output data register status are shown in table 9 RRDY and WRDY can be specified independent of target/initiator mode.

The counter for counting the number of bytes in the input/output data register can be initialized as shown in table 9. The counter should be initialized in cases such as when DMA transfer is abnormally performed.

SCSI Bus Status Register 1 (Read): The same address ($02) is allocated to SCSI bus status register 1. The bit allocation of this register is also the same as SCSI bus control register 1. Bits 0 to 3 of this register show the SCSI bus status. Bit 4 (RRDY) and bit 5 (WRDY) are flags indicating the input/output data register status in both initiator and target modes, as shown in table 10.



The RRDY flag is cleared by reading the input data register.



The WRDY flag is cleared by writing to the output data register. In DMA mode or string transfer mode, additional writing is inhibited by hardware. In all other modes, writing is not inhibited by hardware, and thus the software must not allow any more writing to be done.

Table 9. Input/Output Register Condition

Bit	Setting	Description
RRDY	1	–
	0	Initializes the counter of input data register
WRDY	1	Initializes the counter of output data register
	0	–

Table 10. Status of Input/Output Data Register

Bit	Setting	Description
RRDY	1	Data has been set in the input data register
	0	Data has not been set in the input data register
WRDY	1	Data can be written to the output data register
	0	Data cannot be written to the output data register

SCSI Bus Control Register 2 (Write): The SCSI bus control register 2 (figure 15) outputs SCSI bus control signals in initiator or target mode. The BSY, SEL, and RST signals can be output in either mode, but the ACK and ATN signals can't output in target mode.

SCSI Bus Status Register 2 (Read): The same address ($03) is allocated to SCSI bus status register 2 and the same bit allocation is employed as for SCSI bus control register 2. The signals on the SCSI bus corresponding to this register can be read.

Transfer Mode

Data transfer via the SCSI bus is performed by handshaking of the $\overline{REQ}/\overline{ACK}$ signals from the target to the initiator and vice versa. $\overline{REQ}/\overline{ACK}$ signal transfer is shown in figure 16 and 18, and its timing is shown in figure 17 and 19.

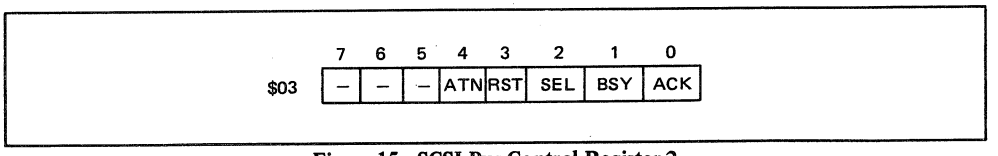
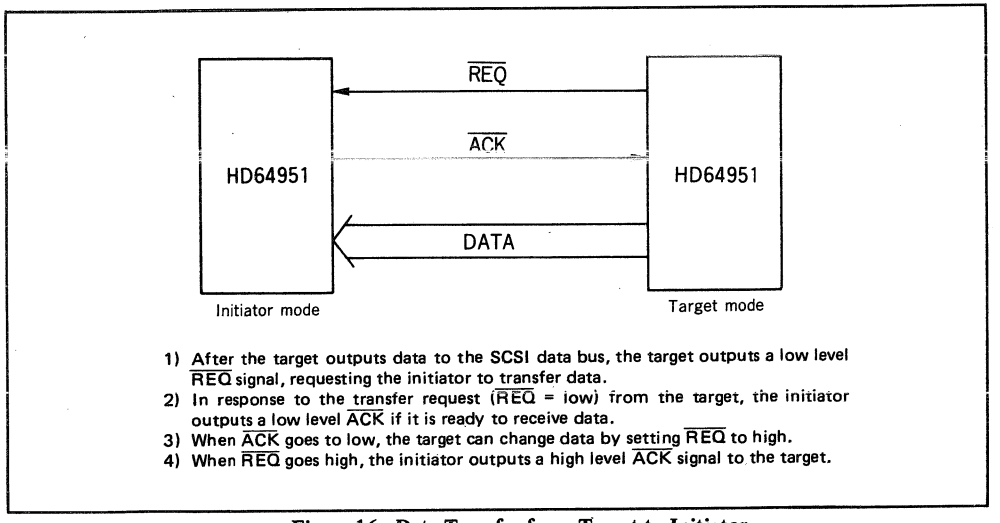


Figure 15. SCSI Bus Control Register 2



1) After the target outputs data to the SCSI data bus, the target outputs a low level $\overline{REQ}$ signal, requesting the initiator to transfer data.
2) In response to the transfer request ($\overline{REQ}$ = low) from the target, the initiator outputs a low level $\overline{ACK}$ if it is ready to receive data.
3) When $\overline{ACK}$ goes to low, the target can change data by setting $\overline{REQ}$ to high.
4) When $\overline{REQ}$ goes high, the initiator outputs a high level $\overline{ACK}$ signal to the target.

Figure 16. Data Transfer from Target to Initiator

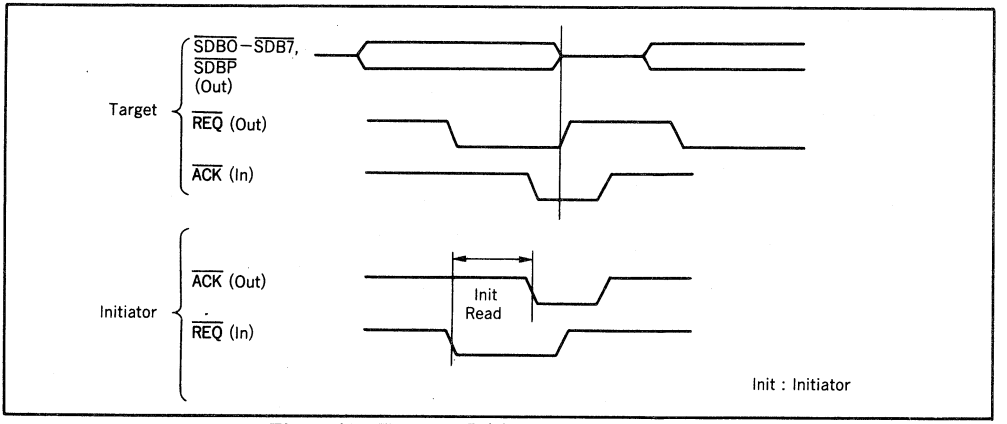
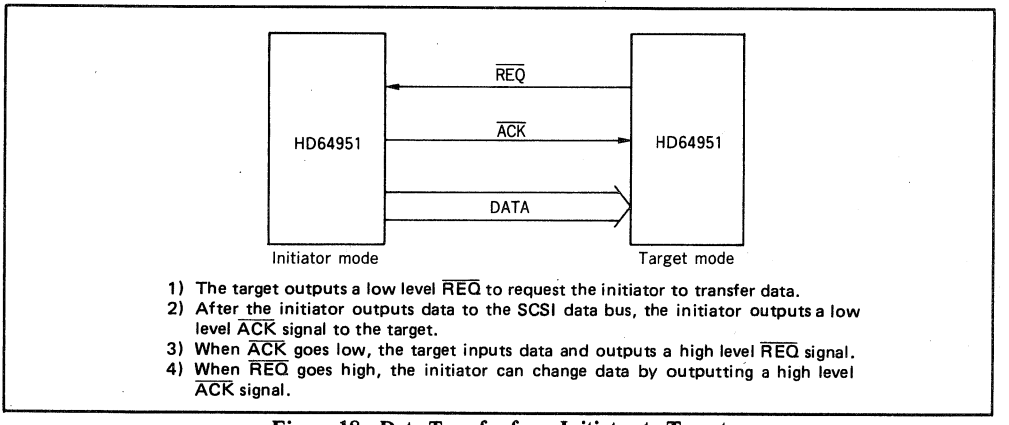


Figure 17. Target to Initiator Data Transfer Timing



1) The target outputs a low level REQ to request the initiator to transfer data.
2) After the initiator outputs data to the SCSI data bus, the initiator outputs a low level ACK signal to the target.
3) When ACK goes low, the target inputs data and outputs a high level REQ signal.
4) When REQ goes high, the initiator can change data by outputting a high level ACK signal.

Figure 18. Data Transfer from Initiator to Target

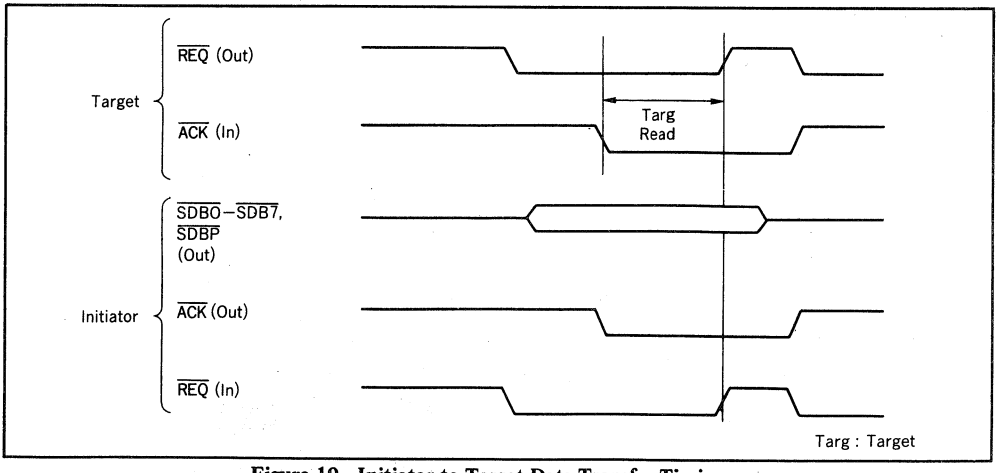


Figure 19. Initiator to Target Data Transfer Timing

Input/Output Data Registers

The two input/output data registers have a 8 bit length and are allocated to the same address:

- Input data register
- Output data register

Data transfer to/from the SCSI bus is performed through the input/output data registers.

Output data register (Write): The MPU or DMAC output data to the SCSI bus through the output data register (figure 20).

1. When an 8-bit MPU/DMAC is used: When 8-bit data is output to the SCSI bus, output data register at $00 is used for the system bus (D0–D7), and output data register at $01 is used for the DMA transfer data bus (D8–D15).
2. When a 16-bit MPU/DMAC is used: In MPU and DMA mode, 16-bit data is output to the SCSI bus using addresses $00 and $01; the data at $00 is first output to the SCSI bus and than that at $01 is output. (The first data input to this register is written to $00 and the following is written to $01).

Note: When a 16-bit MPU/DMAC is used, data written to this register at $00 is first output to the SCSI bus after a delay of about two of the chip's operation clocks (CLK).

Input Data Register (Read):

1. When an 8-bit MPU/DMAC is used: In MPU mode, 8-bit data is input from the SCSI bus using address $00 of register. In DMA mode, 8-bit data is input using $01.
2. When a 16-bit MPU/DMAC is used: In MPU mode, when 16-bit data is input from the SCSI bus using $00 and $01 of this register, the first data input is stored at $00 and the following data is stored at $01.

As shown in figures 17 and 19, the input data register inputs data which has been latched by $\overline{\text{REQ}}/\overline{\text{ACK}}$ signal handshaking.

Input Data Status Register (Read): The input data status register (figure 22) holds the status of SCSI data bus. It can input data on the SCSI bus without latching. In this case, although only 8-bit-by-8-bit input is permittsd, there is no need to access the $\overline{\text{REQ}}/\overline{\text{ACK}}$ signals, thereby facilitating reading data on SCSI data bus to obtain the status.

Own ID/Partner ID Registers

Up to eight initiators and targets in total can be connected to the SCSI bus for data transfer via the SCSI bus. However only two devices among them are permitted to transfer data via the SCSI bus at any one time. Other initiators and targets are logically separated from the bus at this time. The initiator and target which transfer data via the SCSI bus are specified by the read/write own ID/partner ID registers.

Own Register: The own ID register (figure 23) stores the ID of this particular device. This is accomplished by decoding the ID signals input to pins ID0 to ID2 of the device at reset; the decoded bit is set to 1 and all others to 0 (table 11).

Note: The ID bits specified during reset can be changed by subsequent writing to the own ID Register.

Partner ID Register: The partner ID register specifies the ID bit of a device's partner for the selection/reselection phase. The ID determined for selection or reselection can be read in the selection/reselection phase.

Bus Settle/Bus Free Register and Arbitration/Selection Delay Register

These two registers determine the following delay times (figure 25):

1. Delay time taken to detect bus free phase (bus settle delay)
2. Delay time from bus free phase detection to the start of arbitration phase (bus free delay)
3. Delay time from $\overline{\text{BSY}}$ signal assertion to $\overline{\text{SEL}}$ signal assertion (arbitration delay)
4. Delay time from $\overline{\text{SEL}}$ signal assertion to the start of selection phase (selection delay)

Delay times 1 and 2 above are determined by the bus settle/bus free delay register, and delay times 3 and 4 are determined by the arbitration/selection delay register.

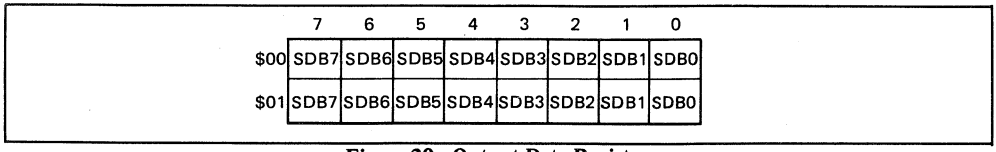


Figure 20. Output Data Register

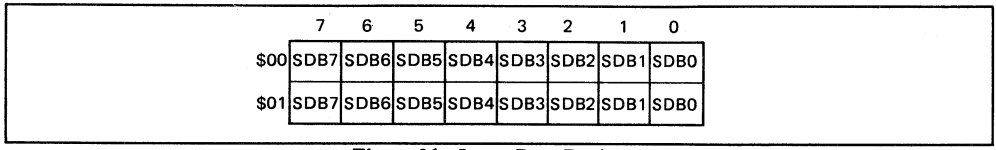


Figure 21. Input Data Register

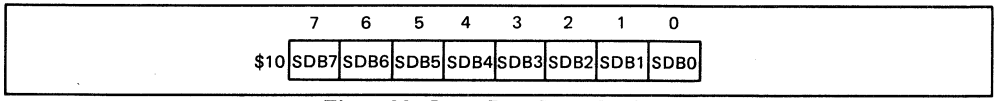


Figure 22. Input Data Status Register

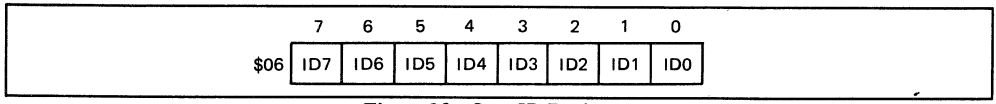


Figure 23. Own ID Register

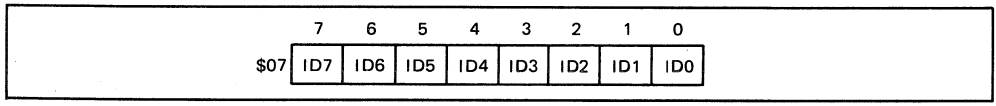


Figure 24. Partner ID Register

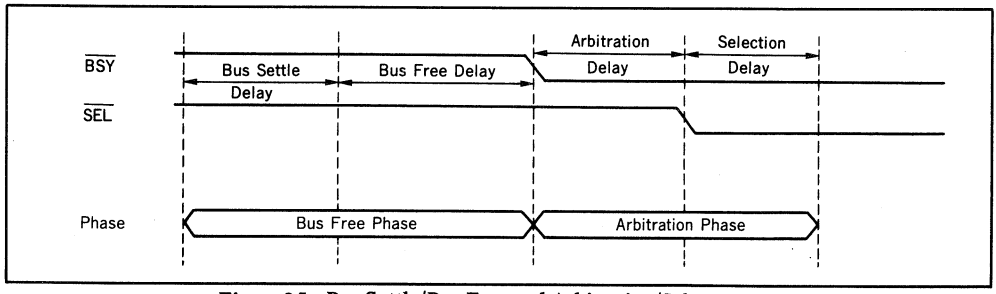


Figure 25. Bus Settle/Bus Free and Arbitration/Selection Delay

Table 11. ID0 to ID2 Decoding Table

Input Pins			Decoded Result (Bit Set to 1)	
ID0	ID1	ID2		
0	0	0	ID0	Low prioring
0	0	1	ID1	
0	1	0	ID2	
0	1	1	ID3	
1	0	0	ID4	
1	0	1	ID5	
1	1	0	ID6	
1	1	1	ID7	High prioring

Bus Settle/Bus Free Delay Register: Bits 0 to 3 of the read/write bus settle/bus free delay register determine bus settle delay and bits 4 to 7 specify bus free delay. For detailed settings, see table 12.

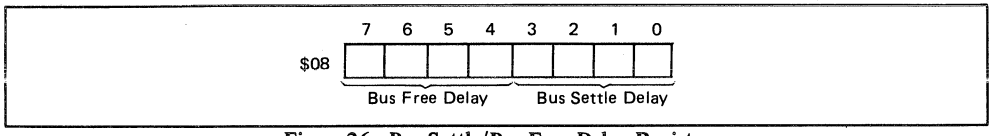


Figure 26. Bus Settle/Bus Free Delay Register

Table 12. Bus Settle/Bus Free Delay Settings

b7	b6	b5	b4	Bus Free Delay	b3	b2	b1	b0	Bus Settle Delay
0	0	0	0	Inhibited	0	0	0	0	Inhibited
0	0	0	1	2 Clock cycles	0	0	0	1	2 Clock cycles
0	0	1	0	3 Clock cycles	0	0	1	0	3 Clock cycles
0	0	1	1	4 Clock cycles	0	0	1	1	4 Clock cycles
0	1	0	0	5 Clock cycles	0	1	0	0	5 Clock cycles
0	1	0	1	6 Clock cycles	0	1	0	1	6 Clock cycles
0	1	1	0	7 Clock cycles	0	1	1	0	7 Clock cycles
0	1	1	1	8 Clock cycles	0	1	1	1	8 Clock cycles
1	0	0	0	9 Clock cycles	1	0	0	0	9 Clock cycles
1	0	0	1	10 Clock cycles	1	0	0	1	10 Clock cycles
1	0	1	0	11 Clock cycles	1	0	1	0	11 Clock cycles
1	0	1	1	12 Clock cycles	1	0	1	1	12 Clock cycles
1	1	0	0	13 Clock cycles	1	1	0	0	13 Clock cycles
1	1	0	1	14 Clock cycles	1	1	0	1	14 Clock cycles
1	1	1	0	15 Clock cycles	1	1	1	0	15 Clock cycles
1	1	1	1	16 Clock cycles	1	1	1	1	16 Clock cycles

Note: 1. Clock cycle = Input Clock Cycle Time (tcyc)

Arbitration/Selection Delay Register: Bits 0 to 3 of the read/write arbitration/selection delay register determine arbitration delay and bits 4 to 7 determine selection delay. For delay settings, see table 13.

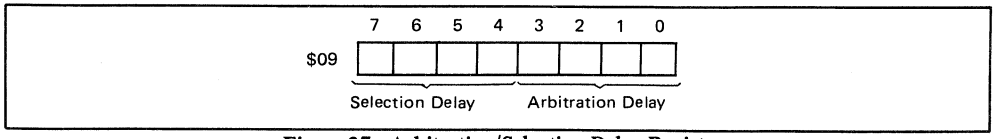


Figure 27. Arbitration/Selection Delay Register

Table 13. Arbitration/Selection Delay/Setting

b7	b6	b5	b4	Selection Delay	b3	b2	b1	b0	Arbitration Delay
0	0	0	0	Inhibited	0	0	0	0	Inhibited
0	0	0	1	4 Clock cycles	0	0	0	1	4 Clock cycles
0	0	1	0	6 Clock cycles	0	0	1	0	6 Clock cycles
0	0	1	1	8 Clock cycles	0	0	1	1	8 Clock cycles
0	1	0	0	10 Clock cycles	0	1	0	0	10 Clock cycles
0	1	0	1	12 Clock cycles	0	1	0	1	12 Clock cycles
0	1	1	0	14 Clock cycles	0	1	1	0	14 Clock cycles
0	1	1	1	16 Clock cycles	0	1	1	1	16 Clock cycles
1	0	0	0	18 Clock cycles	1	0	0	0	18 Clock cycles
1	0	0	1	20 Clock cycles	1	0	0	1	20 Clock cycles
1	0	1	0	22 Clock cycles	1	0	1	0	22 Clock cycles
1	0	1	1	24 Clock cycles	1	0	1	1	24 Clock cycles
1	1	0	0	26 Clock cycles	1	1	0	0	26 Clock cycles
1	1	0	1	28 Clock cycles	1	1	0	1	28 Clock cycles
1	1	1	0	30 Clock cycles	1	1	1	0	30 Clock cycles
1	1	1	1	32 Clock cycles	1	1	1	1	32 Clock cycles

Note: 1. Clock cycle = Input Clock Cycle Time (tcyc)

Arbitration Command/DMA Command Register
The arbitration command and DMA command registers specify selection/reselection phase and transfer-mode-related operations.

Arbitration Command Register: The read/write arbitration command register (figure 28) specifies the selection or reselection phase. When bit 0 is set and bus free is detected, arbitration, selection or reselection is automatically performed.

- Bit 0: Specifies start of command (to perform arbitration phase) transfer
- Bit 1: In arbitration phase, the initiator or target acquires the SCSI bus: The initiator acquires it by specifying selection phase (bit 1 = 0) while the target does so by specifying reselection phase (bit 1 = 1) (figure 29).

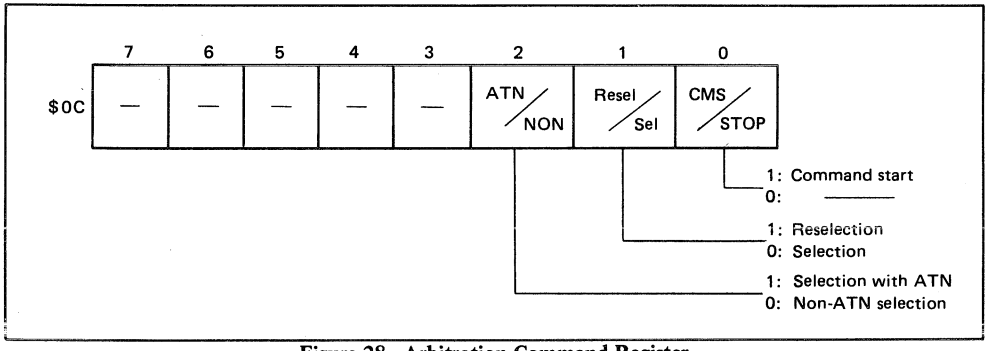


Figure 28. Arbitration Command Register

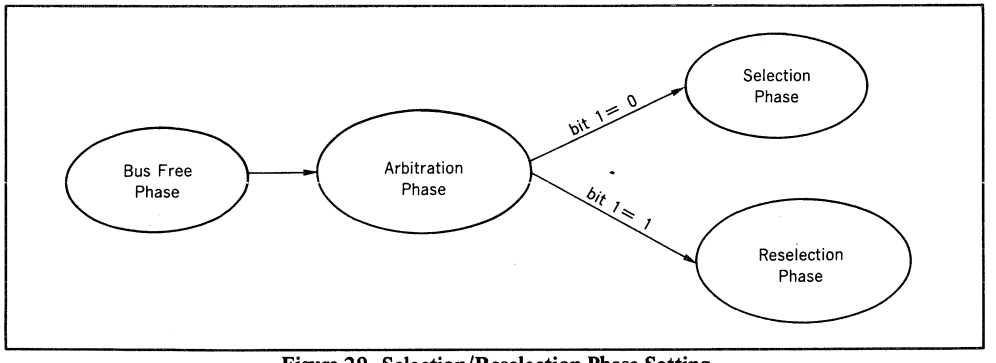


Figure 29. Selection/Reselection Phase Setting

- Bit 2: Specified ATN or non-ATN selection. This bit setting is required only when selection phase is specified by bit 1. When selection with ATN is specified, the initiator issues an attention condition to the target during the selection phase. Message-out phase is then entered automatically after the selection phase has been completed. When non-ATN selection is specified, the attention condition is not generated after the selection phase. In this case, an information transfer phase must be specified after completion of the selection phase. Bits 0 to 2 are cleared on completion of command processing.

DMA Command Register: The read/write DMA command register (figure 30) specifies the start or stop of DMA transfer and MPU string transfer, and also specifies the type of connected DMAC based on $\overline{DRD}$ and $\overline{DONE}$ signal timing.

- Bit 0: Specifies DMA transfer start or stop.
- Bit 1: Specifies MPU string transfer start or stop.
- Bit 7: Must be set to 1 if the period from $\overline{DRD}$ signal assertion to $\overline{DONE}$ signal assertion exceeds 200 ns during an external DMAC read. Must be cleared if the above period does not exceed 200 ns. See figure 31.

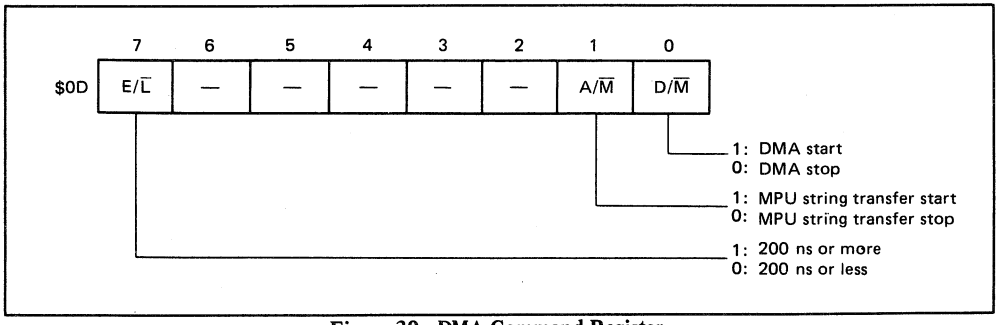


Figure 30. DMA Command Register

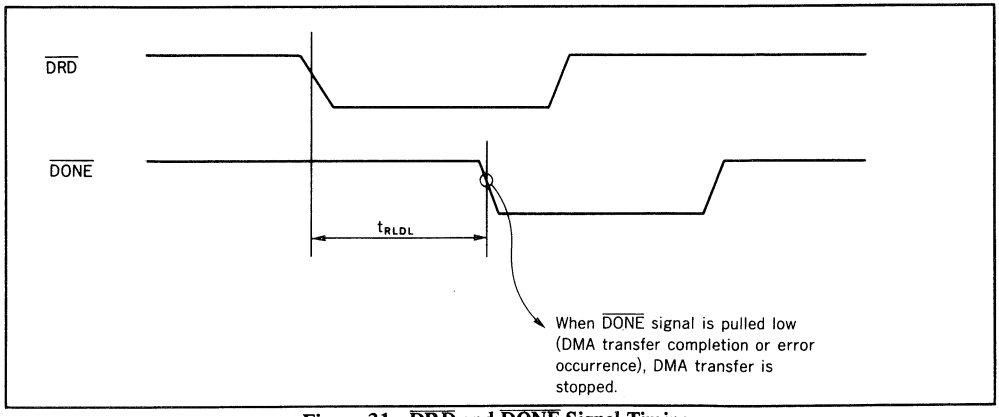
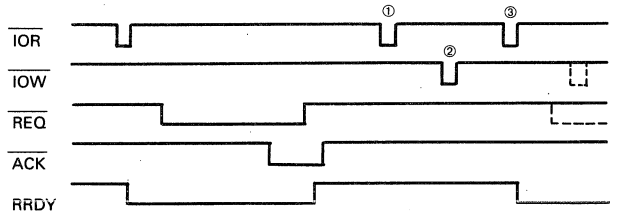


Figure 31. $\overline{DRD}$ and $\overline{DONE}$ Signal Timing

An MPU with $\overline{DTACK}$ (READY) input pin can perform automatic handshaking string transfer without access to the SCSI control/status registers of this chip by setting DMA command register bit 1 with the HD64951 $\overline{MPU}$ $\overline{DTACK}$ (MPU READY) connected to the MDU's $\overline{DTACK}$ (READY)

Note 1. When the $\overline{DONE}$ pin is active, bits 0 and 1 are automatically cleared.
2. Follow the procedure shown in Figures 32 and 33 to stop MPU string transmission.

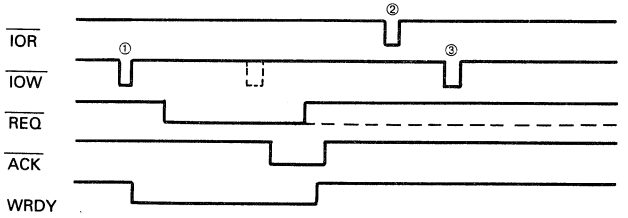
① Wait until RRDY (bit 4) of SCSI Bus Control Register 1 becomes "1".
② Write #00 into the DMA Command Register.
③ Read the Input Data Register.



Notes: Confirmation of $\overline{REQ}$/$\overline{ACK}$ handshake completion is carried out using "①".
If "③" occurs before "②", $\overline{REQ}$ is asserted again.
(See the dotted lines in the above diagram.)

(a) Initiator → Target ($\overline{I/O}$ = "High")

① Write information into the output data register.
② Wait until WRDY (bit 5) of SCSI Bus Control Register 1 becomes "1".
③ Write #00 into the DMA Command Register.

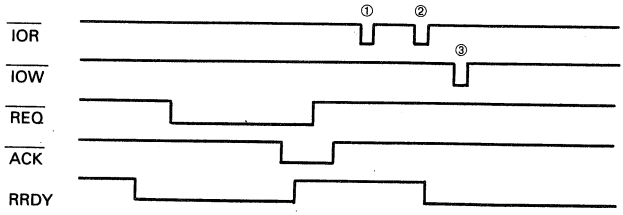


Notes: Confirmation of $\overline{REQ}$/$\overline{ACK}$ handshake completion is carried out using "②".
If "③" occurs before "②", $\overline{REQ}$ may not be negated.
(See the dotted lines in the above diagram.)

(b) Target → Initiator ($\overline{I/O}$ = "Low")

Figure 32. Method for Stopping MPU String Transmission in Target Mode

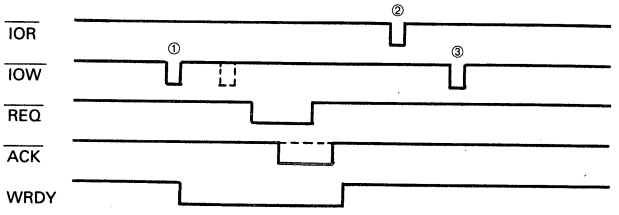
① Wait until RRDY (bit 4) of SCSI Bus Control Register 1 becomes "1" and $\overline{ACK}$ goes "high".
② Read the Input Data Register.
③ Write #00 into the DMA Command Register.



Notes: Confirmation of $\overline{REQ}/\overline{ACK}$ handshake completion is carried out using "①".
It makes no difference whether "②" occurs before "③" or vice versa.

(a) Target → Initiator ($\overline{I/O}$ = "Low")

① Write information into the output data register.
② Wait until WRDY (bit 5) of SCSI Bus Control Register 1 becomes "1".
③ Write #00 into the DMA Command Register.



Notes: Confirmation of $\overline{REQ}/\overline{ACK}$ handshake completion is carried out using "②".
If "③" occurs before "②", the information written at "①" may not be transmitted.
(See the dotted lines in the above diagram.)

(b) Initiator → Target ($\overline{I/O}$ = "High")

Figure 33. Method for Stopping MPU String Transmission in Initiator Mode

Arbitration Status Register

The read/write arbitration status register (figure 34) contains the following bits:

- Bit 0 (Selected): Indicates that selection phase is performed on the SCSI bus and as a result, this chip is selected by another device (initiator).
- Bit 1 (Reselected): Indicates that reselection phase is performed on the SCSI bus and as a result, this chip is selected by another device (target).
- Bit 2 (Selection/reselection end): After arbitration phase completion, selection/reselection phase is performed and then completed.
- Bit 3 (Arbitration not won): Although arbitration phase has been completed, another bus device has acquired the SCSI bus.

Timer

The timer consists of three 8-bit registers

- Time out register
- Time out control
- Time out counter

Time Out Register: The read/write time out register (figure 35) set-preset data for time control. The value set to this register is used as the initial value for the time out counter. The values set in this register are not changed even if the time out counter values are decremented.

Time Out Control Register: The write-only time out control register (figure 36) contains the following bits:

- Bit 0: Preset data specified by the time out register is loaded into the time out counter every time this bit is cleared. Before writing 1 to this bit to enable the time out counter, the preset data bus must be set to the time out counter.
- Bit 1: Every time this bit is set, time out counter values are decremented. In this case, the INC pin must be fixed to low.

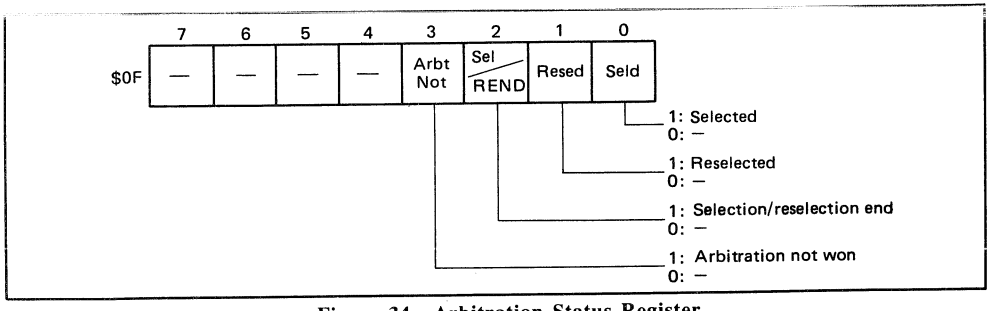


Figure 34. Arbitration Status Register

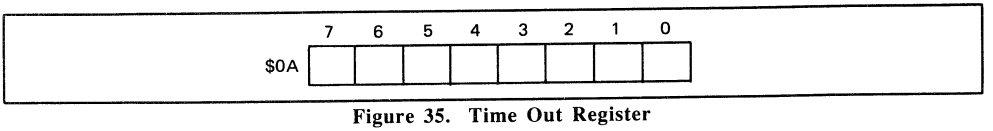


Figure 35. Time Out Register

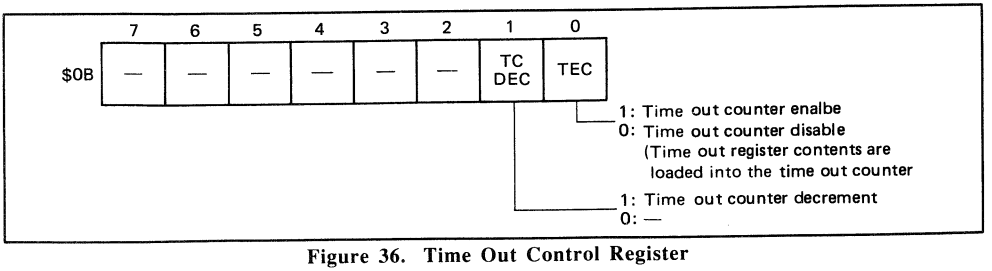


Figure 36. Time Out Control Register

Time Out Counter: Time out counter (figure 37) values can be decremented by a clock externally supplied through the INC pin or by writing $03 to the time out control register. This counter is a read-only register which cannot be directly written. Data can be set in this counter by writing data to the time out register and then writing 0 to time out control register bit 0.

Interrupt Enable/Status Registers

Interrupt enable/status registers consist of:

- Interrupt enable register (8 bits)
- Interrupt status register (8 bits)

The interrupt enable register is used to issue an interrupt when an error is detected in this chip.

Interrupt Enable Register: When errors indicated by the interrupt status register are detected, the read/write interrupt enable register (figure 38) allows an interrupt signal from the $\overline{IRQ}$ pin if the corresponding bit is set. Since the bit allocation of the interrupt enable register is the same as that of the interrupt status register, interrupts at each bit can be separately enabled. When the interrupt status register bits indicate errors with the corresponding bits of this register set to 1, interrupts are automatically generated. Accordingly, to inhibit interrupt generation, these register bits must be cleared (figure 39). Immediately after reset, all bits are in the interrupt disable state (cleared).

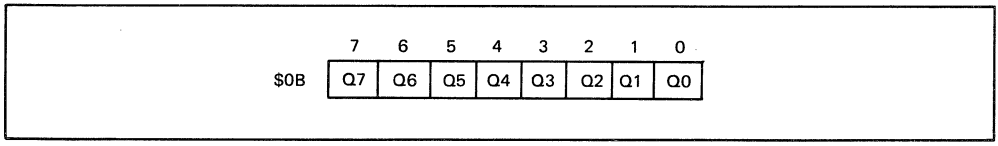


Figure 37. DMA Command Register

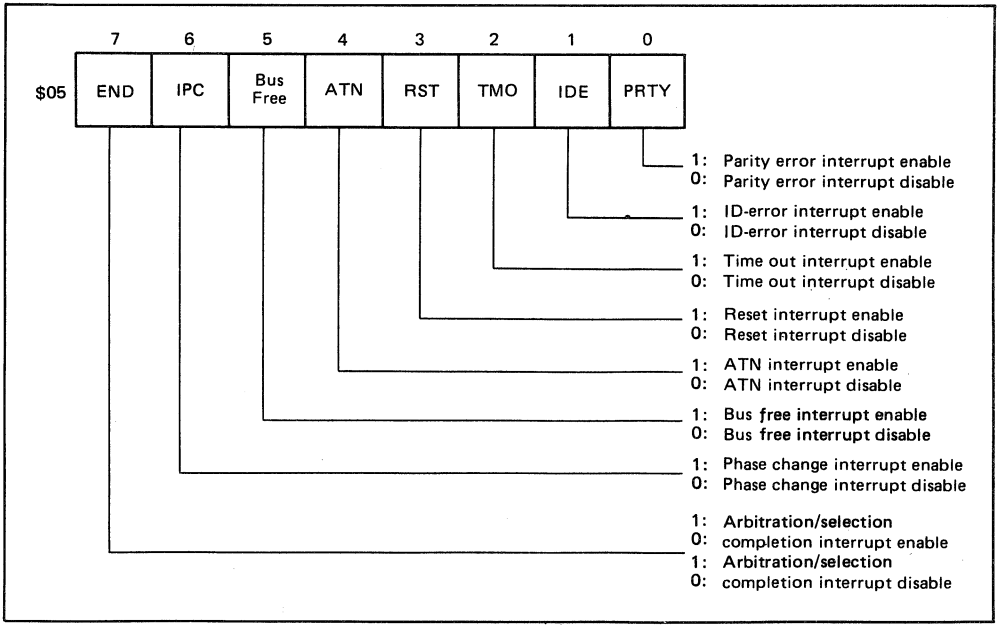


Figure 38. Interrupt Enable Register

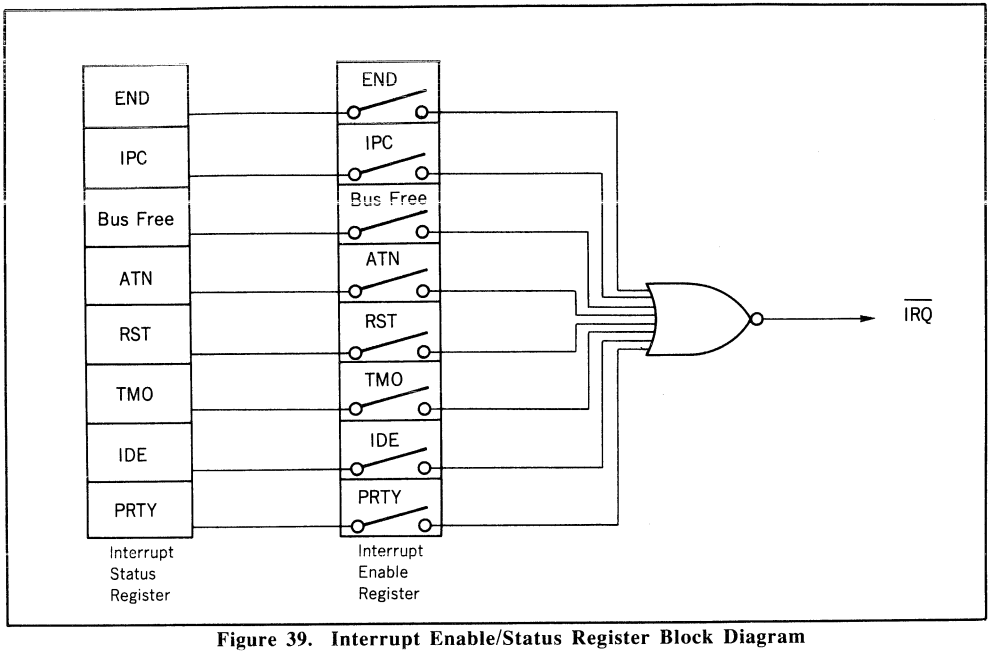


Figure 39. Interrupt Enable/Status Register Block Diagram

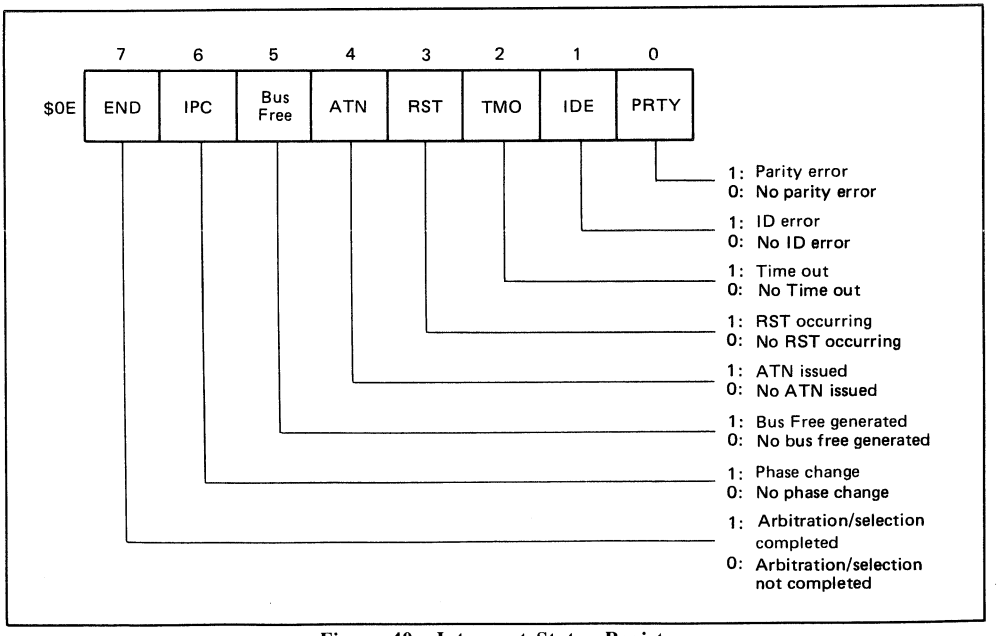


Figure 40. Interrupt Status Register

Interrupt Status Register: The read/write interrupt status register (figure 40) indicates interrupt status and is referenced when interrupts are processed. An interrupt occurs even if only a single bit of this register is set to 1, unless the bit is masked by the interrupt enable register.

- Bit 0: A parity error is detected on the SCSI bus. No parity check is performed during arbitration phase.
- Bit 1: ID-related error is detected on the SCSI bus.

  Example: With a non-single initiator (mode register bit 4 = 1), three or more IDs exist on the SCSI data bus during reselection phase: (own ID, selection/reselection partner ID, another ID). With a single initiator (mode register bit 4 = 0), two or more IDs exist on the SCSI bus during selection/reselection phase: (selectionpartner ID, another ID)
- Bit 2: Set to 1 if no response is received from a selected device after a period specified by the time out register when selection/reselection phase is performed.
- Bit 3: Reset condition is detected on the SCSI bus.
- Bit 4: An attention condition is detected on the SCSI bus.
- Bit 5: Bus free phase is detected on the SCSI bus.
- Bit 6: An interrupt is issued because the phases specified by the initiator and target do not agree in the information transfer phase. (Only in initiator mode.)
- Bit 7: Arbitration/selection phase is completed on the SCSI bus.

Reset

Usually, the reset is performed by pulling the $\overline{\text{RESET}}$ pin low (400 ns min). The write-only reset register (figure 41) can also be used to perform reset.

All of the HD64951's internal circuits can be reset by setting bit 0 of this register (except in MPU bus mode). Hard reset starts during the cycle in which data $01 has been written to address $10, and continues for 8 clock cycles. On completion of reset, bit 0 is automatically cleared to relieve the reset, thus eliminating the need for writing 0 to the reset register.

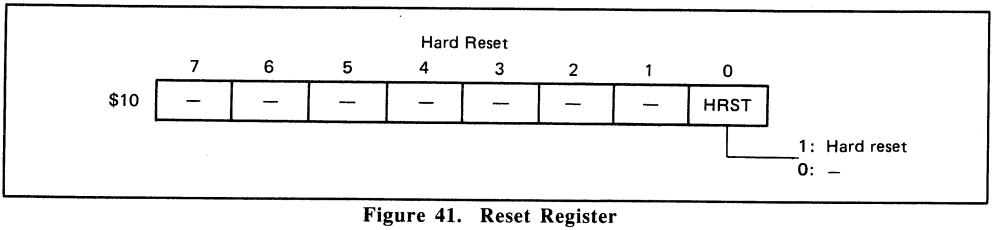


Figure 41. Reset Register

Attention and Limitation

1. Phase change interrupt detection method

1.1 Phenomenon

If phase change detection is carried out by polling the Interrupt Status Register, there is a possibility that the phase change will not be able to be detected because the IPC flag may be cleared by the read operation.

1.2 Countermeasures

(1) Prohibit polling of the Interrupt Status Register and carry out processing according to interrupts.

(2) Carry out polling of changes in C/D, I/O, and MSG.

Use either (1) or (2).

2. IPC flag when reselection phase is completed

2.1 Phenomenon

During reselection, the IPC flag is set 8 clocks after the END interrupt is generated at the completion of the reselection phase.

2.2 Countermeasure

Ignore the IPC flag immediately after the END interrupt is generated during reselection.

3. Input timing relationship between $\overline{IOR}$, $\overline{DRD}$ and the clock during the read operation

3.1 Phenomenon

When a read operation is carried out during MPU string transmission or DMA transmission when the unit is in initiator mode, it is possible that $\overline{ACK}$ may not be output if the time between the rise of $\overline{IOR}$, $\overline{DRD}$ and the fall of the clock is 16-20 ns, as shown in Figure 42.

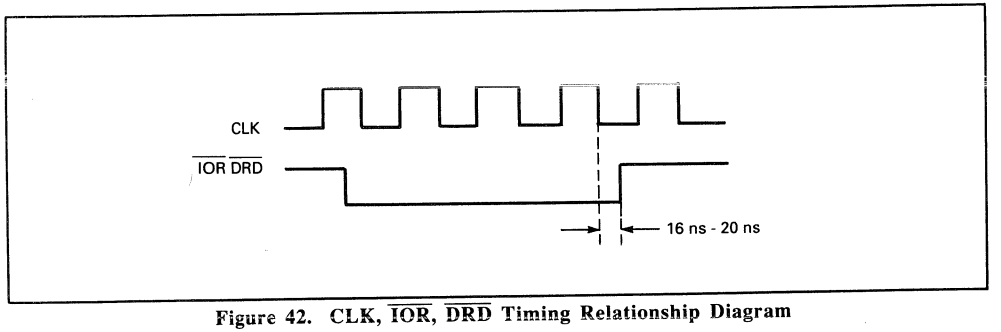


Figure 42. CLK, $\overline{IOR}$, $\overline{DRD}$ Timing Relationship Diagram

3.2 Countermeasures

(1) Make the frequency of the clock and $\overline{IOR}$, $\overline{DRD}$ equal and set so that the fall of $\overline{IOR}$, $\overline{DRD}$ and the fall of the clock do not occur within 16-20 ns of each other.

(2) Use the external countermeasure circuit shown in Figure 43 so that the rise of the $\overline{IOR}$, $\overline{DRD}$ signal input into the HD64951 occurs only during the "High" period of the clock, as shown in Figure 44.

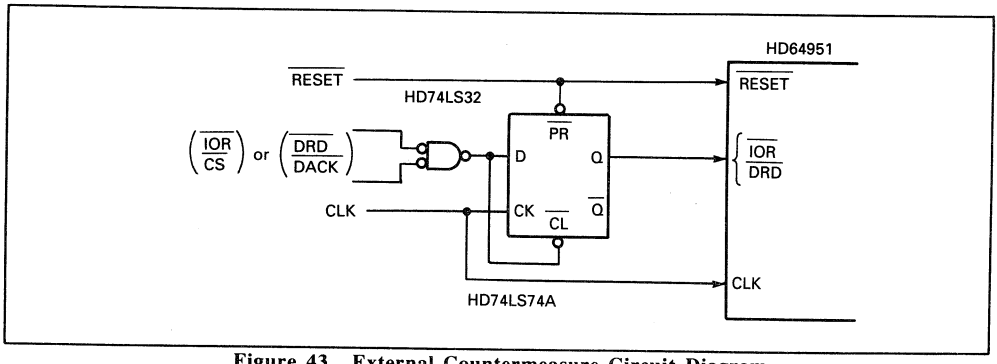


Figure 43. External Countermeasure Circuit Diagram

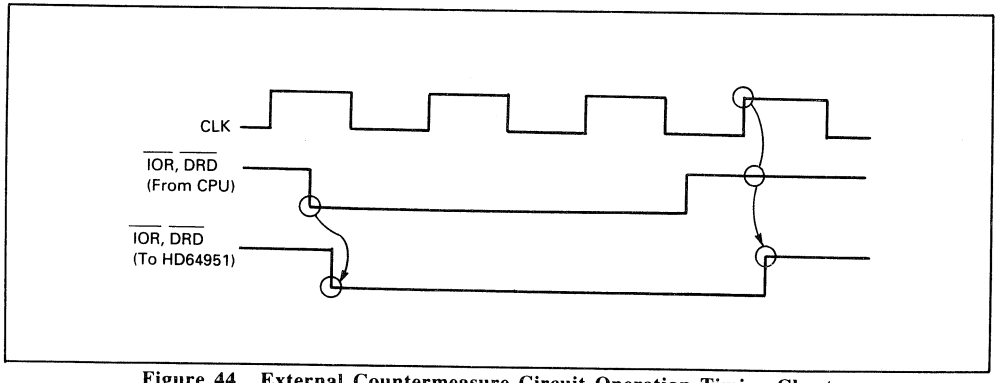


Figure 44. External Countermeasure Circuit Operation Timing Chart

4. $\overline{\text{RESET}}$/$\overline{\text{RST}}$ input during execution of auto arbitration and auto-selection/reselection sequence

4.1 Phenomenon

When $\overline{\text{RESET}}$ (For HD64951) or $\overline{\text{RST}}$ (For SCSI) input become "Low" during excution of auto-arbitration and auto-selection/reselect sequence, execution of sequence stops. However, internal circuit isn't initialize at this time. Sequence which is set on $0E: Interrupt-Status Register and $0F: Arbitration Status Register is still executed after setting $\overline{\text{RESET}}$ or $\overline{\text{RST}}$ "High". So contents of the register isn't cleared.

4.2 Countermeasures

PLS read $0E: Interrupt-Status Register and $0F: Arbitration Status Register as dummy to clear the register after $\overline{\text{RESET}}$ or $\overline{\text{RST}}$ is set "High" and it takes more than 100 CLK time (12.5 µs at 8 MHz).

5. $\overline{\text{RST}}$-input at occurrence of parity error

5.1 Phenomenon

When $\overline{\text{RST}}$-input becomes "Low" at occurrence of parity error (bit 0: PRTY on $0E: Interrupt-Status Register is "1".), you can't clear parity-bit until $\overline{\text{RST}}$ becomes "High", even if you read interrupt-status register.

5.2 Countermeasures

PLS read interrupt-status register as dummy to clear parity-bit after setting $\overline{\text{RST}}$ "High".

6. In case of writing on interrupt enable register, $\overline{\text{IRQ}}$ abnormal pulse output.

6.1 Phenomenon

(1) If you do writing on interrupt enable register during occurrence of the interrupt factor masked by $05: Interrupt Enable Register (the bit, which corresponds to the factor, on $0E: Interrupt Status Register is "1".), $\overline{\text{IRQ}}$ becomes "Low" for a moment. (PLS refer to Figure 45)

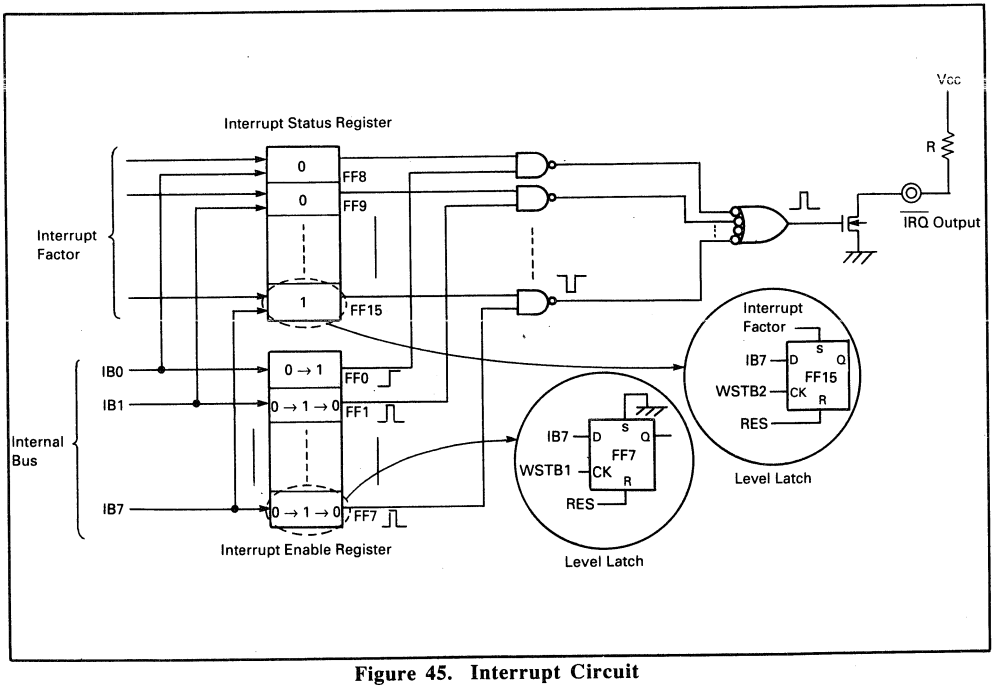


Figure 45. Interrupt Circuit

(2) When one bit of interrupt enable register is "1", and if you write "0" in the bit which corresponds to one factor on interrupt status register, $\overline{IRQ}$ becomes "Low" for a moment.

(3) As shown in figure 45, when interrupt status register is "0", if you write "0" on interrupt status register, the register is changed to $0 \rightarrow 1 \rightarrow 0$. At this time, MOS which drives $\overline{IRQ}$ is "On", and $\overline{IRQ}$ becomes "Low" for a moment.
(Although time when MOS becomes "On" is 60 ns, time of "H" level depends on charge current determined by external register. In case of R=1.5 kΩ and load capacity = 10 pF, it's 100 ns.)

(4) When one bit on interrupt enable register is "1", if you write "0" in the bit which correcponds to one factor on interrupt status register, $\overline{IRQ}$ becomes "L". (The Same as (3))

6.2 Countermeasures

Even if $\overline{IRQ}$ becomes "Low" (Abnormal pulse) for a moment, you need external circuit as shown in Figure 47 not to output signal of interrupt to MPU. This can be done by sampling $\overline{IRQ}$ signal with 500 ns period time in the circuit, and take logic-AND between shifting 1 clock and $\overline{IRQ}$ signal. When abnormal pulse occures, $\overline{IRQOUT}$ becomes "H". In case of normal operation ($\overline{IRQ}$ = "L" time-500 ns) $\overline{IRQOUT}$ becomes "L".
(Please refer to Figure 48)

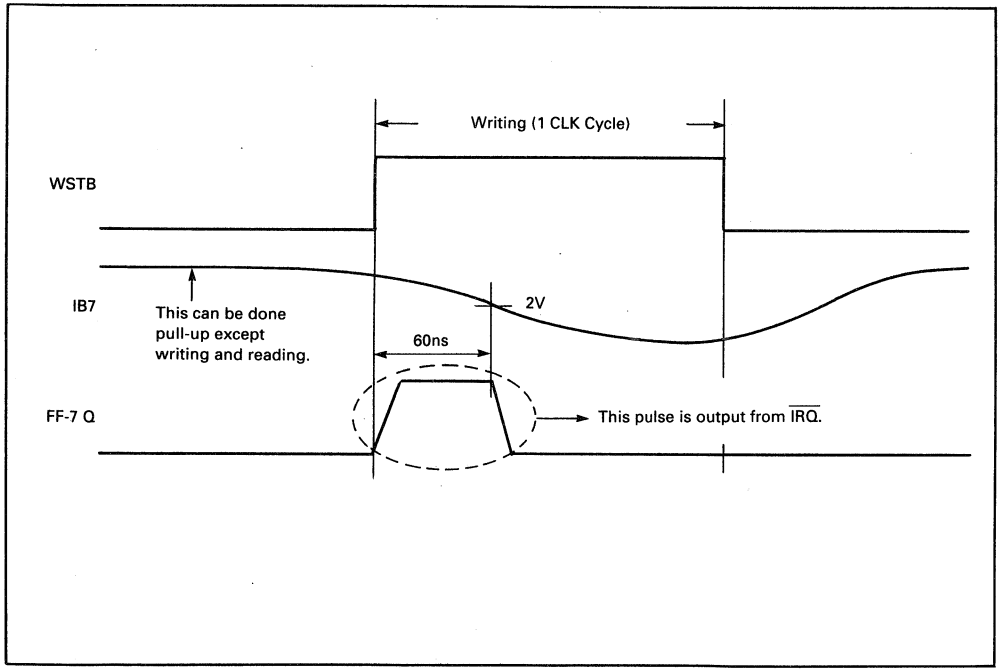


Figure 46. Timing of Writing on Register

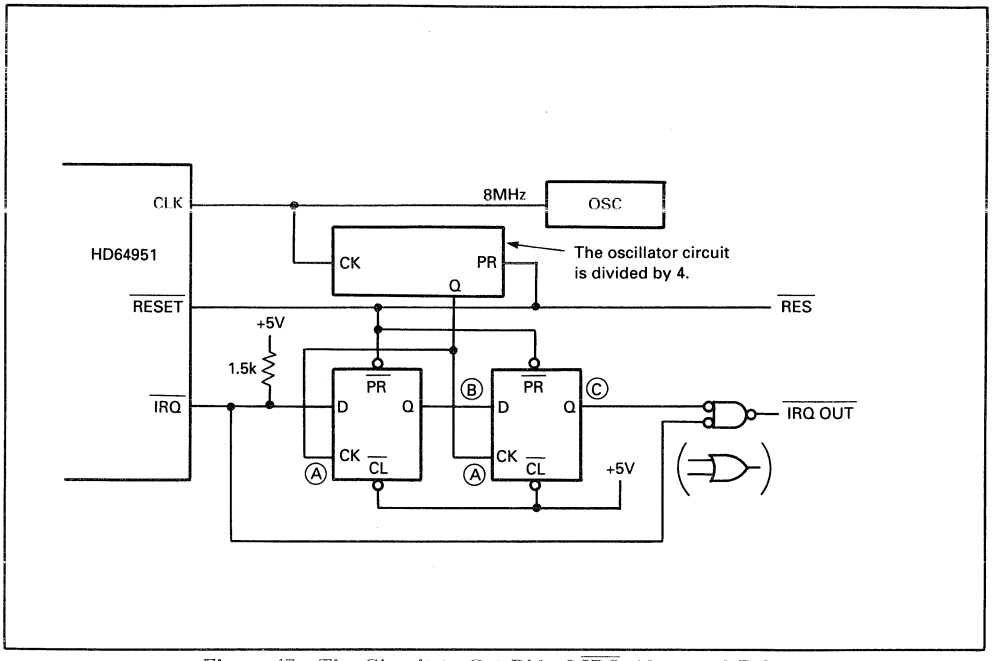


Figure 47. The Circuit to Get Rid of $\overline{IRQ}$ Abnormal Pulse

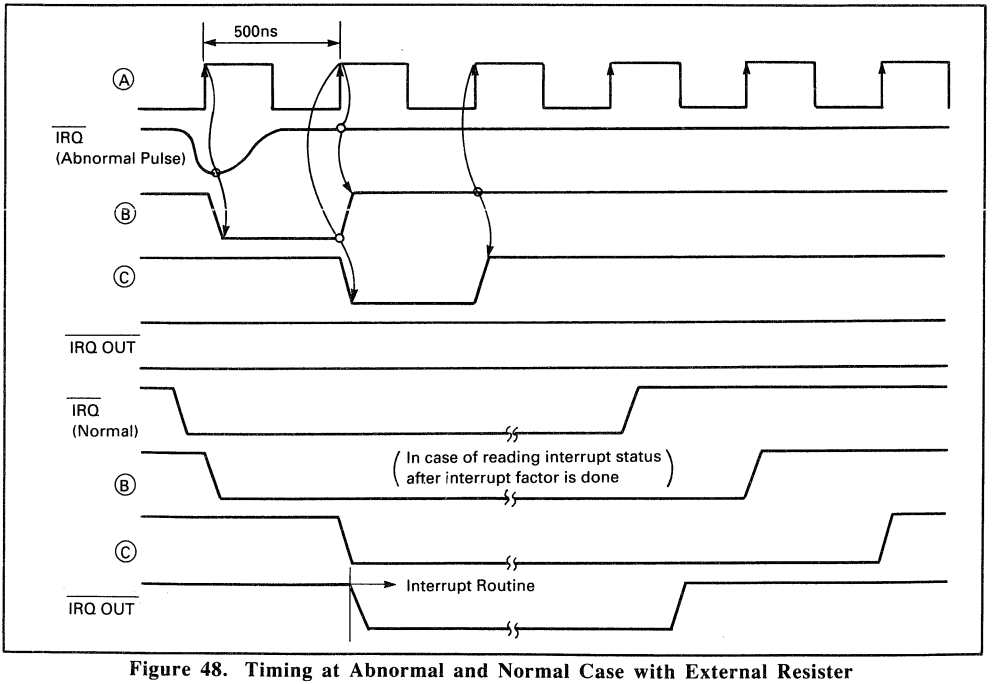


Figure 48. Timing at Abnormal and Normal Case with External Resister

7. $\overline{\text{WAIT}}$ signal during DMA transmission

7.1 Phenomenon

The $\overline{\text{WAIT}}$ signal of the HD64951 goes "Low" when $\overline{\text{DRD}}$, $\overline{\text{DWR}}$, etc. is negated during DMA transmission. With some DMACs, however, a wait may occur even when $\overline{\text{DRD}}$, $\overline{\text{DWR}}$, etc. is negated.

7.2 Countermeasure

Use $\overline{\text{WAIT}}$ and $\overline{\text{DRD}}$, $\overline{\text{DWR}}$, $\overline{\text{DACK}}$, etc. to create a $\overline{\text{WAIT1}}$ (normally ready) signal as shown in Figure 49.

8. DMA transmission mode which is not accompanied with data transmission

8.1 Phenomenon

If the $\overline{\text{DONE}}$ input goes "Low" for some reason immediately after DMA transmission begins, the $\overline{\text{DREQ}}$ signal is not negated and DMA transmission remains incomplete.

8.2 Countermeasure

By setting $\overline{\text{DONE}}$ and $\overline{\text{DACK}}$ to "Low", DMA transmission is judged as complete and $\overline{\text{DREQ}}$ is negated.

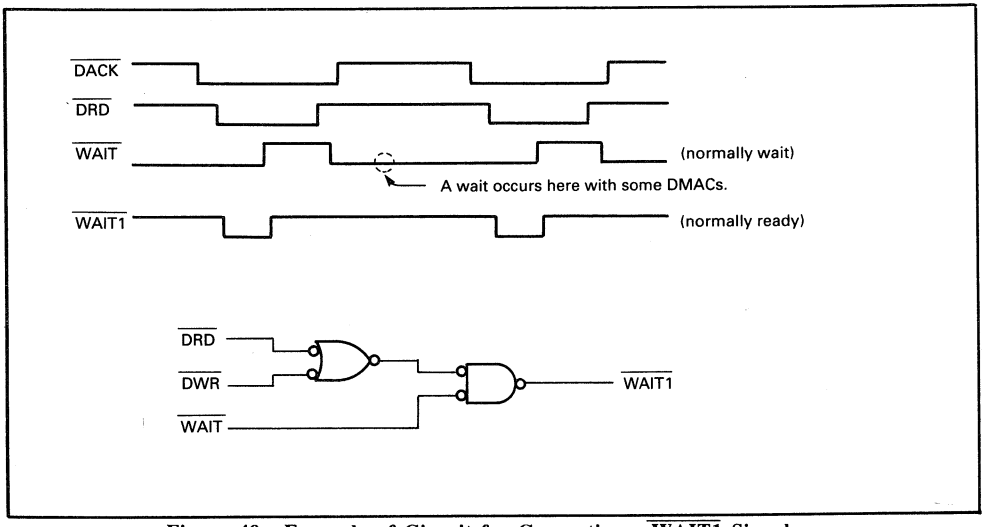


Figure 49. Example of Circuit for Generating a $\overline{\text{WAIT1}}$ Signal

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Output voltage	V_{OUT}	7	V
Output current	I_{OUT1} (Note 1)	50	mA
	I_{OUT2} (Note 2)	10	mA
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Maximum junction temperature	T_{jop}	125	°C

Notes: 1. Output current of the driver/receiver circuit
2. Output current of all internal circuits other than driver/receiver

DC Characteristics (V_{CC} = 5 V ± 5%)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Pins
Input voltage	V_{IH}	2.0	–	V_{CC}	V	V_{CC} = 5 V ±5%	$\overline{SDB0}$ – $\overline{SDB7}$, $\overline{SDBP}$ $\overline{REQ}$, $\overline{ACK}$, $\overline{SEL}$, $\overline{BSY}$, $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{ATN}$, $\overline{RST}$
	V_{IL}	−0.3	–	0.8	V	V_{CC} = 5 V ±5%	
Hysteresis voltage	V_{HYS}	0.2	–	–	V	V_{CC} = 5 V ±5%	
Input current	I_{IH}	–	–	50	µA	V_{IH} = 5.25 V	
	I_{IL}	−0.4	–	–	mA	V_{IL} = 0.4 V	
Output voltage	V_{OL}	–	–	0.5	V	V_{CC} = 4.75 V I_{OL} = 48 mA	
Input voltage	V_{IH}	2.0	–	V_{CC}	V	V_{CC} = 5 V ±5%	Input pins other than those above (including $\overline{DONE}$ pin)
	V_{IL}	−0.3	–	0.8	V	V_{CC} = 5 V ±5%	
Input current	I_{IH}	–	–	20	µA	V_{IH} = 5.25 V	
	I_{IL}	–	–	−20	µA	V_{IL} = 0.4 V	
Output voltage	V_{OH}	2.4	–	–	V	V_{CC} = 4.75 V I_{OH} = −0.4 mA	D0–D15
	V_{OL}	–	–	0.5	V	I_{OL} = 8 mA	
	V_{OH}	2.4	–	–	V	V_{CC} = 4.75 V, I_{OH} = −0.4 mA	$\overline{DREQ}$, $\overline{WAIT}$
	V_{OL}	–	–	0.5	V	I_{OL} = 4 mA	
	V_{OL}	–	–	0.5	V	I_{OL} = 4 mA	$\overline{IRQ}$, $\overline{DONE}$, $\overline{MPU\ DTACK}$ (Open drain output)
Supply current	I_{CC}	–	100	–	mA	V_{CC} = 5.25 V All outputs low	Sum of DV_{CC} and V_{CC}

AC Characteristics

Read/Write Timing for 68-and 80-Series MPU/DMAC

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{CS}$ Low to $\overline{IOR}$ Low $\overline{LSD}/\overline{UDS}$ Low	t_{CLRL}	20	–	–	ns	Figs 50 and 52	Read cycle
$\overline{IOW}$ High to $\overline{CS}$ Low	t_{WHCL}	0	–	–	ns	Figs 52	Read cycle
Address valid to $\overline{IOR}$, $\overline{IOW}$, Low $\overline{LDS}$, $\overline{UDS}$ Low	t_{AST}	20	–	–	ns	Figs 50 to 53	
R/$\overline{W}$ High to $\overline{LDS}/\overline{UDS}$ Low D$\overline{R}$/W Low to $\overline{DSTB}$ Low	t_{RST}	20	–	–	ns	Figs 50, 54	
$\overline{CS}$ Low to MPU READY Low $\overline{DACK}$ Low to $\overline{WAIT}$ Low	t_{CRDY}	10	–	150	ns	Figs 52 to 57	
Read Strobe Low Width	t_{RLW}	2.5 tcyc	–	–	ns	Figs 50, 53, 54 and 56	8-bit read Notes 1, 2 and 4
$\overline{IOR}$ Low to MPU READY High $\overline{LDS}/\overline{UDS}$ Low to $\overline{MPU\ DTACK}$ Low	t_{RRDYM}	20	–	2 tcyc +70	ns	Figs 50 and 52	8-bit read cycle Notes 3 and 4
$\overline{DRD}$ Low to $\overline{WAIT}$ High $\overline{DSTB}$ Low to $\overline{WAIT}$ High	t_{RRDYD}	20	–	2 tcyc +70	ns	Figs 54 and 56	8-bit read cycle Notes 3 and 4
Read Strobe Low to Data Bus Active	t_{RLDI}	10	–	150	ns	Figs 50 and 52	Note 2
Read Strobe Low to Data Valid	t_{RLDV}	50	–	1 tcyc +125	ns	Figs 50, 52, 54 and 56	8-bit read Notes 2 and 4
MPU READY High to $\overline{IOR}$ High $\overline{MPU\ DTACK}$ Low to $\overline{LDS}/\overline{UDS}$ High	t_{RDYRHM}	0.5 tcyc	–	–	ns	Figs 50 and 52	Read cycle Note 4
$\overline{WAIT}$ High to $\overline{DRD}$ High $\overline{WAIT}$ High to $\overline{DSTB}$ High	t_{RDYRHD}	0.5 tcyc	–	–	ns	Figs 54 and 56	Read cycle Note 4
$\overline{IOR}$ High to $\overline{CS}$ High $\overline{LDS}/\overline{UDS}$ High to $\overline{CS}$ High	t_{RHCHM}	0	–	–	ns	Figs 50 and 52	Read cycle
$\overline{DRD}$ High to $\overline{DACK}$ High $\overline{DSTB}$ High to $\overline{DACK}$ High	t_{RHCHD}	0	–	–	ns	Figs 54 and 56	Read cycle
$\overline{CS}$ High Width	t_{CHW}	200	–	–	ns	Figs 50 to 53	
Read Strobe High Width	t_{RHW}	230	–	–	ns	Figs 50, 52, 54 and 56	Note 2

Notes: 1. When the input data register is read in auto-handshaking mode, t_{RLW} must be extended to satisfy t_{RDYRH} specification (in DMA mode as well).
2. Read Strobe: $\overline{IOR}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{DRD}$, $\overline{DSTB}$ (read cycle)
3. In auto-handshaking mode and DMA mode, see t_{ALRDY} and t_{ALRD}
4. tcyc = Input Clock Cycle Time

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{CS}$ High to $\overline{IOW}$ Low $\overline{DACK}$ High to $\overline{DWR}$ Low	t_{CHWL}	50	–	–	ns	Figs 52 and 56	
$\overline{IOR}$, $\overline{IOW}$, $\overline{LDS}$/$\overline{UDS}$ High to Address Invalid	t_{AHLD}	0	–	–	ns	Figs 50 to 53	
$\overline{LDS}$/$\overline{UDS}$ High to R/$\overline{W}$ Low	t_{RHLDM}	0	–	–	ns		
$\overline{DSTB}$ High to DR/W High	t_{RHLDD}	0	–	–	ns	Fig 54	
Read Strobe High to DATA Invalid	t_{RDHLD}	30	–	230	ns	Figs 50, 52, 54 and 56	Note 2
$\overline{LDS}$/$\overline{UDS}$ High to $\overline{MPU}$ $\overline{DTACK}$ High	t_{DAKH}	30	–	100	ns	Figs 50 and 51	
Read Strobe Low to $\overline{DONE}$ Low	t_{RLDL}	–	–	1 tcyc	ns	Figs 50, 52, 54 and 56	Target mode E/L = 0 only (Notes 2 and 4)
DONE Low to $\overline{IOR}$, $\overline{IOW}$ High	t_{DNST1}	50	–	–	ns	Figs 52 and 53	
DONE Low to $\overline{LDS}$, $\overline{UDS}$ High	t_{DNST2}	50	–	–	ns	Figs 50 and 51	
DONE Low to $\overline{DRD}$, $\overline{DWR}$ High	t_{DNST3}	50	–	–	ns	Figs 56 and 57	
DONE Low to $\overline{DSTB}$ High	t_{DNST4}	50	–	–	ns	Figs 54 and 55	
$\overline{IOR}$, $\overline{IOW}$ High to $\overline{DONE}$ High	t_{DNHLD1}	0	–	–	ns	Figs 52 and 53	
$\overline{LDS}$, $\overline{UDS}$ High to $\overline{DONE}$ High	t_{DNHLD2}	0	–	–	ns	Figs 50 and 51	
$\overline{DRD}$, $\overline{DWR}$ High to $\overline{DONE}$ High	t_{DNHLD3}	0	–	–	ns	Figs 56 and 57	
$\overline{DSTB}$ High to $\overline{DONE}$ High	t_{DNHLD4}	0	–	–	ns	Figs 54 and 55	
$\overline{IOR}$ High to $\overline{CS}$ Low	t_{RHCL}	100	–	–	ns	Fig 53	
$\overline{CS}$ Low $\overline{IOW}$, $\overline{LDS}$/$\overline{UDS}$ Low	t_{CLW1}	0	–	–	ns	Figs 51 and 53	Write cycle

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{DACK}$ Low to $\overline{DWR}$, $\overline{DSTB}$ Low	t_{CLWL2}	0	–	–	ns	Figs 55 and 57	Write cycle
R/$\overline{W}$ Low to $\overline{LDS}$/$\overline{UDS}$ Low DR/W High to $\overline{DSTB}$ Low	t_{WST}	20	–	–	ns	Figs 51 and 55	Write cycle
Write Strobe Low Width	t_{WLW}	3 tcyc	–	–	ns	Figs 51, 53, 55 and 57	Notes 4, 5 and 6
$\overline{IOW}$ Low to MPU READY High $\overline{LDS}$/$\overline{UDS}$ Low to $\overline{MPU}$ $\overline{DTACK}$ Low	t_{WRDYM}	50	–	1 tcyc +150	ns	Figs 51 and 53	Write cycle Note 4
$\overline{DWR}$ Low to $\overline{WAIT}$ High $\overline{DSTB}$	t_{WRDYD}	50	–	1 tcyc +130	ns	Figs 55 and 57	Write cycle Note 4
MPU READY High to $\overline{IOW}$ High $\overline{MPU}$ $\overline{DTACK}$ Low to $\overline{LDS}$/$\overline{UDS}$ High	t_{RDYWHM}	0.5 tcyc	–	–	ns	Figs 51 and 53	Notes 4 and 7 Write cycle
$\overline{WAIT}$ High to $\overline{DWR}$ High $\overline{WAIT}$ High to $\overline{DSTB}$ High	t_{RDYWHD}	0.5 tcyc	–	–	ns	Figs 55 and 57	Notes 4 and 7 Write cycle
Data Valid to Write Strobe High	t_{WDST}	100	–	–	ns	Figs 51 and 57	Note 5
Write Strobe High to Data Invalid	t_{WDHLD}	10	–	–	ns	Figs 51, 53, 55 and 57	Note 5
$\overline{IOW}$, $\overline{LDS}$/$\overline{UDS}$ High to $\overline{CS}$ High	t_{WHCH}	0	–	–	ns	Figs 51 and 53	Write cycle
Write Strobe High Width	t_{WHW}	2 tcyc	–	–	ns	Figs 51, 53, 55 and 57	8-bit write Notes 4 and 5
$\overline{IOW}$ High to $\overline{IOR}$ Low DWR High to $\overline{DRD}$ Low	t_{WHRL}	3 tcyc	–	–	ns	Figs 53 and 57	Note 4

Notes: 5. Write Strobe: $\overline{IOW}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{DWR}$, $\overline{DSTB}$ (write cycle)

6. It is unnecessary to meet t_{WLW} as long as t_{RDYWH} is satisfied. In handshake mode, however, t_{WLW} must be extended to meet t_{RDYWH}.

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{CS}$ High to $\overline{IOR}$ Low $\overline{DACK}$ High to $\overline{DRD}$ Low	t_{CHRL}	100	–	–	ns	Figs 53 and 57	
$\overline{LDS}/\overline{UDS}$ High to R/$\overline{W}$ High $\overline{DSTB}$ High to DR/$\overline{W}$ Low	t_{WHLD}	0	–	–	ns	Figs 51 and 55	
$\overline{DREQ}$ Low to $\overline{DACK}$ Low	t_{DRDAL}	0	–	–	ns	Figs 54 to 57	
$\overline{DACK}$ High Width	t_{DACHW}	0	–	–	ns	Figs 54 to 57	DMA being performed
$\overline{DRD}$, $\overline{DWR}$ High to $\overline{WAIT}$ Low	t_{SHWTL1}	30	–	150	ns	Figs 56 and 57	
$\overline{DSTB}$ High to $\overline{WAIT}$ Low	t_{SHWTL2}	30	–	150	ns	Figs 54 and 55	
$\overline{DACK}$ High to $\overline{WAIT}$ High (Last DMA Cycle)	t_{CHWTH}	30	–	2 tcyc +100	ns	Figs 54 to 57	Last cycle DMA only Note 4
$\overline{DONE}$ Low to $\overline{DREQ}$ High	t_{DNDR}	30	–	150	ns	Figs 54 to 57	
DR/$\overline{W}$ High Width	t_{DRWHW}	0	–	–	ns	Fig 54	
DR/$\overline{W}$ Low Width	t_{DRWLW}	0	–	–	ns	Fig 55	
$\overline{DACK}$ Low to $\overline{DRD}$, $\overline{DSTB}$ Low	t_{CLRL}	0	–	–	ns	Figs 54 and 56	Read cycle
$\overline{DWR}$ High to $\overline{DACK}$ High $\overline{DSTB}$ High to $\overline{DACK}$ High	t_{WHCH}	0	–	–	ns	Figs 55 and 57	Write cycle

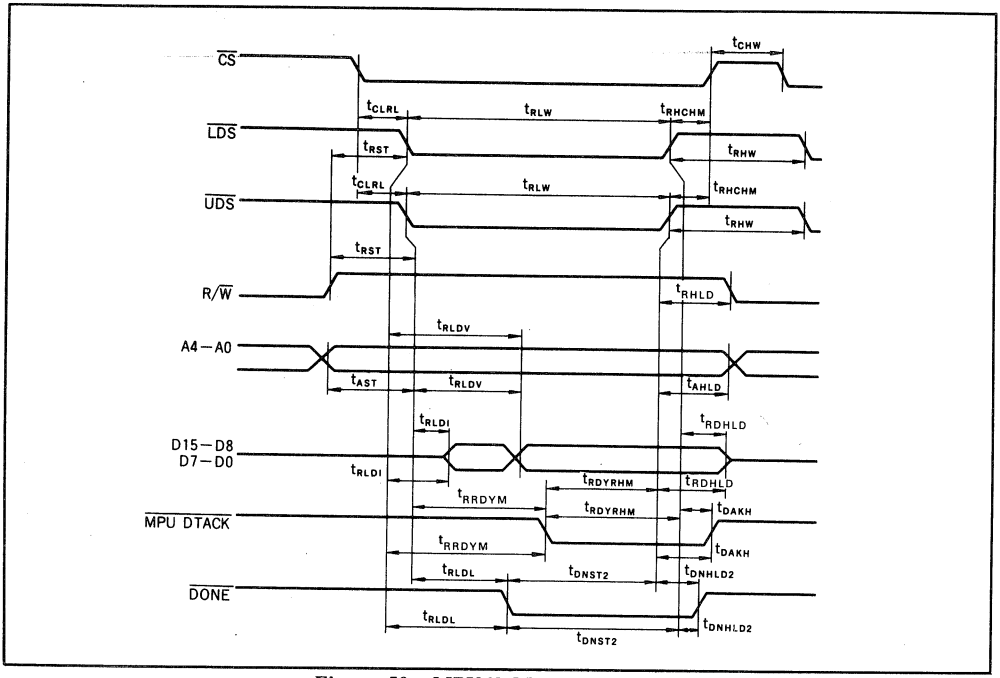


Figure 50. MPU68 Mode Read Timing

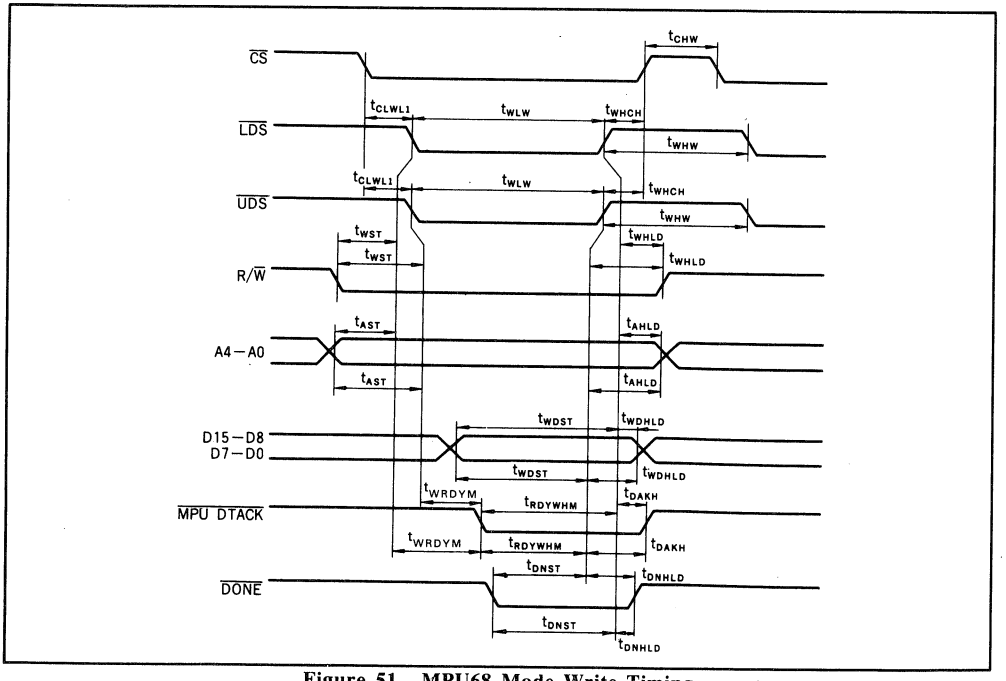


Figure 51. MPU68 Mode Write Timing

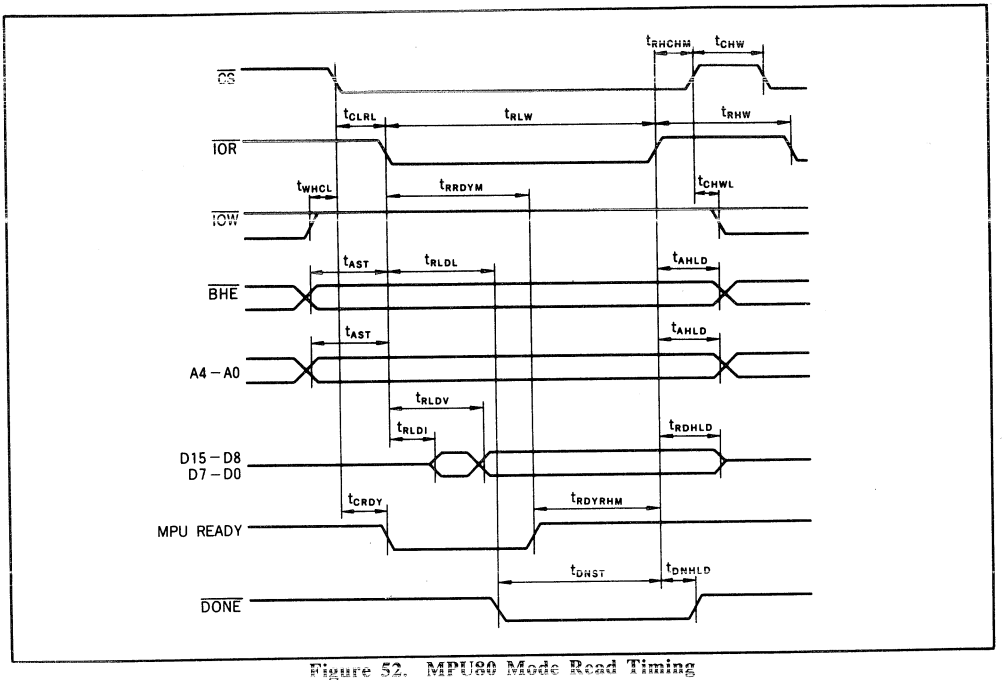


Figure 52. MPU80 Mode Read Timing

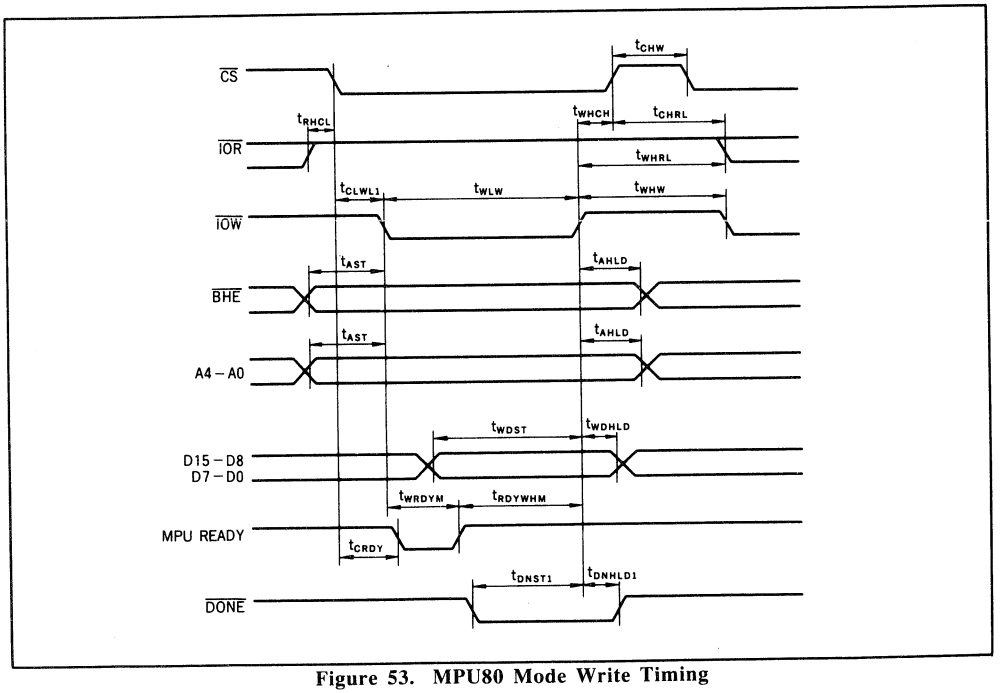
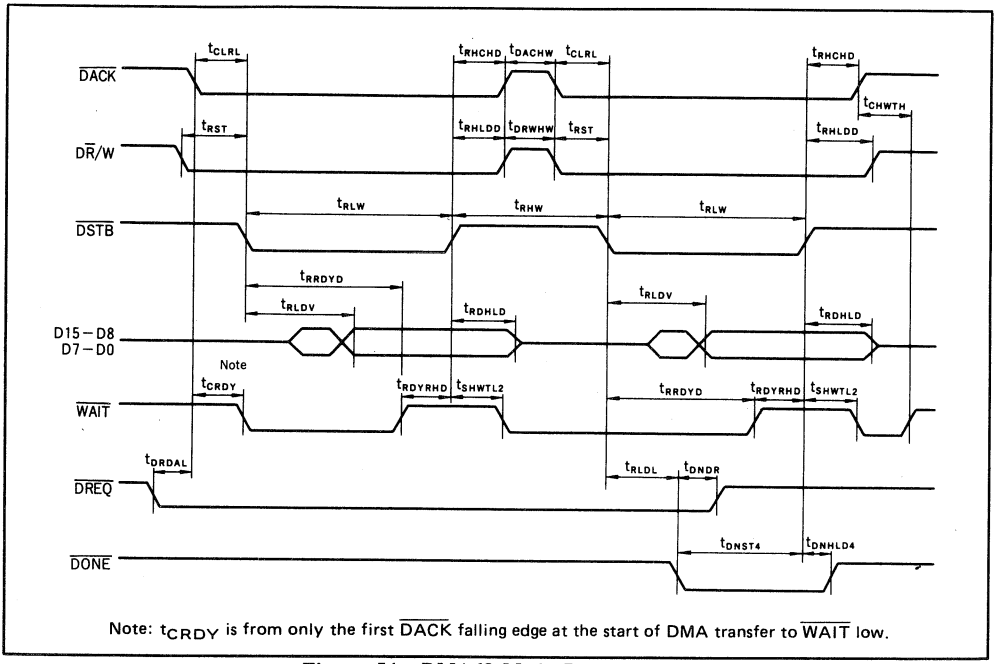
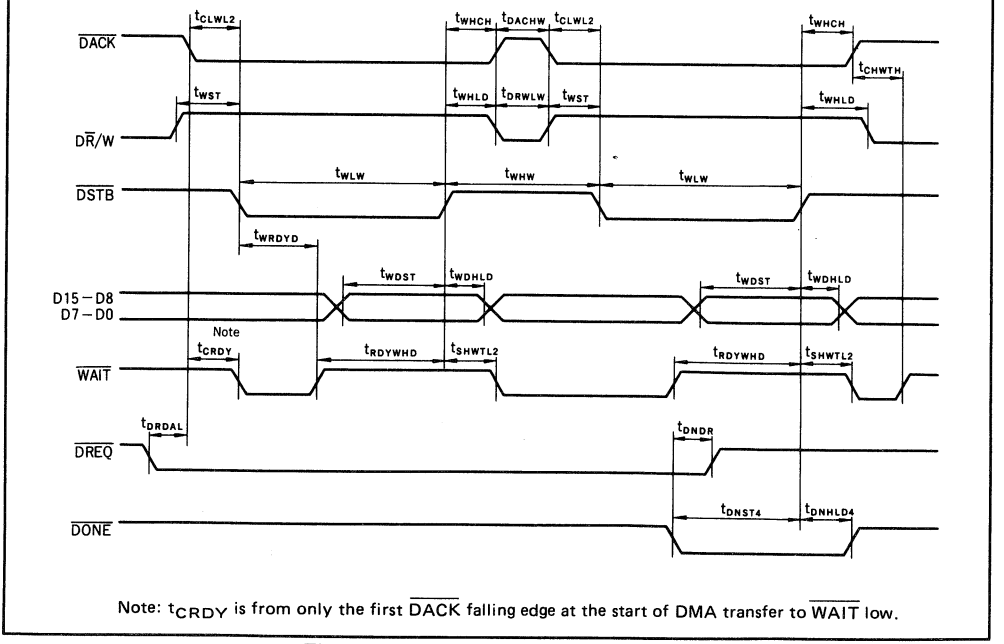


Figure 53. MPU80 Mode Write Timing



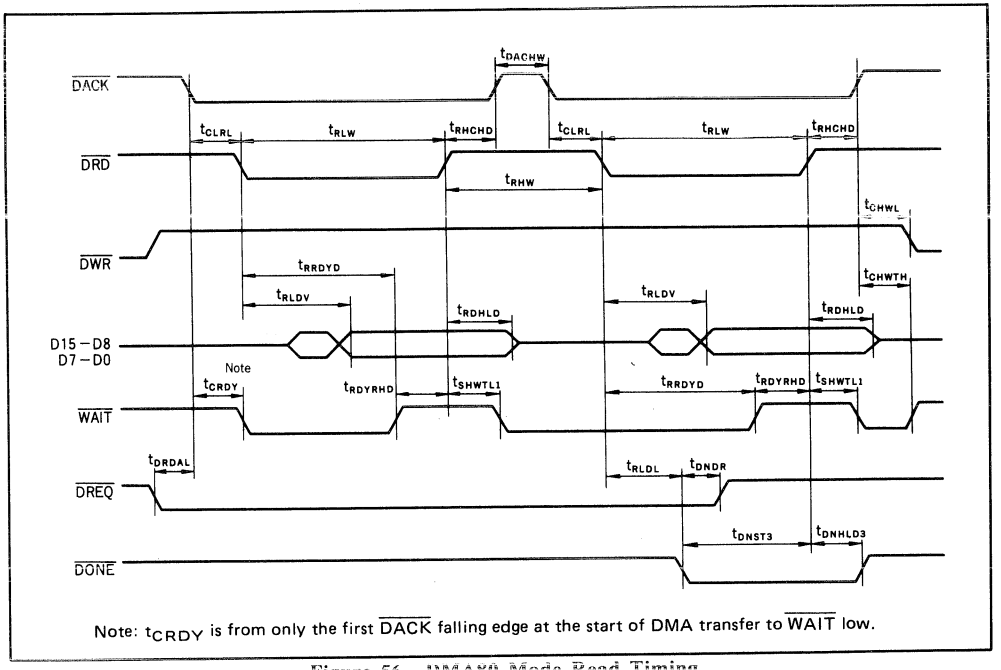
Note: t_{CRDY} is from only the first $\overline{DACK}$ falling edge at the start of DMA transfer to $\overline{WAIT}$ low.

Figure 54. DMA68 Mode Read Timing



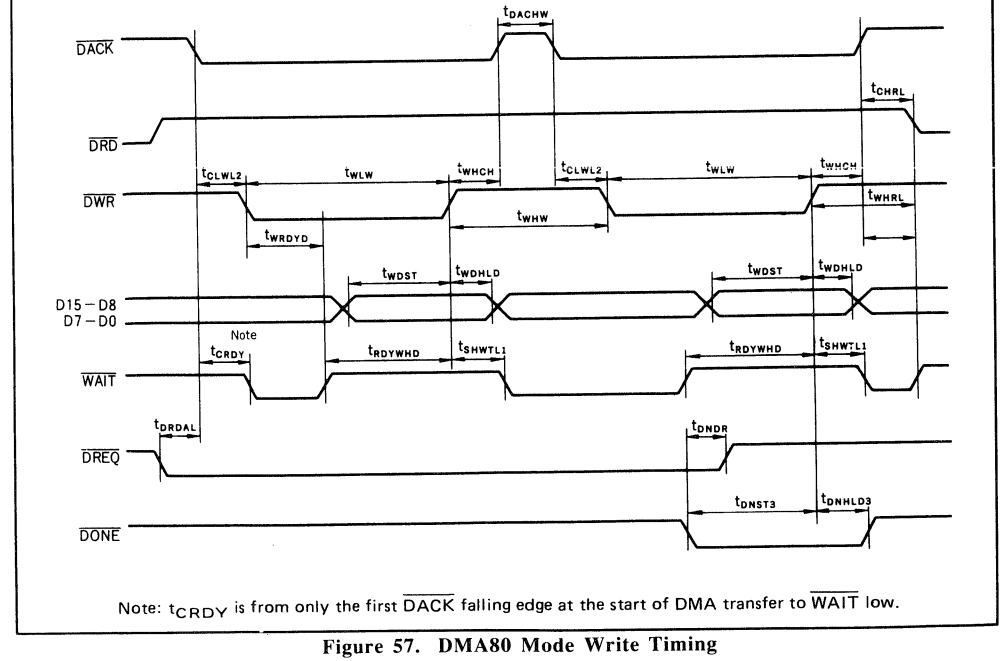
Note: t_{CRDY} is from only the first $\overline{DACK}$ falling edge at the start of DMA transfer to $\overline{WAIT}$ low.

Figure 55. DMA68 Mode Write Timing



Note: t_{CRDY} is from only the first $\overline{DACK}$ falling edge at the start of DMA transfer to $\overline{WAIT}$ low.

Figure 56. DMA80 Mode Read Timing



Note: t_{CRDY} is from only the first $\overline{DACK}$ falling edge at the start of DMA transfer to $\overline{WAIT}$ low.

Figure 57. DMA80 Mode Write Timing

MPU String Transfer Timing

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{ACK}$ Low to $\overline{REQ}$ High (Target Mode, Data Input)	t_{AQIN1}	30	–	1 tcyc +260	ns	Figs 58 and 60	I/O = 0 Target Note 1
$\overline{REQ}$ Low to $\overline{ACK}$ Low (Initiator Mode, Data Input)	t_{AQIN2}	30	–	1 tcyc +260	ns	Figs 58 and 60	I/O = 0 Initiator Note 1
$\overline{ACK}$ High to $\overline{REQ}$ Low (Target Mode, Data Input)	t_{AHQL1}	0.5 tcyc +30	–	1.5 tcyc +260	ns	Figs 58 and 60	I/O = 0 Target Note 1
$\overline{REQ}$ High to $\overline{ACK}$ High (Initiator Mode)	t_{QHAH}	30	–	1 tcyc +300	ns	Figs 58 to 61	Initiator Note 1
$\overline{SDB}$ Valid to $\overline{ACK}$ Low (Target Mode, Data Input)	t_{SDST1}	0	–	–	ns	Figs 58 and 60	
$\overline{SDB}$ Valid to $\overline{REQ}$ Low (Initiator Mode, Data Input)	t_{SDST2}	0	–	–	ns	Figs 58 and 60	
$\overline{ACK}$ Low $\overline{SDB}$ Invalid (Target Mode, Data Input)	t_{SDHLD1}	–	–	100	ns	Figs 58 and 60	
$\overline{REQ}$ Low $\overline{SDB}$ Invalid (Initiator Mode, Data Input)	t_{SDHLD2}	–	–	100	ns	Figs 58 and 60	
$\overline{ACK}$ Low to Read Data Valid (Target Mode)	t_{ALRD1}	1 tcyc +30	–	2 tcyc +250	ns	Figs 58 and 60	I/O = 0 Note 1
$\overline{REQ}$ Low to Read Data Valid (Initiator Mode)	t_{ALRD2}	1 tcyc +30	–	2 tcyc +250	ns	Figs 58 and 60	I/O = 1 Note 1
$\overline{ACK}$ Low to: $\overline{MPU\ READY}$ High $\overline{MPU\ DTACK}$ Low $\overline{WAIT}$ High (Target Mode)	t_{ALRDY1}	2.5 tcyc +30	–	3.5 tcyc +180	ns	Figs 58 and 60	I/O = 0 Note 1
$\overline{REQ}$ Low to: $\overline{MPU\ READY}$ High $\overline{MPU\ DTACK}$ Low $\overline{WAIT}$ High (Initiator Mode)	t_{ALRDY2}	2.5 tcyc +30	–	3.5 tcyc +180	ns	Figs 58 and 60	I/O = 1 Note 1
Read Strobe High to $\overline{REQ}$ Low (Target Mode)	t_{RHQL}	50	–	1 tcyc +250	ns	Figs 58 and 60	E/L = 1 Note 1
$\overline{MPU\ READY}$ High to $\overline{REQ}$ Low $\overline{MPU\ DTACK}$ Low to $\overline{REQ}$ Low $\overline{WAIT}$ High to $\overline{REQ}$ Low (Target Mode)	t_{RDYQL}	1.5 tcyc	–	1.5 tcyc +230	ns	Figs 58 and 60	I/O = 0 Note 1

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
MPU READY High to $\overline{ACK}$ Low $\overline{MPU}$ DTACK Low to $\overline{ACK}$ Low $\overline{WAIT}$ High to $\overline{ACK}$ Low (Initiator Mode)	t_{RDYAL}	20	–	0.5 tcyc +190	ns	Figs 58 and 60	I/O = 1 Note 1
Write Strobe High to $\overline{SDB}$ Valid	t_{WHSD}	0.5 tcyc	–	1.5 tcyc +270	ns	Figs 59 and 61	Note 1
$\overline{SDB}$ Valid to $\overline{REQ}$ Low (Target Mode, Data Output)	t_{SDQAL1}	1 tcyc −40	–	1.5 tcyc +150	ns	Figs 59 and 61	I/O = 1 Note 1
$\overline{SDB}$ Valid to $\overline{ACK}$ Low (Initiator Mode, Data Output)	t_{SDQAL2}	1 tcyc −40	–	1.5 tcyc +150	ns	Figs 59 and 61	I/O = 0 Note 1
$\overline{ACK}$ High to $\overline{REQ}$ Low (Target Mode, Data Output)	t_{AQQT1}	0.5 tcyc +50	–	1.5 tcyc +260	ns	Figs 59 and 61	I/O = 1 Note 1
$\overline{REQ}$ Low to $\overline{ACK}$ Low (Initiator Mode, Data Output)	t_{AQQT2}	0.5 tcyc +50	–	1.5 tcyc +290	ns	Figs 59 and 61	I/O = 0 Note 1
$\overline{ACK}$ Low to $\overline{REQ}$ High (Target Mode, Data Output)	t_{ALQH}	50	–	1 tcyc +260	ns	Figs 59 and 61	I/O = 1 Note 1
$\overline{ACK}$ Low to $\overline{SDB}$ Invalid (Target Mode, Data Output)	t_{QHSD1}	1 tcyc	–	2 tcyc +340	ns	Figs 59 and 61	I/O = 1 Note 1
$\overline{REQ}$ High to $\overline{SDB}$ Invalid (Initiator Mode, Data Output)	t_{QHSD2}	1 tcyc	–	2 tcyc +340	ns	Figs 59 and 61	I/O = 0 Note 1
$\overline{ACK}$ Low to: MPU READY High $\overline{MPU}$ $\overline{DTACK}$ Low $\overline{WAIT}$ High (Target Mode)	t_{QHRDY1}	1.5 tcyc	–	2.5 tcyc +200	ns	Figs 59 and 61	I/O = 1 Note 1
$\overline{REQ}$ High to MPU READY High $\overline{REQ}$ High to $\overline{MPU}$ $\overline{DTACK}$ Low $\overline{REQ}$ High to $\overline{WAIT}$ High (Initiator Mode)	t_{QHRDY2}	1.5 tcyc	–	2.5 tcyc +200	ns	Figs 59 and 61	I/O = 0 Note 1

Note: 1. tcyc = Input Clock Cycle Time

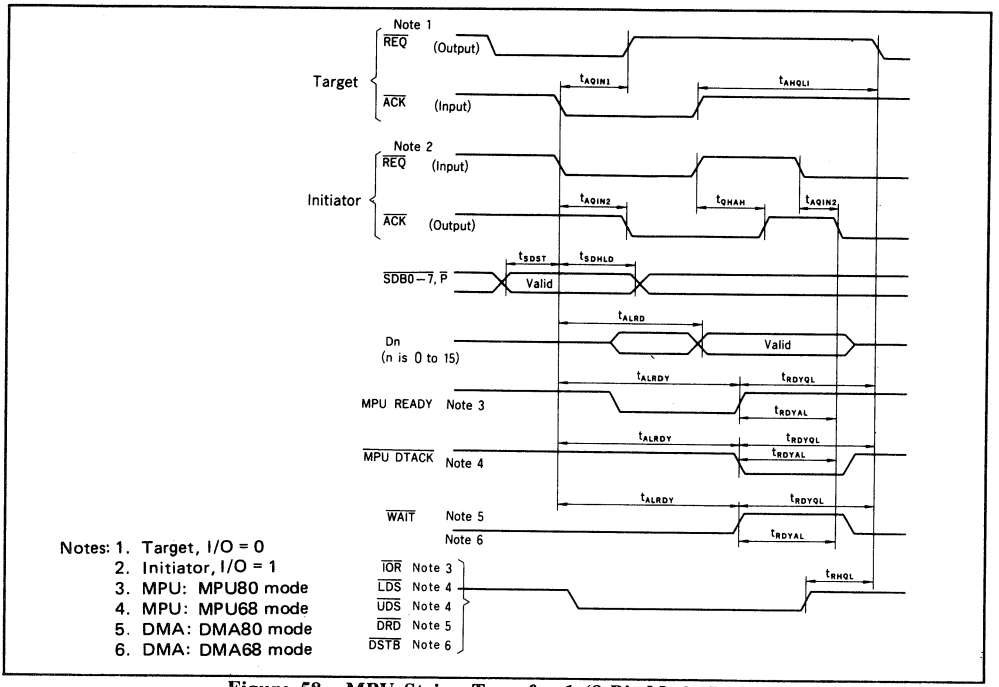


Figure 58. MPU String Transfer 1 (8-Bit Mode Read)

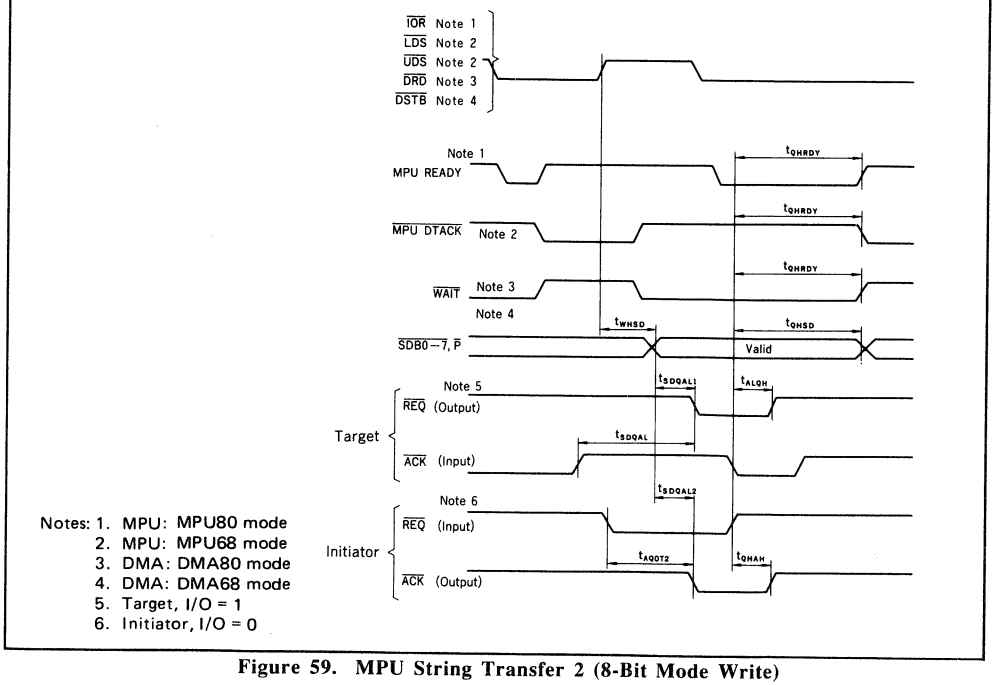
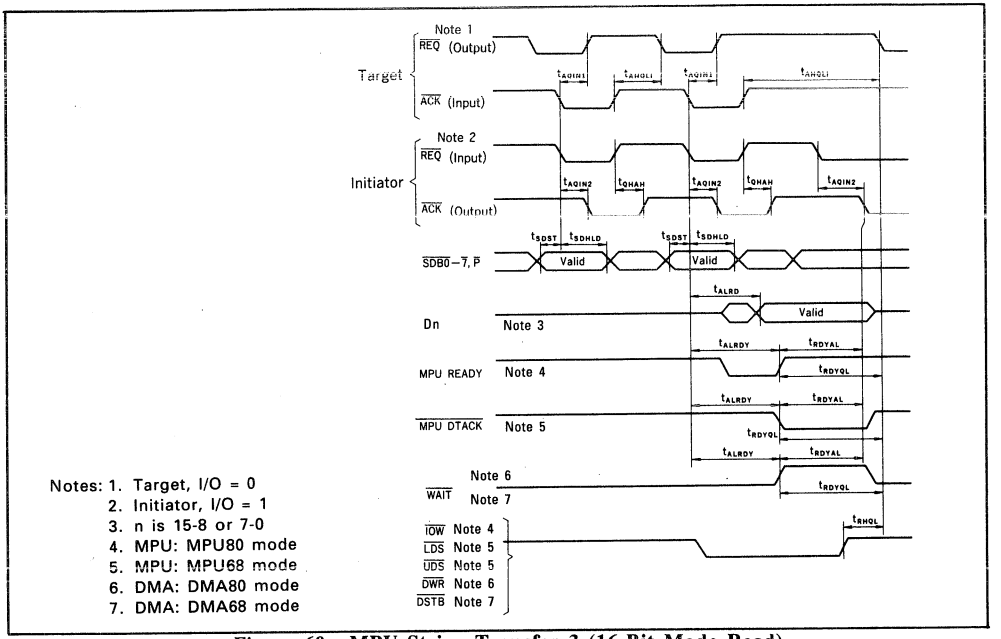
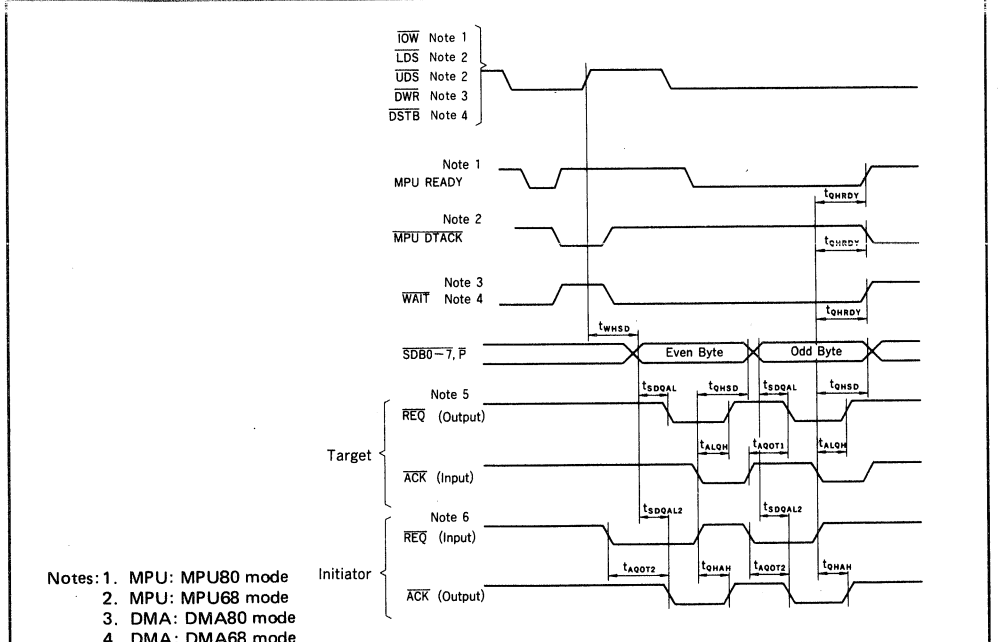


Figure 59. MPU String Transfer 2 (8-Bit Mode Write)



Notes: 1. Target, I/O = 0
2. Initiator, I/O = 1
3. n is 15-8 or 7-0
4. MPU: MPU80 mode
5. MPU: MPU68 mode
6. DMA: DMA80 mode
7. DMA: DMA68 mode

Figure 60. MPU String Transfer 3 (16-Bit Mode Read)



Notes: 1. MPU: MPU80 mode
2. MPU: MPU68 mode
3. DMA: DMA80 mode
4. DMA: DMA68 mode
5. Target, I/O = 1
6. Initiator, I/O = 0

Figure 61. MPU String Transfer 4 (16-Bit Mode Write)

External DMAC Access Timing

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{IOW}$ High to $\overline{DREQ}$ Low $\overline{LDS}/\overline{UDS}$ High to $\overline{DREQ}$ Low	t_{WHDRL8}	1 tcyc	–	2 tcyc +200	ns	Fig 62	8-bit write Note 1
$\overline{REQ}$ Low to $\overline{DREQ}$ Low	t_{QLDRL}	50	–	200	ns	Fig 62	Initiator mode

Note: 1. tcyc = Input Clock Cycle Time

Reset Pulse and Clock Pulse

Item	Symbol	Min	Typ	Max	Unit	Test Condition
$\overline{RESET}$ Low Width	t_{RESET}	400	—	—	ns	Fig 63
CLK Period	t_{cyc}	125	—	1000	ns	Fig 64
CLK High Width	t_{HCLK}	55	—	—	ns	Fig 64
CLK Low Width	t_{LCLK}	55	—	—	ns	Fig 64

Reset Condition Detect and Attention Condition Interrupt Timing

Item	Symbol	Min	Typ	Max	Unit	Test Condition
$\overline{RST}$ Low Width	t_{BRSTW}	3 tcyc	—	—	ns	Fig 65
$\overline{RST}$ Low to SCSI Bus Release	t_{RSBH}	—	—	3 tcyc +300	ns	Fig 65
$\overline{ATN}$ Low Width	t_{ATNW}	3 tcyc	—	—	ns	Fig 65
$\overline{ATN}$ Low to $\overline{IRQ}$ Low	t_{ATIRQ}	—	—	2.5 tcyc +100	ns	Fig 65

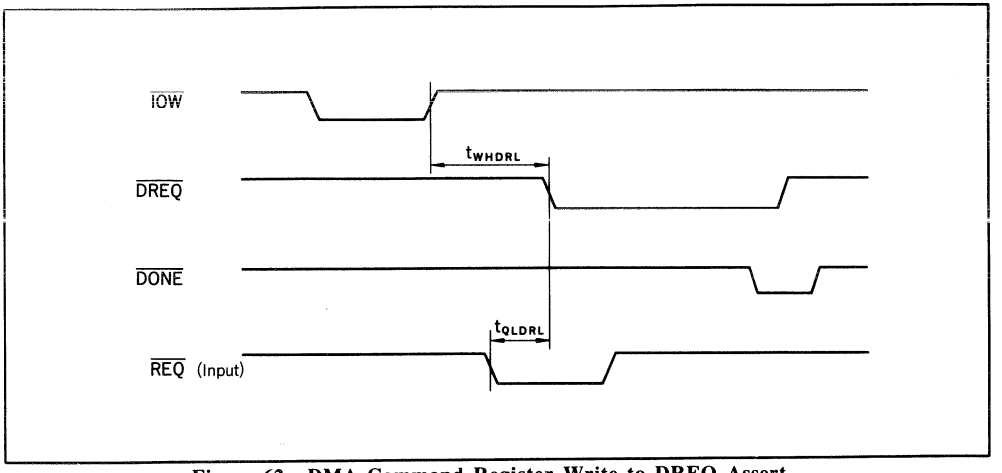


Figure 62. DMA Command Register Write to DREQ Assert

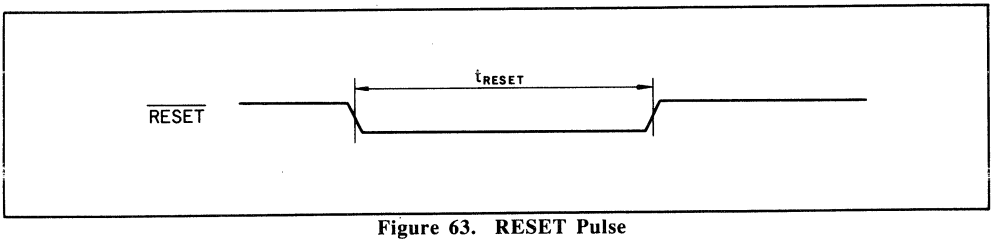


Figure 63. RESET Pulse

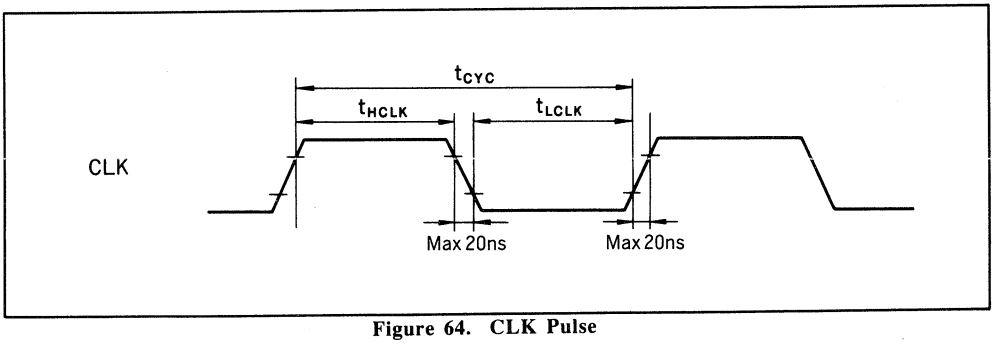


Figure 64. CLK Pulse

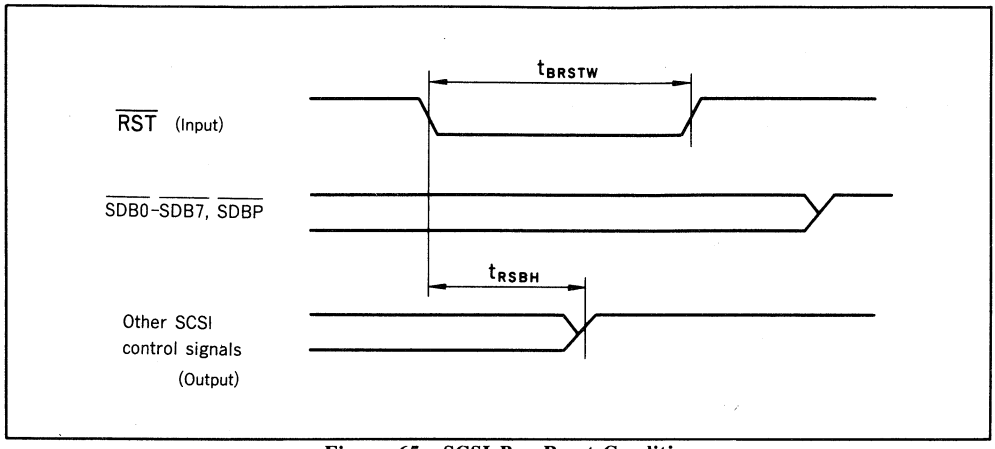


Figure 65. SCSI Bus Reset Condition

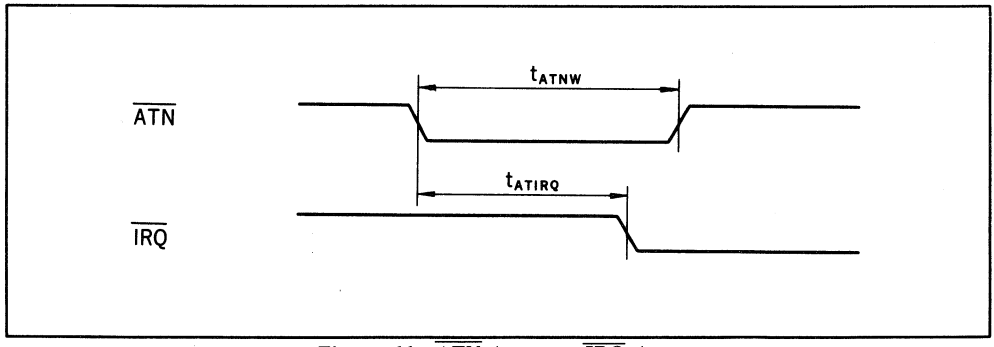
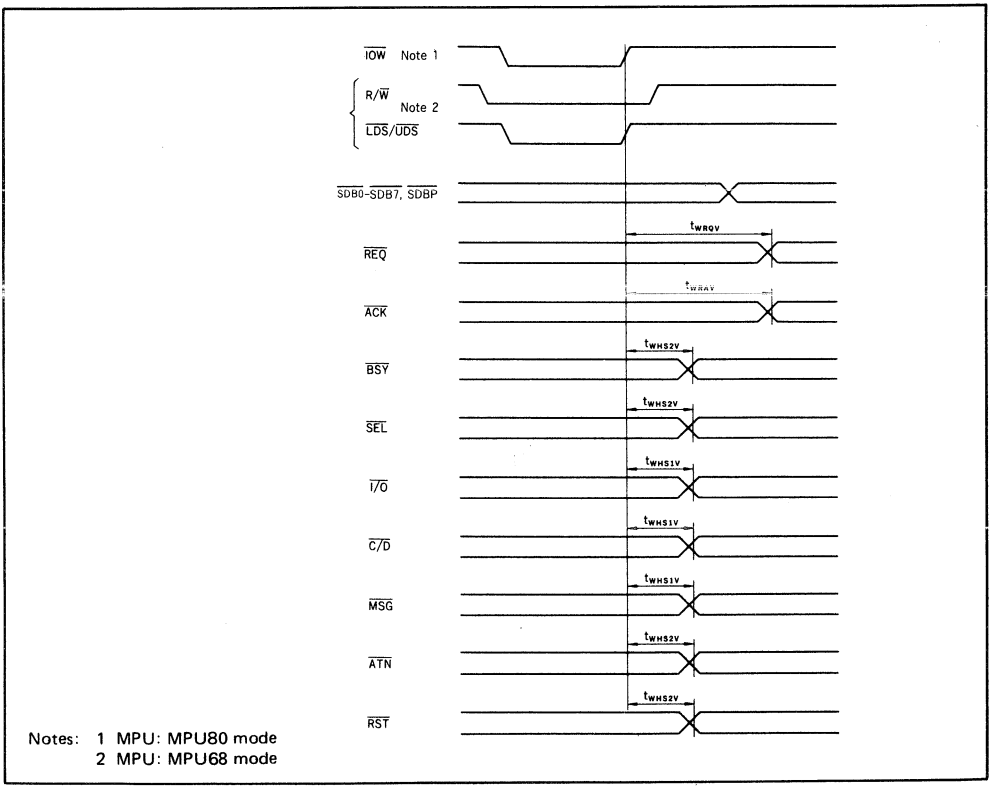


Figure 66. $\overline{ATN}$ Assert to $\overline{IRQ}$ Assert

SCSI Output Bus Timing

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{IOW}$ High to $\overline{REQ}$ Valid $\overline{LDS}/\overline{UDS}$ High to $\overline{REQ}$ Valid	t_{WRQV}	2.5 tcyc	–	3.5 tcyc +260	ns	Fig 67	Target mode
$\overline{IOW}$ High to $\overline{ACK}$ Valid $\overline{LDS}/\overline{UDS}$ High to $\overline{ACK}$ Valid	t_{WRAV8}	2.5 tcyc	–	3.5 tcyc +260	ns	Fig 67	Initiator mode 8-bit write
IOW, LDS/UDS High to $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$ Valid	t_{WHSIV}	1 tcyc	–	2 tcyc +280	ns	Fig 67	Target mode
$\overline{IOW}$, $\overline{LDS}/\overline{UDS}$ High to $\overline{BSY}$, $\overline{SEL}$, $\overline{RST}$, $\overline{ATN}$ Valid	t_{WHS2V8}	1 tcyc	–	2 tcyc +280	ns	Fig 67	8-bit write $\overline{ATN}$: Only Initiator mode

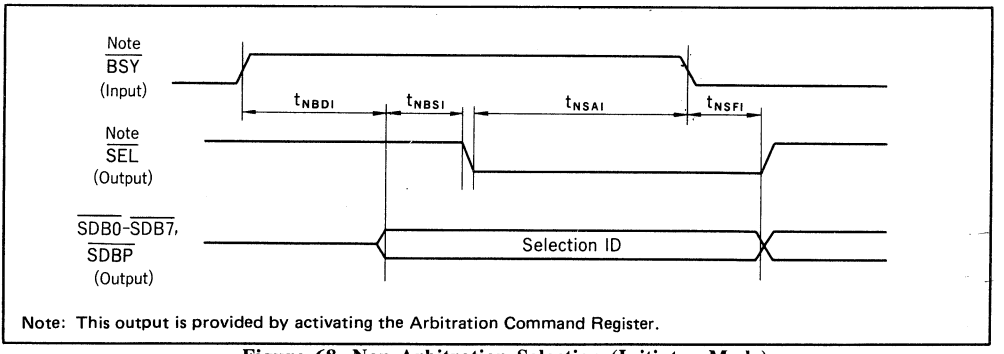


Notes: 1 MPU: MPU80 mode
2 MPU: MPU68 mode

Figure 67. SCSI Bus Output Timing

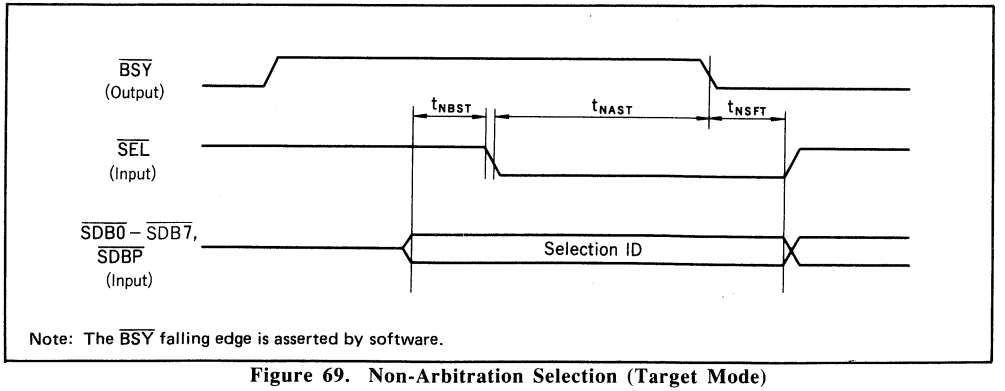
SCSI bus timing

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{BSY}$ High to $\overline{SDB0}$ – $\overline{SDB7}$, $\overline{SDBP}$ Valid	t_{NBDI}	L x tcyc	–	L x tcyc +200	ns	Fig 68	L: Bus Free Delay + Bus Settle Delay
$\overline{SDB0}$ – $\overline{SDB7}$, $\overline{SDBP}$ Valid to $\overline{SEL}$ Hold	t_{NBSI}	tcyc–20	–	–	ns		
$\overline{SEL}$ Low to $\overline{BSY}$ Low	t_{NSAI}	0.4	–	–	µs		
$\overline{BSY}$ Low to $\overline{SEL}$, $\overline{SDB0}$ – $\overline{SDB7}$, $\overline{SDBP}$ Valid	t_{NSFI}	20 x tcyc	–	60 x tcyc	ns		
$\overline{SDB0}$ – $\overline{SDBP7}$, $\overline{SDBP}$ Valid to $\overline{SEL}$ Low	t_{NBST}	90	–	–	ns	Fig 69	
$\overline{SEL}$ Low to $\overline{BSY}$ Low	t_{NSAT}	0.4	–	–	µs		
$\overline{BSY}$ Low to $\overline{SEL}$, $\overline{SDB0}$ – $\overline{SDB7}$, $\overline{SDBP}$ Valid	t_{NSFT}	0	–	–	ns		



Note: This output is provided by activating the Arbitration Command Register.

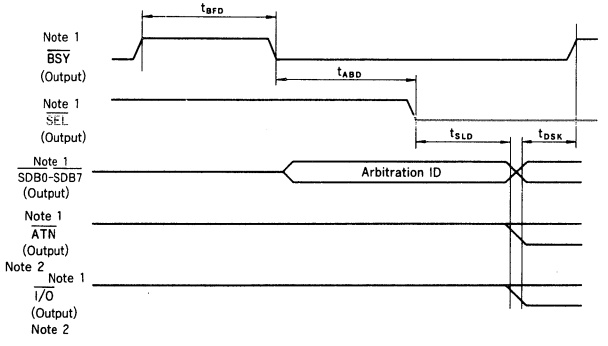
Figure 68. Non-Arbitration Selection (Initiator Mode)



Note: The $\overline{BSY}$ falling edge is asserted by software.

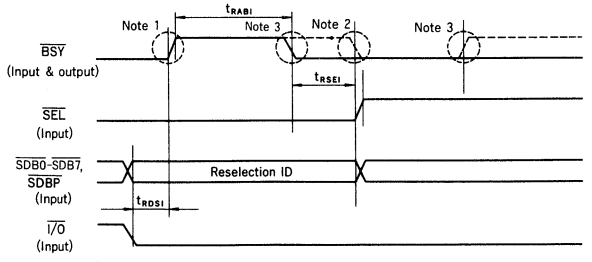
Figure 69. Non-Arbitration Selection (Target Mode)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{BSY}$ High to $\overline{BSY}$ Low	t_{BFD}	L x tcyc	—	L x tcyc +200	ns	Fig 70	L: Bus Settle Delay + Bus Free Delay
$\overline{BSY}$ Low to $\overline{SEL}$ Low	t_{ABD}	M x tcyc	—	M x tcyc + 200	ns		M: Arbitration Delay
$\overline{SEL}$ Low to $\overline{SDB0}$–$\overline{SDB7}$, $\overline{ATN}$, $\overline{I/O}$ Hold	t_{SLD}	N x tcyc − 200	—	N x tcyc + 200	ns		N: Selection Delay
$\overline{SDB0}$–$\overline{SDB7}$ Valid to $\overline{BSY}$ High	t_{DSK}	tcyc−25	—	tcyc + 150	ns		
$\overline{SDB0}$ – $\overline{SDB7}$ Valid to $\overline{BSY}$ High	t_{RDSI}	90	—	—	ns	Fig 71	
$\overline{BSY}$ High to $\overline{BSY}$ Low	t_{RABI}	0.4	—	–	µs		
$\overline{BSY}$ Low to $\overline{SEL}$, $\overline{SDB0}$ – $\overline{SDB7}$, $\overline{SDBP}$ Hold	t_{RSEI}	90	—	—	ns		



Notes: 1. During arbitration phase this output is provided by activating the Arbitration Command Register.
2. When the Target is in reselection phase, this output is provided.

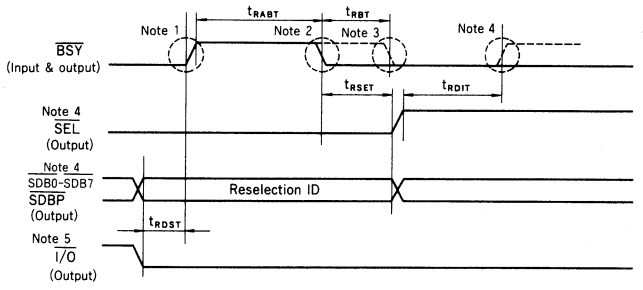
Figure 70. Arbitration Phase



Notes: 1. The rising edge of $\overline{BSY}$ signal is provided by the Target.
2. Target output
3. Initiator output (controlled by software)

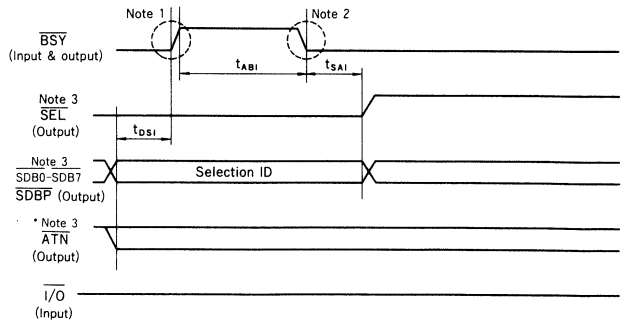
Figure 71. Reselection Phase (Initiator Mode)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
$\overline{SDB0}$–$\overline{SDB7}$ Valid, I/O Low to $\overline{BSY}$, Hold	t_{RDST}	tcyc–25	–	tcyc+50	ns	Fig 72
$\overline{BSY}$ High to $\overline{BSY}$ Low	t_{RABT}	0.4	–	–	µs	
$\overline{BSY}$ Low to TARG Asserts $\overline{BSY}$	t_{RBT}	15	–	50	tcyc	
$\overline{SEL}$ High to INIT Disasserts $\overline{BSY}$	t_{RDIT}	0	–	–	ns	
$\overline{BSY}$ Low to $\overline{SEL}$, $\overline{SDB0}$ – $\overline{SDB7}$, $\overline{SDBP}$ Hold	t_{RSET}	20	–	60	tcyc	
$\overline{SDB0}$ – $\overline{SDB7}$, $\overline{SDBP}$ Valid to $\overline{BSY}$ High	t_{DSI}	tcyc–20	–	–	ns	Fig 73
$\overline{BSY}$ High to $\overline{BSY}$ Low	t_{ABI}	0.4	–	–	µs	
$\overline{BSY}$ Low to $\overline{SEL}$, $\overline{SDB0}$–$\overline{SDB7}$, $\overline{SDBP}$ Hold	t_{SAI}	20	–	60	tcyc	



Notes: 1. The rising edge of $\overline{BSY}$ signal is output by the Target, provided by activating the arbitration command register.
2. The falling edge of $\overline{BSY}$ signal is output by the initiator.
3. Target output, provided by activating the arbitration command register.
4. Initiator output
5. During reselection phase, this output is provided by activation the arbitration command register.

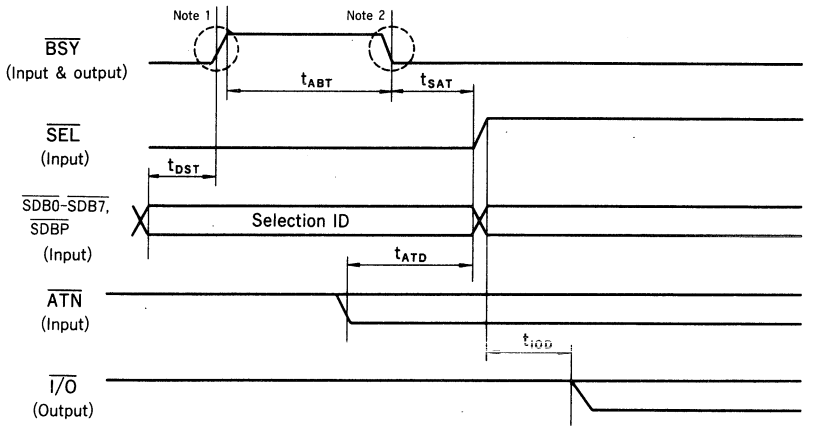
Figure 72. Reselection Phase (Target Mode)



Notes: 1. The rising edge of $\overline{BSY}$ signal is output by the initiator, provided by activating the arbitration command register.
2. The falling edge of $\overline{BSY}$ signal is output by the target.
3. During selection phase, this output is provided by activating the arbitration command register.

Figure 73. Selection Phase (Initiator Mode)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
$\overline{SDB0}$–$\overline{SDB7}$ Valid to $\overline{BSY}$ High	t_{DST}	90	—	—	ns	Fig 74
$\overline{BSY}$ High to $\overline{BSY}$ Low	t_{ABT}	0.4	—	—	µs	
$\overline{BSY}$ Low to $\overline{SEL}$ High $\overline{SDB0}$ to $\overline{SDB7}$, $\overline{SDBP}$ Valid	t_{SAT}	90	—	—	ns	
$\overline{ATN}$ Low to $\overline{SEL}$ Hold	t_{ATD}	0	—	—	ns	
$\overline{SEL}$ High to $\overline{I/O}$ Hold	t_{IOD}	0	—	—	ns	



Notes: 1. The rising edge of $\overline{BSY}$ signal is provided by the initiator.
2. The falling edge of $\overline{BSY}$ signal is provided by the target (controlled by software).

Figure 74. Selection Phase (Target)

General I/O LSI

HD63140

Universal Pulse Processor (UPP)

Description

The Hitachi HD63140 Universal Pulse Processor is a CMOS peripheral LSI consisting of four independent modules: The universal pulse processor core (UPC), 10-bit A/D converter, 1024-byte RAM, and watchdog timer.

The UPC functions as a programmable pulse I/O module with a 16-bit ALU. It can realize an effective pulse I/O system suitable for versatile applications owing to 16 bit pulse I/O terminals and 24 16-bit universal registers programmable as counter, shifter, compare or capture register. The UPC automatically performs complicated pulse control through the use of 15 commands, which sharply reduces the burden on the MPU. The HD63140 supports an asynchronous bus interface and is easily to connect to the HD6301X, HD6301Y, and HD68HC000 MPUs.

Features

- Universal Pulse Processor Core (UPC)
  - 15 commands for executing pulse I/O operation
  - Up to 16 functions are programmble from the MPU into the function table (RAM)
  - 24 16-bit universal registers (UDR)
  - 16 I/O terminals (8 internal registers for pulse I/O control are also provided)
  - Interrupts can occur at the falling or rising edge of all pulse signals
  - Pulse width resolution is 5 μs when executing 16 commands at 4 MHz operating frequency
- A/D Converter
  - 10-bit $\times$ 10 channels successive approximation A/D converter
  - Scanning operation for up to 4-channels of analog input
  - Interrupts can occur upon completion of conversion
- RAM
  - 1024-byte static RAM
- Watchdog Timer (WDT)
  - Overflow time is selected from 0.128 msec to 131 msec under 4 MHz operation frequency
- Low Power Dissipation
  - Low Power dissipation due to CMOS process
  - Standby mode is available

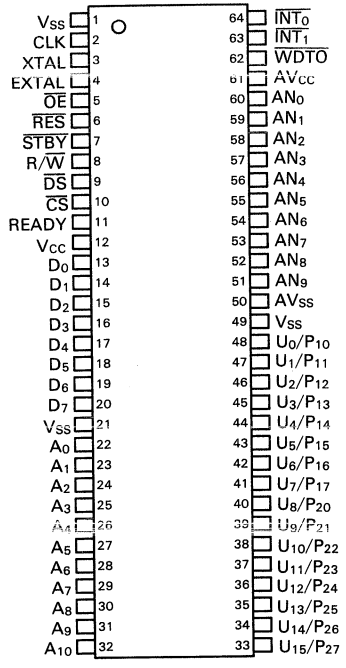
Ordering Information

Type No.	Max Operating Frequency	Clock Circuit	On-chip Clock Oscillator	External Clock Operation	Package
HD63140 A00 PS	4.0MHz*	Divide-by-4 Circuit	Yes	Available	64-pin plastic shrink DIP (DP-64S)
HD63140 B00 PS	4.0MHz**	Divide-by-2 Circuit	No	Available	64-pin plastic shrink DIP (DP-64S)
HD63140 A00 CP	4.0MHz*	Divide-by-4 Circuit	Yes	Available	68 pin PLCC (CP-68)
HD63140 B00 CP	4.0MHz**	Divide-by-2 Circuit	No	Available	68 pin PLCC (CP-68)

* 16MHz crystal or 16MHz external clock
** 8MHz external clock

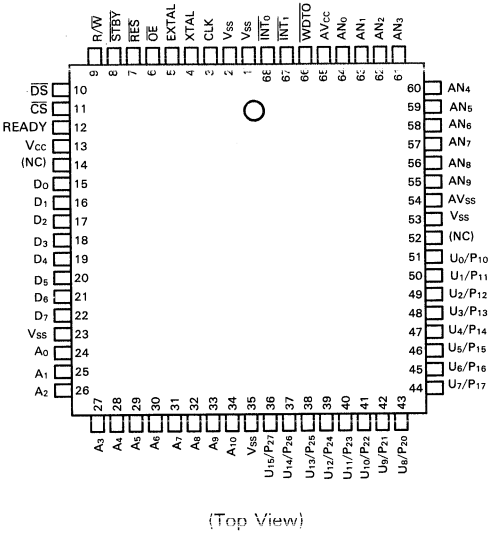
Pin Arrangement

1. 64-pin Plastic Shrink DIP



(Top View)

2. 68-pin PLCC



(Top View)

Note) NC: Non-connected pins; Nothing can be connected to NC pins.

Pin Description

Symbol	Pin No. DP-64S	Pin No. CP-68	Pin Name	I/O
Vcc	12	13	Vcc	I
Vss	1, 21, 49	1, 2, 23, 35, 53	Vss	I
AVcc	61	65	AVcc	I
AVss	50	54	AVss	I
XTAL	3	4	XTAL	I
EXTAL	4	5	EXTAL	I
CLK	2	3	Clock	O
$\overline{RES}$	6	7	Reset	I
$\overline{STBY}$	7	8	Standby	I
D_0-D_7	13-20	15-22	Data bus	I/O
A_0-A_{10}	22-32	24-34	Address bus	I
R/$\overline{W}$	8	9	Read/Write	I
$\overline{DS}$	9	10	Data strobe	I
$\overline{OE}$	5	6	Output enable	I
$\overline{CS}$	10	11	Chip select	I
READY	11	12	Ready	O
$\overline{INT_0}$	64	68	Interrupt 0	O (open drain)
$\overline{INT_1}$	63	67	Interrupt 1	O (open drain)
$\overline{WDTO}$	62	66	Watchdog Timer Out	O (open drain)
U_0/P_{10}-U_{15}/P_{27}	48-33	51-36	U_0/P_{10}~ U_{15}/P_{27}	I/O
AN_0-AN_9	60-51	64-55	Analog input	I

Pin Function

Power Supply

V_{CC}: Power supply pin (+5 V).

V_{SS}: Ground pin: Connect all Vss to ground.

AV_{CC}: Analog power supply pin for A/D converter (+5 V).

AV_{SS}: Ground pin for A/D converter; connect to ground together with V_{SS} (AVss = Vss = GND)

Clock

XTAL, EXTAL: A00: Connect to a crystal whose frequency is four times the operation frequency (16 MHz crystal for 4 MHz operation).

When using an external clock, its frequency should be four times the operation frequency (16 MHz clock for 4 MHz operation), and the XTAL pin must be disconnected.

B00: The frequency of the external clock should be two times that of the internal clock (8 MHz clock for 4 MHz operation), and the XTAL pin must be disconnected.

CLK: CLK outputs a clock signal whose frequency is twice the operation frequency (8 MHz clock for 4 MHz operation).

Reset

$\overline{RES}$: Low level input at $\overline{RES}$ initializes the LSI.

Standby

$\overline{STBY}$: Low level input at $\overline{STBY}$ stops the internal clocks and puts the LSI into standby mode; RAM's data is preserved and other circuits are reset.

MPU Interface

D_0-D_7: 8-bit bidirectional data bus.

A_0-A_{10}: Address input pins for specifying memory or registers.

R/$\overline{W}$: Controls data transfer direction between UPP and MPU. In general, R/$\overline{W}$ signal output from the MPU is connected to R/$\overline{W}$.

$\overline{DS}$: Read/write operation is performed during low level of $\overline{DS}$.

$\overline{OE}$: Controls D_0-D_7 outputs. D_0-D_7 are in high-impedance state during high level of $\overline{OE}$ even in the read cycle.

$\overline{CS}$: Read/write operations to/from memory or registers are performed during low level of $\overline{CS}$. In general, decoded signals for MPU upper addresses are input to $\overline{CS}$.

READY: Inserts a wait cycle for MPU. This is a three-state output. When accessing registers other than RAM, it enters the output state during low level of $\overline{CS}$. Except for this case, it is in high-impedance state.

$\overline{INT_0}$: Logical sum (OR) output of interrupt request registers IRR0-IRR15.

$\overline{INT_1}$: Logical sum (OR) output of interrupt request registers IRR16-IRR23 and interrupt request at the completion of A/D conversion.

WDT Output

$\overline{WDTO}$: Overflow output of watchdog timer.

UPP Input/Output

U_0/P_{10}-U_{15}/P_{27}: UPP pulse I/O pins. They can also be used as an MPU port according to the set data of the UPP contact enable register. Input level of U_0/P_{10}-U_7/P_{17} is TTL, and U_8/P_{20}-U_{15}/P_{27} are Schmitt-trigger inputs.

Analog Input

AN_0-AN_9: Analog input pins for 10-channel A/D converter.

Command Table

Commands		Functions
Counter/Timer, Pulse Input Functions	FRS	Free-Running Counter/Timer with Sampling
		Performs free-running counts and captures the counter at the rising or falling edge of the specified signal.
	INS	Interval Counter/Timer with Sampling
		Counter is captured and reset at the rising or falling edge of the specified signal. (Measures pulse cycle.)
	UDS	Up-Down Counter/Timer with Sampling
		Counter counts upward or downward according to the count direction specification signal, and is captured at the rising or falling edge of the specified signal.
	GTS	Gated Counter/Timer with Sampling
		Clock signal of counter is gated by the specified signal, and the counter is captured and reset at the rising or falling edge of the gate signal.
Counter/Timer, Pulse Output Functions	FRC	Free-Running Counter/Timer witn Compare
		Performs free-running counts, and outputs the result of comparison between compare register data and counter.
	INC	Interval Counter/Timer with Compare
		If counter is the same as the compare register data, pulse is output and counter is reset. (Outputs synchronous pulse.)
	PWC	Pulse Width Counter/Timer with Compare
		Result of comparison between compare register data and counter is output while counter is counting. Counter is reset at the rising or falling edge of the specified signal.
	OSC	One Shot Counter/Timer with Compare
		Counter continuously outputs one-shot pulses from the specified edge of the specified signal until the counter becomes equal to the compare register data.
Special Counter/ Timer Functions	FFC	Fifty-Fifty Duty Cycle Counter/Timer with Compare
		Outputs 50% duty cycle pulse.
	TPC	Two Phase Up-Down Counter
		Increments or decrements counter according to the relation between two-phase pulse signals.
	GTC	Gated Counter/Timer with Compare
		The counter clock signal is gated by the specified signal, and the result of the comparison between compare register data and counter is output. Counter is reset at the specified edge of the gate signal. (Compares pulse width.)
	CTO	Combination Trigger One Shot Counter/Timer
		Counter continuously outputs one-shot pulses, ANDing trigger signal and enable signal until the counter becomes equal to the compare register data.
Shifter and Pulse I/O Functions	SIT	Shift Input
		Input signal is shifted and latched at the specified edge of the specified signal.
	SOT	Shift Output
		Outputs reloaded data, shifting or rotating it. (Outputs scan signal.)
	SPO	Shift Parallel Output
		Outputs reloaded data in parallel, shifting or rotating it.

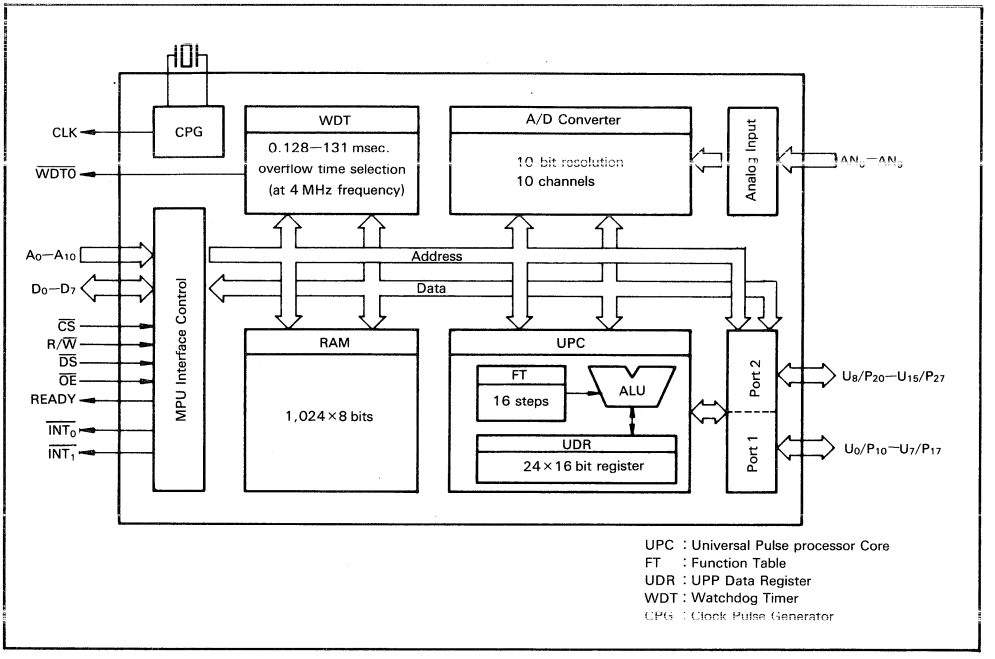
Internal Registers

Address (HEX)	Register Name	Symbol	R/W	Bit 7	6	5	4	3	2	1	0	Reset Data
000	Data Direction Register 2	DDR2	W									00
001	Data Direction Register 1	DDR1	W									00
002	Port 2 Data Register	PORT2	R/W									*
003	Port 1 Data Register	PORT1	R/W									*
005	Watchdog Timer Register	WDTR	R/W	OVF	WOE	—	MOD	—	OVC2	OVC1	OVC0	08
006	A/D Control and Status Register	ADCSR	R/W	ADEND	ADIE	ADST	SCAN	CH3	CH2	CH1	CH0	00
007	A/D Data Register 0 (H)	ADDR0	R/W	(MSB)								*
008	A/D Data Register 0 (L)	ADDR0	R/W		(LSB)	—	—	—	—	—	—	*
009	A/D Data Register 1 (H)	ADDR1	R/W	(MSB)								*
00A	A/D Data Register 1 (L)	ADDR1	R/W		(LSB)	—	—	—	—	—	—	*
00B	A/D Data Register 2 (H)	ADDR2	R/W	(MSB)								*
00C	A/D Data Register 2 (L)	ADDR2	R/W		(LSB)	—	—	—	—	—	—	*
00D	A/D Data Register 3 (H)	ADDR3	R/W	(MSB)								*
00E	A/D Data Register 3 (L)	ADDR3	R/W		(LSB)	—	—	—	—	—	—	*
00F	RAM Control Register	RAMCR	R/W	RAME	—	—	—	—	—	—	—	FF
010	UPP Contact Enable Register 2	UCER2	W	UCE15	UCE14	UCE13	UCE12	UCE11	UCE10	UCE9	UCE8	00
011	UPP Contact Enable Register 1	UCER1	W	UCE7	UCE6	UCE5	UCE4	UCE3	UCE2	UCE1	UCE0	00
012	UPP Output Register 2	UOR2	W	U15	U14	U13	U12	U11	U10	U9	U8	*
013	UPP Output Register 1	UOR1	W	U7	U6	U5	U4	U3	U2	U1	U0	*
014	Next Data Enable Register	NDER	W									00
016	Next Data Register	NDR	W									*
020	UPP System Control Register	USCR	R/W	TST	TST	TST	TST	—	TST	GFE	UROME	08
021	Maximum Function Number Register	MFNR	R/W	—	—	—	MFN4	MFN3	MFN2	MFN1	MFN0	*
022	Function Number Register	FNR	R/W	—	—	—	FN4	FN3	FN2	FN1	FN0	*
023	Command Register	CMR	R/W	CMD3	CMD2	CMD1	CMD0	OM3	OM2	OM1	OM0	*
024	Register Assignment Register A	RASRA	R/W	—	—	—	CTN4	CTN3	CTN2	CTN1	CTN0	*
025	Register Assignment Register B	RASRB	R/W	—	—	—	CCN4	CCN3	CCN2	CCN1	CCN0	*
026	I/O Assignment Register A	IOARA	R/W	—	FEDGA	FEDGA	CPN4	CPN3	CPN2	CPN1	CPN0	*
027	I/O Assignment Register B	IOARB	R/W	—	FEDGB	FEDGB	SPN4	SPN3	CPN2	SPN1	SPN0	*
028	I/O Assignment Register C	IOARC	R/W	—	—	—	LPNA4	LPNA3	LPNA2	LPNA1	LPNA0	*
029	I/O Assignment Register D	IOARD	R/W	—	—	—	LPNB4	LPNB3	LPNB2	LPNB1	LPNB0	*
02A	Interrupt Enable Register 3	IER3	R/W	IRE23	IRE22	IRE21	IRE20	IRE19	IRE18	IRE17	IRE16	00
02B	Interrupt Enable Register 2	IER2	R/W	IRE15	IRE14	IRE13	IRE12	IRE11	IRE10	IRE9	IRE8	00
02C	Interrupt Enable Register 1	IER1	R/W	IRE7	IRE6	IRE5	IRE4	IRE2	IRE2	IRE1	IRE0	00
02D	Interrupt Request Register 3	IRQR3	R	IRR23	IRR22	IRR21	IRR20	IRR19	IRR18	IRR17	IRR16	00
02E	Interrupt Request Register 2	IRQR2	R	IRR15	IRR14	IRR13	IRR12	IRR11	IRR10	IRR9	IRR8	00
02F	Interrupt Request Register 1	IRQR1	R	IRR7	IRR6	IRR5	IRR4	IRR3	IRR2	IRR1	IRR0	00
030	Interrupt Status Register 3	ISR3	R	IRS23	IRS22	IRS21	IRS20	IRS19	IRS18	IRS17	IRS16	00
031	Interrupt Status Register 2	ISR2	R	IRS15	IRS14	IRS13	IRS12	IRS11	IRS10	IRS9	IRS8	00
032	Interrupt Status Register 1	ISR1	R	IRS7	IRS6	IRS5	IRS4	IRS3	IRS2	IRS1	IRS0	00
033	Interrupt Status Clear Register 3	ISCR3	W	IRSC23	IRSC22	IRSC21	IRSC20	IRSC19	IRSC18	IRSC17	IRSC16	00
034	Interrupt Status Clear Register 2	ISCR2	W	IRSC15	IRSC14	IRSC13	IRSC12	IRSC11	IRSC10	IRSC9	IRSC8	00
035	Interrupt Status Clear Register 1	ISCR1	W	IRSC7	IRSC6	IRSC5	IRSC4	IRSC3	IRSC2	IRSC1	IRSC0	00
036	UPP I/O Register	UIOR	R/W	U23	U22	U21	U20	U19	U18	U17	U16	*
040	UPP Data Register 0 (H)	UDR0	R/W									*
041	UPP Data Register 0 (L)	UDR0	R/W									*
042	UPP Data Register 1 (H)	UDR1	R/W									*
043	UPP Data Register 1 (L)	UDR1	R/W									*
044	UPP Data Register 2 (H)	UDR2	R/W									*
045	UPP Data Register 2 (L)	UDR2	R/W									*
046	UPP Data Register 3 (H)	UDR3	R/W									*

: Function table
* : Undetermined
Note : Reset data of not-used bit is described "1" (which is equal to read data) in this table. Read data of write-only bits is different from reset data described in this table.

Address (HEX)	Register Name	Symbol	R/W	Bit 7	6	5	4	3	2	1	0	Reset Data
047	UPP Data Register 3 (L)	UDR3	R/W									*
048	UPP Data Register 4 (H)	UDR4	R/W									*
049	UPP Data Register 4 (L)	UDR4	R/W									*
04A	UPP Data Register 5 (H)	UDR5	R/W									*
04B	UPP Data Register 5 (L)	UDR5	R/W									*
04C	UPP Data Register 6 (H)	UDR6	R/W									*
04D	UPP Data Register 6 (L)	UDR6	R/W									*
04E	UPP Data Register 7 (H)	UDR7	R/W									*
04F	UPP Data Register 7 (L)	UDR7	R/W									*
050	UPP Data Register 8 (H)	UDR8	R/W									*
051	UPP Data Register 8 (L)	UDR8	R/W									*
052	UPP Data Register 9 (H)	UDR9	R/W									*
053	UPP Data Register 9 (L)	UDR9	R/W									*
054	UPP Data Register 10 (H)	UDR10	R/W									*
055	UPP Data Register 10 (L)	UDR10	R/W									*
056	UPP Data Register 11 (H)	UDR11	R/W									*
057	UPP Data Register 11 (L)	UDR11	R/W									*
058	UPP Data Register 12 (H)	UDR12	R/W									*
059	UPP Data Register 12 (L)	UDR12	R/W									*
05A	UPP Data Register 13 (H)	UDR13	R/W									*
05B	UPP Data Register 13 (L)	UDR13	R/W									*
05C	UPP Data Register 14 (H)	UDR14	R/W									*
05D	UPP Data Register 14 (L)	UDR14	R/W									*
05E	UPP Data Register 15 (H)	UDR15	R/W									*
05F	UPP Data Register 15 (L)	UDR15	R/W									*
060	UPP Data Register 16 (H)	UDR16	R/W									*
061	UPP Data Register 16 (L)	UDR16	R/W									*
062	UPP Data Register 17 (H)	UDR17	R/W									*
063	UPP Data Register 17 (L)	UDR17	R/W									*
064	UPP Data Register 18 (H)	UDR18	R/W									*
065	UPP Data Register 18 (L)	UDR18	R/W									*
066	UPP Data Register 19 (H)	UDR19	R/W									*
067	UPP Data Register 19 (L)	UDR19	R/W									*
068	UPP Data Register 20 (H)	UDR20	R/W									*
069	UPP Data Register 20 (L)	UDR20	R/W									*
06A	UPP Data Register 21 (H)	UDR21	R/W									*
06B	UPP Data Register 21 (L)	UDR21	R/W									*
06C	UPP Data Register 22 (H)	UDR22	R/W									*
06D	UPP Data Register 22 (L)	UDR22	R/W									*
06E	UPP Data Register 23 (H)	UDR23	R/W									*
06F	UPP Data Register 23 (L)	UDR23	R/W									*
400 ↓ 7FF	RAM		R/W									*

Internal Block Diagram



Universal Pulse Processor Core (UPC)

Figure 1 shows a block diagram of the UPC. The functions stored in the function table ① are sequentially read by the function number register (FNR), which has a counting function. The UPP control unit ② interprets and executes these functions by controlling the execution unit ③ (consisting of UPP data registers and an ALU) and pulse I/O ④.
HD63140 has a RAM for use as a function table. RAM must be selected by the UPP system control register. The MPU's user program can write functions to the RAM. In addition, read/write to and from all registers in UPC can be performed from the MPU, to monitor the UPC operating condition.
The number of UPP pulse inputs and outputs is 24 (U_0 to U_{23}). Among these, U_0 to U_{15} possess UPP output registers 1 and 2, and pulses can be input and output from external terminals U_0/P_{10} to U_{15}/P_{27}. U_{16} to U_{23} have no input/output terminals, and are only input/output to the internal UPP I/O registers.

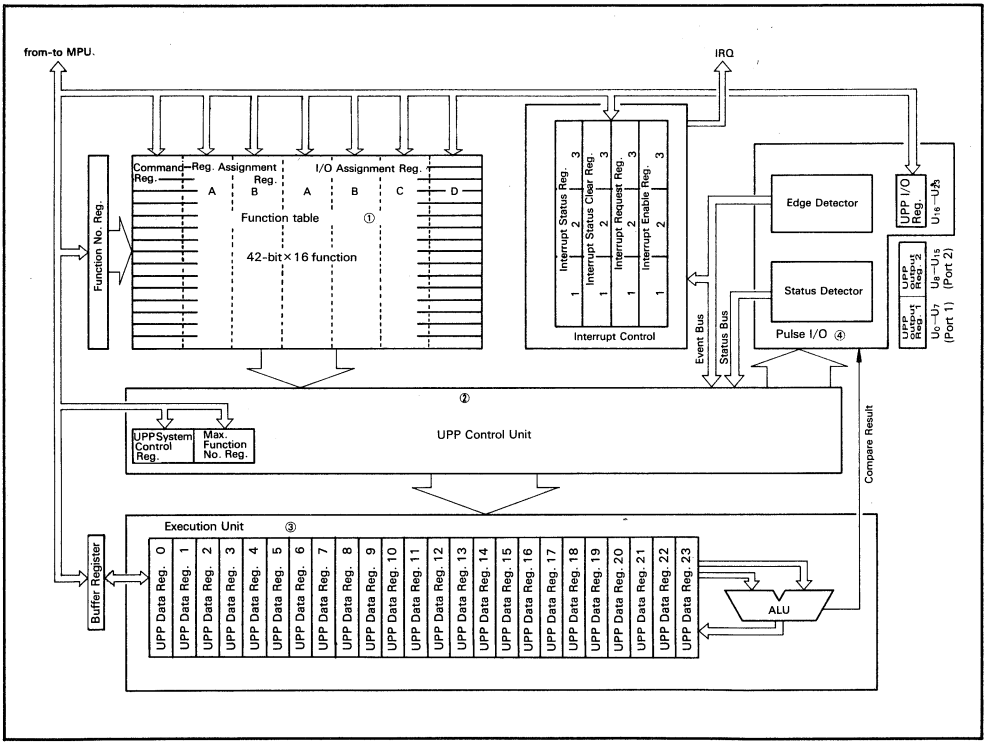


Figure 1. UPC Block Diagram

A/D Converter

Figure 2 shows a block diagram of the UPP's built-in 10-bit succesive approximation A/D converter. It has 10 input channels. The input level of the channel selected by the multiplexer is compared with the output of the 10-bit D/A converter shown. The result is converted bit by bit from the upper bit and fed back to the compare register. When a 10-bit converted result is finally obtained in the compare data registers, this data is output to the A/D data register. Since a scanner is incoporated in the channel selecting circuit of this A/D converter, a maximum of four channels can be scanned, depending on the conditions set in the A/D status and control register. The conversion rate is 42 μs/channel in either single mode or scan mode.

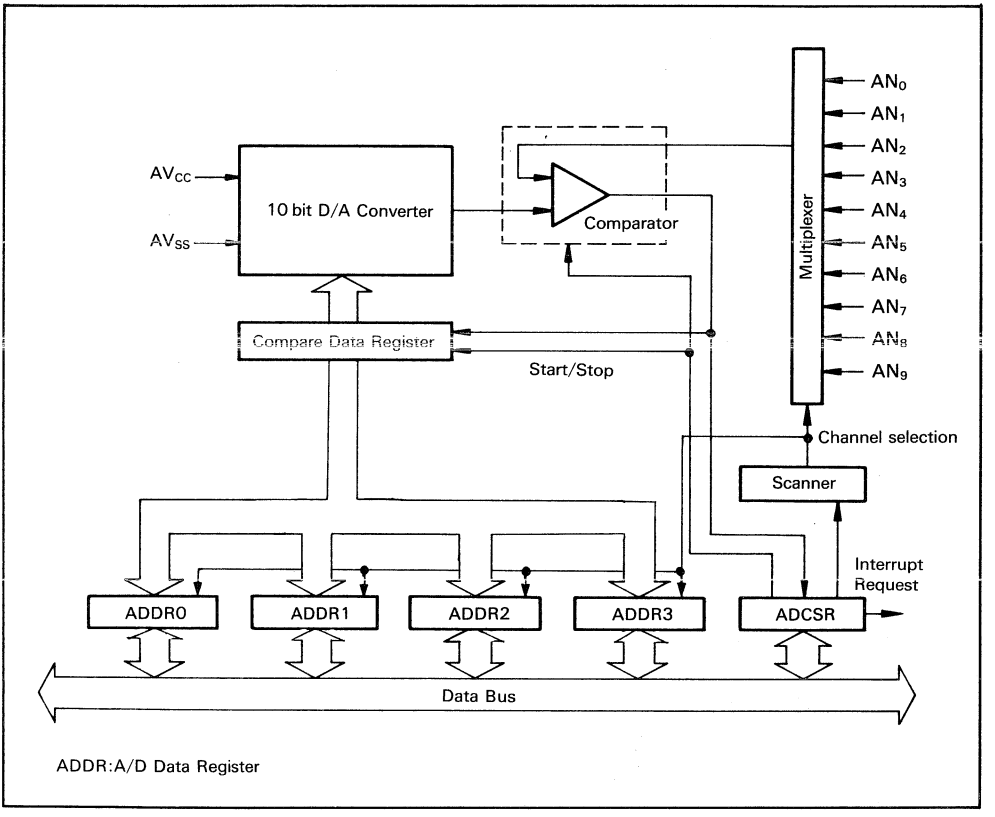


Figure 2. A/D Converter Block Diagram

Watchdog Timer (WDT)

The watchdog timer consists of a 10-bit prescaler, 8-bit counter, and watchdog timer register (WDTR) as shown in figure 3. The prescaler counts 2 MHz internal clock pulses (4 MHz operation), and outputs the carry to the 8-bit counter. The dividing rate of the prescaler can be specified in 7 steps from 0.128 to 131 ms according to the specified value of the WDTR. The 10-bit prescaler cannot be accessed from external circuits; however, the 8-bit counter can be reset during counting. Usually, this counter is periodically reset by the MPU to prevent overflow. If the 8-bit counter overflows, overflow flag (OVF) of WDTR is set and a low pulse is output for approximately 8.5 μs (4 MHz operation) to the $\overline{\text{WDTO}}$ pin. Accordingly, if this pin is connected to the reset pin of the MPU, the MPU can be reset when it doesn't reset the counter for some reasons like malfunctions. When this timer is used as an interval timer, OVF's inverse signal can be directly output to $\overline{\text{WDTO}}$, specified by WDTR. In this case, when the timer overflows, $\overline{\text{WDTO}}$ holds its output low until OVF is cleared by the MPU reading WDTR.

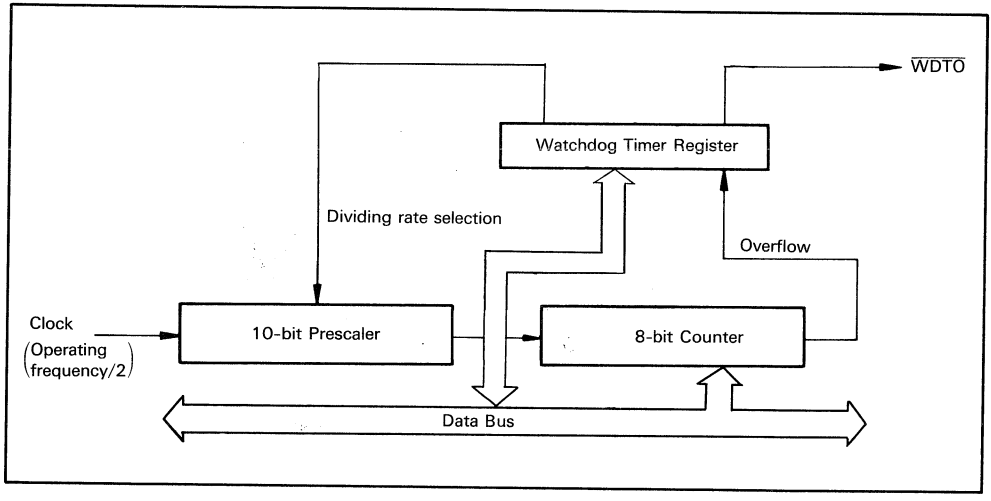


Figure 3. Watchdog Timer Block Diagram

System Block Example

An example of system is shown in figure 4.

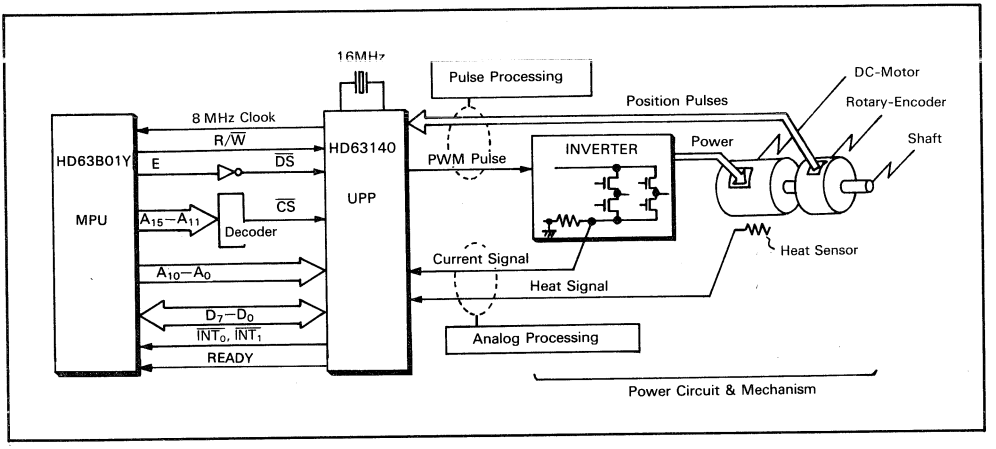


Figure 4. System Block Diagram

UPC, Port 1, and Port 2 Internal Registers

UPP Control Circuit

Maximum Function Number Register (MFNR)

Bit 7	6	5	4	3	2	1	0
–	–	–	MFN4	MFN3	MFN2	MFN1	MFN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 021

Bits 7-5 : Not used

MFN4-MFN0 (Maximum function number): MFN4-MFN0 bits specify the maximum value of the function number register (FNR) which is incremented from 0 during UPC operation. The number of functions to be executed and pulse width resolution are determined by specified values. The relationship between specified values and the number of functions to be executed is shown in table 1. The pulse width resoltion at 4 MHz operation is:

$$(\text{MFNR}) \times \frac{1}{\text{Operating frequency (MHz)}} = (\text{MFNR}) \times 0.25\ \mu\text{s}$$

When MFNR is 0, however, the resolution is 8 μs

Table 1. MFNR and Number of Functions to be Executed

MFNR Value (MFNR)	MFN4	MFN3	MFN2	MFN1	MFN0	Number of Functions to be Executed
0	0	0	0	0	0	16
1	0	0	0	0	1	0
2	0	0	0	1	0	1
3	0	0	0	1	1	2
4	0	0	1	0	0	3
5	0	0	1	0	1	4
6	0	0	1	1	0	4
7	0	0	1	1	1	5
8	0	1	0	0	0	6
9	0	1	0	0	1	7
10	0	1	0	1	0	8
11	0	1	0	1	1	8
12	0	1	1	0	0	9
13	0	1	1	0	1	10
14	0	1	1	1	0	11
15	0	1	1	1	1	12
16	1	0	0	0	0	12
17	1	0	0	0	1	13
18	1	0	0	1	0	14
19	1	0	0	1	1	15
20	1	0	1	0	0	16
21	1	0	1	0	1	16
22	1	0	1	1	0	16
23	1	0	1	1	1	16
24	1	1	0	0	0	16
25	1	1	0	0	1	16
26	1	1	0	1	0	16
27	1	1	0	1	1	16
28	1	1	1	0	0	16
29	1	1	1	0	1	16
30	1	1	1	1	0	16
31	1	1	1	1	1	16

Function Number Register (FNR)

Bit 7	6	5	4	3	2	1	0
–	–	–	FN4	FN3	FN2	FN1	FN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 022

Bits 7-5 : Not used

FN4-FN0 (Function number): Function number register (FNR) selects functions from the function table like a program counter. During UPC operation, the FNR is automatically incremented and functions stored in the function table are read and executed sequentially. Note that FNR = 0, 5, 10, or 15 indicates cycles for the MPU to read or write the UPP data register; no functions are executed during these cycles. FNR is reset if its value becomes equal to that specified by MFNR. FNR cannot be accessed by the MPU during UPC operation, but can be when the UPC stops operation. Function numbers from 1 to 4, 6 to 9, 11 to 14, or 16 to 19 are to be specified in this register when programming functions. "UPC operation" means the state in which the GFE bit of the UPP system control register (USCR) is equal to 1.
UPC operation is started from the same FNR value as it has when a 1 is written into the GFE bit. For example, if the data of FNR when a 1 is written into the GFE bit is egual to 1, UPC operation is started from FNR = 1.

UPP System Control Register (USCR)

Bit 7	6	5	4	3	2	1	0
TST	TST	TST	TST	–	TST	GFE	UROME
W	W	W	W		R/W	R/W	R/W

Address: $ 020

TST (Test): Test bits (bit 7-bit 4) are for testing, and cannot be used for user applications; clear to 0s when setting USCR.

Bit 3: Not used

TST (Test): Test bit (bit 2) is also for testing only; clear to 0 when setting USCR.

GFE (General function enable): The UPC is in operation and executes functions when GFE = 1, and is stopped when GFE = 0. This bit is cleared by reset.

UROME (UPP ROM enable): RAM is selected as the function table when UROME = 0, and mask ROM when UROME = 1. This bit is cleared by reset.
Clear to 0 (select RAM) when setting USCR because mask ROM isn't supported.

Function Table

As shown in figure 5, the HD63140 has a RAM as a function table, and the function table consists of a command register (CMR), two blocks of register assignment registers (RASRA, RASRB), and four blocks of I/O assignment registers (IOARA, IOARB, IOARC, IOARD). Each register has 16 registers corresponding to function numbers. First, the registers in the vertical column are selected by setting numbers in FNR; next, the registers in the horizontal column are selected by address inputs. RAM function programming is enabled only when GFE is equal to 0; that is, the UPC is not in operation. (Do not set functions when UPC is in operation.) In this case, values greater than those set in FNR, or 0, must be set in MFNR.

Command Register (CMR):

Bit 7	6	5	4	3	2	1	0
CMD3	CMD2	CMD1	CMD0	OM3	OM2	OM1	OM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 023

CMD3-CMD0 (Command code): CMD3-CMD0 bits specify the command code. Refer to "UPP Commands" for each command description. Also, refer to notes on UPP command setting (1).

OM3-OM0 (Operation mode): OM3-OM0 bits specify the command contents in detail. Refer to "UPP Commands" for details.

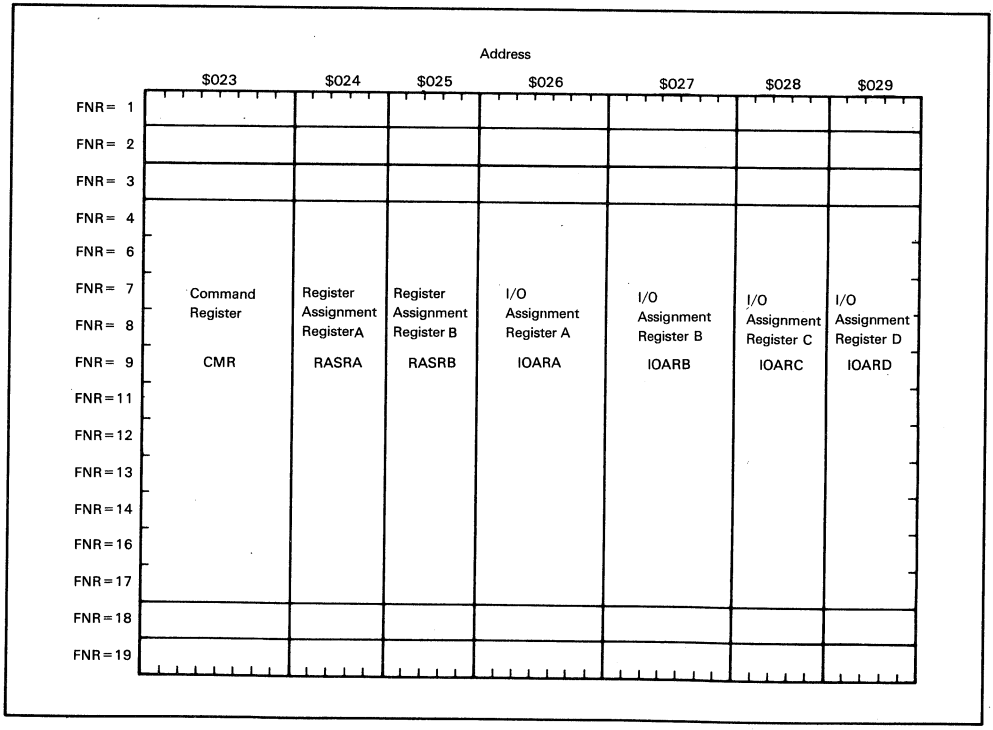


Figure 5. Function Table Configuration

Register Assignment Register A (RASRA)

Bit 7	6	5	4	3	2	1	0
–	–	–	CTN4	CTN3	CTN2	CTN1	CTN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 024

Bits 7-5 : Not used

CTN4-CTN0 (Counter/timer/shifter no.): CTN4-CTN0 bits specify the number of UPP data register (UDR) (0 to 23) to be used as a counter, timer, or shifter in each function. (A counter counts clocks specified by the I/O assignment register, and a timer counts internal clocks of periodic cycle.) The same register can be specified by other functions.

Register Assignment Register B (RASRB)

Bit 7	6	5	4	3	2	1	0
–	–	–	CCN4	CCN3	CCN2	CCN1	CCN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 025

Bits 7-5 : Not used

CCN4-CCN0 (Capture/compare/reload register no.): CCN4-CCN0 bits specify the UDR number to be used as a capture register, compare register, or data register (shift command) in each function. The register numbers are 0 to 23; however, 24 to 31 are set if these registers are not used. The same register can be specified by other functions. (A register, for example, which is specified as a counter by one function, can be specified as a compare register by another function.)

I/O Assignment Register A (IOARA):

This register specifies the clock input pin number as well as the edge direction to define the external clock for a shifter or counter specified by RASRA. This register data is ignored in shift mode by an internal clock and timer mode.

Bit 7	6	5	4	3	2	1	0
–	FEDGA	REDGA	CPN4	CPN3	CPN2	CPN1	CPN0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 026

Bit 7: Not used

FEDGA (Falling edge A): When FEDGA bit is 1, counting or shifting is performed on the falling edge of the signal specified by CPN4-CPN0.

REDGA (Rising edge A): When REDGA bit is 1, counting or shifting is performed on the rising edge of the signal specified by CPN4-CPN0.

When FEDGA and REDGA are both 1, counting or shifting is performed at both edges. When FEDGA and REDGA are both 0, counting or shifting is not performed even if the function is executed.

CPN4-CPN0 (Clock/Shift clock Pin No.): CPN4-CPN0 bits specify the input pin number (0 to 23) of the clock signal for counter or shifter. (No external input/output pins are provided on 16 to 23. The bits of the UPP I/O register, which is one of internal registers, correspond to 16 to 23.)

I/O Assignment Register B (IOARB): This register specifies the pulse input pin number as well as the edge direction for defining sampling pulse, trigger pulse, reset pulse, and data set pulse for the shifter.

Bit 7	6	5	4	3	2	1	0
–	FEDGB	REDGB	SPN4	SPN3	SPN2	SPN1	SPN0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 027

Bit 7: Not used

FEDGB (Falling edge B): When this bit is 1, sampling, triggering, resetting, or setting is performed on the falling edge of the signal specified by SPN4-SPN0.

REDGB (Rising edge B): When this bit is 1, sampling, triggering, resetting, or setting is performed on the rising edge of the signal specified by SPN4-SPN0.

When FEDGB and REDGB are both 1, the above operation is performed at both edges. When they are both 0, the operation is not performed.

SPN4-SPN0 (Sampling/trigger/reset/set pin no.): SPN4-SPN0 bits specify the input pin number (0 to 23)* of the sampling pulse for a capture register, trigger pulse for one-shot pulse output, reset pulse for counter, set pulse for shifter, one pulse signal for two-phase pulse counting, and gate signal.

I/O Assignment Register C (IOARC)

Bit 7	6	5	4	3	2	1	0
–	–	–	LPNA4	LPNA3	LPNA2	LPNA1	LPNA0
			R/W	R/W	R/W	R/W	R/W

Address: $ 028

Bits 7-5 : Not used

LPNA4-LPNA0 (Level pin no. A): LPNA4-LPNA0 bits specify the pulse output pin number (0 to 23).* When no pulses are output, 24 to 31 are specified.
For the TPC and SPO commands, refer to "UPP Commands" in this data sheet.

I/O Assignment Register D (IOARD)

Bit 7	6	5	4	3	2	1	0
–	–	–	LPNB4	LPNB3	LPNB2	LPNB1	LPNB0
			R/W	R/W	R/W	R/W	R/W

Address: $ 029

Bits 7-5 : Not used

LPNB4-LPNB0 (Level pin no. B): LPNB4-LPNB0 bits specify the pulse input pin number (0 to 23)* of direction setting signal for the counter or shiter, the input pin number of gate signal or tigger enable signal, and the input pin number of one pulse signal for two-phase pulse counting.

* No external input/output pins are provided on 16 to 23. The bits of the UPP I/O register, which is one of internal registers, correspond to 16 to 23.

UPP Data Registers 0-23 (UDR0-UDR23)

UDR, consisting of twenty-four 16-bit registers, can function as counter/timer, shifter, capture, or compare registers according to function settings.

The same register can be specified as referred by several functions.

UDR is accessible by the MPU while both executing functions and suspended via a 16-bit buffer register.

When a MPU write a data to the address of the UDR upper byte, the data is written into the upper byte of the buffer register. When it continuously write a data to the address of the UDR lower byte, the data is written into the lower byte of the buffer register and all the 16 bits data of the buffer register is transferred to the UDR at the same time.

During a read cycle, the reverse operation is performed. When a MPU read the UDR upper byte, all the 16 bits data of the UDR is transferred to the buffer register and then the data in the upper byte of the buffer register is read. When it continuously read the UDR lower byte, the data in the lower byte of the buffer register is read.

In this way, UDR should be read or written in the order of upper byte first and lower byte second.

Address: $40 - $06F

I/O Port

HD63140 has sixteen I/O pins (U_0/P_{10}-U_7/P_{17}, U_8/P_{20}-U_{15}/P_{27}) and an 8-bit UPP I/O register (UIOR) for pulse input and output. As shown in figure 6, these I/O pins are connected with UPP output registers (UOR1, UOR2), port data registers (Port1, Port2), UPP contact enable registers (UCER1, UCER2), and data direction registers (DDR1, DDR2). These pins can also be used as an MPU I/O port. In addition, U_8/P_{20} to U_{15}/P_{27} are connected with next data register (NDR) and next data enable register (NDER), and data set in NDR can be output at a certain timing. UIOR can be used when external output is not necessary like when using the output of one function as input for another function.

The block structure of the registers is shown in figure 7.

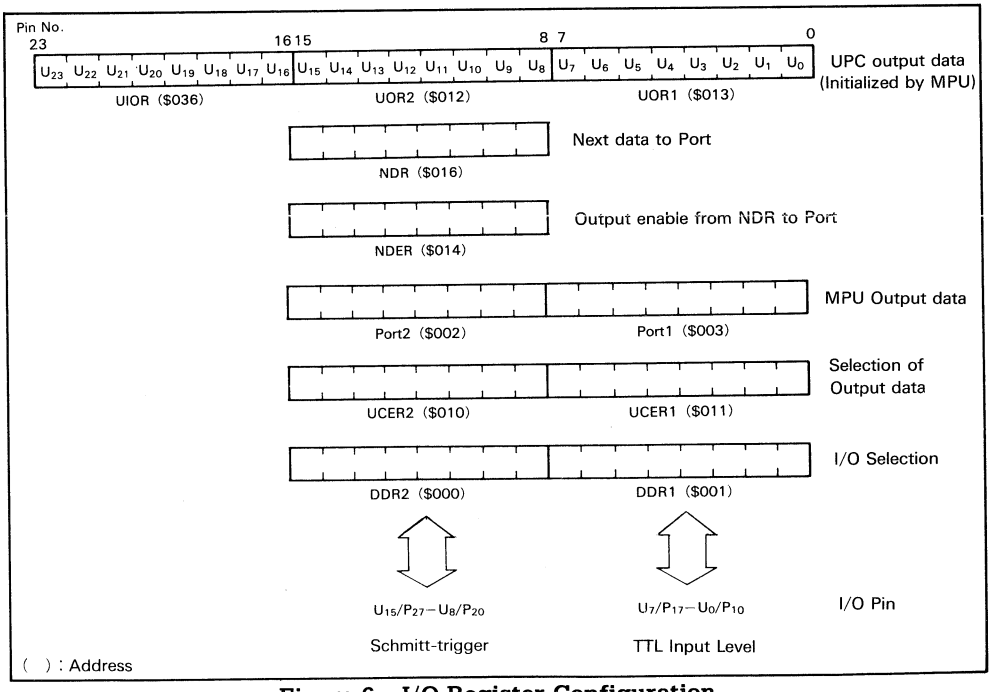


Figure 6. I/O Register Configuration

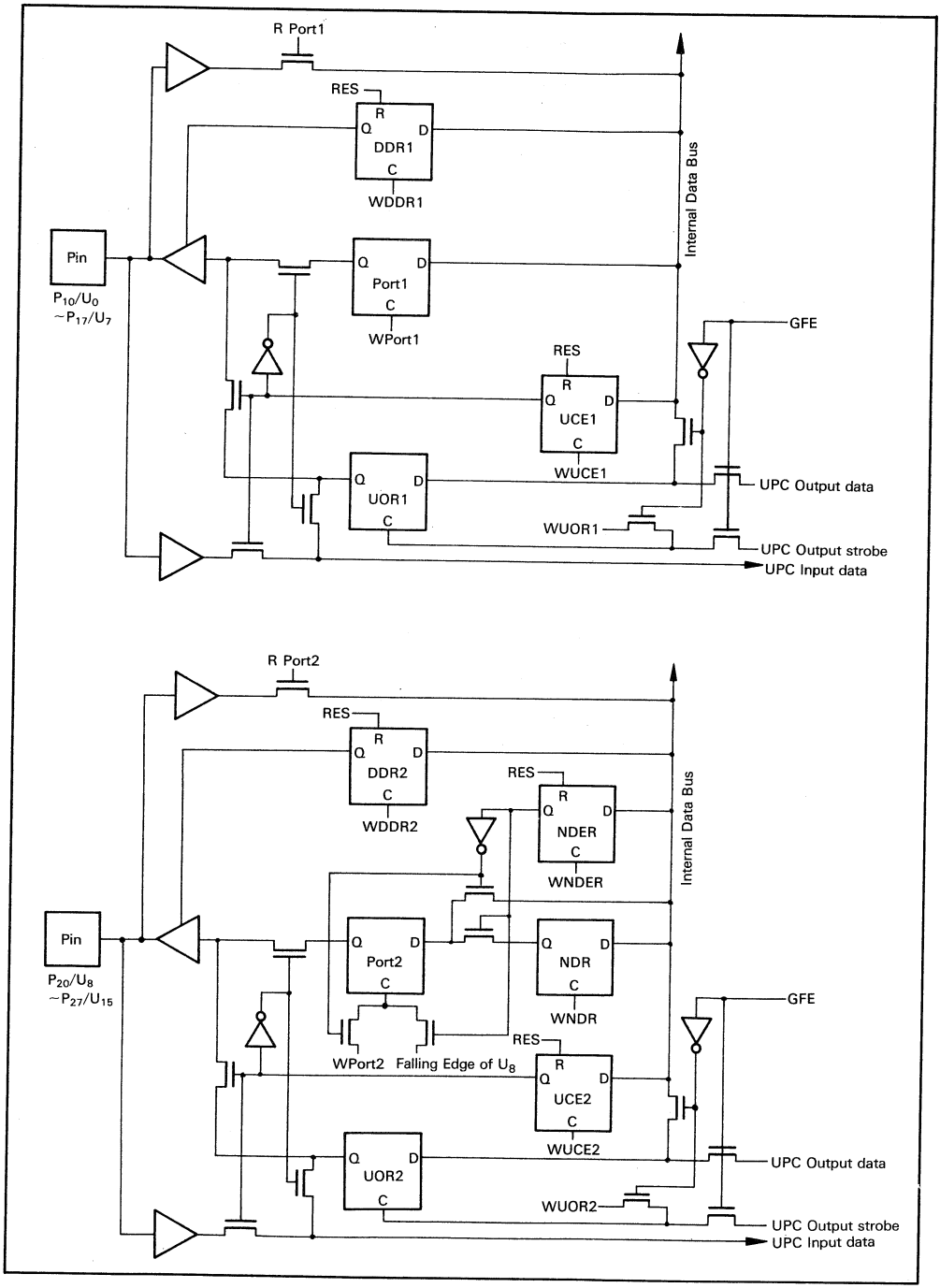


Figure 7. Block Configuration of I/O Resisters

Data Direction Register 1, 2 (DDR1, DDR2): DDR1, DDR2 specify data direction of the corresponding bits of a port. Data is output when the bit is 1, and input when 0. DDR1 and DDR2 are cleared by reset.

UPP Output Register 1, 2 (UOR1, UOR2): During UPC operation, these registers cannot be accessed by the MPU since data are being stored here by the UPC. However, while the UPC is stopped, they are write accessible by the MPU. After reset, this register value is indefinite and should be initialized before setting GFE as required. These registers cannot be read directly during both operation and suspension of the UPC.

UPP I/O Register (UIOR): As the UPP I/O register has no external input/output pins, pulses cannot be input to or output from it. However it can be used for relay when the output of one function is used as the input of another function. This register is accessible by the MPU both while executing and suspending UPC operation, but when UPC is in operation, the bit specified as output of UPC cannot be set by the MPU.
After reset, this register value is indefinite and should be initialized before setting GFE as required.

Port Data Register 1, 2 (Port1, Port2): These are output data registers when I/O pins are used as an MPU port. Reading the port data registers address returns the input/output value of the pins.

UPP Contact Enable Register 1, 2 (UCER1, UCER2): UCER1, UCER2 determine whether I/O pins are used as pulse I/O pins of the UPC or as I/O ports of the MPU in bit units.

(1) Setting a UCE bit to 1 specifies the corresponding pin as a pulse I/O pin of the UPC. The corresponding contents of UOR are output onto this pin when DDR=1. If this pin is specified as an input pin of the UPC, I/O value of the pin is input regardless of DDR.

(2) When a UCE bit is 0, the corresponding pin is specified as I/O pins of the MPU port. The corresponding contents of port data register are output onto this pin when DDR=1. UOR is now separated from the pin, but can be used as an I/O register of the UPC. If this pin is specified as an input pin of the UPC, the values of UORl and UOR2 are input.

Next Data Register (NDR): The next data register is write-enabled from the MPU. It is used when data, which was set in advance, is output in a certain timing. NDR value is output to port 2 upon transition of bit 0 of UOR2 from 1 to 0, when the next data enable register (NDER) is 1.

Next Data Enable Register (NDER): The next data enble register determines bit by bit whether or not data in NDR is output to port 2. When a bit is 1, the corresponding data in NDR can be output to port 2, and the corresponding bit of port 2 cannot be set by the MPU. When 0, it functions as a standard port, and the NDR value is not output to port 2.

Interrupt Request

The UPC can post interrupt requests at the edge of input/output pulse U_0-U_{23}. As shown in figure 8, interrupt processing is controlled by the following four sets of registers: interrupt status registers (ISR1-ISR3), interrupt enable registers (IER1-IER3), interrupt request registers (IRQR1-IRQR3), and interrupt status clear register (ISCR1-ISCR3). Interrupt requests from pins 0 to 15 are output to $\overline{INT_0}$, and those from pins 16-23 to $\overline{INT_1}$.

Interruput Status Register (ISR1-ISR3): The corresponding bits of this register are set on detecting the edges of pulse signals from U_0 to U_{23}. ISR3 is set at the falling edge of the pulse signal. The upper 4 bits of ISR1 and ISR2 are set at the rising edge of the pulse signal, and lower 4 bits are set at its falling edge. This register is cleared by reset, as well as by setting the interrupt status clear register.

Interrupt Enable Register (IER1-IER3): IER1-IER3 enables or disables interrupt requests. An interrupt is generated if the corresponding bit of the interrupt status ragister is set when this register bit is 1, and it is masked when it is 0. This register is cleared by reset.

Interrupt Request Register (IRQR1-IRQR3): IRQR1-IRQR3 is set by a logical AND of the interrupt status register and the interrupt enable register. Interrupt request is allowed by logical OR between each bit of this register as shown in figure 9.

Interrupt Status Clear Register (ISCR1-ISCR3): ISCR1-ISCR3 clears the interrupt status registers. The corresponding bits of the interrupt status register are cleared by writing a 0 into this register. When a 1 is written into this register, the data of the corresponding bits of the interrupt status register are held.

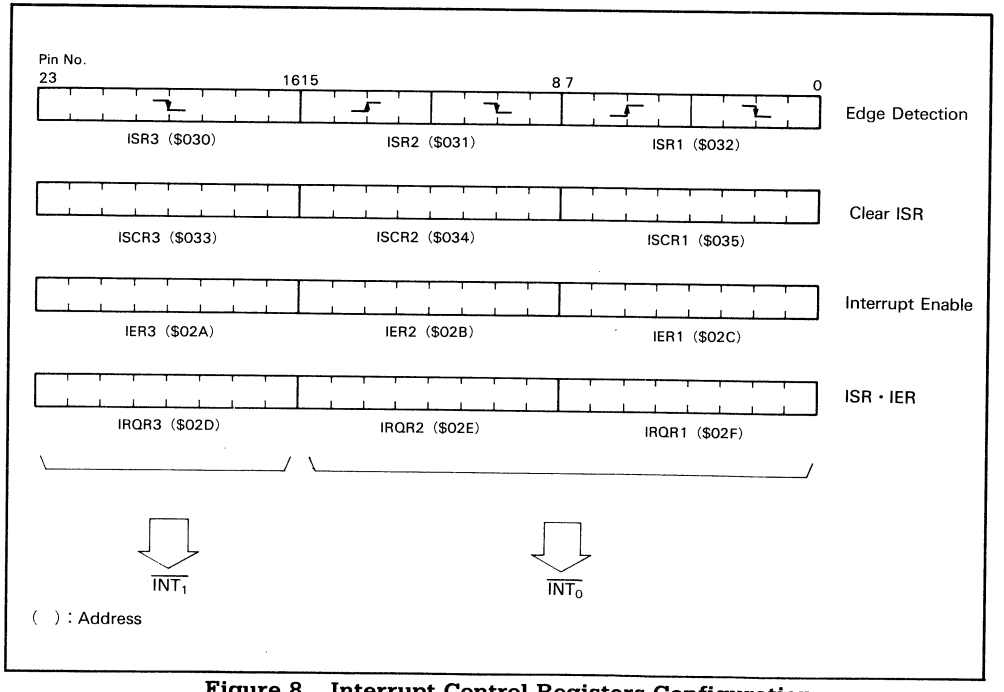


Figure 8. Interrupt Control Registers Configuration

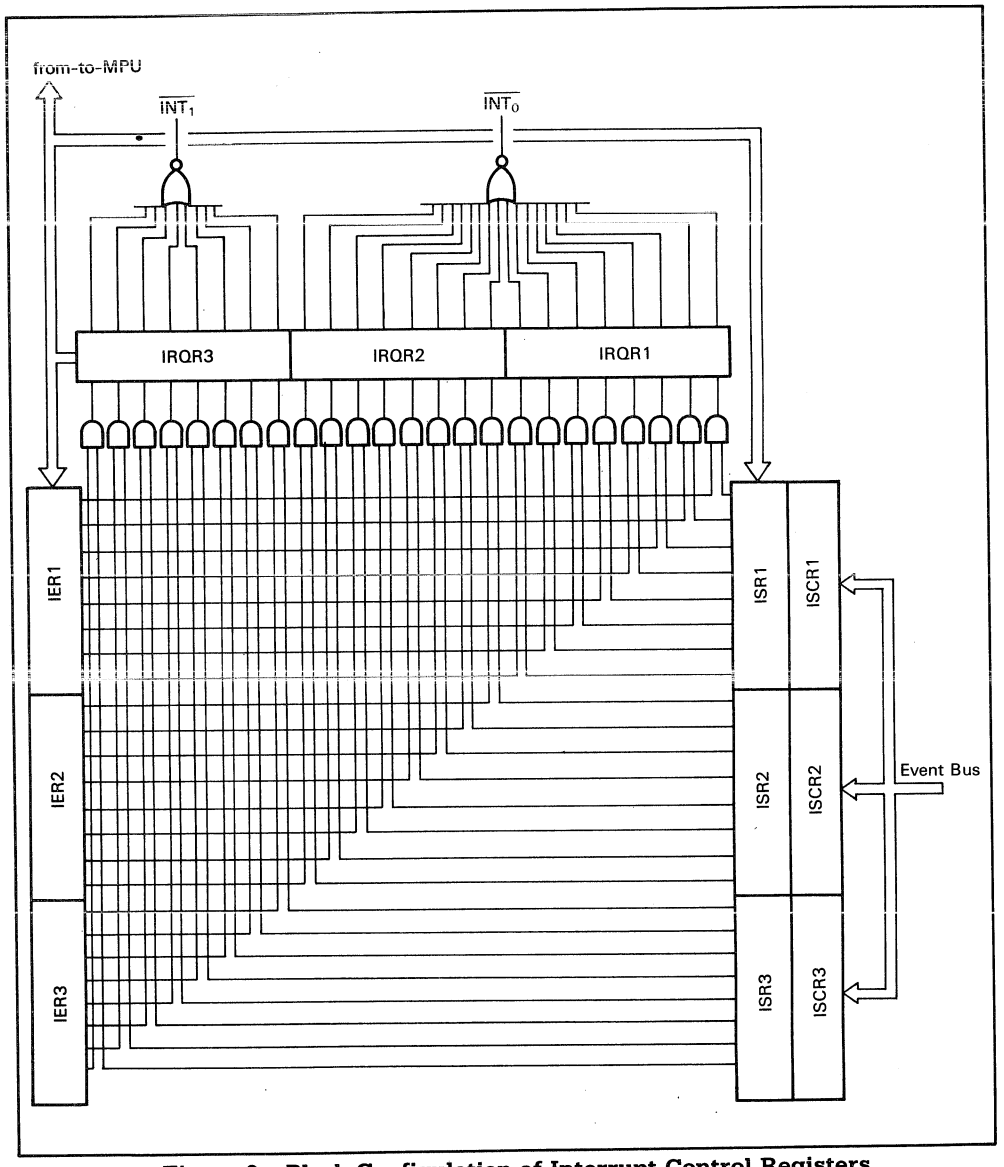


Figure 9. Block Configulation of Interrupt Control Registers

A/D Converter Internal Registers

A/D Control Status Register (ADCSR)

Bit 7	6	5	4	3	2	1	0
ADEND	ADIE	ADST	SCAN	CH 3	CH 2	CH 1	CH 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 006

ADEND (A/D end): The ADEND bit is set to 1 upon completion of A/D conversion. In scan mode, it is set to 1 when the first A/D conversion of all the selected channels is completed. It is cleared by reading ADDR after reading ADCSR, or by writing a 0 into this bit. This bit cannot be written with a 1.

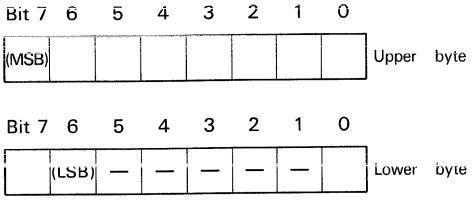
ADIE (A/D interrupt enable): The ADIE flag enables an interrupt request. Interrupt request ($\overline{INT_1}$) is generated by setting ADEND if this bit is set to 1, and is masked if it is 0. This bit is cleared by reset.

ADST (A/D start): Writing a 1 into this bit starts A/D conversion. It remains 1 during conversion, and in single mode, it is cleared upon conversion completion. In scan mode, conversion is started by setting this bit, and continues until this bit is cleared by the MPU. Writing a 1 again during conversion restarts A/D conversion from the beginning.

SCAN (Scan mode selection): Scan mode is selected when this bit is 1, and single mode when 0. In single mode, A/D conversion of the selected channel is executed only once. In scan mode, conversion of all the selected channels is sequentially continued until the ADST bit is cleared. These bits are cleared by reset.

CH3-CH0 (Channel selection): The CH3-CH0 bits select an analog input channel. The relationship between these bits and selected channels in single and scan mode is shown in table 2. These bits are cleared by reset.

A/D Data Register (ADDR0-ADDR3)



The result of A/D conversion is set in the A/D data register. It consists of 2 bytes. The upper 8 bits of 10-bit A/D conversion data are set in the ADDR's upper byte, and its lower 2 bits are set in the upper 2 bits of ADDR's lower byte, taking 8-bit resolution into consideration. In scan mode, when the upper byte of data is read, the lower byte of data is not updated until the lower byte is read. The UPP possesses four A/D registers so that scanning can be performed for a maximum of four channels. Which channel's conversion result is output to which register is determined in both scan mode and single mode. This relation is shown in table 2. When read, bits 0 to 5 of the ADDR's lower byte are output as 0.

Table 2. Relation between Selected Channel and ADDR in Single and Scan Modes

Mode	SCAN	CH3	CH2	CH1	CH0	ADDR0 ($007, 008)	ADDR1 ($009, 00A)	ADDR2 ($00B, 00C)	ADDR3 ($00D, 00E)
Single Mode	0	0	0	0	0	AN_0	—	—	—
		0	0	0	1	—	AN_1	—	—
		0	0	1	0	—	—	AN_2	—
		0	0	1	1	—	—	—	AN_3
		0	1	0	0	AN_4	—	—	—
		0	1	0	1	—	AN_5	—	—
		0	1	1	0	—	—	AN_6	—
		0	1	1	1	—	—	—	AN_7
		1	0	0	0	AN_8	—	—	—
		1	0	0	1	—	AN_9	—	—
Scan Mode	1	0	0	0	0	AN_0	—	—	—
		0	0	0	1	AN_0	AN_1	—	—
		0	0	1	0	AN_0	AN_1	AN_2	—
		0	0	1	1	AN_0	AN_1	AN_2	AN_3
		0	1	0	0	AN_4	—	—	—
		0	1	0	1	AN_4	AN_5	—	—
		0	1	1	0	AN_4	AN_5	AN_6	—
		0	1	1	1	AN_4	AN_5	AN_6	AN_7
		1	0	0	0	AN_8	—	—	—
		1	0	0	1	AN_8	AN_9	—	—

RAM Internal Resister

RAM Control Register (RAMCR)

Bit 7	6	5	4	3	2	1	0
RAME	–	–	–	–	–	–	–
R/W							

Address: $ 00F

RAME (RAM Enable): Writing 0 to this bit disables access to RAM (address $400-$7FF), preserving RAM data. This is useful when entering the standby mode. This bit is set to 1 by reset.

Bit 6-0: Not used

Watchdog Timer Internal Register

HD63140 is provided with a built-in programmable 8-bit watchdog timer and can monitor the system. This watchdog timer consists of a prescaler, 8-bit counter, and watchdog timer register (WDTR).
When the timer overflows, low is output at $\overline{\text{WDTO}}$ pin.
The 8-bit counter and the watchdog timer register (WDTR) are mapped at the same address. With the first write to this address after reset, data is set in the WDTR, and at the same time, the 8 -bit counter starts counting up. However, with the second or subsequent accesses, data is set in the counter and no data can be written to the WDTR until the counter overflows. When this address is read, WDTR contents are read, and counter contents cannot be read. When the timer overflows, 1 is set in WDTR's OVF bit, and the timer starts counting from 0. When OVF bit is 1, the WDTR can be set again after reading the WDTR. When WDTR read is not performed, not the WDTR but the counter is set.

Bit 7	6	5	4	3	2	1	0
OVF	WOE	–	MOD	–	OVC2	OVC1	OVC0
R	R/W		R/W		R/W	R/W	R/W

Address: $ 005

OVF (Overflow flag): When the 8-bit counter reaches $FF, this bit is set to 1. It is cleared by reset or reading WDTR.

WOE (WDT Output enable): When OVF is 1 with WOE set to 1, low is output from the $\overline{\text{WDTO}}$ pin. When it is 0, no pulse is output. This bit is cleared by reset.

Bit 5: Not used

MOD (Mode): The MOD bit specifies the output method of the overflow signal from the $\overline{\text{WDTO}}$ pin. If the counter overflows when the MOD bit is 0, low is output for approximately 8.5μs (4 MHz operation). When it is 1, the inverse signal of the WDTR's OVF is directly output to the $\overline{\text{WDTO}}$ pin, and low output is held until OVF is cleared by reading the WDTR by MPU.

Bit 3: Not used

OVC2-OVC0 (Overflow cycle): OVC2-OVC0 bits specify the dividing ratio of the 10-bit prescaler, and defines the interval between WDTR setting and counter overflow. The relation between the specified values of OVC2 to OVC0 and overflow time is shown in table 3.

Table 3. Overflow Time of Watchdog Timer (4 MHz operation)

OVC2	OVC1	OVC0	Interval (ms)
0	0	0	131.072
0	0	1	32.768
0	1	0	8.192
0	1	1	2.048
1	0	0	1.024
1	0	1	0.512
1	1	0/1	0.128

UPP Commands

Table 5 shows the function format of the UPP. The function consists of command, register assignment, and I/O assignment. In each function, register i functions as a timer, counter, or shifter. In commands other than TPC command, either of internal clock or external clock is selectable as clock for the register i by setting the bit 3 of CMR register.

For each command description in the following pages, an external clock is utilized. In this case, the value of register i is incremented, decremented or shifted upon function execution only when the specified edge of the specified signal is detected.

On the other hand, when an internal clock is utilized, the contents of IOARA defining a clock are ignored. The value of register i is incremented, decremented, or shifted upon every function execution if necessary conditions such as a gate signal are satisfied. Therefore, the apparent internal clock frequency is determined by the interval between executions of the same function which is the inverse of pulse width resolution (refer to MFNR description.)

In commands having pulse output capability, the increment or decrement of register i (which functions as a counter or timer) and the comparision between register i and compare register j are performed at the same time by the ALU. (Comparison is performed between this incremented or decremented value and register j.) Table 4 shows the relation between the value of register i (i), that of j (j), and comparison result CR. Refer to each command description for the relation between CR and output pulses. Reset value of counter or timer is 0 at both incrementation and decrementation.

Table 4. Register Data and Comparison Result

D/$\overline{U}$	Condition	Comparison Result CR
0	(i) < (j)	0
	(i) ≧ (j)	1
1	(i) ≦ (j)	0
	(i) > (j)	1

(i): Register i (counter/timer) data
(j): Register j (compare register) data

Table 5. UPP Function Format

Register	Command Register (CMR)								Register Assignment Register A (RASRA)					Register Assignment Register B (RASRB)					I/O Assignment Register A (IOARA)							I/O Assignment Register B (IOARB)							I/O Assignment Register C (IOARC)					I/O Assignment Register D (IOARD)				
Bit / Command	7	6	5	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0	6	5	4	3	2	1	0	6	5	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
FRS	0	0	0	0	C/$\overline{T}$	D/$\overline{U}$	0	0		i					j				FA	RA		p				FB	RB		q					r					–			
INS	0	0	0	1	C/$\overline{T}$	D/$\overline{U}$	0	0		i					j				FA	RA		p				FB	RB		q					r					–			
UDS	0	0	1	0	C/$\overline{T}$	I/$\overline{N}$	0	0		i					j				FA	RA		p				FB	RB		q					r					s			
GTS	0	0	1	1	C/$\overline{T}$	D/$\overline{U}$	0	H/$\overline{L}$		i					j				FA	RA		p				FB	RB		s					r					s			
FRC	0	1	0	0	C/$\overline{T}$	D/$\overline{U}$	0	H/$\overline{L}$		i					j				FA	RA		p				–	–		–					r					–			
INC	0	1	0	1	C/$\overline{T}$	0	0	H/$\overline{L}$		i					j				FA	RA		p				–	–		–					r					–			
PWC	0	1	1	0	C/$\overline{T}$	0	0	H/$\overline{L}$		i					j				FA	RA		p				FB	RB		q					r					–			
OSC	0	1	1	1	C/$\overline{T}$	0	0	H/$\overline{L}$		i					j				FA	RA		p				FB	RB		q					r					–			
FFC	1	0	0	0	C/$\overline{T}$	0	0	0		i					j				FA	RA		p				–	–		–					r					–			
TPC	1	0	0	1	1	I/$\overline{N}$	0	0		i					–				FA	RA		p				FB	RB		q					p					q			
GTC	1	0	1	0	C/$\overline{T}$	D/$\overline{U}$	0	H/$\overline{L}$		i					j				FA	RA		p				FB	RB		s					r					s			
CTO	1	0	1	1	C/$\overline{T}$	0	0	H/$\overline{L}$		i					j				FA	RA		p				FB	RB		q					r					s			
SIT	1	1	0	0	E/$\overline{I}$	L/$\overline{R}$	0	0		i					j				FA	RA		p				FB	RB		q					r					–			
SOT	1	1	0	1	E/$\overline{I}$	S2	S1	S0		i					j				FA	RA		p				FB	RB		q					r					s			
SPO	1	1	1	0	E/$\overline{I}$	S2	S1	S0		i					j				FA	RA		p				FB	RB		q		04	03	02	01	00		s			
NOP	1	1	1	1	–	–	–	–		–					–				–	–		–				–	–		–					–					–			

C/$\overline{T}$ (CTR/$\overline{TMR}$) : When 0, register i functions as a timer and counts internal clock pulses. When 1, register i functions as a counter and counts the specified direction edge of signal Up.

E/$\overline{I}$ (EXT/$\overline{INT}$) : When 0, register i is shifted according to an internal clock. When 1, register i is shifted at the specified direction edge of external clock signal Up.

D/$\overline{U}$ (DWN/$\overline{UP}$) : When 0, register i functions as an up-counter. When 1, register i functions as a down-counter.

I/$\overline{N}$ (INV/$\overline{NINV}$) : Controls counting direction of a counter. For details, refer to the command description.

H/$\overline{L}$ (HIGH/$\overline{LOW}$) : This bit specifies polarity of output pulse and gate signal. The polarity of the counter overflow signal is not affected by this bit. For details, refer to the command description.

L/$\overline{R}$ (LEFT/$\overline{RIGHT}$) : When 0, register i is shifted to right. When 1, register i is shifted to left.

i : Number of UDR functioning as a counter/timer or shifter.

j : Number of UDR functioning as a capture register, compare register, or data register (shift command).

p: Clock input pin No.

q: Pulse input pin No.

r: Pulse output pin No.

s: Count direction control signal, gate signal, trigger enable signal, or shift direction control signal input pin No.

FA (FEDGA): Detects falling edge of signal Up when FA = 1.

RA (REDGA): Detects rising edge of signal Up when RA = 1.

FB (FEDGB): Detects falling edge of signal Uq or Us when FB = 1.

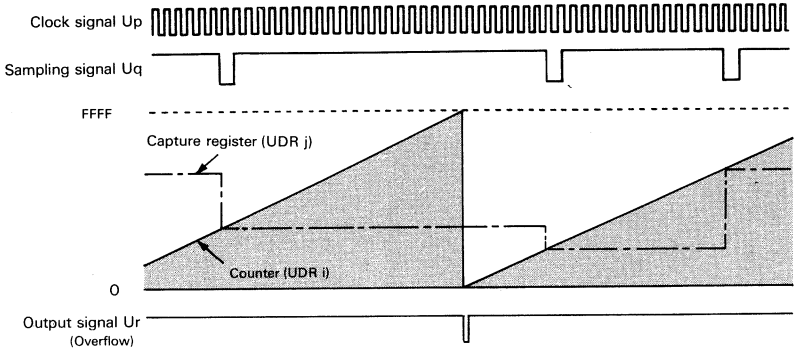
RB (REDGB): Detects rising edge of signal Uq or Us when RB = 1.

S0-S2, O0-O4: Specify the shift mode and output method of shift commands. For details, refer to the command description.

COMMAND **1. Free-Running Counter/Timer with Sampling (FRS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. Value of register i is set into register j (capture register) on detecting the specified direction edge of sampling signal Uq.
3. Overflow signal of register i is output to Ur.
   (Pulse signal counting)

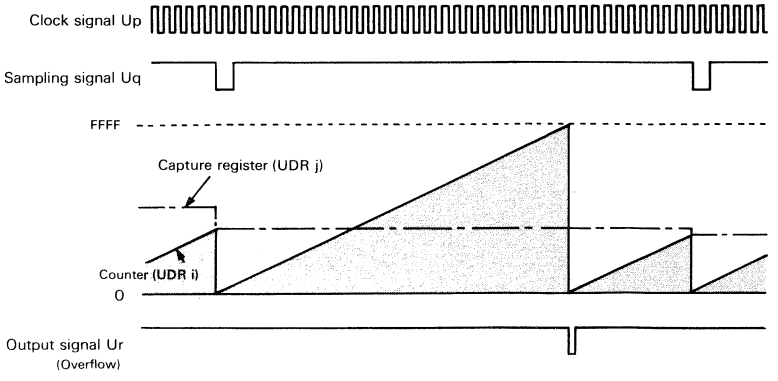
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, D/$\overline{U}$ = 0, FB = 1, RB = 0**



COMMAND **2. Interval Counter/Timer with Sampling (INS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. Value of register i is set into register j (capture register) and register i is reset on detecting the specified direction edge of sampling signal Uq.
3. Overflow signal of register i is output to Ur.
   (Pulse signal interval measurement)

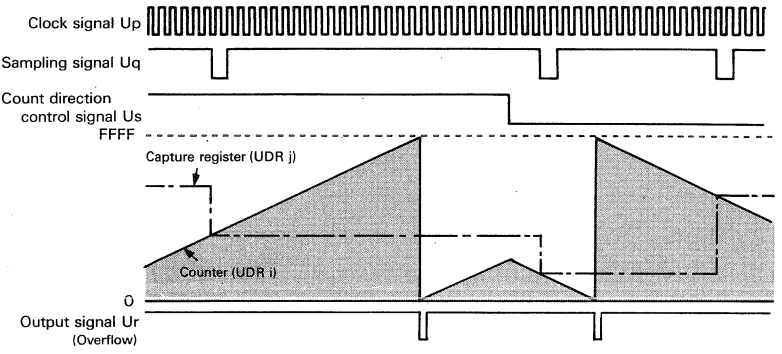
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, D/$\overline{U}$ = 0, FB = 1, RB = 0**



COMMAND **3. Up-Down Counter/Timer with Sampling (UDS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by count direction control signal Us and bit 2 (I/$\overline{N}$) of CMR.
   Incrementation is performed if I/$\overline{N}$ ⊕ Us=1, and decrementation if I/$\overline{N}$ ⊕ Us=0.
2. Value of register i is set into register j (capture register) on detecting the specified direction edge of sampling signal Uq.
3. Overflow signal of register i is output to Ur.

EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, I/$\overline{N}$ = 0, FB = 1, RB = 0**

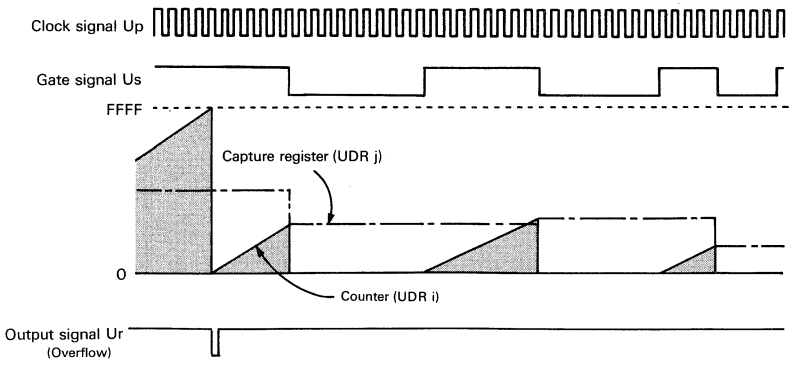


COMMAND **4. Gated Counter/Timer with Sampling (GTS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up, when gate signal Us is set as bit 0 (H/ $\overline{L}$) of the CMR. Incrementation or decrementation is determined by bit 2 of CMR.
2. Value of register i is set into register j (capture register) and register i is reset on detecting at the specified direction edge of signal Uq.
3. Overflow signal of register i is output to Ur.

(Gate width measurement)

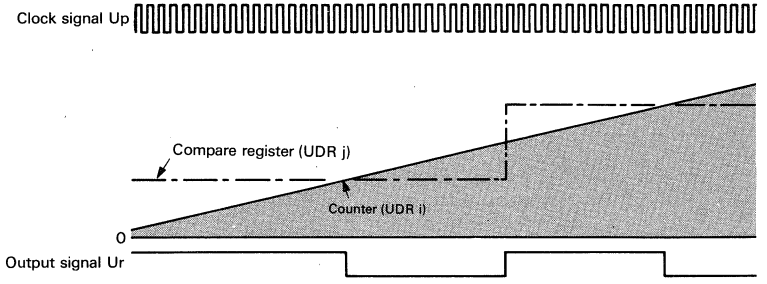
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, D/$\overline{U}$ = 0, H/$\overline{L}$ = 1, FB = 1, RB = 0**



COMMAND **5. Free-Running Counter/Timer with Compare (FRC)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. Comparison result CR between register i and register j (compare register) is output to Ur. Output level is specified by bit 0 of CMR, and is equal to $\overline{CR \oplus H/\overline{L}}$.

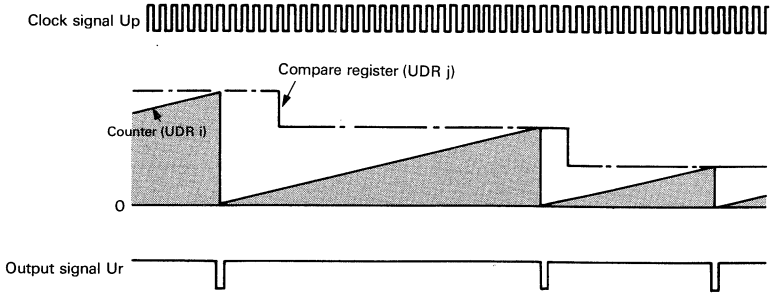
EXAMPLE **Program in Function Table: $C/\overline{T} = 1$, $D/\overline{U} = 0$, $H/\overline{L} = 0$**



COMMAND **6. Interval Counter/Timer with Compare (INC)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. When comparison result CR between register i and register j (compare register) is 1, the pulse signal specified by bit 0 of CMR is output to Ur and register i is reset.
   Range of register i is from 0 to (j) − 1 ((j) = the data of register j).
   Output pulse width is equal to pulse width resolution both in timer mode and counter mode.
   (Interval pulse output)

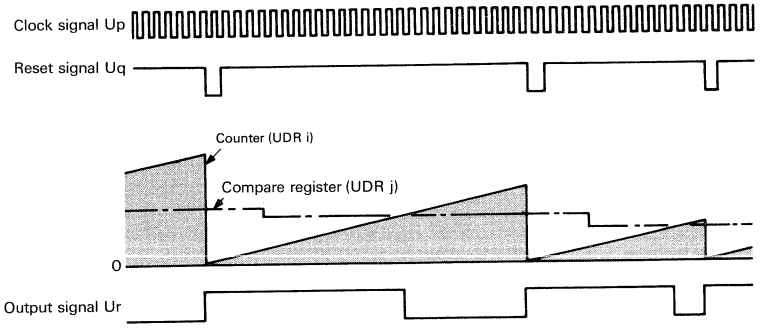
EXAMPLE **Program in Function Table: $C/\overline{T} = 1$, $H/\overline{L} = 0$**



COMMAND **7. Pulse Width Counter/Timer with Compare (PWC)**

1. The inverse of the signal level specified by bit 0 of CMR is output to Ur and register i (counter) is reset on detecting the specified direction edge of reset signal Uq.
2. Register i is incremented on detecting the specified direction edge of clock signal Up.
3. When comparison result CR between register i and register j (compare register) is 1, the output level of Ur is inverted and held until the next reset pulse is input. Register i keeps incrementing while CR=1. It is not reset while CR=0 even if a reset pulse is input.
(When a reset pulse is input, the output level of Ur is inverted regardless of the value of CR. Accordingly if the value of compare register j is set to 0, the pulse width does not become 0, and a pulse having the same width as the pulse width resolution can be obtained.)

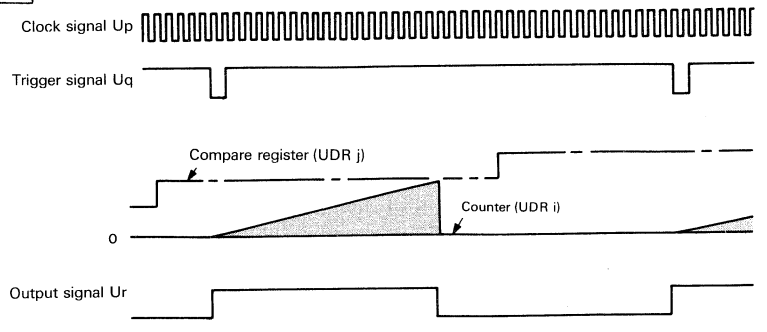
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, H/$\overline{L}$ = 0, FB = 1, RB = 0**



COMMAND **8. One Shot Counter/Timer with Compare (OSC)**

1. Counter (UDR i) starts and the inverse of the signal level specified by CMR's bit 0 is output to Ur on detecting the specified edge of trigger signal Uq, and the value of register i (counter) is incremented on detecting the specified direction edge of clock signal Up.
2. When comparison result CR between register i and register j (compare register) is 1, the output level of Ur is inverted, register i is reset, and this level is held until the next trigger signal is input.
Even if the next trigger signal is input while CR=0, it is ignored and no trigger takes place. (Similarly to the case of PWC, if the value of compare register j is set to 0, the pulse width does not become 0, and a pulse having the same width as the pulse width resolution can be obtained.)
(One-shot pulse output)

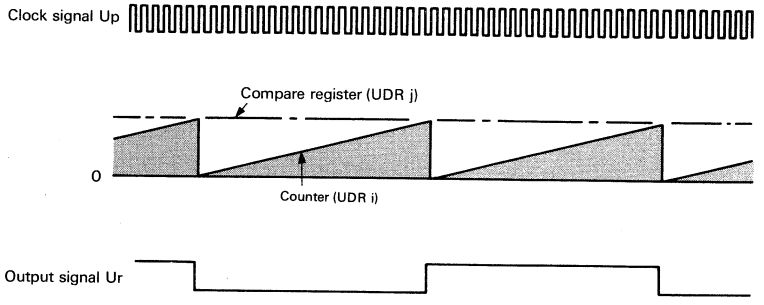
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, H/$\overline{L}$ = 0, FB = 1, RB = 0**



COMMAND **9. Fifty-Fifty Duty Cycle Counter/Timer with Compare (FFC)**

1. Value of register i (counter) is incremeted on detecting the specified direction edge of clock signal Up.
2. When comparison result CR between register i and register j (compare register) is 1, register i is reset and the output level of Ur is inverted.
(50% duty cycle pulse output)

EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1**



COMMAND **10. Two Phase Up-Down Counter (TPC)**

Value of register i (counter) is incremented or decremented according to the phase relation between two-phase pulse signals Up and Uq, as shown in table 6. Incrementation or decrementation is determined by the specified value of $I/\overline{N}$.

(Two-phase pulse signal counting)

EXAMPLE **Program in Function Table: $I/\overline{N}$ = 0, FA=RA=FB=RB=1**

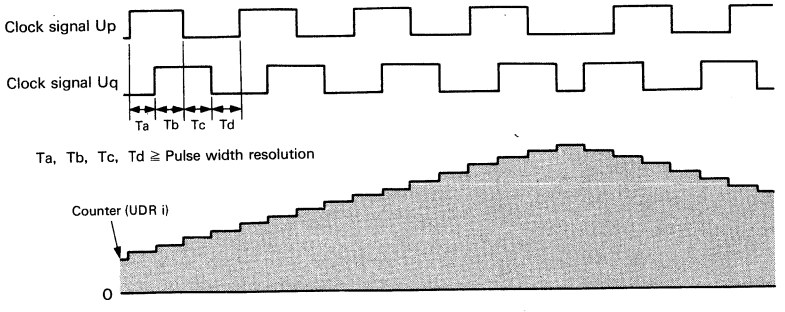


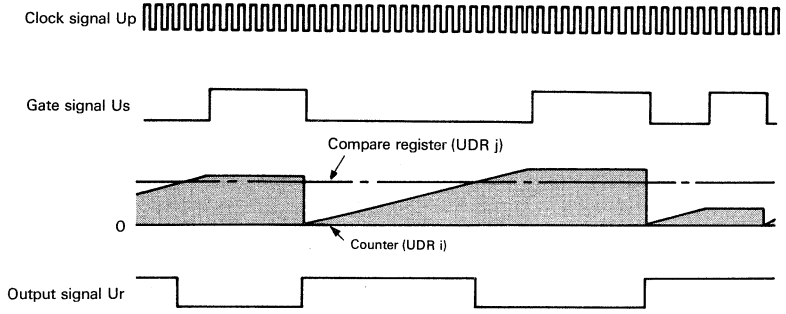
Table 6. TPC Command Function

P	q	Condition	$I/\overline{N}=0$	$I/\overline{N}=I$
↑	0	RA = 1	(i) +1 → (i)	(i) −1 → (i)
1	↑	RB = 1	(Incrementation)	(Decrementation)
↓	1	FA = 1		
0	↓	FB = 1		
↑	1	RA = 1	(i) −1 → (i)	(i) +1 → (i)
1	↓	FB = 1	(Decrementation)	(Incrementation)
↓	0	FA = 1		
0	↑	RB = 1		

COMMAND **11. Gated Counter/Timer with Compare (GTC)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up, when gate signal Us is set as specified by bit 0 of the CMR. Incrementation or decrementaion is determined by bit 2 of CMR.
2. Comparison result CR between register i and register j (compare register) is output onto Ur. The output level is specified by bit 0 of CMR, and is equal to $\overline{CR \oplus H/\overline{L}}$.
   Register i is reset at the specified direction edge of the gate signal.
   (Gate width definition)

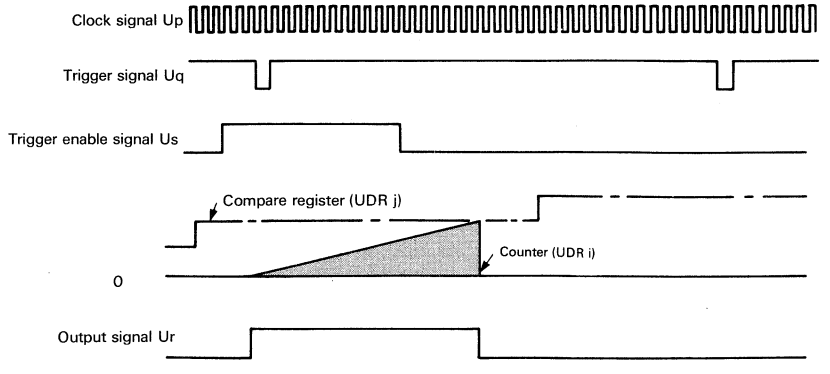
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, D/$\overline{U}$ = 0, H/$\overline{L}$ = 0, FB = 1, RB = 0**



COMMAND **12. Combination Trigger One Shot Counter/Timer (CTO)**

1. When trigger enable signal Us is 1, the inverse of the signal level specified by CMR's bit 0 is output to Ur on detecting the specified direction edge of trigger signal Uq, and then register i (counter) is incremented on detecting the specified direction edge of clock signal Up.
2. When comparision result CR between register i and register j (compare register) is 1, the output level of Ur is inverted, register i is reset, and this level of Ur is held until the next trigger signal is input.
   Even if the next trigger signal is input while CR=0, it is ignored and no trigger takes place.
   (One-shot pulse output with trigger enable)

EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, H/$\overline{L}$ = 0, FB = 1, RB = 0**

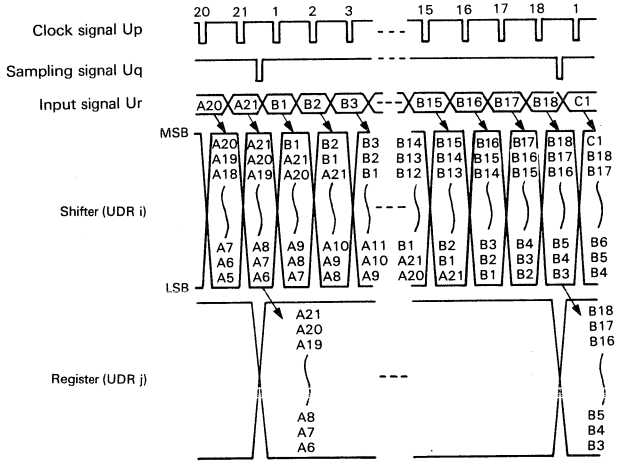


COMMAND **13. Shift Input (SIT)**

1. Value of register i (shifter) is shifted and value of Ur is read to register i on detecting the specified direction edge of clock pulse Up. Shifting direction is determined by bit 2 (L/ $\overline{R}$) of CMR.
2. Value of register i is set into register j on detecting the specified direction edge of sampling pulse Uq.

(Serial input)

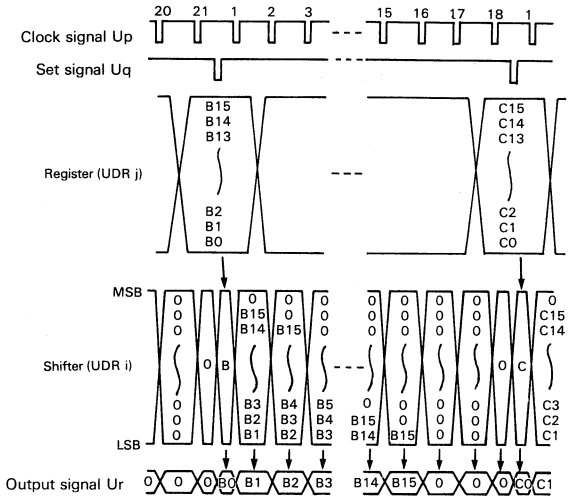
EXAMPLE **Program in Function Table: E/$\overline{I}$ = 1, L/$\overline{R}$ = 0, $\overline{FA}$ = 1, $\overline{RA}$ = 0, $\overline{FB}$ = 1, $\overline{RB}$ = 0**



COMMAND **14. Shift Output (SOT)**

1. Value of register j is set into register i (shifter) on detecting the specified direction edge of set signal Uq.
2. Value of register i is shifted or rotated, and the shift output value is presented onto Ur on detecting the specified direction edge of clock signal Up.
   Mode for shift and rotation is determined by bits 2-0 of CMR as shown in table 7.
   The direction of rotation can be specified by shift direction control signal Us in certain modes as shown in table 7.
3. When S2(CMR's bit 2)=0, the LSB of register i is output to Ur, while S2=1, the MSB of register i is output to Ur.

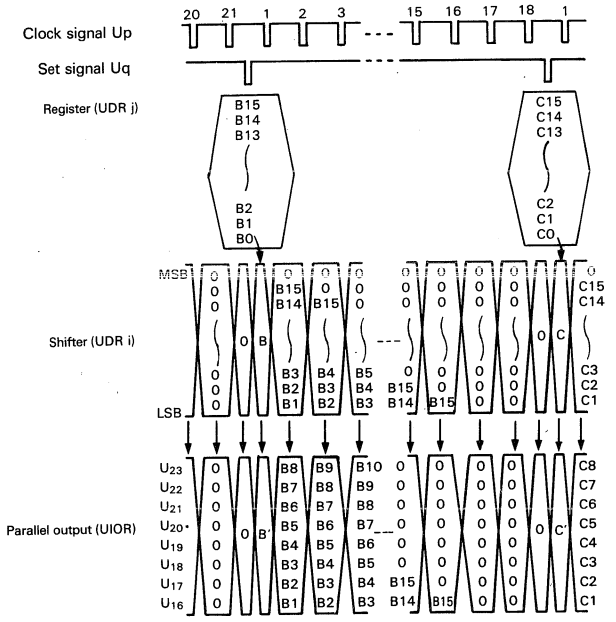
EXAMPLE **Program in Function Table: E/$\overline{I}$ = 1, S0 = S1 = S2 = 0, FA = 1, RA = 0, FB = 1, RB = 0**



COMMAND **15. Shift Parallel Output (SPO)**

1. Value of register j is set into register i (shifter) on detecting the specified direction edge of set signal Uq.
2. Value of register i is shifted or rotated and the lower 8 bits are output on detecting the specified direction edge of clock signal Up.
   Mode for shift and rotation is determind by bits 2-0 of CMR register as shown in table 7.
   The direction of rotation can be specified by shift direction control signal Us in certain modes as shown in table 7.
3. The lower 8 bits of the shifter are output according to the specification of IOARC. The specification method of the output is described in table 8. O4 determines the output destination, UOR1 or UIOR, and O3 to O0 are output-enable bits in 2-bit units.
   The SPO command cannot be output to UOR2.

EXAMPLE **Program in Function Table: E/$\overline{I}$ = 1, SO = S1 = S2 = 0, FA = 1, RA = 0, FB = 1, RB = 0**



Note: B', C' are respectively the lower 8 bits of data B and C.

Table 7. The Relationship between S0 to S2 and Shift or Rotation Mode in the SOT and SPO Commands. (Output to Ur is only for SOT.)

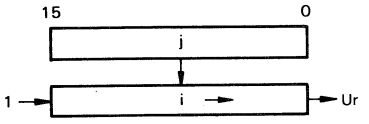
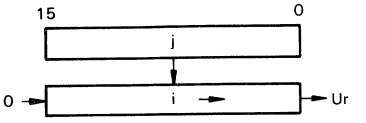
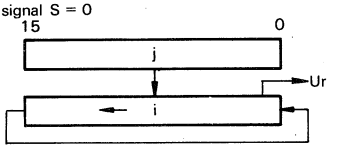
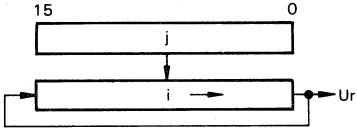
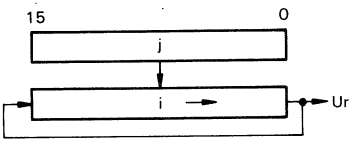
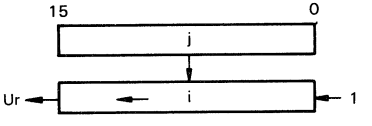
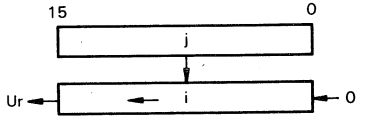
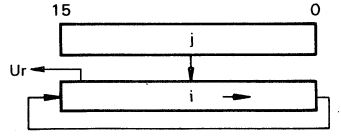
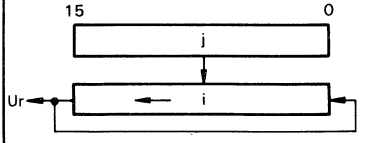
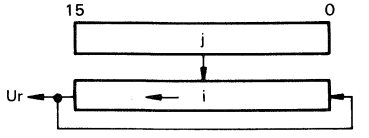
S2	S1	S0 = 1	S0 = 0
0	0		
0	1	Input signal S = 0  Input signal S = 1 	
1	0		
1	1	Input signal S = 0  Input signal S = 1 	

Table 8. Output Destination in the SPO Command

	O4 = 1	O4 = 0
O0 = 1	Shifter bit 0 → U_0	Shifter bit 0 → U_{16}
	Shifter bit 1 → U_1	Shifter bit 1 → U_{17}
O1 = 1	Shifter bit 2 → U_2	Shifter bit 2 → U_{18}
	Shifter bit 3 → U_3	Shifter bit 3 → U_{19}
O2 = 1	Shifter bit 4 → U_4	Shifter bit 4 → U_{20}
	Shifter bit 5 → U_5	Shifter bit 5 → U_{21}
O3 = 1	Shifter bit 6 → U_6	Shifter bit 6 → U_{22}
	Shifter bit 7 → U_7	Shifter bit 7 → U_{23}

Note: If O0 to O3 are 0, the shifter data is not output, and corresponding UOR1 and UIOR bits are not affected by the SPO command.

Notes

Oscillator

The internal clock signal is obtained from the HD63140A00 oscillator by connecting a crystal to XTAL and EXTAL pins or by inputting an external clock to EXTAL pin. The frequency of the crystal or the external clock should be four times that of the internal clock. The oscillator's divide-by-four circuit outputs a system clock signal whose frequency is twice the operation frequency.

Figure 10 shows a crystal connection. An AT-cut parallel resonant crystal should be used. Required characteristics of the crystal (Co, Rs) and capacitance (CL_1, CL_2) are listed in the table 9.

As shown in figure 10, routing signal lines adjacent to the oscillator may result in faulty oscillation due to induction, and such a board design should be avoided. In addition, the crystal and capacitor should be positioned adjacent to XTAL and EXTAL pins. An example of board design is shown in figure 11.

When applying an external clock, the XTAL pin must be disconnected. External clock duty cycle must be 50±5%, and high level voltage must be more than $V_{CC} \times 0.7$ V.

The frequency of the external clock must be two times that of the internal clock (8 MHz clock for 4 MHz operation) in HD63140B00. With HD63140B00, clock duty cycle must be 50±5%, and high level voltage must be more than 2.0 V.

Table 9. Typical Crystal Characteristics

	Oscillation Frequency		
Item	**4 MHz**	**4 MHz<f≦12.288 MHz**	**12.288 MHz<f≦16 MHz**
Co	<7 pF	<7 pF	<7 pF
Rs	<60Ω	<60Ω	<35Ω
CL_1, CL_2*	10–22 pF±10%	10–22 pF±10%	10 pF±20%

* CL_1, CL_2 contains stray capacity of wired lines.

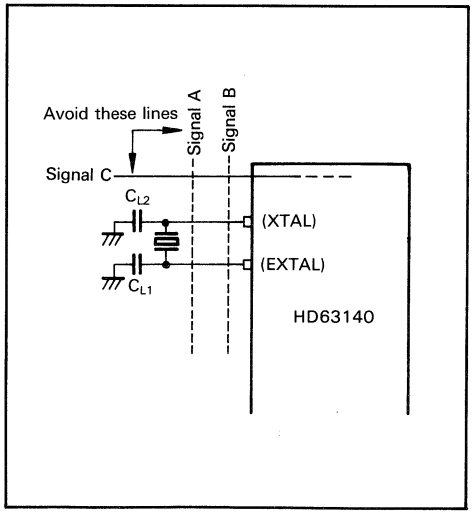


Figure 10. Crystal Connection

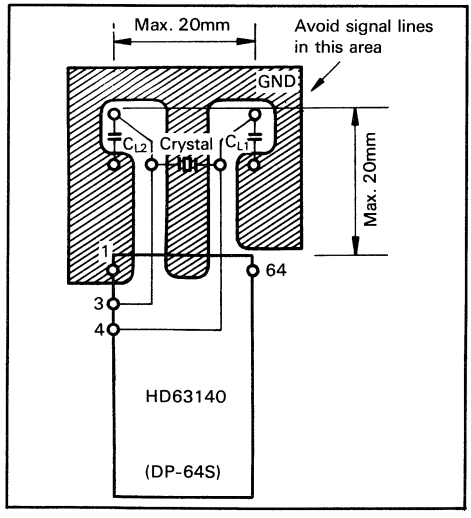


Figure 11. Typical Board Design

Standby Mode

Applying a low level to the $\overline{STBY}$ pin places the HD63140 into standby mode. In standby mode, RAM contents are preserved, all clocks of the HD63140 are inactive, and current dissipation is lowered to 15 μA or less (except for AIcc). All pins except power supply pins (V_{cc}, V_{ss}), $\overline{STBY}$, $\overline{RES}$, and XTAL (outputs low level) are disconnected from internal circuits and the LSI is reset.

HD63140 can return from standby mode by reset start. When entering standby mode with a low level on the $\overline{STBY}$ pin, it does not matter whether the $\overline{RES}$ pin is low or high; however, when returning from standby mode it must be held low until oscillation stabilization. This relationship is shown in figure 12.

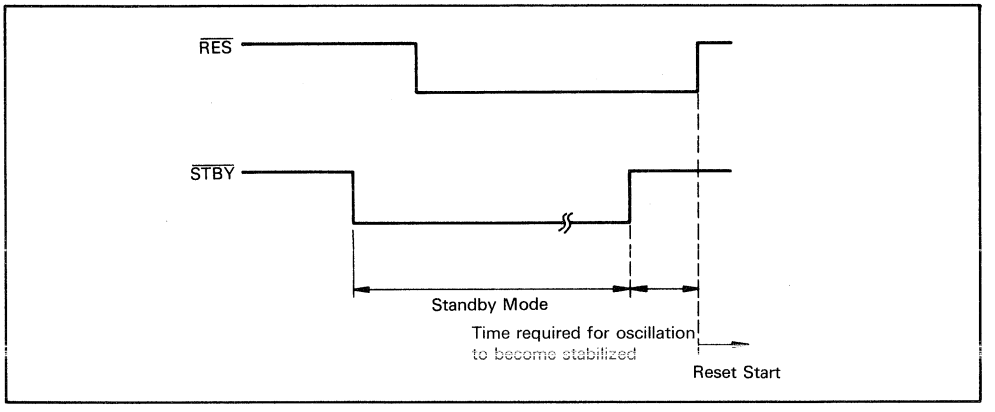


Figure 12. Standby Mode Timing

Notes on using the watchdog timer.

The watchdog timer is undefined at power-on and is not reset until the rising edge of the $\overline{RES}$ signal. Therefore the $\overline{WDTO}$ pin may output a low level while a low level is input to the $\overline{RES}$ pin after power-on.
This may cause your system to stay in the reset state after power-on if the system is constructed as shown in figure A.

Please connect the output of the power-on-reset circuit directly to the $\overline{RES}$ pin of the HD63140 in order to avoid this malfunction (see figure B).

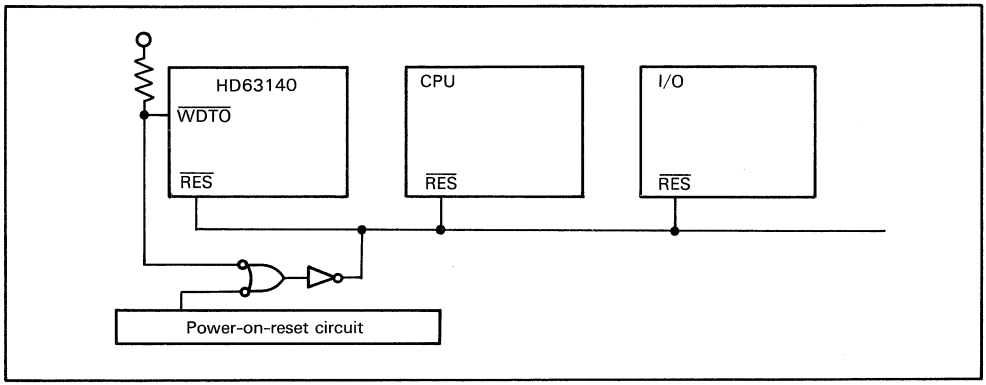


Figure A

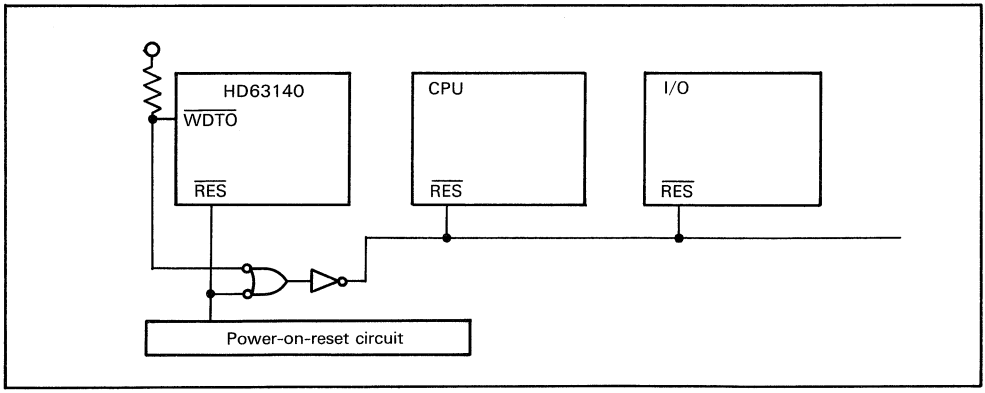


Figure B

Notes on UPP Command Setting (1)

The UPP's pulse width resolution depends on the specified value of maximum function number register MFNR: the resolution is inversely proportional to the specified values. Accordingly, to increase resolution, a minimum value should be set in the MFNR according to the number of functions to be executed.

In addition, when a value larger than the necessary minimum value (or 0) is set in MFNR so as to adjust pulse width resolution, set NOP in the command registers (CMR) of unused function numbers in the function table (figure 13). Since the values in the function table after reset are undefined, they may affect the execution of other functions if they are read and executed.

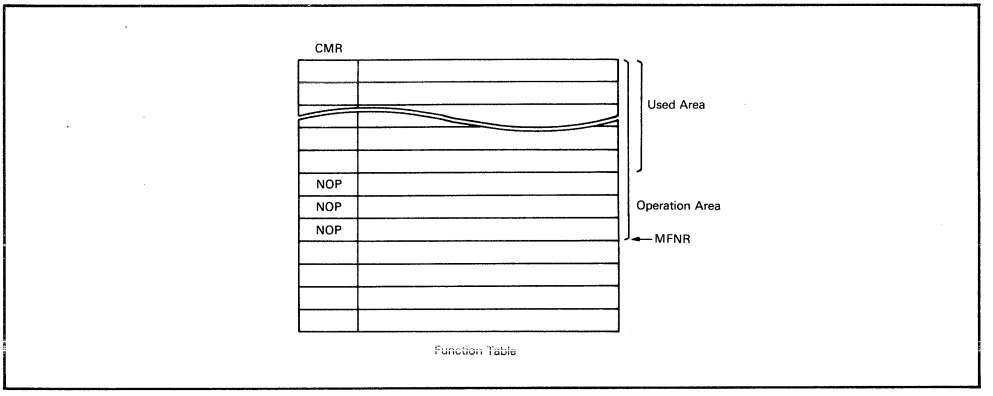


Figure 13. Filling Function Table with NOP

Notes on UPP Command Setting (2)

In the HD63140, an edge detecting cirucit is provided on each pulse input and output of U_0 to U_{23}. Edges are detected by sampling the input and output level and comparing them with the previous sampling value at the timing the function number register (FNR) periodically returns to 0 during UPC operation. Accordingly, while UPC is not in operation, no edges can be detected. In addition, even in operation, narrower pulse edges than the sampling interval cannot be detected (refer to A of figure 14).
Flip-flops for sampling have been cleared by reset. Consequently, as indicated by B of figure 14, if GFE is set while U_0 to U_{23} are 1, rising edges are detected. Accordingly, if edge detection, which is performed at GFE setting, is a problem, avoid such setting combination of the pulse and the edge detecting direction, or set and reset GFE at FNR=1.

At UPC re-start after interruption, flip-flops for sampling store the data just before interruption.

Notes on using capture commands

When the HD63140 generates an interrupt request signal to MPU at a capturing operation at the edge of input signal, a gap will appear between the timing of the interrupt request signal generation and the capturing operation as shown in figure 15. Therefore, extra care should be taken when processing the value in the capture register in the interrupt request routine.

The UPC samples the input signal every time the value of the function number register becomes 0. It detects the edge of the input signal by the change of the sampled value. Interrupt request signal appears immediately after the sampling at which the edge of the input signal has been detected, but the capturing operation is delayed until the capture command is performed after the sampling. Therefore, the value of the capture register is not updated for 5μs (max) at 4 MHz operation. If this dalay time is inconvenient, set the capture command to as small a function number as possible.

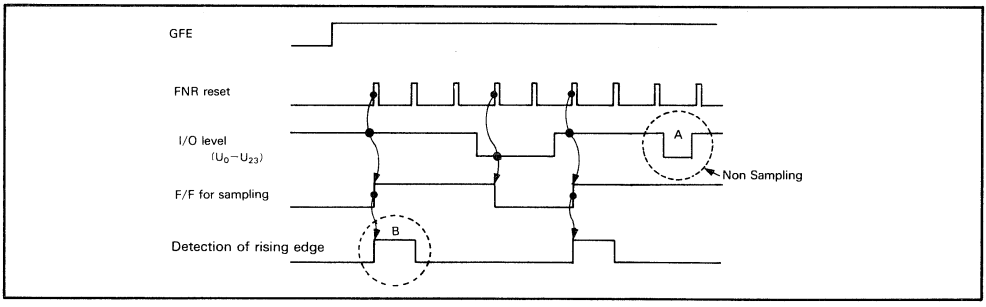


Figure 14. Edge Detection Timing

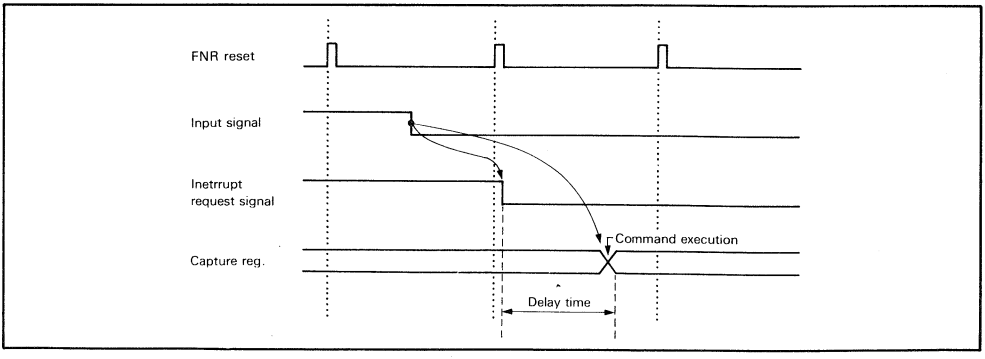


Figure 15. Timing of Interrupt Request and Capture

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	Vcc (Note 2)	−0.3 to + 7.0	V
Input Voltage	Vin (Note 2)	−0.3 to Vcc + 0.3	V
Analog Supply Voltage	AVcc (Note 2)	−0.3 to + 7.0	V
Analog Input Voltage	V_{AN} (Note 2)	−0.3 to AVcc + 0.3	V
Operating Temperature (Note 1)	Topr	−20 to +75	°C
Storage Temperature	Tstg	−55 to +150	°C
Allowable Output Current	|Io| (Note 3)	10	mA
Total Allowable Output Current	|Σ Io| (Note 4)	100	mA

Notes:
1. Wide temperature range (−40°C to+ 85°C) version is also available. For details, please contact the sales department.
2. With respect to V_{SS} (system GND)
3. The allowable output current is the maximum current that may be drawn from, or flow out to, one output terminal or one input/output common terminal.
4. The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.
5. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect the reliability of the LSI.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}*	4.5	5.0	5.5	V
Input Low Voltage	V_{IH}*	2.0	–	V_{CC}	V
Input High Voltage	V_{IL}*	0	–	0.8	V
Schmitt-trigger Input Voltage	V_T^-*	1.0	–	2.0	V
Schmitt-trigger Input Voltage	V_T^+*	3.0	–	4.0	V
Analog Supply Voltage	AV_{CC}*	–	5.0	–	V
Analog Input Voltage	V_{AN}*	0	–	AV_{CC}	V
Operating Temperature	T_{opr}	−20	25	75	°C

Note: * With respect to $V_{SS}=AV_{SS}=0V$

Electrical Characteristics

DC Characteristics

(Vcc = 5 V ±10%, Vss = 0 V, Ta = −20°C to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Schmitt-trigger Input Voltage	$U_8/P_{20}-U_{15}/P_{27}$	V_T^-	1.0	–	2.0	V	Figure 16 V_{cc} = 5.0 V
		V_T^+	3.0	–	4.0	V	
		$V_T^+ - V_T^-$	1.0	–	–	V	
Input high Voltage	$\overline{RES}$, $\overline{STBY}$	V_{IH}	Vcc−0.5	–	Vcc+0.3	V	
	EXTAL		Vcc×0.7	–	Vcc+0.3	V	
	Other Inputs		2.0	–	Vcc+0.3	V	
Input low Voltage	All Inputs	V_{IL}	−0.3	–	0.8	V	
Input Leakage Current	$\overline{RES}$, $\overline{STBY}$ A_0-A_{10}, $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$, $\overline{OE}$, AN_0-AN_9	$\lvert I_{IN}\rvert$	–	–	1.0	μA	Vin = 0.5− Vcc−0.5
Three State Leakage Current (Off state)	D_0-D_7, READY $U_0/P_{10}-U_7/P_{17}$ $U_8/P_{20}-U_{15}/P_{27}$	$\lvert I_{TSI}\rvert$	–	–	1.0	μA	Vin = 0.5− Vcc−0.5
Output high Voltage	All Outputs	V_{OH}	2.4	–	–	V	I_{OH} = −200 μA
			Vcc−0.7	–	–	V	I_{OH} = −10 μA
Output low Voltage	All Outputs	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output Leakage Current (Off state)	$\overline{INT_0}$, $\overline{INT_1}$, $\overline{WDTO}$	I_{LOH}	–	–	1.0	μA	V_{IN} = Vcc−0.5
Input Capacitance	All Inputs	Cin	–	–	15	pF	Vin = 0 V f = 1.0 MHz Ta = 25°C
Current Dissipation*		Icc	–	–	30	mA	fopr = 4 MHz **
Standby Current (Except Alcc)		I_{STB}	–	–	15	μA	
RAM Standby Voltage		V_{RAM}	2.0	–	–	V	
Analog Supply Current		Alcc	–	–	1	mA	

Notes: * Current dissipation varies in proportion to operating frequency (fopr).

** fopr = $f_{XTAL}/4$ or $f_{EXT}/4$: HD63140A00
= $f_{EXT}/2$: HD63140B00

AC Characteristics
(Vcc = 5 V ±10%, Vss = 0 V, Ta = −20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Oscillation Stable Time	t_{RC}	–	–	20	ms	Figure 17
Clock Frequency	f_{opr}	1.0	–	4.0	MHz	Figure 25
Output Clock Frequency	f_{CLK}	–	foprx2	–	MHz	
Output Clock High Pulse Width	t_{CWH}	55	–	–	ns	
Output Clock Low Pulse Width	t_{CWL}	55	–	–	ns	
Output Clock Rise Time	t_{Cr}	–	–	10	ns	
Output Clock Fall Time	t_{Cf}	–	–	10	ns	
Address Set-up Time	t_{AS}	30	–	–	ns	Figure 18-22
Address Hold Time	t_{AH}	5	–	–	ns	Figure 25
Delay Time from $\overline{CS}$ Low until READY Low (Other than RAM)	t_{CRD1}	–	–	60	ns	
Delay Time from $\overline{DS}$ Low until READY High	t_{WAIT} UDR(UPC)*	–	–	3	μs	
	Others*			750	ns	
Delay Time from $\overline{DS}$ High until READY Low	t_{CRD2}	–	–	80	ns	
$\overline{DS}$ High Pulse Width	t_{DWH}	80	–	–	ns	Figure 18
R/$\overline{W}$ Set-Up Time	t_{RS}	10	–	–	ns	Figure 20
R/$\overline{W}$ Hold Time	t_{RH}	5	–	–	ns	Figure 21
Read Data Delay Time (RAM)	t_{RDD}	–	–	140	ns	Figure 25
Read Data Delay Time from READY High	t_{RRDD}	–	–	60	ns	
Read Data Delay Time from $\overline{OE}$	t_{ORDD}	–	–	80	ns	
Read Data Hold Time	t_{RDH}	10	–	–	ns	
Read Data Hold Time from $\overline{OE}$ High	t_{ORDH}	10	–	–	ns	
Write Data Delay Time *	t_{WDD}	–	–	120	ns	Figure 19
Write Data Set-Up Time	t_{WDS}	100	–	–	ns	Figure 21
Write Pulse Hold Time from READY High*	t_{WH}	120	–	–	ns	Figure 25
Write Pulse Low Width	t_{WWL}	100	–	–	ns	
Write Data Hold Time	t_{WDH}	5	–	–	ns	
READY Turn Off Time from $\overline{CS}$ High	t_{RTO}	–	–	50	ns	Figure 20-22 Figure 25

Notes: * At fopr = 4 MHz, these times vary in inverse ratio to operating frequency (fopr).

Port I/O Characteristics
(Vcc = 5 V ±10%, Vss = 0 V, Ta = −20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Port Input Data Set-up Time	t_{PDS}	60	–	–	ns	Figure 23
Port Input Data Hold Time	t_{PDH}	60	–	–	ns	
Port Output Data Delay Time*	t_{PDD}	–	–	170	ns	Figure 24. 25

Notes: * At fopr = 4 MHz, these times vary in inverse ratio to operating frequency (fopr).

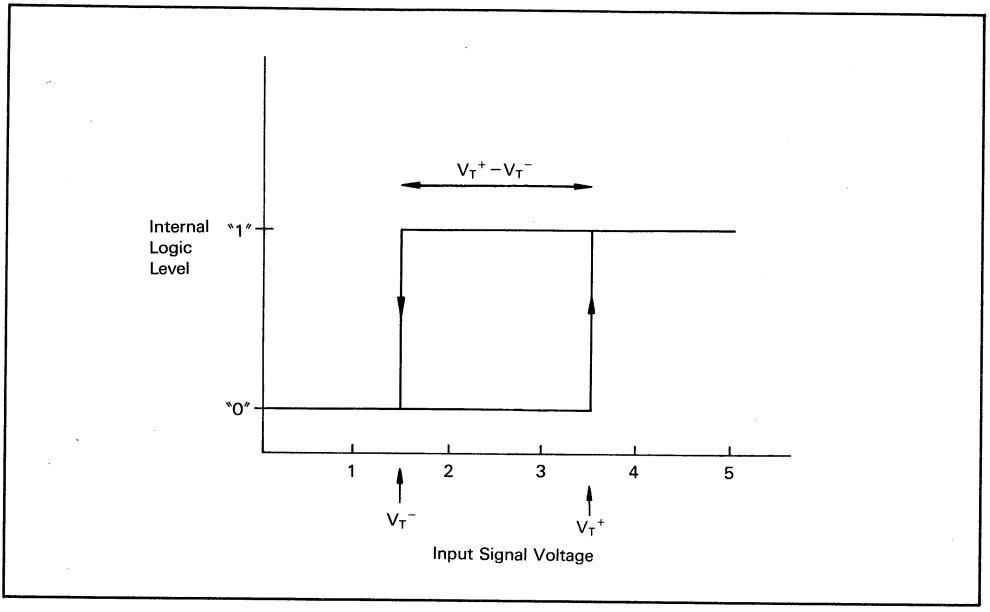


Figure 16. Schmitt Trigger Threshold Level

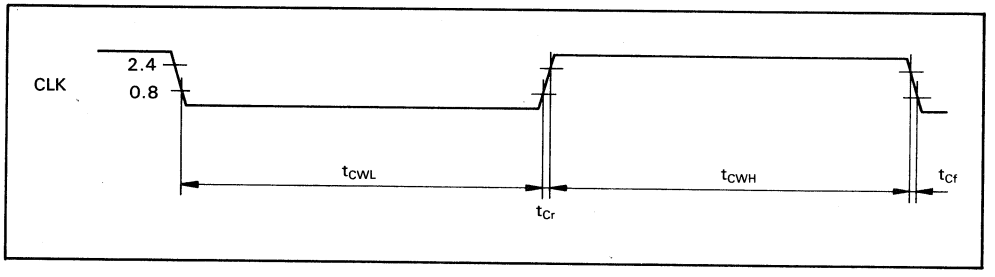
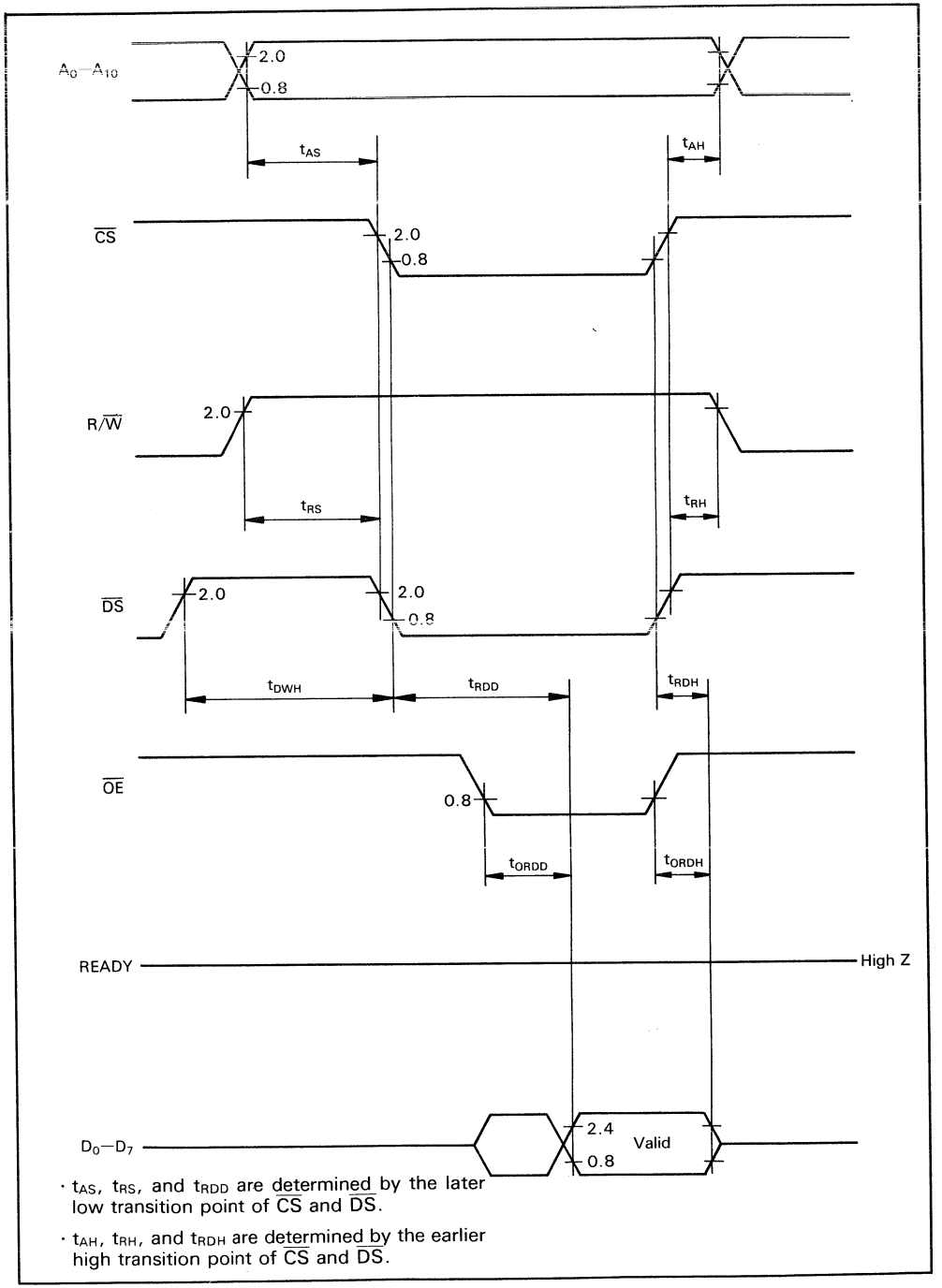
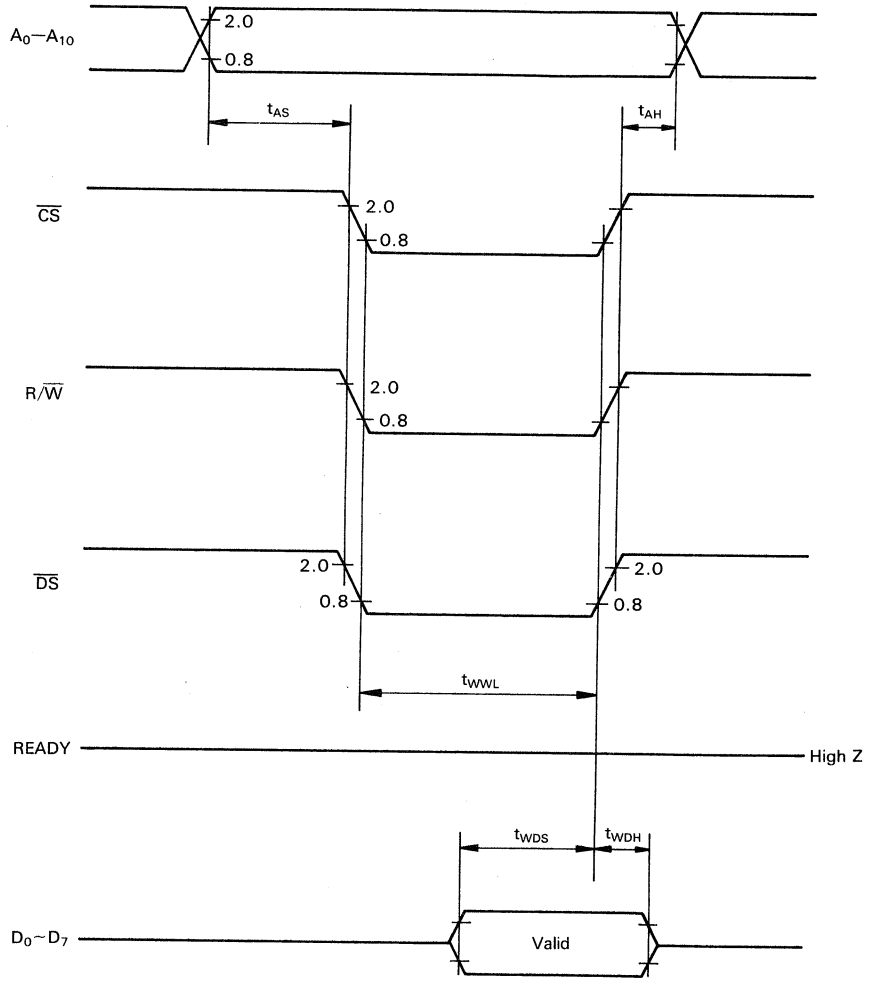


Figure 17. Output Clock Waveform



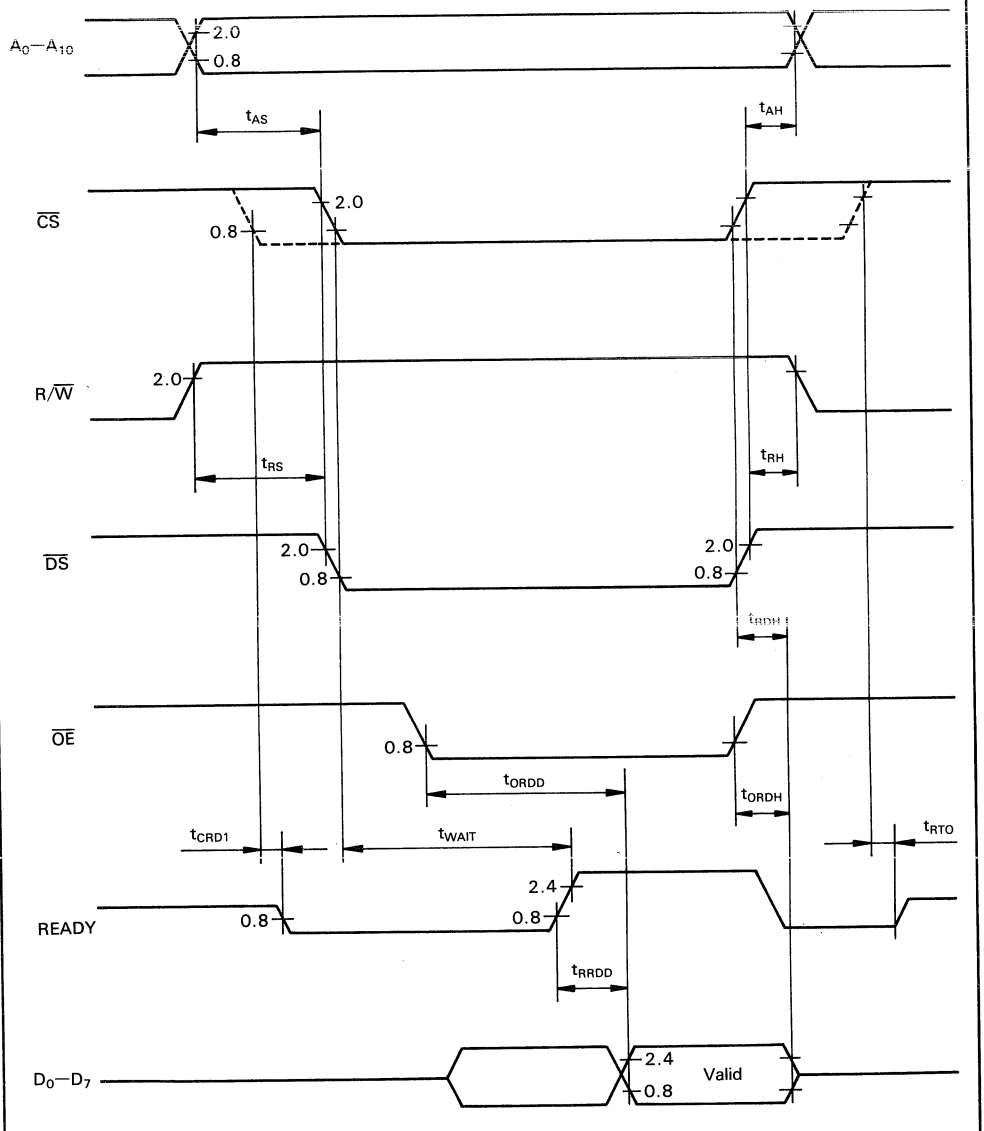
- t_{AS}, t_{RS}, and t_{RDD} are determined by the later low transition point of $\overline{CS}$ and $\overline{DS}$.
- t_{AH}, t_{RH}, and t_{RDH} are determined by the earlier high transition point of $\overline{CS}$ and $\overline{DS}$.

Figure 18. Read Cycle Bus Timing (RAM)



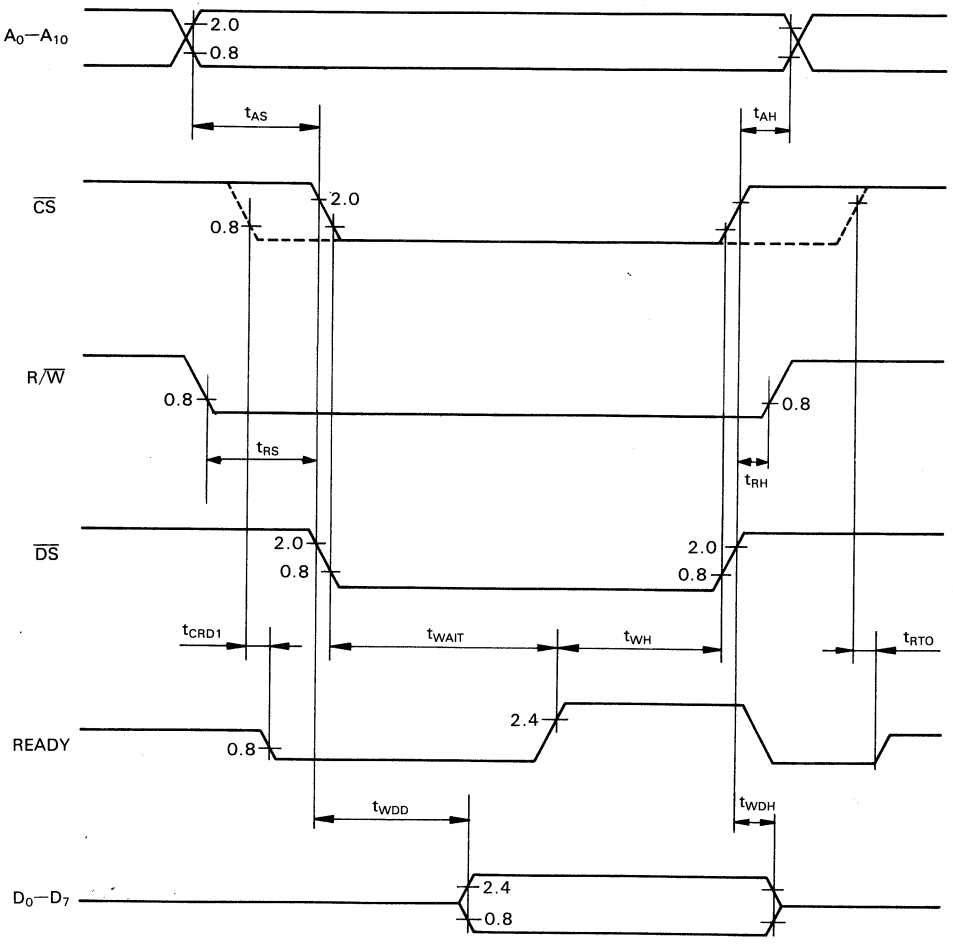
- t_{AS} is determined by the latest low transition point of $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$.
- t_{WWL} is determined by the latest low transition point and the earliest high transition point of $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$.
- t_{AH} is determined by the earliest high transition point of $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$.

Figure 19. Write Cycle Bus Timing (RAM)



- t_{AS}, t_{RS}, and t_{WAIT} are determined by the later low transition point of $\overline{CS}$ and $\overline{DS}$.
- t_{AH}, t_{RH}, and t_{RDH} are determined by the earlier high transition point of $\overline{CS}$ and $\overline{DS}$.

Figure 20. Read Cycle Bus Timing (Excluding RAM)



- t_{AS}, t_{RS}, t_{WDD}, and t_{WAIT} are determined by the latest low transition point of $\overline{CS}$, and $\overline{DS}$.
- t_{WH}, t_{RH}, t_{AH}, and t_{WDH} are determined by the earliest high transition point of $\overline{CS}$, and $\overline{DS}$.

Figure 21. Write Cycle Bus Timing (Excluding RAM)

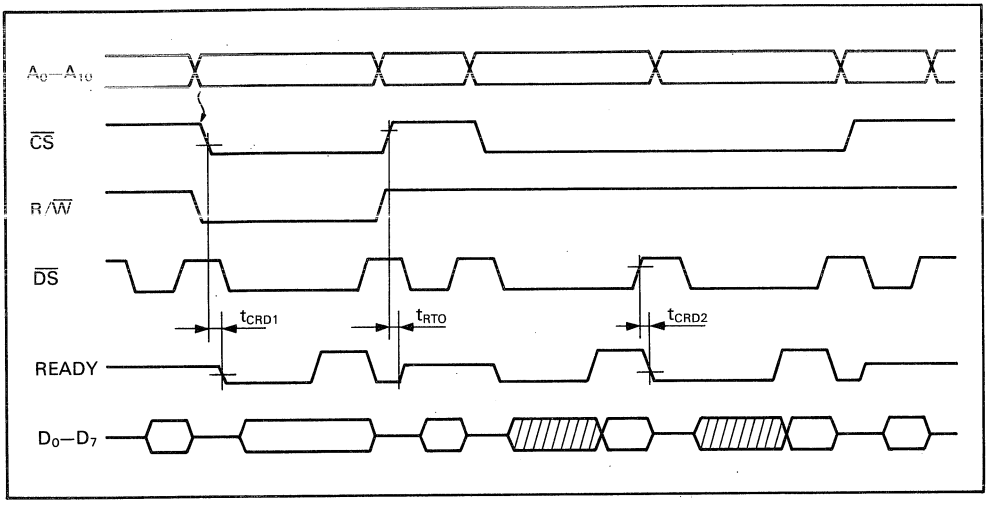


Figure 22. READY Timing for 1-Byte (Write) and 2-Byte (Read) Access

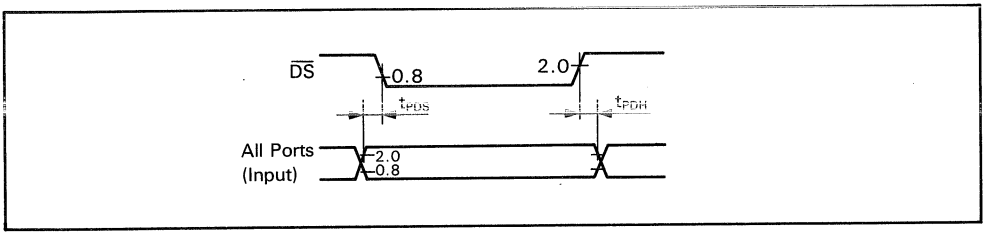


Figure 23. Port Input Timing

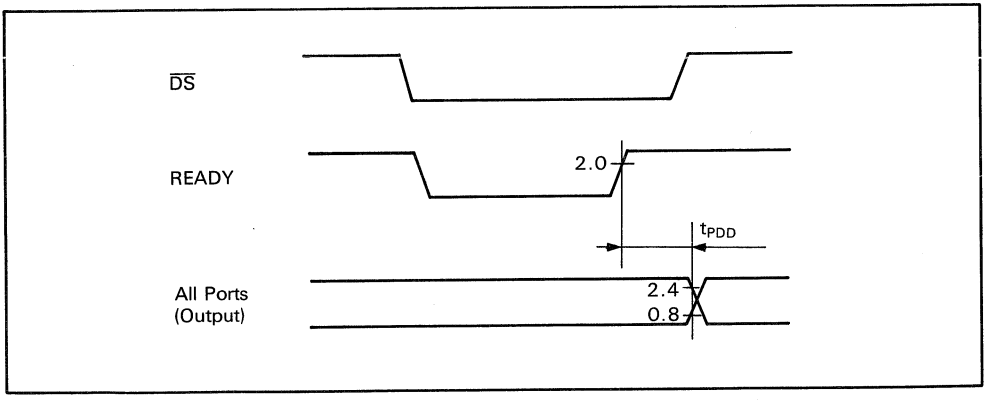
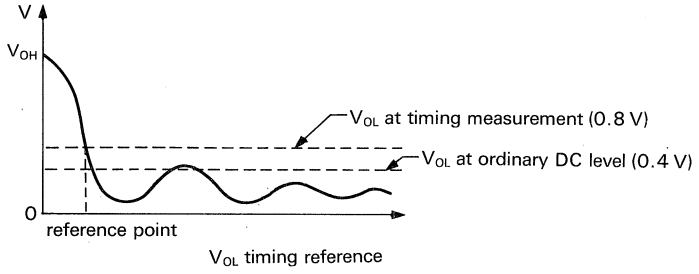


Figure 24. Port Output Timing

Timing Measurement Method

Output low voltage at measurement is 0.8 V.

Whereas ordinary output low voltage (DC characteristics) is 0.4 V.



Timing Measurement point of V_{OL}

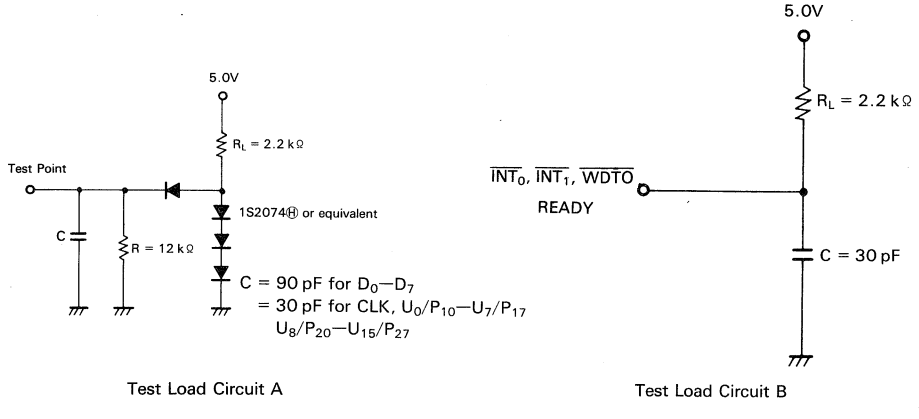


Figure 25. Test Load Cicurit

A/D Conversion (Vcc = 5.0 V, AVcc = 5.0 V, Vss = AVss = 0V, Ta = −20°C−75°C, unless otherwise noted)

Item	Min	Typ	Max	Unit
Resolution	–	10	–	bits
Non-Linearity Error	–	±1	±1.5	LSB
Offset Error	–	–	±1	LSB
Full-Scale Error	–	–	±1	LSB
Quantization Error	–	–	±0.5	LSB
Absolute Accuracy	–	±1.5	±2	LSB

Note: The external input resistance must be lower than 10 k Ω.

The definition of A/D conversion accuracy for the HD63140 is described below.

Resolution: The number of output binary digit.

Offset Error: The deviation from the ideal A/D conversion characteristics of an analog input volrage value when a digital output changes from a minimum voltage value of 000...0 to 000.....1. (Refer to figure 26)

Full-Scale Error: The deviation from the ideal A/D conversion characteristics of an analog input voltage value when digital output changes from 1111....10 to full-scale value 1111....11.

Quantization error: This error is intrinsic to A/D converters and is represented by ±0.5 LSB.

Non-Linearity Error: The deviation from the ideal A/D conversion characteristics from O V to the full-scale voltage, except for the offset error, full-scale error, and quantization error.

Absolute error: The deviation between a digital output value and analog input value. All errors from (2) to (5) are included.

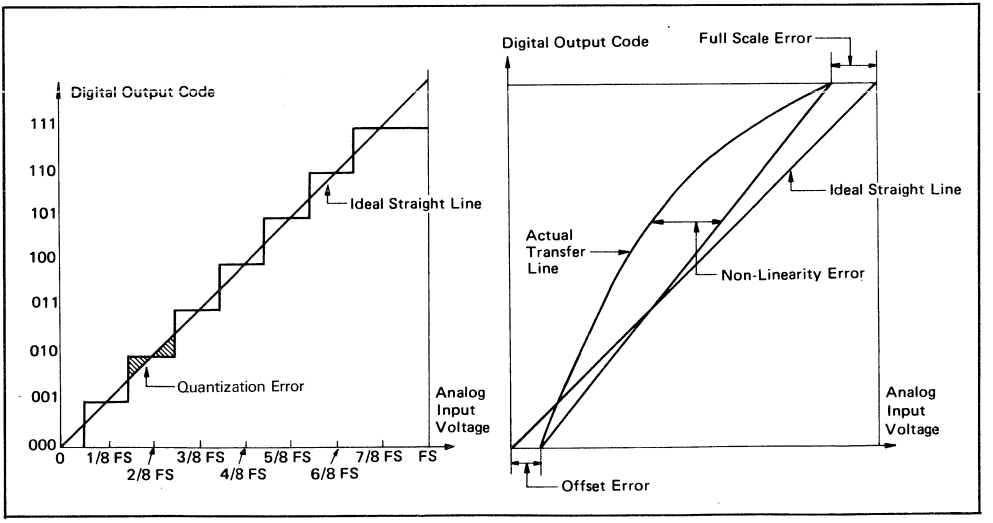


Figure 26. The Definition of A/D Conversion

Refer to application note (No. ADE-502-002) for detail of this product.

HD63143

Universal Pulse Processor (UPP-III)

Description

The Hitachi HD63143 Universal Pulse Processor is a CMOS peripheral LSI consisting of four independent modules: The universal pulse processor core (UPC), two serial communication interfaces (SCI1, SCI2), and 1024-byte RAM.

The UPC functions as a programmable pulse I/O module with a 16-bit ALU. It can realize an effective pulse I/O system suitable for versatile applications owing to 16 bit pulse I/O terminals and 24 16-bit universal registers programmable as counter, shifter, compare or capture register. The UPC automatically performs complicated pulse control through the use of 15 commands, which sharply reduces the burden on the MPU. The HD63143 supports an asynchronous bus interface and is easily to connect to the HD6301X, HD6301Y, and HD68HC000 MPUs.

Features

- Universal Pulse Processor Core (UPC)
  - 15 commands for executing pulse I/O operation
  - Up to 16 functions are programmble from the MPU into the function table (RAM)
  - 24 16-bit universal registers (UDR)
  - 16 I/O terminals (8 internal registers for pulse I/O control are also provided)
  - Interrupts can occur at the falling or rising edge of all pulse signals
  - Pulse width resolution is 5 μs when executing 16 commands at 4 MHz operating frequency
- Serial Communication Interface 1 (SCI1)
  - Selectable as asynchronouse mode (8 transmit formats) or clock synchronouse mode
- Serial Communication Interface 2 (SCI2)
  - Clock synchronouse mode
- RAM
  - 1024-byte static RAM
- Low Power Dissipation
  - Low power dissipation due to CMOS process
  - Standby mode is available

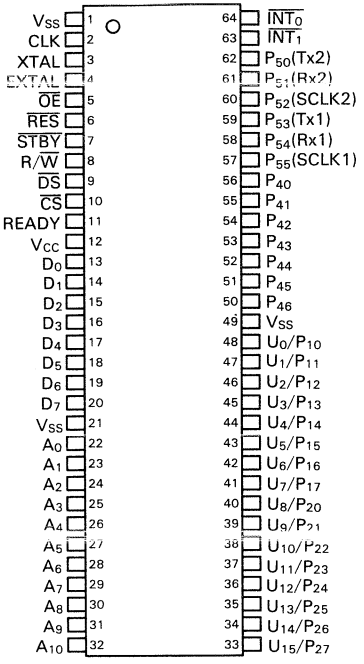
Ordering Information

Type No.	Max Operating Frequency	Clock Circuit	On-chip Clock Oscillator	External Clock Operation	Package
HD63143 A00 PS	4.0MHz*	Divide-by-4 Circuit	Yes	Available	64-pin plastic shrink DIP (DP-64S)
HD63143 B00 PS	4.0MHz**	Divide-by-2 Circuit	No	Available	64-pin plastic shrink DIP (DP-64S)
HD63143 A00 CP	4.0MHz*	Divide-by-4 Circuit	Yes	Available	68 pin PLCC (CP-68)
HD63143 B00 CP	4.0MHz**	Divide-by-2 Circuit	No	Available	68 pin PLCC (CP-68)

* 16MHz crystal or 16MHz external clock
** 8MHz external clock

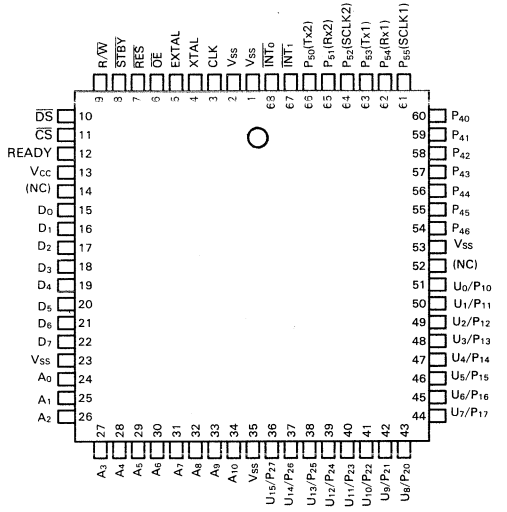
Pin Arrangement

1. 64-pin Plastic Shrink DIP



(Top View)

2. 68-pin PLCC



(Top View)

Note) NC: Non-connected pins; Nothing can be connected to NC pins.

Pin Description

Symbol	Pin No. DP-64S	CP-68	Pin Name	I/O
Vcc	12	13	Vcc	I
Vss	1, 21, 49	1, 2, 23, 35, 53	Vss	I
XTAL	3	4	XTAL	I
EXTAL	4	5	EXTAL	I
CLK	2	3	Clock	O
$\overline{RES}$	6	7	Reset	I
$\overline{STBY}$	7	8	Standby	I
D_0-D_7	13-20	15-22	Data bus	I/O
A_0-A_{10}	22-32	24-34	Address bus	I
R/$\overline{W}$	8	9	Read/Write	I
$\overline{DS}$	9	10	Data strobe	I
$\overline{OE}$	5	6	Output enable	I
$\overline{CS}$	10	11	Chip select	I
READY	11	12	Ready	O
$\overline{INT_0}$	64	68	Interrupt 0	O (open drain)
$\overline{INT_1}$	63	67	Interrupt 1	O (open drain)
P_{40}-P_{46}	50-56	54-60	MPU Input/ output port	I/O
U_0/P_{10}-U_{15}/P_{27}	48-33	51-36	U_0/P_{10}~ U_{15}/P_{27}	I/O
P_{50}-P_{55}	57-62	61-66	SCI input/ output	I/O

Pin Function

Power Supply

V_{CC}: Power supply pin (+5 V).

V_{SS}: Ground pin: Connect all Vss to ground.

Clock

XTAL, EXTAL: A00: Connect to a crystal whose frequency is four times the operation frequency (16 MHz crystal for 4 MHz operation).

When using an external clock, its frequency should be four times the operation frequency (16 MHz clock for 4 MHz operation), and the XTAL pin must be open.

B00: The frequency of the external clock should be two times that of the internal clock (8 MHz clock for 4 MHz operation), and the XTAL pin must be open.

CLK: CLK outputs a clock signal whose frequency is twice the operation frequency (8 MHz clock for 4 MHz operation).

Reset

$\overline{RES}$: Low level input at $\overline{RES}$ initializes the LSI.

Standby

$\overline{STBY}$: Low level input at $\overline{STBY}$ stops the internal clocks and puts the LSI into standby mode; RAM's data is preserved and other circuits are reset.

MPU Interface

D_0-D_7: 8-bit bidirectional data bus.

A_0-A_{10}: Address input pins for specifying memory or registers.

R/$\overline{W}$: Controls data transfer direction between UPP and MPU. In general, R/$\overline{W}$ signal output from the MPU is connected to R/$\overline{W}$.

$\overline{DS}$: Read/write operation is performed during low level of $\overline{DS}$.

$\overline{OE}$: Controls D_0-D_7 outputs. D_0-D_7 are in high-impedance state during high level of $\overline{OE}$ even in the read cycle.

$\overline{CS}$: Read/write operations to/from memory or registers are performed during low level of

$\overline{CS}$. In general, decoded signals for MPU upper addresses are input to $\overline{CS}$.

$\overline{READY}$: Inserts a wait cycle for MPU. This is a three-state output. When accessing registers other than RAM, it enters the output state during low level of $\overline{CS}$. Except for this case, it is in high-impedance state.

$\overline{INT_0}$. Logical sum (OR) output of interrupt request registers IRR0-IRR23.

$\overline{INT_1}$: Logical sum (OR) output of interrupt request from SCI1 and SCI2.

UPP Input/Output

U_0/P_{10}-U_{15}/P_{27}: UPP pulse I/O pins. They can also be used as an MPU port according to the set data of the UPP contact enable register.

Input level of U_0/P_{10}-U_7/P_{17} is TTL, and U_8/P_{20}-U_{15}/P_{27} are Schmitt-trigger inputs.

MPU Input/Output Port

P_{40}-P_{46}: P_{40}-P_{46} are MPU I/O port. The input level is TTL compatible.

SCI Input/Output

P_{50}-P_{55}: When the SCI2 is receiving or transmitting serial data, P_{50}, P_{51}, and P_{52} transmit data, receive data, and input/output the serial clock respectively. When the SCI1 is receiving or transmitting serial data, P_{53}, P_{54}, and P_{55} transmit data, receive data, and input/output the serial clock respectively. They can also be used as MPU input/output ports with TTL-compatible input levels.

Command Table

Commands		Functions
Counter/Timer, Pulse Input Functions	FRS	Free-Running Counter/Timer with Sampling
		Performs free-running counts and captures the counter at the rising or falling edge of the specified signal.
	INS	Interval Counter/Timer with Sampling
		Counter is captured and reset at the rising or falling edge of the specified signal. (Measures pulse cycle.)
	UDS	Up-Down Counter/Timer with Sampling
		Counter counts upward or downward according to the count direction specification signal, and is captured at the rising or falling edge of the specified signal.
	GTS	Gated Counter/Timer with Sampling
		Clock signal of counter is gated by the specified signal, and the counter is captured and reset at the rising or falling edge of the gate signal.
Counter/Timer, Pulse Output Functions	FRC	Free-Running Counter/Timer witn Compare
		Performs free-running counts, and outputs the result of comparison between compare register data and counter.
	INC	Interval Counter/Timer with Compare
		If counter is the same as the compare register data, pulse is output and counter is reset. (Outputs synchronous pulse.)
	PWC	Pulse Width Counter/Timer with Compare
		Result of comparison between compare register data and counter is output while counter is counting. Counter is reset at the rising or falling edge of the specified signal.
	OSC	One Shot Counter/Timer with Compare
		Counter continuously outputs one-shot pulses from the specified edge of the specified signal until the counter becomes equal to the compare register data.
Special Counter/ Timer Functions	FFC	Fifty-Fifty Duty Cycle Counter/Timer with Compare
		Outputs 50% duty cycle pulse.
	TPC	Two Phase Up-Down Counter
		Increments or decrements counter according to the relation between two-phase pulse signals.
	GTC	Gated Counter/Timer with Compare
		The counter clock signal is gated by the specified signal, and the result of the comparison between compare register data and counter is output. Counter is reset at the specified edge of the gate signal. (Compares pulse width.)
	CTO	Combination Trigger One Shot Counter/Timer
		Counter continuously outputs one-shot pulses, ANDing trigger signal and enable signal until the counter becomes equal to the compare register data.
Shifter and Pulse I/O Functions	SIT	Shift Input
		Input signal is shifted and latched at the specified edge of the specified signal.
	SOT	Shift Output
		Outputs reloaded data, shifting or rotating it. (Outputs scan signal.)
	SPO	Shift Parallel Output
		Outputs reloaded data in parallel, shifting or rotating it.

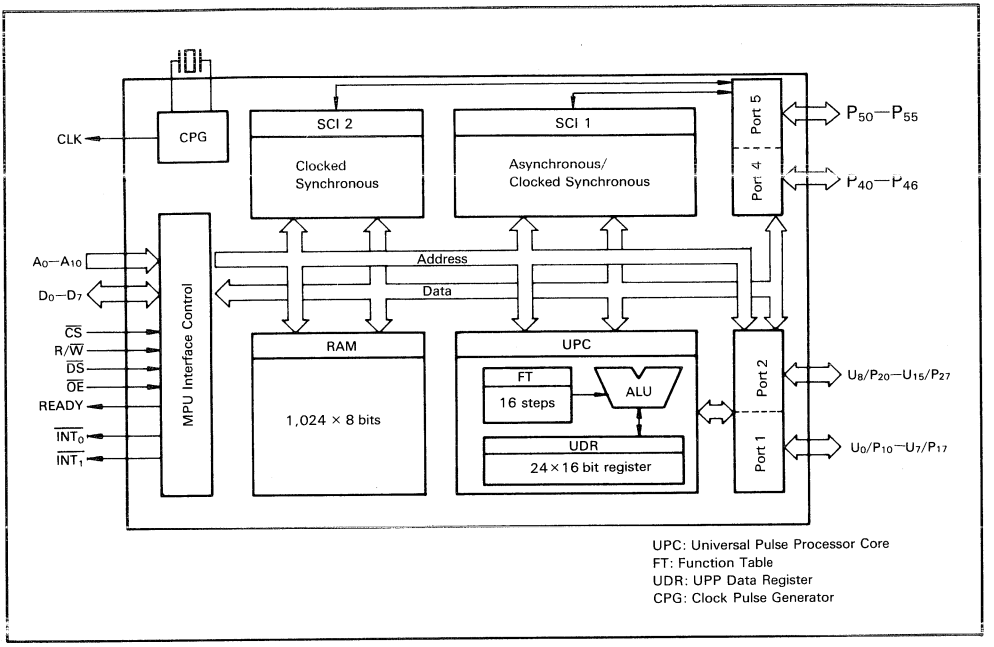
Internal Registers

Address (HEX)	Register Name	Symbol	R/W	Bit 7	6	5	4	3	2	1	0	State Data
000	Data Direction Register 2	DDR2	W									00
001	Data Direction Register 1	DDR1	W									00
002	Port2 Data Register	PORT2	R/W									*
003	Port1 Data Register	PORT1	R/W									*
004	Data Direction Register 5	DDR5	W	–	–							C0
005	Data Direction Register 4	DDR4	W	–								80
006	Port5 Data Register	Port5	R/W	–	–							*
007	Port4 Data Register	Port4	R/W	–								*
00A	Rate/Mode Control Register	RMCR	R/W	TEST	CC2	CC1	CC0	–	BR2	BR1	BR0	08
00B	Tx/Rx Control and Status Register 1	TRCSR1	R/W	RDRF	ORFE	TDRE	RIE	RE	TIE	TE	–	21
00C	Tx/Rx Control and Status Register 2	TRCSR2	R/W	RDRF	ORFE	TDRE	PER	–	PEN	EOP	SBL	28
00D	Receive Data Register	RDR	R									*
00E	Transmit Data Register	TDR	W									*
00F	RAM Control Register	RAMCR	R/W	RAME	–	–	–	–	–	–	–	FF
010	UPP Control Enable Register 2	UCER2	W	UCE15	UCE14	UCE13	UCE12	UCE11	UCE10	UCE9	UCE8	00
011	UPP Control Enable Register 1	UCER1	W	UCE7	UCE6	UCE5	UCE4	UCE3	UCE2	UCE1	UCE0	00
012	UPP Output Register 2	UOR2	W	U15	U14	U13	U12	U11	U10	U9	U8	*
013	UPP Output Register 1	UOR1	W	U7	U6	U5	U4	U3	U2	U1	U0	*
014	Next Data Enable Register	NDER	W									00
016	Next Data Register	NDR	W									*
018	SCI2 Control Register	SCR	R/W	SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0	00
019	SCI2 Status Register	SSR	R/W	SSR7	SSR6	SSR5	SSR4	SSR3	–	–	–	37
01A	SCI2 Data Register	SDR	R/W									*
020	UPP System Control Register	USCR	R/W	TST	TST	TST	TST	–	TST	GFE	UROME	08
021	Maximum Function Number Register	MFNR	R/W	–	–	–	MFN4	MFN3	MFN2	MFN1	MFN0	*
022	Function Number Register	FNR	R/W	–	–	–	FN4	FN3	FN2	FN1	FN0	*
023	Command Register	CMR	R/W	CMD3	CMD2	CMD1	CMD0	OM3	OM2	OM1	OM0	*
024	Register Assignment Register A	RASRA	R/W	–			CTN4	CTN3	CTN2	CTN1	CTN0	*
025	Register Assignment Register B	RASRB	R/W	–	–	–	CCN4	CCN3	CCN2	CCN1	CCN0	*
026	I/O Assignment Register A	IOARA	R/W	–	FEDGA	FEDGA	CPN4	CPN3	CPN2	CPN1	CPN0	*
027	I/O Assignment Register B	IOARB	R/W	–	FEDGB	FEDGB	SPN4	SPN3	SPN2	SPN1	SPN0	*
028	I/O Assignment Register C	IOARC	R/W	–	–	–	LPNA4	LPNA3	LPNA2	LPNA1	LPNA0	*
029	I/O Assignment Register D	IOARD	R/W	–	–	–	LPNB4	LPNB3	LPNB2	LPNB1	LPNB0	*
02A	Interrupt Enable Register 3	IER3	R/W	IRE23	IRE22	IRE21	IRE20	IRE19	IRE18	IRE17	IRE16	00
02B	Interrupt Enable Register 2	IER2	R/W	IRE15	IRE14	IRE13	IRE12	IRE11	IRE10	IRE9	IRE8	00
02C	Interrupt Enable Register 1	IER1	R/W	IRE7	IRE6	IRE5	IRE4	IRE2	IRE2	IRE1	IRE0	00
02D	Interrupt Request Register 3	IRQR1	R	IRR23	IRR22	IRR21	IRR20	IRR19	IRR18	IRR17	IRR16	00
02E	Interrupt Request Register 2	IRQR2	R	IRR15	IRR14	IRR13	IRR12	IRR11	IRR10	IRR9	IRR8	00
02F	Interrupt Request Register 1	IRQR1	R	IRR7	IRR6	IRR5	IRR4	IRR3	IRR2	IRR1	IRR0	00
030	Interrupt Status Register 3	ISR3	R	IRS23	IRS22	IRS21	IRS20	IRS19	IRS18	IRS17	IRS16	00
031	Interrupt Status Register 2	ISR2	R	IRS15	IRS14	IRS13	IRS12	IRS11	IRS10	IRS9	IRS8	00
032	Interrupt Status Register 1	ISR1	R	IRS7	IRS6	IRS5	IRS4	IRS3	IRS2	IRS1	IRS0	00
033	Interrupt Status Clear Register 3	ISCR3	W	IRSC23	IRSC22	IRSC21	IRSC20	IRSC19	IRSC18	IRSC17	IRSC16	00
034	Interrupt Status Clear Register 2	ISCR2	W	IRSC15	IRSC14	IRSC13	IRSC12	IRSC11	IRSC10	IRSC9	IRSC8	00
035	Interrupt Status Clear Register 1	ISCR1	W	IRSC7	IRSC6	IRSC5	IRSC4	IRSC3	IRSC2	IRSC1	IRSC0	00
036	UPP I/O Register	UIOR	R/W	U23	U22	U21	U20	U19	U18	U17	U16	*
040	UPP Data Register 0 (H)	UDR0	R/W									*
041	UPP Data Register 0 (L)	UDR0	R/W									*
042	UPP Data Register 1 (H)	UDR1	R/W									*
043	UPP Data Register 1 (L)	UDR1	R/W									*
044	UPP Data Register 2 (H)	UDR2	R/W									*
045	UPP Data Register 2 (L)	UDR2	R/W									*
046	UPP Data Register 3 (H)	UDR3	R/W									*

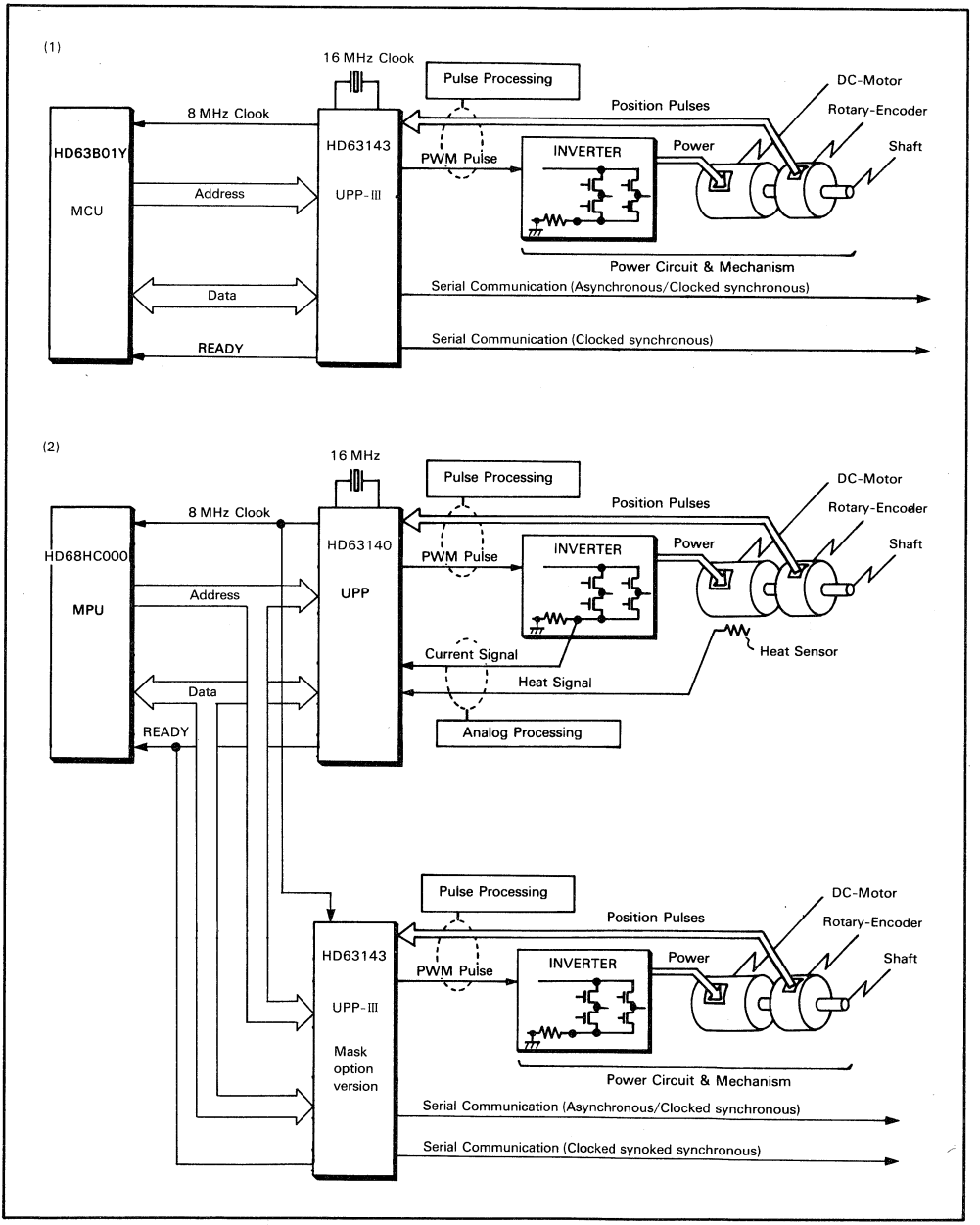
▨ : Function table
* : Undetermined
Note : Reset data of not-used bit is described "1" (which is equal to read data) in this table. Read data of write-only bits is different from reset data described in this table.

Address (HEX)	Register Name	Symbol	R/W	Bit 7	6	5	4	3	2	1	0	Reset Data
047	UPP Data Register 3 (L)	UDR3	R/W									*
048	UPP Data Register 4 (H)	UDR4	R/W									*
049	UPP Data Register 4 (L)	UDR4	R/W									*
04A	UPP Data Register 5 (H)	UDR5	R/W									*
04B	UPP Data Register 5 (L)	UDR5	R/W									*
04C	UPP Data Register 6 (H)	UDR6	R/W									*
04D	UPP Data Register 6 (L)	UDR6	R/W									*
04E	UPP Data Register 7 (H)	UDR7	R/W									*
04F	UPP Data Register 7 (L)	UDR7	R/W									*
050	UPP Data Register 8 (H)	UDR8	R/W									*
051	UPP Data Register 8 (L)	UDR8	R/W									*
052	UPP Data Register 9 (H)	UDR9	R/W									*
053	UPP Data Register 9 (L)	UDR9	R/W									*
054	UPP Data Register 10 (H)	UDR10	R/W									*
055	UPP Data Register 10 (L)	UDR10	R/W									*
056	UPP Data Register 11 (H)	UDR11	R/W									*
057	UPP Data Register 11 (L)	UDR11	R/W									*
058	UPP Data Register 12 (H)	UDR12	R/W									*
059	UPP Data Register 12 (L)	UDR12	R/W									*
05A	UPP Data Register 13 (H)	UDR13	R/W									*
05B	UPP Data Register 13 (L)	UDR13	R/W									*
05C	UPP Data Register 14 (H)	UDR14	R/W									*
05D	UPP Data Register 14 (L)	UDR14	R/W									*
05E	UPP Data Register 15 (H)	UDR15	R/W									*
05F	UPP Data Register 15 (L)	UDR15	R/W									*
060	UPP Data Register 16 (H)	UDR16	R/W									*
061	UPP Data Register 16 (L)	UDR16	R/W									*
062	UPP Data Register 17 (H)	UDR17	R/W									*
063	UPP Data Register 17 (L)	UDR17	R/W									*
064	UPP Data Register 18 (H)	UDR18	R/W									*
065	UPP Data Register 18 (L)	UDR18	R/W									*
066	UPP Data Register 19 (H)	UDR19	R/W									*
067	UPP Data Register 19 (L)	UDR19	R/W									*
068	UPP Data Register 20 (H)	UDR20	R/W									*
069	UPP Data Register 20 (L)	UDR20	R/W									*
06A	UPP Data Register 21 (H)	UDR21	R/W									*
06B	UPP Data Register 21 (L)	UDR21	R/W									*
06C	UPP Data Register 22 (H)	UDR22	R/W									*
06D	UPP Data Register 22 (L)	UDR22	R/W									*
06E	UPP Data Register 23 (H)	UDR23	R/W									*
06F	UPP Data Register 23 (L)	UDR23	R/W									*
400 ∫ 7FF	RAM		R/W									*

Internal Block Diagram



System Block Example



UPC, Port1, and Port2 Internal Registers

Universal Pulse Processor Core (UPC)

Figure 1 shows a block diagram of the UPC. The functions stored in the function table ① are sequentially read by the function number register (FNR), which has a counting function. The UPP control unit ② interprets and executes these functions by controlling the execution unit ③ (consisting of UPP data registers and an ALU) and pulse I/O ④.
HD63143 has a RAM for use as a function table. RAM must be selected by the UPP system control register. The MPU's user program can write functions to the RAM. In addition, read/write to and from all registers in UPC can be performed from the MPU, to monitor the UPC operating condition.
The number of UPP pulse inputs and outputs is 24 (U_0 to U_{23}). Among these, U_0 to U_{15} possess UPP output registers 1 and 2, and pulses can be input and output from external terminals U_0/P_{10} to U_{15}/P_{27}. U_{16} to U_{23} have no input/output terminals, and are only input/output to the internal UPP I/O registers.

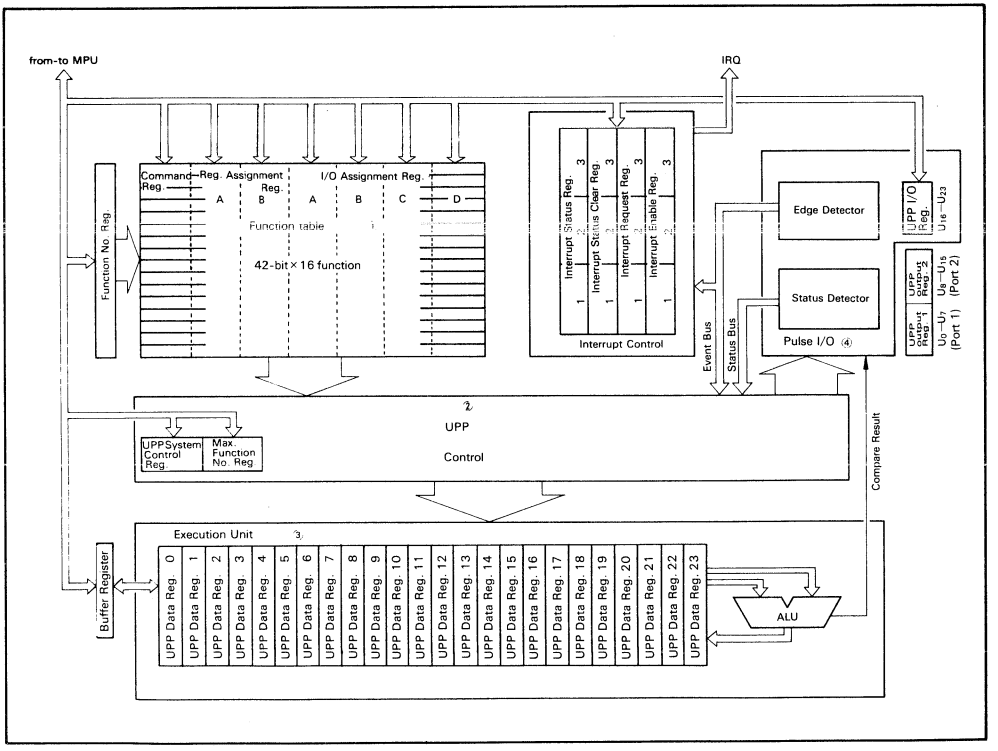


Figure 1. UPC Block Diagram

Maximum Function Number Register (MFNR)

Bit 7	6	5	4	3	2	1	0
–	–	–	MFN4	MFN3	MFN2	MFN1	MFN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 021

Bits 7-5 : Not used

MFN4-MFN0 (Maximum function number): MFN4-MFN0 bits specify the maximum value of the function number register (FNR) which is incremented from 0 during UPC operation. The number of functions to be executed and pulse width resolution are determined by specified values. The relationship between specified values and the number of functions to be executed is shown in table 1. The pulse width resoltion at 4 MHz operation is:

$$(\text{MFNR}) \times \frac{1}{\text{Operating frequency (MHz)}} = (\text{MFNR}) \times 0.25\ \mu s$$

When MFNR is 0, however, the resolution is 8 μs.

Table 1. MFNR and Number of Functions Executed

MFNR Value (MFNR)	MFN4	MFN3	MFN2	MFN1	MFN0	Number of Functions to be Executed
0	0	0	0	0	0	16
1	0	0	0	0	1	0
2	0	0	0	1	0	1
3	0	0	0	1	1	2
4	0	0	1	0	0	3
5	0	0	1	0	1	4
6	0	0	1	1	0	4
7	0	0	1	1	1	5
8	0	1	0	0	0	6
9	0	1	0	0	1	7
10	0	1	0	1	0	8
11	0	1	0	1	1	8
12	0	1	1	0	0	9
13	0	1	1	0	1	10
14	0	1	1	1	0	11
15	0	1	1	1	1	12
16	1	0	0	0	0	12
17	1	0	0	0	1	13
18	1	0	0	1	0	14
19	1	0	0	1	1	15
20	1	0	1	0	0	16
21	1	0	1	0	1	16
22	1	0	1	1	0	16
23	1	0	1	1	1	16
24	1	1	0	0	0	16
25	1	1	0	0	1	16
26	1	1	0	1	0	16
27	1	1	0	1	1	16
28	1	1	1	0	0	16
29	1	1	1	0	1	16
30	1	1	1	1	0	16
31	1	1	1	1	1	16

Function Number Register (FNR)

Bit 7	6	5	4	3	2	1	0
–	–	–	FN4	FN3	FN2	FN1	FN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 022

Bits 7-5 : Not used

FN4-FN0 (Function number): Function number register (FNR) selects functions from the function table like a program counter. During UPC operation, the FNR is automatically incremented and functions stored in the function table are read and executed sequentially. Note that FNR = 0, 5, 10, or 15 indicates cycles for the MPU to read or write the UPP data register; no functions are executed during these cycles. FNR is reset if its value becomes equal to that specified by MFNR. FNR cannot be accessed by the MPU during UPC operation, but can be when the UPC stops operation. Function numbers from 1 to 4, 6 to 9, 11 to 14, or 16 to 19 are to be specified in this register when programming functions. "UPC operation" means the state in which the GFE bit of the UPP system control register (USCR) is equal to 1.
UPC operation is started from the same FNR value as it has when a 1 is written into the GFE bit. For example, if the data of FNR when a 1 is written into the GFE bit is egual to 1, UPC operation is started from FNR = 1.

UPP System Control Register (USCR)

Bit 7	6	5	4	3	2	1	0
TST	TST	TST	TST	–	TST	GFE	UROME
W	W	W	W		R/W	R/W	R/W

Address: $ 020

TST (Test): Test bits (bit 7-bit 4) are for testing, and cannot be used for user applications; clear to 0s when setting USCR.

Bit 3: Not used

TST (Test): Test bit (bit 2) is also for testing only; clear to 0 when setting USCR.

GFE (General function enable): The UPC is in operation and executes functions when GFE = 1, and is stopped when GFE = 0. This bit is cleared by reset.

UROME (UPP ROM enable): RAM is selected as the function table when UROME = 0, and mask ROM when UROME = 1. This bit is cleared by reset.
Clear to 0 (select RAM) when setting USCR because mask ROM isn't supported.

Function Table

As shown in figure 2, the HD63143 has a RAM as a function table, and the function table consists of a command register (CMR), two blocks of register assignment registers (RASRA, RASRB), and four blocks of I/O assignment registers (IOARA, IOARB, IOARC, IOARD). Each register has 16 registers corresponding to function numbers. First, the registers in the vertical column are selected by setting numbers in FNR; next, the registers in the horizontal column are selected by address inputs. RAM function programming is enabled only when GFE is equal to 0; that is, the UPC is not in operation. (Do not set functions when UPC is in operation.) In this case, values greater than those set in FNR, or 0, must be set in MFNR.

Command Register (CMR)

Bit 7	6	5	4	3	2	1	0
CMD3	CMD2	CMD1	CMD0	OM3	OM2	OM1	OM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 023

CMD3-CMD0 (Command code): CMD3-CMD0 bits specify the command code. Refer to "UPP Commands" for each command description. Also, refer to notes on UPP command setting (1).

OM3-OM0 (Operation mode): OM3-OM0 bits specify the command contents in detail. Refer to "UPP Commands" for details.

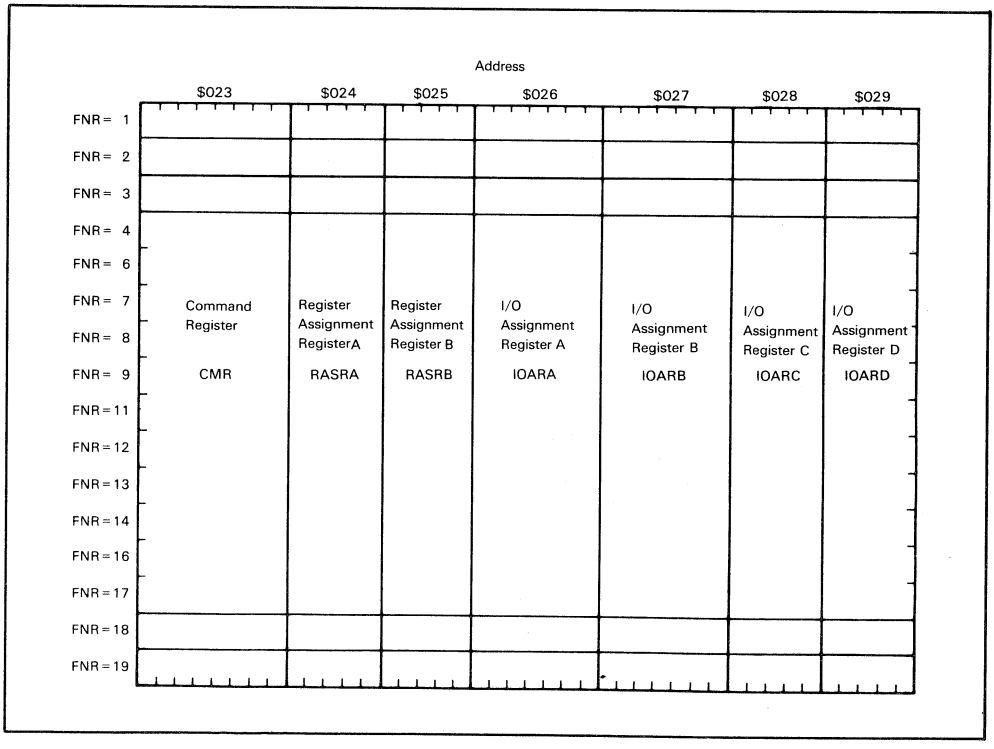


Figure 2. Function Table Configuration

Register Assignment Register A (RASRA)

Bit 7	6	5	4	3	2	1	0
–	–	–	CTN4	CTN3	CTN2	CTN1	CTN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 024

Bits 7-5 : Not used

CTN4-CTN0 (Counter/timer/shifter No.): CTN4-CTN0 bits specify the number of UPP data register (UDR) (0 to 23) to be used as a counter, timer, or shifter in each function. (A counter counts clocks specified by the I/O assignment register, and a timer counts internal clocks of periodic cycle.) The same register can be specified by other functions.

Register Assignment Register B (RASRB)

Bit 7	6	5	4	3	2	1	0
–	–	–	CCN4	CCN3	CCN2	CCN1	CCN0
			R/W	R/W	R/W	R/W	R/W

Address: $ 025

Bits 7-5 : Not used

CCN4-CCN0 (Capture/compare/reload register No.): CCN4-CCN0 bits specify the UDR number to be used as a capture register, compare register, or data register (shift command) in each function. The register numbers are 0 to 23; however, 24 to 31 are set if these registers are not used. The same register can be specified by other functions. (A register, for example, which is specified as a counter by one function, can be specified as a compare register by another function.)

I/O Assignment Register A (IOARA)

I/O assignment register A (IOARA) specifies the clock input pin number as well as the edge direction to define the external clock for a shifter or counter specified by RASRA. This register data is ignored in shift mode by an internal clock and timer mode.

Bit 7	6	5	4	3	2	1	0
–	FEDGA	REDGA	CPN4	CPN3	CPN2	CPN1	CPN0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 026

Bit 7: Not used

FEDGA (Falling edge A): When FEDGA bit is 1, counting or shifting is performed on the falling edge of the signal specified by CPN4-CPN0.

REDGA (Rising edge A): When REDGA bit is 1, counting or shifting is performed on the rising edge of the signal specified by CPN4-CPN0.

When FEDGA and REDGA are both 1, counting or shifting is performed at both edges. When FEDGA and REDGA are both 0, counting or shifting is not performed even if the function is executed.

CPN4-CPN0 (Clock/Shift clock Pin No.): CPN4-CPN0 bits specify the input pin number (0 to 23) of the clock signal for counter or shifter. (No external input/output pins are provided on 16 to 23. The bits of the UPP I/O register, which is one of internal registers, correspond to 16 to 23.)

I/O Assignment Register B (IOARB)

I/O assignment register B (IOARB) specifies the pulse input pin number as well as the edge direction for defining sampling pulse, trigger pulse, reset pulse, and data set pulse for the shifter.

Bit 7	6	5	4	3	2	1	0
–	FEDGB	REDGB	SPN4	SPN3	SPN2	SPN1	SPN0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $ 027

Bit 7: Not used

FEDGB (Falling edge B): When this bit is 1, sampling, triggering, resetting, or setting is performed on the falling edge of the signal specified by SPN4-SPN0.

REDGB (Rising edge B): When this bit is 1, sampling, triggering, resetting, or setting is performed on the rising edge of the signal specified by SPN4-SPN0.

When FEDGB and REDGB are both 1, the above operation is performed at both edges. When they are both 0, the operation is not performed.

SPN4-SPN0 (Sampling/trigger/reset/set pin no.): SPN4-SPN0 bits specify the input pin number (0 to 23)* of the sampling pulse for a capture register, trigger pulse for one-shot pulse output, reset pulse for counter, set pulse for shifter, one pulse signal for two-phase pulse counting, and gate signal.

I/O Assignment Register C (IOARC)

Bit 7	6	5	4	3	2	1	0
–	–	–	LPNA4	LPNA3	LPNA2	LPNA1	LPNA0
			R/W	R/W	R/W	R/W	R/W

Address: $ 028

Bits 7-5 : Not used

LPNA4-LPNA0 (Level pin no. A): LPNA4-LPNA0 bits specify the pulse output pin number (0 to 23).* When no pulses are output, 24 to 31 are specified.
For the TPC and SPO commands, refer to "UPP Commands" in this data sheet.

I/O Assignment Register D (IOARD)

Bit 7	6	5	4	3	2	1	0
–	–	–	LPNB4	LPNB3	LPNB2	LPNB1	LPNB0
			R/W	R/W	R/W	R/W	R/W

Address: $ 029

Bits 7-5 : Not used

LPNB4-LPNB0 (Level pin no. B): LPNB4-LPNB0 bits specify the pulse input pin number (0 to 23)* of direction setting signal for the counter or shiter, the input pin number of gate signal or tigger enable signal, and the input pin number of one pulse signal for two-phase pulse counting.

* No external input/output pins are provided on 16 to 23. The bits of the UPP I/O register, which is one of internal registers, correspond to 16 to 23.

UPP Data Registers 0-23 (UDR0-UDR23)

UDR, consisting of twenty-four 16-bit registers, can function as counter/timer, shifter, capture, or compare registers according to function settings.
The same register can be specified as referred by several functions.
UDR is accessible by the MPU while both executing functions and suspended via a 16-bit buffer register.
When a MPU write a data to the address of the UDR upper byte, the data is written into the upper byte of the buffer register. When it continuously write a data to the address of the UDR lower byte, the data is written into the lower byte of the buffer register and all the 16 bits data of the buffer register is transferred to the UDR at the same time.
During a read cycle, the reverse operation is performed. When a MPU read the UDR upper byte, all the 16 bits data of the UDR is transferred to the buffer register and then the data in the upper byte of the buffer register is read. When it continuously read the UDR lower byte, the data in the lower byte of the buffer register is read.

In this way, UDR should be read or written in the order of upper byte first and lower byte second.

Address: $40 - $06F

I/O Port

HD63143 has sixteen I/O pins (U_0/P_{10}-U_7/P_{17}, U_8/P_{20}-U_{15}/P_{27}) and an 8-bit UPP I/O register (UIOR) for pulse input and output. As shown in figure 3, these I/O pins are connected with UPP output registers (UOR1, UOR2), port data registers (Port1, Port2), UPP contact enable registers (UCER1, UCER2), and data direction registers (DDR1, DDR2). These pins can also be used as an MPU I/O port. In addition, U_8/P_{20} to U_{15}/P_{27} are connected with next data register (NDR) and next data enable register (NDER), and data set in NDR can be output at a certain timing. UIOR can be used when external output is not necessary like when using the output of one function as input for another function.

The block structure of the registers is shown in figure 4.

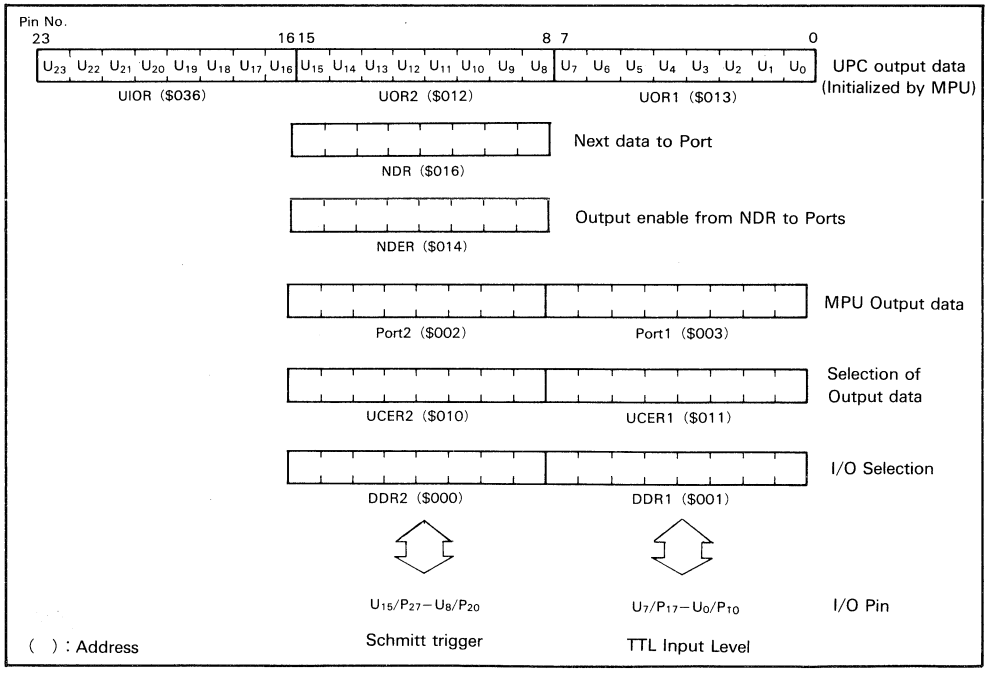


Figure 3. I/O Register Configuration

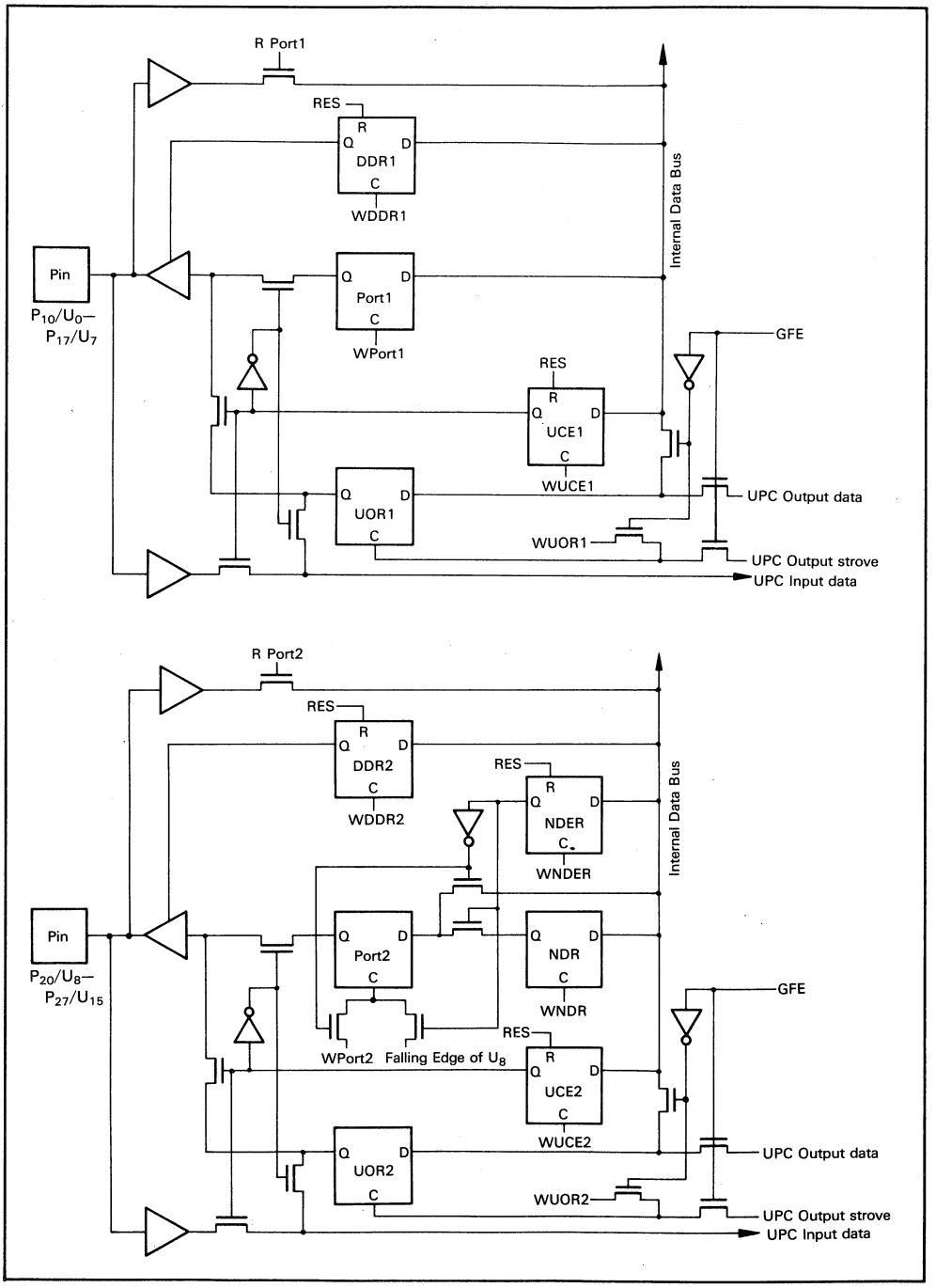


Figure 4. Block Configuration of I/O Registers

Data Direction Register 1, 2 (DDR1, DDR2): DDR1, DDR2 specify data direction of the corresponding bits of a port. Data is output when the bit is 1, and input when 0. DDR1 and DDR2 are cleared by reset.

UPP Output Register 1, 2 (UOR1, UOR2): During UPC operation, these registers cannot be accessed by the MPU since data are being stored here by the UPC. However, while the UPC is stopped, they are write accessible by the MPU. After reset, this register value is indefinite and should be initialized before setting GFE as required. These registers cannot be read directly during both operation and suspension of the UPC.

UPP I/O Register (UIOR): As the UPP I/O register has no external input/output pins, pulses cannot be input to or output from it. However it can be used for relay when the output of one function is used as the input of another function. This register is accessible by the MPU while both executing and suspending UPC operation, but when UPC is in operation, the bit specified as output of UPC cannot be set by the MPU.
After reset, this register value is indefinite and should be initialized before setting GFE as required.

Port Data Register 1, 2 (Port1, Port2): These are output data registers when I/O pins are used as an MPU port. Reading the port data registers address returns the input/output value of the pins.

UPP Contact Enable Register 1, 2 (UCER1, UCER2): UCER1, UCER2 determine whether I/O pins are used as pulse I/O pins of the UPC or as I/O ports of the MPU for each bit.

(1) Setting a UCE bit to 1 specifies the corresponding pin as a pulse I/O pin of the UPC. The corresponding contents of UOR are output onto this pin when DDR=1. If this pin is specified as an input pin of the UPC, I/O value of the pin is input regardless of DDR.

(2) When a UCE bit is 0, the corresponding pin is specified as I/O pins of the MPU port. The corresponding contents of port data register are output onto this pin when DDR=1. UOR is separated from the pin, but can be used as an I/O register of the UPC. If this pin is specified as an input pin of the UPC, the values of UOR1 and UOR2 are input.

Next Data Register (NDR): The next data register is write-enabled from the MPU. It is used when data, which was set in advance, is output in a certain timing. NDR value is output to port 2 upon transition of bit 0 of UOR2 from 1 to 0, when the next data enable register (NDER) is 1.

Next Data Enable Register (NDER): The next data enble register determines bit by bit whether data in NDR is output to port 2 or not. When a bit is 1, the corresponding data in NDR can be output to port 2, and the corresponding bit of port 2 cannot be set by the MPU. When 0, it functions as a standard port, and the NDR value is not output to port 2.

Interrupt Request

The UPC can post interrupt requests at the edge of input/output pulse U_0-U_{23}. As shown in figure 5, interrupt processing is controlled by the following four sets of registers: interrupt status registers (ISR1-ISR3), interrupt enable registers (IER1-IER3), interrupt request registers (IRQR1-IRQR3), and interrupt status clear registers (ISCR1-ISCR3). Interrupt requests from pins 0 to 23 are output to $\overline{INT_0}$.

Interruput Status Register (ISR1-ISR3): The corresponding bits of this register are set on detecting the edges of pulse signals from U_0 to U_{23}. ISR3 is set at the falling edge of the pulse signal. The upper 4 bits of ISR1 and ISR2 are set at the rising edge of the pulse signal, and lower 4 bits are set at its falling edge. This register is cleared by reset, as well as by setting the interrupt status clear register.

Interrupt Enable Register (IER1-IER3): IER1-IER3 enables or disables interrupt requests. An interrupt is generated if the corresponding bit of the interrupt status ragister is set when this register bit is 1, and it is masked when it is 0. This register is cleared by reset.

Interrupt Request Register (IRQR1-IRQR3): IRQR1-IRQR3 is set by a logical AND of the interrupt status register and the interrupt enable register. Interrupt request is allowed by logical OR between each bit of this register as shown in figure 6.

Interrupt Status Clear Register (ISCR1-ISCR3): ISCR1-ISCR3 clears the interrupt status registers. The corresponding bits of the interrupt status register are cleared by writing a 0 into this register. When a 1 is written into this register, the data of the corresponding bits of the interrupt status register are held.

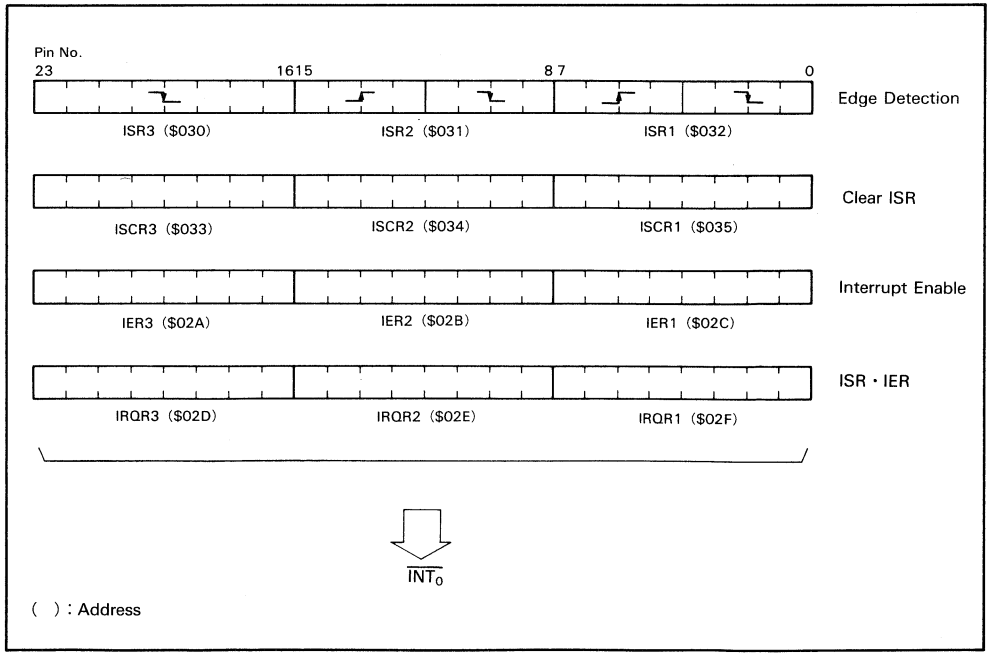


Figure 5. Interrupt Control Registers Configuration

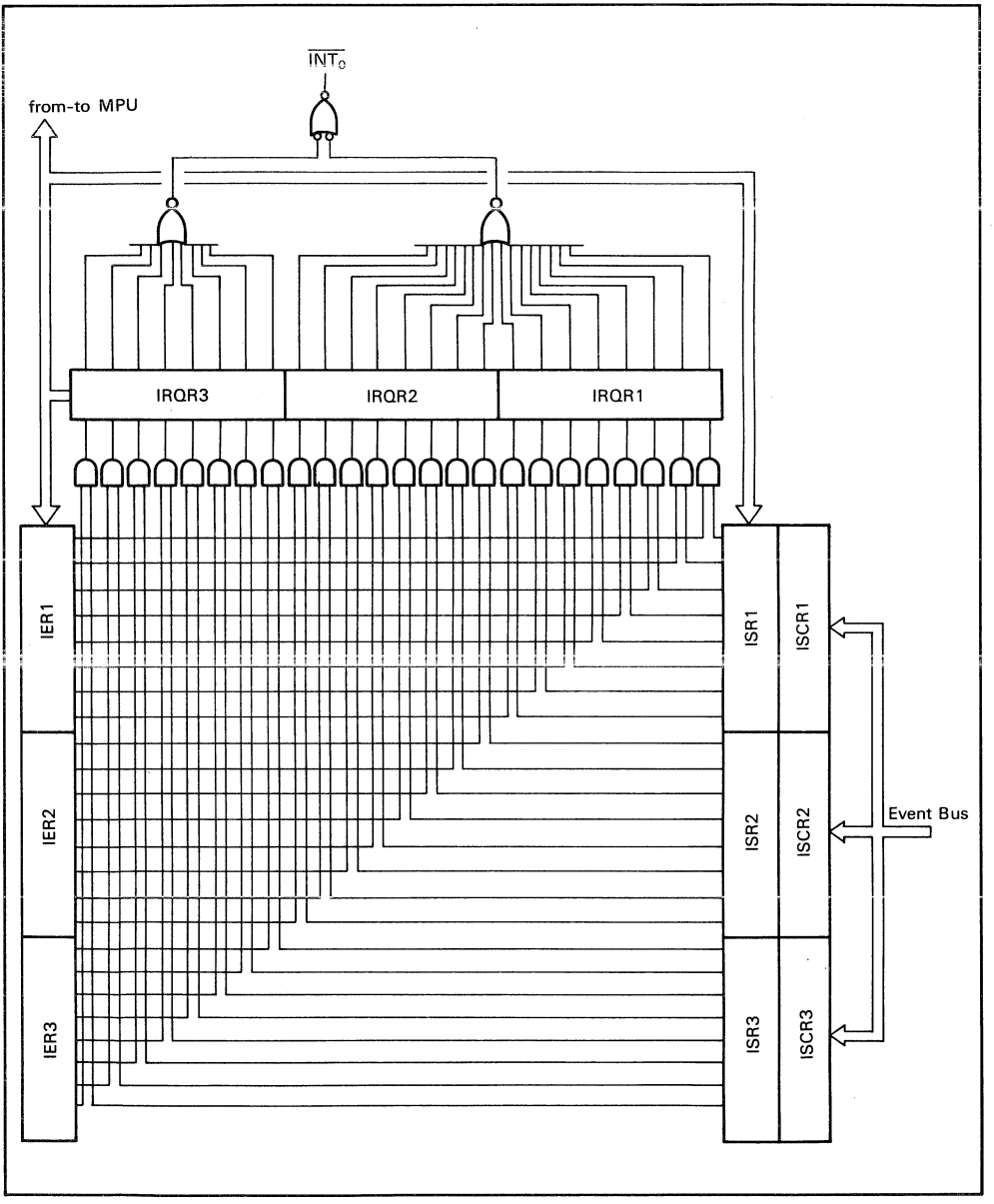


Figure 6. Block Configulation of Interrupt Control Registers

UPP Commands

Table 3 shows the function format of the UPP. The function consists of command, register assignment, and I/O assignment. In each function, register i functions as a timer, counter, or shifter. In commands other than TPC command, either of internal clock or external clock is selectable as clock for the register i by setting the bit 3 of CMR register.

For each command description in the following pages, an external clock is utilized. In this case, the value of register i is incremented, decremented or shifted upon function execution only when the specified edge of the specified signal is detected.

On the other hand, when an internal clock is utilized, the contents of IOARA defining a clock are ignored. The value of register i is incremented, decremented, or shifted upon every function execution if necessary conditions such as a gate signal are satisfied. Therefore, the apparent internal clock frequency is determined by the interval between executions of the same function which is the inverse of pulse width resolution (refer to MFNR description.)

In commands having pulse output capability, the increment or decrement of register i (which functions as a counter or timer) and the comparision between register i and compare register j are performed at the same time by the ALU. (Comparison is performed between this incremented or decremented value and register j.) Table 2 shows the relation between the value of register i (i), that of j (j), and comparison result CR. Refer to each command description for the relation between CR and output pulses. Reset value of counter or timer is 0 at both incrementation and decrementation.

Table 2. Register Data and Comparison Result

D/$\overline{U}$	Condition	Comparison Result CR
0	(i) < (j)	0
	(i) ≧ (j)	1
1	(i) ≦ (j)	0
	(i) > (j)	1

(i): Register i (counter/timer) data
(j): Register j (compare register) data

Table 3. UPP Function Format

Register	Command Register (CMR)								Register Assignment Register A (RASRA)	Register Assignment Register B (RASRB)	I/O Assignment Register A (IOARA)			I/O Assignment Register B (IOARB)			I/O Assignment Register C (IOARC)					I/O Assignment Register D (IOARD)				
Bit / Command	7	6	5	4	3	2	1	0	4 3 2 1 0	4 3 2 1 0	6	5	4 3 2 1 0	6	5	4 3 2 1 0	4	3	2	1	0	4	3	2	1	0
FRS	0	0	0	0	C/$\overline{T}$	D/$\overline{U}$	0	0	i	j	FA	RA	p	FB	RB	q	r					–				
INC	0	0	0	1	C/$\overline{T}$	D/$\overline{U}$	0	0	i	j	FA	RA	p	FB	RB	q	r					–				
UDS	0	0	1	0	C/$\overline{T}$	I/$\overline{N}$	0	0	i	j	FA	RA	p	FB	RB	q	r					s				
GTS	0	0	1	1	C/$\overline{T}$	D/$\overline{U}$	0	H/$\overline{L}$	i	j	FA	RA	p	FB	RB	s	r					s				
FRC	0	1	0	0	C/$\overline{T}$	D/$\overline{U}$	0	H/$\overline{L}$	i	j	FA	RA	p	–	–	–	r					–				
INC	0	1	0	1	C/$\overline{T}$	0	0	H/$\overline{L}$	i	j	FA	RA	p	–	–	–	r					–				
PWC	0	1	1	0	C/$\overline{T}$	0	0	H/$\overline{L}$	i	j	FA	RA	p	FB	RB	q	r					–				
OSC	0	1	1	1	C/$\overline{T}$	0	0	H/$\overline{L}$	i	j	FA	RA	p	FB	RB	q	r					–				
FFC	1	0	0	0	C/$\overline{T}$	0	0	0	i	j	FA	RA	p	–	–	–	r					–				
TPC	1	0	0	1	1	I/$\overline{N}$	0	0	i	–	FA	RA	p	FB	RB	q	p					q				
GTC	1	0	1	0	C/$\overline{T}$	D/$\overline{U}$	0	H/$\overline{L}$	i	j	FA	RA	p	FB	RB	s	r					s				
CTO	1	0	1	1	C/$\overline{T}$	0	0	H/$\overline{L}$	i	j	FA	RA	p	FB	RB	q	r					s				
SIT	1	1	0	0	E/$\overline{I}$	L/$\overline{R}$	0	0	i	j	FA	RA	p	FB	RB	q	r					–				
SOT	1	1	0	1	E/$\overline{I}$	S2	S1	S0	i	j	FA	RA	p	FB	RB	q	r					s				
SPO	1	1	1	0	E/$\overline{I}$	S2	S1	S0	i	j	FA	RA	p	FB	RB	q	04	03	02	01	00	s				
NOP	1	1	1	1	–	–	–	–	–	–	–	–	–	–	–	–	–					–				

C/$\overline{T}$ (CTR/$\overline{TMR}$) : When 0, register i functions as a timer and counts internal clock pulses. When 1, register i functions as a counter and counts the specified direction edge of signal Up.

E/$\overline{I}$ (EXT/$\overline{INT}$) : When 0, register i is shifted according to an internal clock. When 1, register i is shifted at the specified direction edge of external clock signal Up.

D/$\overline{U}$ (DWN/$\overline{UP}$) : When 0, register i functions as an up-counter. When 1, register i functions as a down-counter.

I/$\overline{N}$ (INV/$\overline{NINV}$) : Controls counting direction of a counter. For details, refer to the command description.

H/$\overline{L}$ (HIGH/$\overline{LOW}$) : This bit specifies polarity of output pulse and gate signal. The polarity of the counter overflow signal is not affected by this bit. For details, refer to the command description.

L/$\overline{R}$ (LEFT/$\overline{RIGHT}$) : When 0, register i is shifted to right. When 1, register i is shifted to left.

i : Number of UDR functioning as a counter/timer or shifter.

j : Number of UDR functioning as a capture register, compare register, or data register (shift command).

p: Clock input pin No.

q: Pulse input pin No.

r : Pulse output pin No.

s: Count direction control signal, gate signal, trigger enable signal, or shift direction control signal input pin No.

FA (FEDGA): Detects falling edge of signal Up when FA = 1.

RA (REDGA): Detects rising edge of signal Up when RA = 1.

FB (FEDGB): Detects falling edge of signal Uq or Us when FB = 1.

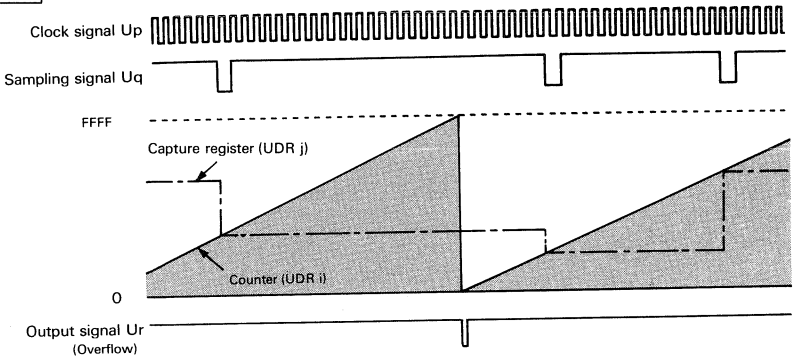
RB (REDGB): Detects rising edge of signal Uq or Us when RB = 1.

S0-S2, O0-O4: Specify the shift mode and output method of shift commands. For details, refer to the command description.

COMMAND **1. Free-Running Counter/Timer with Sampling (FRS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. Value of register i is set into register j (capture register) on detecting the specified direction edge of sampling signal Uq.
3. Overflow signal of register i is output to Ur.
   (Pulse signal counting)

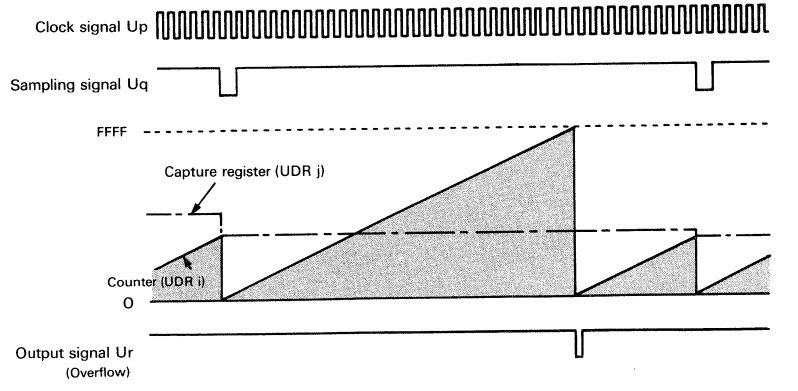
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, D/$\overline{U}$ = 0, FB = 1, RB = 0**



COMMAND **2. Interval Counter/Timer with Sampling (INS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. Value of register i is set into register j (capture register) and register i is reset on detecting the specified direction edge of sampling signal Uq.
3. Overflow signal of register i is output to Ur.
   (Pulse signal interval measurement)

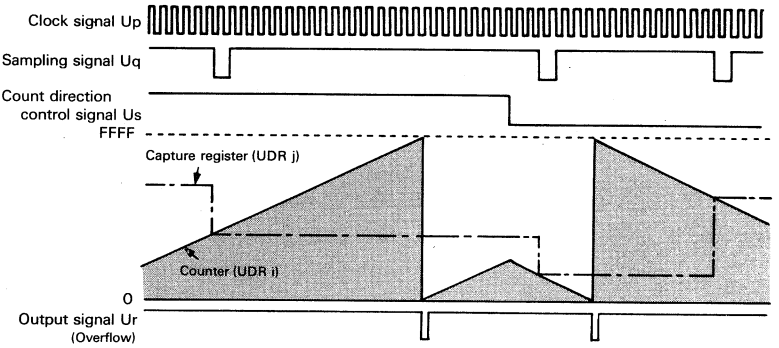
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, D/$\overline{U}$ = 0, FB = 1, RB = 0**



COMMAND **3. Up-Down Counter/Timer with Sampling (UDS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by count direction control signal Us and bit 2 ($I/\overline{N}$) of CMR.
   Incrementation is performed if $I/\overline{N} \oplus Us=1$, and decrementation if $I/\overline{N} \oplus Us=0$.
2. Value of register i is set into register j (capture register) on detecting the specified direction edge of sampling signal Uq.
3. Overflow signal of register i is output to Ur.

EXAMPLE **Program in Function Table: $C/\overline{T}$ = 1, $I/\overline{N}$ = 0, FB = 1, RB = 0**

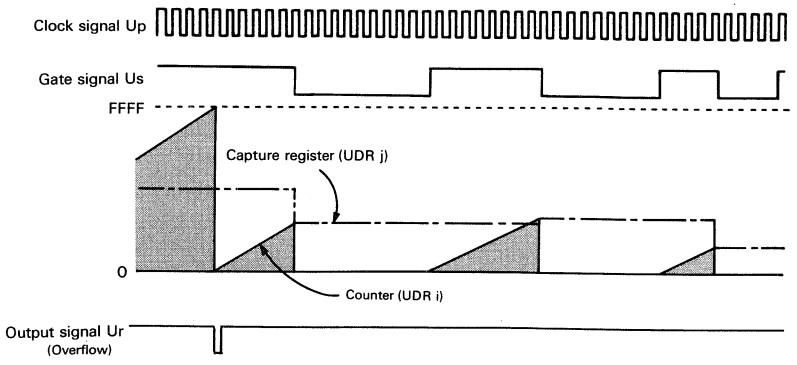


COMMAND **4. Gated Counter/Timer with Sampling (GTS)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up, when gate signal Us is set as bit 0 ($H/\overline{L}$) of the CMR. Incrementation or decrementation is determined by bit 2 of CMR.
2. Value of register i is set into register j (capture register) and register i is reset on detecting at the specified direction edge of signal Uq.
3. Overflow signal of register i is output to Ur.

(Gate width measurement)

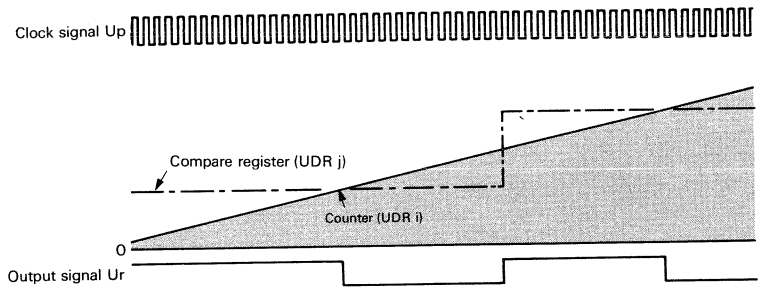
EXAMPLE **Program in Function Table: $C/\overline{T}$ = 1, $D/\overline{U}$ = 0, $H/\overline{L}$ = 1, FB = 1, RB = 0**



COMMAND **5. Free-Running Counter/Timer with Compare (FRC)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. Comparison result CR between register i and register j (compare register) is output to Ur. Output level is specified by bit 0 of CMR, and is equal to $CR \oplus H/\overline{L}$.

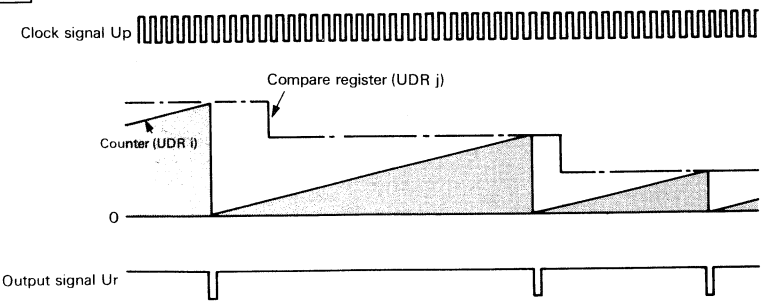
EXAMPLE **Program in Function Table: $C/\overline{T} = 1$, $D/\overline{U} = 0$, $H/\overline{L} = 0$**



COMMAND **6. Interval Counter/Timer with Compare (INC)**

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up. Incrementation or decrementation is determined by bit 2 of CMR.
2. When comparison result CR between register i and register j (compare register) is 1, the pulse signal specified by bit 0 of CMR is output to Ur and register i is reset.
   Range of register i is from 0 to (j) − 1 ((j) = the data of register j).
   Output pulse width is equal to pulse width resolution both in timer mode and counter mode.
   (Interval pulse output)

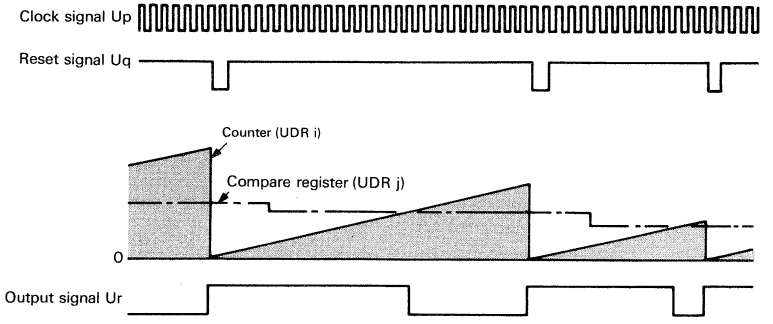
EXAMPLE **Program in Function Table: $C/\overline{T} = 1$, $H/\overline{L} = 0$**



COMMAND **7. Pulse Width Counter/Timer with Compare (PWC)**

1. The inverse of the signal level specified by bit 0 of CMR is output to Ur and register i (counter) is reset on detecting the specified direction edge of reset signal Uq.
2. Register i is incremented on detecting the specified direction edge of clock signal Up.
3. When comparison result CR between register i and register j (compare register) is 1, the output level of Ur is inverted and held until the next reset pulse is input. Register i keeps incrementing while CR=1. It is not reset while CR=0 even if a reset pulse is input. (When a reset pulse is input, the output level of Ur is inverted regardless of the value of CR. Accordingly if the value of compare register j is set to 0, the pulse width does not become 0, and a pulse having the same width as the pulse width resolution can be obtained.)

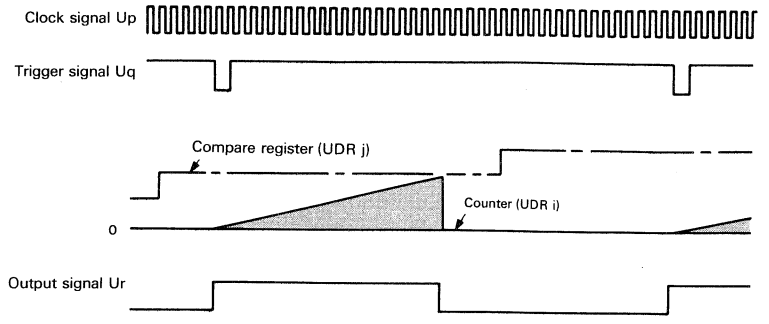
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, H/$\overline{L}$ = 0, FB = 1, RB = 0**



COMMAND **8. One Shot Counter/Timer with Compare (OSC)**

1. Counter (UDR i) starts and the inverse of the signal level specified by CMR's bit 0 is output to Ur on detecting the specified edge of trigger signal Uq, and the value of register i (counter) is incremented on detecting the specified direction edge of clock signal Up.
2. When comparison result CR between register i and register j (compare register) is 1, the output level of Ur is inverted, register i is reset, and this level is held until the next trigger signal is input.
   Even if the next trigger signal is input while CR=0, it is ignored and no trigger takes place. (Similarly to the case of PWC, if the value of compare register j is set to 0, the pulse width does not become 0, and a pulse having the same width as the pulse width resolution can be obtained.)
   (One-shot pulse output)

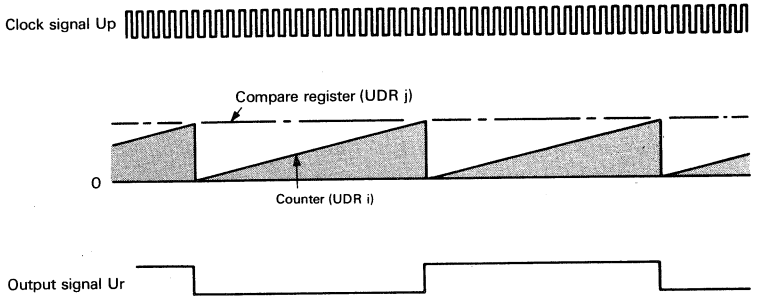
EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1, H/$\overline{L}$ = 0, FB = 1, RB = 0**



COMMAND	9. Fifty-Fifty Duty Cycle Counter/Timer with Compare (FFC)

1. Value of register i (counter) is incremented on detecting the specified direction edge of clock signal Up.
2. When comparison result CR between register i and register j (compare register) is 1, register i is reset and the output level of Ur is inverted.
   (50% duty cycle pulse output)

EXAMPLE **Program in Function Table: C/$\overline{T}$ = 1**



COMMAND **10. Two Phase Up-Down Counter (TPC)**

Value of register i (counter) is incremented or decremented according to the phase relation between two-phase pulse signals Up and Uq, as shown in table 4. Incrementation or decrementation is determined by the specified value of I/$\overline{N}$.
(Two-phase pulse signal counting)

EXAMPLE **Program in Function Table: I/$\overline{N}$ = 0, FA=RA=FB=RB=1**

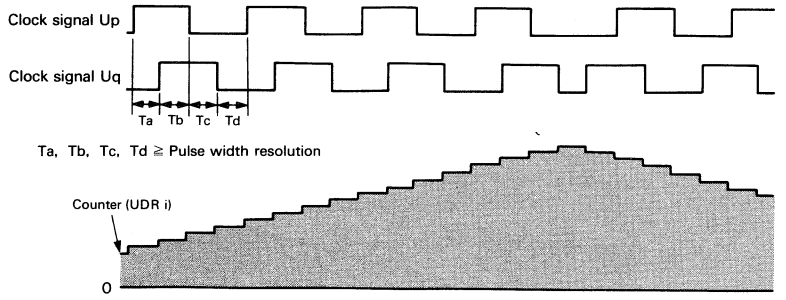


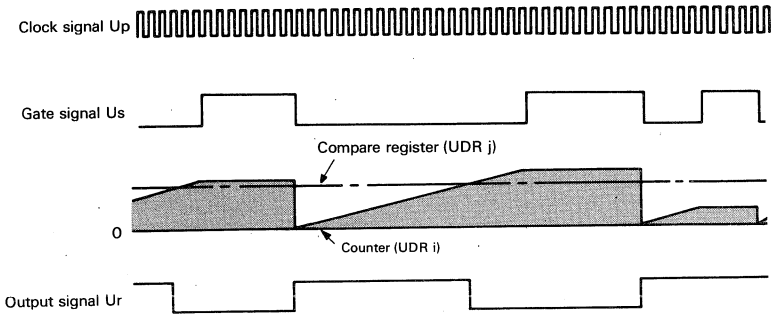
Table 4. TPC Command Function

p	q	Condition	I/$\overline{N}$=0	I/$\overline{N}$=1
↑	0	RA = 1	(i) +1 → (i)	(i) −1 → (i)
1	↑	RB = 1	(Incrementation)	(Decrementation)
↓	1	FA = 1		
0	↓	FB = 1		
↑	1	RA = 1	(i) −1 → (i)	(i) +1 → (i)
1	↓	FB = 1	(Decrementation)	(Incrementation)
↓	0	FA = 1		
0	↑	RB = 1		

COMMAND 11. Gated Counter/Timer with Compare (GTC)

1. Value of register i (counter) is incremented or decremented on detecting the specified direction edge of clock signal Up, when gate signal Us is set as specified by bit 0 of the CMR. Incrementation or decrementaion is determined by bit 2 of CMR.
2. Comparison result CR between register i and register j (compare register) is output onto Ur. The output level is specified by bit 0 of CMR, and is equal to $\overline{CR} \oplus H/\overline{L}$.
   Register i is reset at the specified direction edge of the gate signal.
   (Gate width definition)

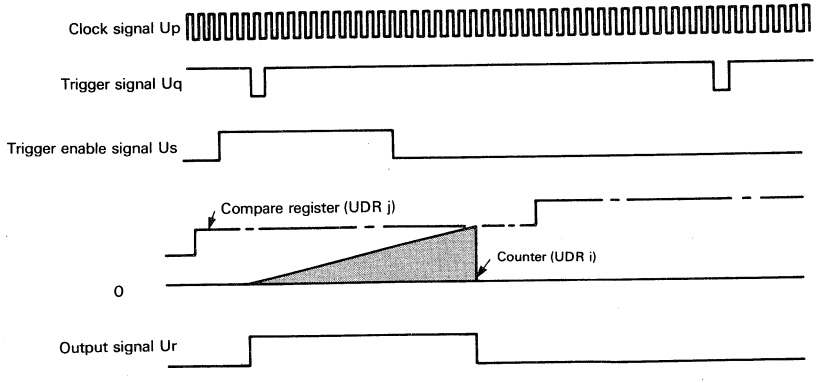
EXAMPLE **Program in Function Table: $C/\overline{T}$ = 1, $D/\overline{U}$ = 0, $H/\overline{L}$ = 0, FB = 1, RB = 0**



COMMAND 12. Combination Trigger One Shot Counter/Timer (CTO)

1. When trigger enable signal Us is 1, the inverse of the signal level specified by CMR's bit 0 is output to Ur on detecting the specified direction edge of trigger signal Uq, and then register i (counter) is incremented on detecting the specified direction edge of clock signal Up.
2. When comparision result CR between register i and register j (compare register) is 1, the output level of Ur is inverted, register i is reset, and this level of Ur is held until the next trigger signal is input.
   Even if the next trigger signal is input while CR = 0, it is ignored and no trigger takes place.
   (One-shot pulse output with trigger enable)

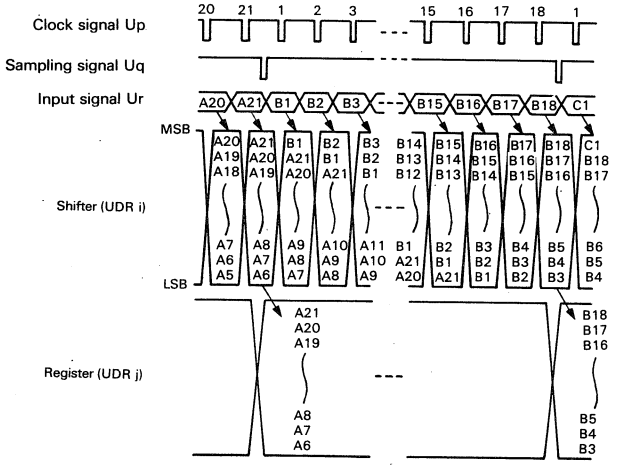
EXAMPLE **Program in Function Table: $C/\overline{T}$ = 1, $H/\overline{L}$ = 0, FB = 1, RB = 0**



COMMAND **13. Shift Input (SIT)**

1. Value of register i (shifter) is shifted and value of Ur is read to register i on detecting the specified direction edge of clock pulse Up. Shifting direction is determined by bit 2 (L/ $\overline{R}$) of CMR.
2. Value of register i is set into register j on detecting the specified direction edge of sampling pulse Uq.
   (Serial input)

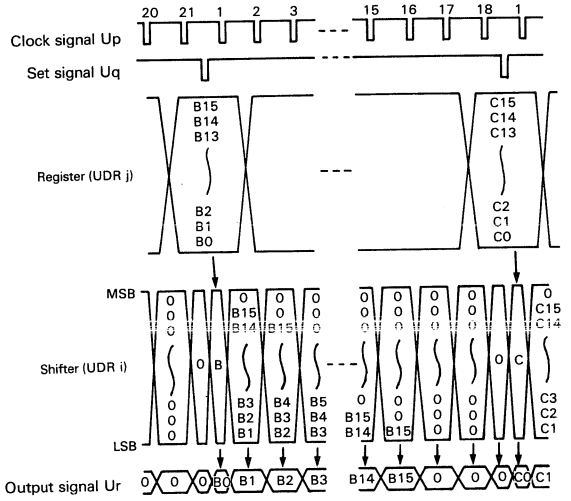
EXAMPLE **Program in Function Table: E/$\overline{I}$ = 1, L/$\overline{R}$ = 0, FA = 1, RA = 0, FB = 1, RB = 0**



COMMAND 14. Shift Output (SOT)

1. Value of register j is set into register i (shifter) on detecting the specified direction edge of set signal Uq.
2. Value of register i is shifted or rotated, and the shift output value is presented onto Ur on detecting the specified direction edge of clock signal Up.
   Mode for shift and rotation is determined by bits 2-0 of CMR as shown in table 5.
   The direction of rotation can be specified by shift direction control signal Us in certain modes as shown in table 5.
3. When S2(CMR's bit 2)=0, the LSB of register i is output to Ur, while S2=1, the MSB of register i is output to Ur.

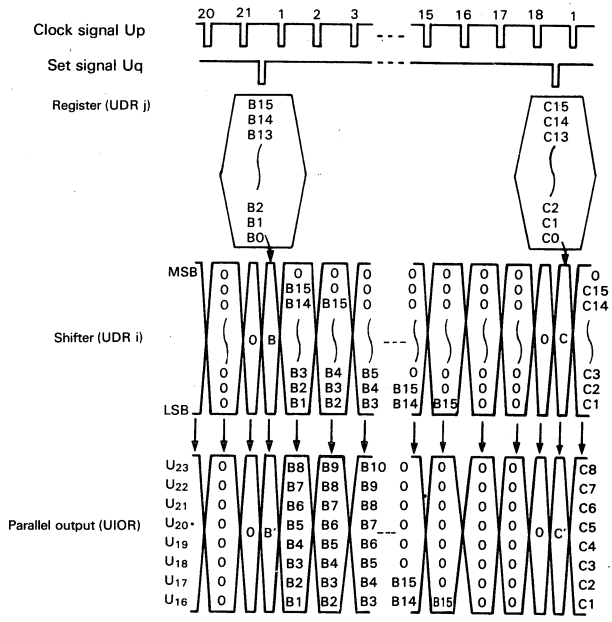
EXAMPLE **Program in Function Table: E/$\overline{I}$ = 1, S0 = S1 = S2 = 0, FA = 1, RA = 0, FB = 1, RB = 0**



COMMAND **15. Shift Parallel Output (SPO)**

1. Value of register j is set into register i (shifter) on detecting the specified direction edge of set signal Uq.
2. Value of register i is shifted or rotated and the lower 8 bits are output on detecting the specified direction edge of clock signal Up.
   Mode for shift and rotation is determined by bits 2-0 of CMR register as shown in table 5. The direction of rotation can be specified by shift direction control signal Us in certain modes as shown in table 5.
3. The lower 8 bits of the shifter are output according to the specification of IOARC. The specification method of the output is described in table 6. O4 determines the output destination, UOR1 or UIOR, and O3 to O0 are output-enable bits in 2-bit units.
   The SPO command cannot be output to UOR2.

EXAMPLE **Program in Function Table: E/$\overline{I}$ = 1, SO = S1 = S2 = 0, FA = 1, RA = 0, FB = 1, RB = 0**



Note: B′, C′ are respectively the lower 8 bits of data B and C.

Table 5. The Relationship between S0 to S2 and Shift or Rotation Mode in the SOT and SPO Commands. (Output to Ur is only for SOT.)

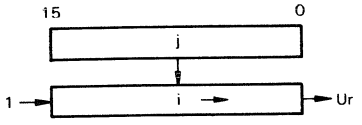
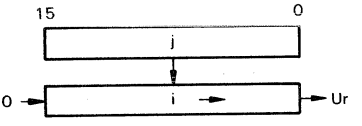
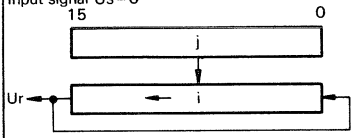
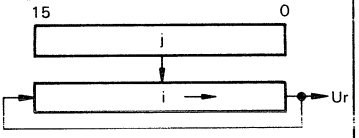
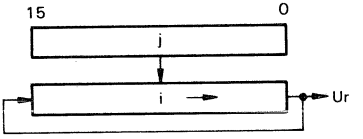
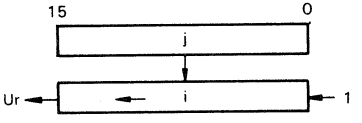
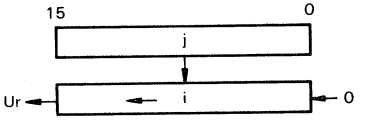
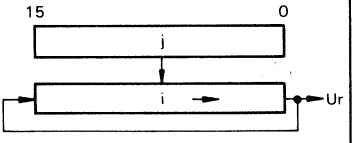
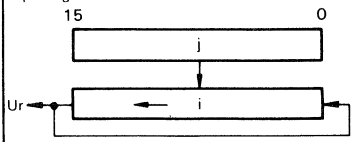
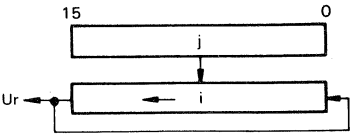
S2	S1	S0 = 1	S0 = 0
0	0		
0	1	Input signal Us=0  Input signal Us=1 	
1	0		
1	1	Input signal Us=0  Input signal Us=1 	

Table 6. Output Destination in the SPO Command

	O4 = 1	**O4 = 0**
O0=1	Shifter bit 0 → U_0	Shifter bit 0 → U_{16}
	Shifter bit 1 → U_1	Shifter bit 1 → U_{17}
O1=1	Shifter bit 2 → U_2	Shifter bit 2 → U_{18}
	Shifter bit 3 → U_3	Shifter bit 3 → U_{19}
O2=1	Shifter bit 4 → U_4	Shifter bit 4 → U_{20}
	Shifter bit 5 → U_5	Shifter bit 5 → U_{21}
O3=1	Shifter bit 6 → U_6	Shifter bit 6 → U_{22}
	Shifter bit 7 → U_7	Shifter bit 7 → U_{23}

Note: If O0 to O3 are 0, the shifter data is not output, and corresponding UOR1 and UIOR bits are not affected by the SPO command.

RAM Internal Resister

RAM Control Register (RAMCR)

Bit 7	6	5	4	3	2	1	0
RAME	–	–	–	–	–	–	–
R/W							

Address: $ 00F

RAME (RAM Enable): Writing 0 to this bit disables access to RAM (address $400-$7FF), preserving RAM data. This is useful when entering the standby mode. This bit is set to 1 by reset.

Bit 6-0: Not used

Serial Communication Interface 1

The serial communication interface 1 (SCI1) has two operating modes: asynchronous with NRZ format, and clock synchronous. The synchronous mode transfers data synchronizing with the serial clock. The asynchronous mode has eight formats with different data bit lengths, parity bits, and stop bit lengths.

The SCI1 has the following registers (figure 7):

- Transmit/receive control/status register 1 (TRCSR1)
- Transmit/receive control/status register 2 (TRCSR2)
- Rate/mode control register (RMCR)
- Receive data register (RDR)
- Receive data shift register (RDSR)
- Transmit data register (TDR)
- Transmit data shift register (TDSR)

Transmit/Receive Control Status Register 1 (TRCSR1)

7	6	5	4	3	2	1	0
RDRF	ORFE	TDRE	RIE	RE	TIE	TE	–
R	R	R	R/W	R/W	R/W	R/W	

Address: $00B

TRCSR1 is located at $00B. Bits 1-7 can be read, and bit 1-4 can be written to. TRCSR1 is initialized to $21 by reset.

RDRF (Receive Data Register Full): RDRF is set when the recieve data is transferred to the RDR without any error. Reading the RDR after reading the TRCSR1 or TRCSR2 clears the RDRF. It is cleared at reset.

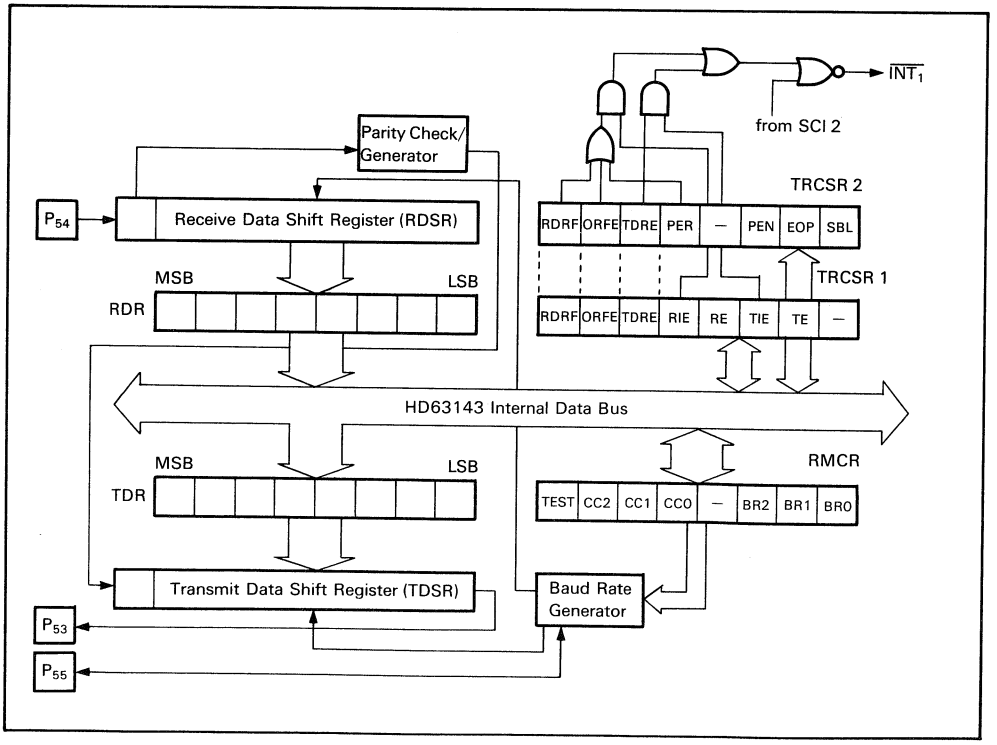


Figure 7. SCI1 Block Diagram

ORFE (Overrun/Framing Error): ORFE is set when an overrun or framing error occurs during data receive. An overrun error occurs when the next data is received while RDRF is 1. A framing error occurs when a stop bit is not 1. ORFE is set only in asynchronous mode. Reading the RDR after reading the TRCSR1 or TRCSR2 clears the ORFE. It is cleared at reset.

TDRE (Transmit Data Register Empty): In asynchronous mode, TDRE is set when the transmit data in TDR is transferred to the TDSR. In the clock synchronous mode, TDRE is set when the TDSR becomes empty. This bit is cleared by reading the TRCSR1 or TRCSR2 and writing new transmit data to the TDRE is set to 1 at reset.

RIE (Receive Interrupt Enable): Setting RIE enables RDRF, ORFE, or PER (TRCSR1 bit 6, 7 or TRCSR2 bit 4) to trigger an interrupt request ($\overline{INT_1}$). Clearing RIE inhibits the interrupt request from these flags.

RE (Receive Enable): Setting RE makes P_{54} a recieve data input pin by clearing bit 4 of DDR5.

TIE (Transmit Interrupt Enable): Setting TIE enables TDRE to trigger an interrupt request ($\overline{INT_1}$). Clearing TIE inhibits the interrupt request from TDRE.

TE (Transmit Enable): When TE is set, SCI1 transmit serial data through P_{53} after a 1-frame preamble in asynchronous mode or immediately in clock synchronous mode. TE sets bit 3 of DDR5 and P_{53} becomes a serial data output pin.

Bit 0: Not used

Rate/Mode Control Register (RMCR)

Bit 7	6	5	4	3	2	1	0
TEST	CC2	CC1	CC0	–	BR2	BR1	BR0
R/W	R/W	R/W	R/W		R/W	R/W	R/W

Address: $00A

The RMCR controls the following for SCI1:

- Baud rate
- Clock source
- Operation mode
- Data format
- P_{55} function

TEST: TEST is used for testing only and can not be used for user applications. When setting RMCR, set this bit to 0.

Tabel 7. SCI Bit Times and Baud Rates (4-MHz Operation Frequency)

BR2	BR1	BR0	Asynchronous	Clock Synchronous
0	0	0	52 μs/bit (19,230.7 Baud)	1 μs/bit
0	0	1	104 μs/bit (9,615.3 Baud)	2 μs/bit
0	1	0	208 μs/bit (4,807.6 Baud)	4 μs/bit
0	1	1	416 μs/bit (2,403.8 Baud)	8 μs/bit
1	0	0	832 μs/bit (1,201.9 Baud)	16 μs/bit
1	0	1	1664 μs/bit (600.9 Baud)	32 μs/bit
1	1	0	3328 μs/bit (300.4 Baud)	64 μs/bit
1	1	1	6656 μs/bit (150.2 Baud)	128 μs/bit

CC2-CC0 (Clock Control/Format Select): CC0, CC1, and CC2 control the clock source and data format (table 8).

Bit 3: Not used

BR2-BR0 (Baud Rate): BR2-BR0 control the baud rate used for the SCI1. Table 7 lists the available baud rates.

Transmit/Receive Control and Status Register 2 (TRCSR2)

7	6	5	4	3	2	1	0
RDRF	ORFE	TDRE	PER	–	PEN	EOP	SBL
R	R	R	R		R/W	R/W	R/W

Address: $00C

Bits 0-2 of TRCSR2 controls the transmit and recieve data format in the asynchronous mode. These bits don't affect the SCI1 operation in the synchronous mode. Bits 5-7 are the same status flugs of TRCSR1 and can also be read by accessing TRCSR1.

RDRF (Receive Data Register Full), ORFE (Overrun/Framing Error), TDRE (Transmit Data Register Empty): Refer to the explanation of TRCSR1.

PER (Parity Error): PER is set when a parity error occurs while the PEN bit is set. The PER bit is cleared by reading TRCSR2 (with PER set), followed by reading the RDR.

Bit 3: Not Used

PEN (Parity Enable): If PEN is cleared in asynchronous mode, no parity bit is generated or checked. If PEN is set, a parity bit is generated or checked. Reset clears the PEN bit.

EOP (Even/Odd Parity): When the PEN is set, EOP selects the parity bit to be generated or checked. If EOP is cleared, even parity is selected and if set, odd parity is selected. Reset clears the EOP bit.

SBL (Stop Bit Length): SBL determines the number of stop bits in the asynchronous mode. If this bit is cleared, one stop bit is used. If set, two stop bits are used. The SBL bit is cleared by reset.

Transmit Data Register (TDR)

TDR is the data register for transmission. In asynchronous mode the next data to be sent can be set after TDRE is set by transferring the old data from TDR to TDSR.

Receive Data Register (RDR)

Receive data is set in RDR. In asychronous mode, in order to avoid overrun errors, receive data should be read before the next stop bit is input.

Table 9 shows set and clear conditions of each status flag in the SCI1.

Table 8. SCI1 Format and Clock Source Control

CC2	CC1	CC0	Format	Mode	Clock Source	P_{55}
0	0	0	8-bit data	Clock synchronous	External	Clock input
0	0	1	8-bit data	Asynchronous	Internal	Not used (note 2)
0	1	0	8-bit data	Asynchronous	Internal	Clock output (note 1)
0	1	1	8-bit data	Asynchronous	External	Clock input
1	0	0	8-bit data	Clock synchronous	Internal	Clock output
1	0	1	7-bit data	Asynchronous	Internal	Note used (note 2)
1	1	0	7-bit data	Asynchronous	Internal	Clock output (note 1)
1	1	1	7-bit data	Asynchronous	External	Clock input

Note: 1. Clock is output regardless of bits TE and RE of TRCSR1.
2. Not used for SCI1.

Operation

The SCI1 must be initialized prior to operation by the following sequence to determin the operation mode (asynchronous mode or clock synchronous mode) and data format.

1. Write the desired operational code to the RMCR.
2. Write the desired operational code to the TRCSR2.
3. Set an enable bit (TE or RE) in the TRCSR1.

The enable bits (TE and RE) must be cleared before the operation mode or data format is changed. They must be set again at least one bit time (at baud rate or bit rate) after the change. If TE or RE is set within one later bit time, the SCI1 may not be initialized.

Transmit Operation in Asynchronous Mode: A data format is selected depending on the RMCR and TRCSR2. (See figure 8). Then transmit operation is enabled by TE bit in the TRCSR1. When this bit is set, the P_{53} becomes an SCI1 output (Tx1) pin, automaticaly setting the corresponding bit of DDR5, and transmission begins after a preamble consisting of 10 or 11 consecutive 1 outputs.

At this point two situations exist.

1. If the transmit data register is empty (TDRE = 1), a continuous string of 1's transmitted

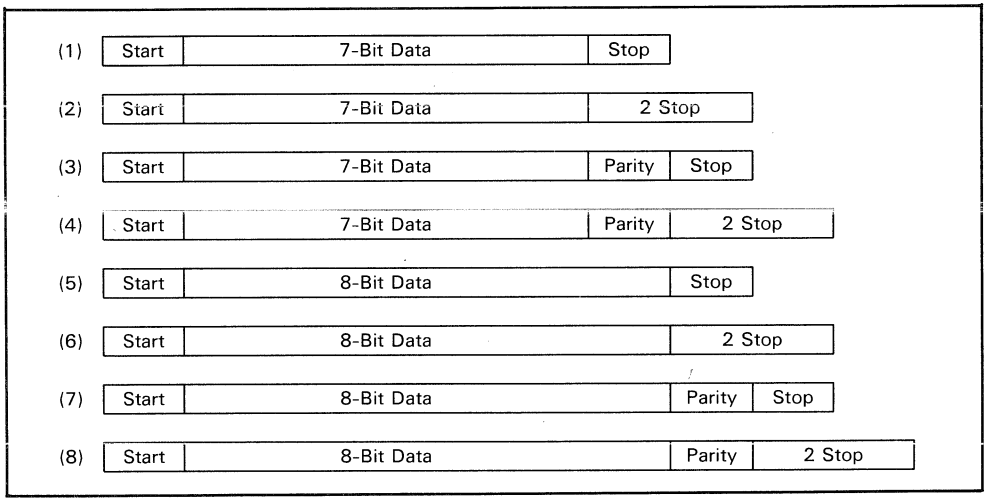


Figure 8. Asynchronous Data Format

Table 9. SCI1 Status Flags

Flag Name	Set Condition	Clear Condition
RDRF	• RDSR → RDR	• Read TRCSR1 or TRCSR2, then read RDR • $\overline{RES}$ = 0
ORFE	• Framing error (async. mode) Stop bit = 0 • Overrun error (async. mode) RDSR → RDR when RDRF = 1	• Read TRCSR1 or TRCSR2, then read RDR • $\overline{RES}$ = 0
TDRE	• TDR → TDSR (async. mode) • TDSR is empty (clock sync. mode) • $\overline{RES}$ = 0	• Read TRCSR1 or TRCSR2, then write to TDR (Clear TDRE only when TE bit= 1)
PER	• Parity error when PEN = 1 (async mode)	• Read TRCSR2, then read RDR $\overline{RES}$ = 0

Note : → : transmission

indicating an idle state.
2. If data has been stored into the TDR (TDRE = 0), the data is transferred to the TDSR and transmission begins.

SCI1 outputs a 0 start bit, 7 or 8-bit data, an odd or even parity bit if PEN is set, and finally one or two 1 stop bits.

When the TDR becomes empty, the TDRE flag bit is set by hardware.

If the MPU does not transmit data responding to this falg, 1 is transmitted instead of a 0 start bit and then 1s are transmitted until the next data is provided to the TDR. As long as the TDRE is set, 0 is not transmitted.

Receive Operation in Asynchronous Mode: First, a desired data format is selected by the RMCR and TRCSR2 and second, receive opration is enabled by the RE bit in the TRCSR1. If this bit is set, the P_{54} will be forced to an SCI1 input (Rx). The received bit stream is synchronized with the leading edge of the first 0 (space) encountered. The SCI1 input is then sampled at the approximate center of each bit time interval for ten or eleven consecutive bits. If the stop bit is not 1, a framing error is assumed and ORFE is set. The data with the framing error is also transferred to the RDR so the MPU can read the data which has caused the error. This allows a line break to be detected.

If the PEN bit is set, a parity check is performed. If a match does not occur between a parity bit and the EOP bit, a parity error is assumed and the PER bit is set instead of the RDRF bit. The data received with a parity error can be read in the same way as the data with a framing error.

The RDRF flag is set when data is received without a framing error or a parity error.

If the RDRF is still set when the stop bit of the next data is received, ORFE will be set indicating that an overrun has occurred, and the old data is held in the receive data register.
If the 7-bit data format is selected, the most significant bit of the receive data register is a 0.

If an internal clock is used with the SCI1, the follwing requirements should be satisfied:

- The CC1, CC0 bits in the RMCR must be set to 10. (See table 8.)
- Clock is generated independently of the states of the TE and the RE.
- The clock frequency is the internal bit rate × 1.

If an external clock is used with the SCI1, the following requirements must be satisfied:

- CC1, CC0 in the RMCR must be set to 11. (See table 8.)
- The clock frequency must be sixteen times (16 times) the desired baud rate.

Transmit Operation in Synchronous Mode: In synchronous mode, data is transfered synchronizing with a clock. See figure 9.

The operation mode and the clock source must be determined by setting the corresponding bits in the RMCR and TRCSR1. Then transmit operation is enabled by the TE bit in the TRCSR1. If the RE bit is set, P_{55} is forced to an output (Tx) setting the corresponding bit in DDR5.

If an external clock is selected, data is trans-

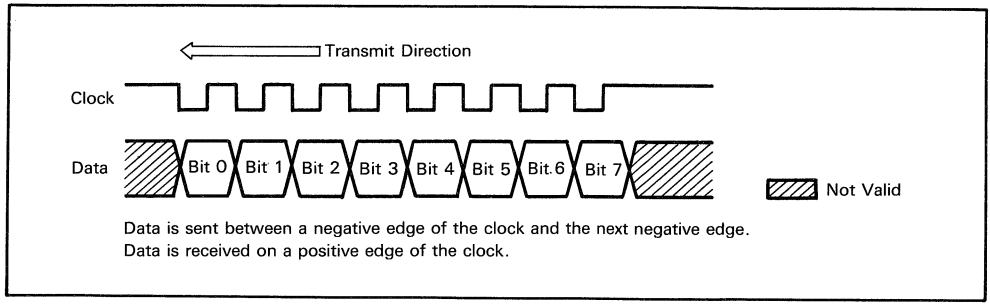


Figure 9. Synchronous Data Transmission

mitted through the P_{55} (Tx) synchronously with eight external clock pulses which are input to P_{53} (SCLK1). TDRE flag is set when the transmit data register becomes empty after transmission. If more than eight clock pulses are input, the SCI1 ignores the surplus clock pulses while TDRE is set.

If an internal clock is selected, the SCI1 outputs data and the clock when transmit data is set into TDR.

Receive Operation in Synchronous Mode: The operation mode and the clock source must be determined by the RMCR and TRCSR1. Then data reception is enabled by the RE bit in the TRCSR1. If this bit is set, the P_{54} (Rx) is forced to an SCI1 input.

If an external clock is selected, the clock should be input to P_{55} and receive data should be input to P_{54} (Rx) synchronously with the clock. The SCI1 receives eight bits into receive shift register synchronousy with the clock, and then transfers the byte to receive data register, then finally sets RDRF bit. If more than eight external clock pulses are input, the SCI1 ignores the surplus clock pulses. RDRF must be cleared when the P_{55} (SCLK) is in a high state because the SCI1 starts the next byte reception as soon as the RDRF is cleared.

If an internal clock is selected, eight clock pulses are output when RE bit is set. A byte should be input synchronizing with these clock pulses. When the first byte is received, the RDRF bit is set. Then reading the RDR causes the clock to be output and initiates the next byte reception.

Transmission and reception cannot be performed at the same time (TE and RE must not be set at the same time) in clock synchronous mode.

Serial Communication Interface 2 (SCI2)

The serial communication interface SCI2 has the following components (figure 10).

- SCI2 status register (SSR)
- SCI2 control register (SCR)
- SCI2 data register (SDR)

SCI2 Control Register (SCR)

7	6	5	4	3	2	1	0
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: $018

SCR7: When SCR7 is set to 1, the corresponding bit of DDR5 is set to 1 and P_{50} becomes the serial output pin of SCI2 (table 10). After reset, this bit is initialized to 0.

SCR6: When SCR6 is set to 1, the corresponding bit of DDR5 is set to 0 and P_{51} becomes the serial input pin of SCI2 (table 11). After reset, this bit is initialized to 0.

SCR5, SCR4: SCR5, SCR4 select a clock source (table 12). After reset, these bits are initialized to 0.

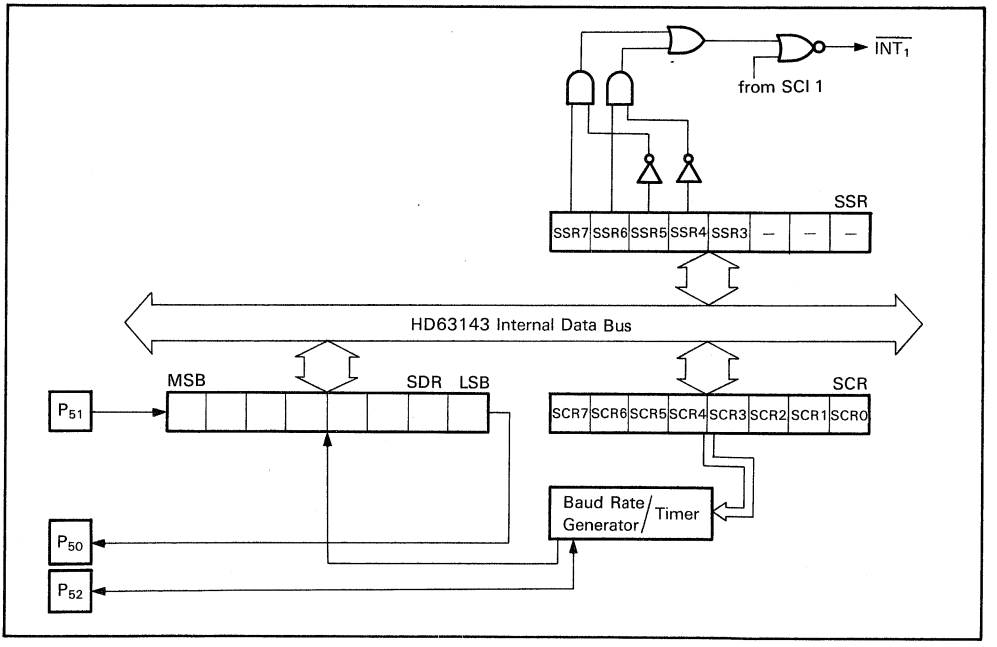


Figure 10. SCI2 Block Diagram

Table 10. P_{50} Terminal Function

SCR7	P_{50} Terminal
0	Used as I/O terminal (by DDR)
1	Serial data output (DDR output)

Table 11. P_{51} Terminal Function

SCR6	P_{51} Terminal
0	Used as I/O terminal (by DDR)
1	Serial data input (DDR input)

SCR3-SCR0: SCR3-SCR0 select a transfer clock rate (table 13). After reset, these bits are initialized to 0.

SCI2 Status Register (SSR)

7	6	5	4	3	2	1	0
SSR7	SSR6	SSR5	SSR4	SSR3			
R/W	R/W	R/W	R/W	R/W			

Address: $019

SSR7: SSR7, the SCI2 interrupt request bit, is set when transmission or reception 8-bit data is complete. It is cleared when the HD63143 is reset or data is written to or read from the SCI2 data register with the SCR5 = 1. This bit can also be cleared by writing 0 into it.

SSR6: SSR6 is the timer interrupt request bit. The timer is also used as the serial clock generator, and this bit is set on every negative edge of the internal transfer clock. When the HD63143 is reset, this bit is cleared. It can also be cleared by writing 0 into it.

SSR5: SSR5, the SCI2 interrupt mask bit, can be set or cleared by software. When this bit is 1, the SCI2 interrupt (SSR7) is masked. Resetting the HD63143 sets this bit to 1.

SSR4: SSR4, the timer interrupt mask bit, can be set or cleared by software. When this bit is 1, the timer interrupt (SSR6) is masked. Resetting the HD63143 sets this bit to 1.

SSR3: Writing 1 into SSR3 initializes the prescaler of the transfer clock generator. This bit is always read as 0.

Bit 2-Bit 0: Not used.

SCI2 Data Register (SDR)

SDR is a serial-parallel conversion register used for data transfer.

Operation

Transmit Operation: The transfer clock rate and the clock source are determined by setting the corresponding SCI2 control register bits, and then P_{50} and P_{52} are set to serial data output pin and serial clock pin respectively. The transmit data should be written into the SDR.

Then, the transmit data is output through the P_{50} pin, starting with the LSB, synchronously with the negative edge of the serial clock. When 8 bits of data have been transmitted, bit 7 of the SSR (interrupt request bit) is set on the positive edge of the last serial clock. This interrupt request can be masked by setting bit 5 of the SSR. After completion of the data transmission, the eighth data (MSB) is held at the P_{50} pin.

If the external clock source is selected, the contents of bit 0 to bit 3 of the SCR are ignored and the P_{52} pin is set as clock input pin. If the internal clock source is selected, P_{52} is set as clock output pin and a clock is output whose rate is determined by bit 0 to 3 of the SCR.

Receive Operation: The transfer clock rate and the clock source are determined by setting the corresponding SCR bits, and the P_{51} pin and the P_{52} pin are set to serial data input pin and serial clock pin respectively.

Then the receive operation is enabled by dummy-reading or writing the SDR. (This procedure is not needed after the first data is received. It is needed after reset or when no data has been received yet.) The data received through the P_{51} pin is input to the

Table 12. Clock Source

SCR5	SCR4	Clock Source	P_{52} Terminal
0	0	–	Used as I/O terminal (by DDR)
0	1	–	
1	0	Internal	Clock output (DDR output)
1	1	External	Clock input (DDR input)

Table 13. Times for Clock Rate

SCR3	SCR2	SCR1	SCR0	Bit Time (4-MHz Operating Frequency)
0	0	0	0	0.5 μs/bit
0	0	0	1	1 μs/bit
0	0	1	0	2 μs/bit
0	0	1	1	4 μs/bit
≀	≀	≀	≀	≀
1	1	1	1	16,384 μs/bit

SDR synchronously with the positive edge of the serial clock. At completion of 8-bit data reception, bit 7 in the SSR (interrupt request bit) is set. This interrupt request can be masked by setting bit 5 of the SSR.

If the external clock source is selected, the contents of bit 0 to bit 3 of the SCR is ignored and data is received sychronously with the input clock through the P_{52} pin. If the internal clock source is selected, the P_{52} becomes a clock output pin and the clock is output at the rate determined by bit 0 to bit 3 of the SCR.

Timer

The SCI2 baud rate generator can also be used as a timer. The SCI2 clock selected by bits 3 to 0 of the SCI2 control register (0.5μs to approx 16 ms in 4 MHz operation) is connected to bit 6 of the SSR, and the timer interrupt request bit is set at each falling edge of the SCI2 clock.

Port 4, Port 5

Port 4, port 5 can be used as MPU input/output ports. Also, the bits of port 5 are forced to act as serial data input pin, serial data output pin, and transmitting clock input/output pin by the control registers of SCI1 and SCI2.

Figure 11 and 12 show the block diagram of port 4 and port 5.

Data Direction Register 4, 5 (DDR4, DDR5)

DDR4, DDR5 specify data direction of the corresponding bits of each port. Data is output when the bit is 1, and input when 0. DDR4, DDR5 are cleared by reset. Note: Reset clears each bit of RMCR and causes the SCI1 to be clock synchronous mode with an exteral clock. P_{55} is forced to act as external clock input pin. When using P_{55} as MPU output port, CC1 and CC0 should be set to 0, 1 for each bit and then bit of DDR5 to 1.

Port Data Register 4, 5 (Port 4, Port 5)

Port 4 and port 5 are output data registers when port 4, 5 are used as MPU output ports. Reading this address returns the input/output values of the pins.

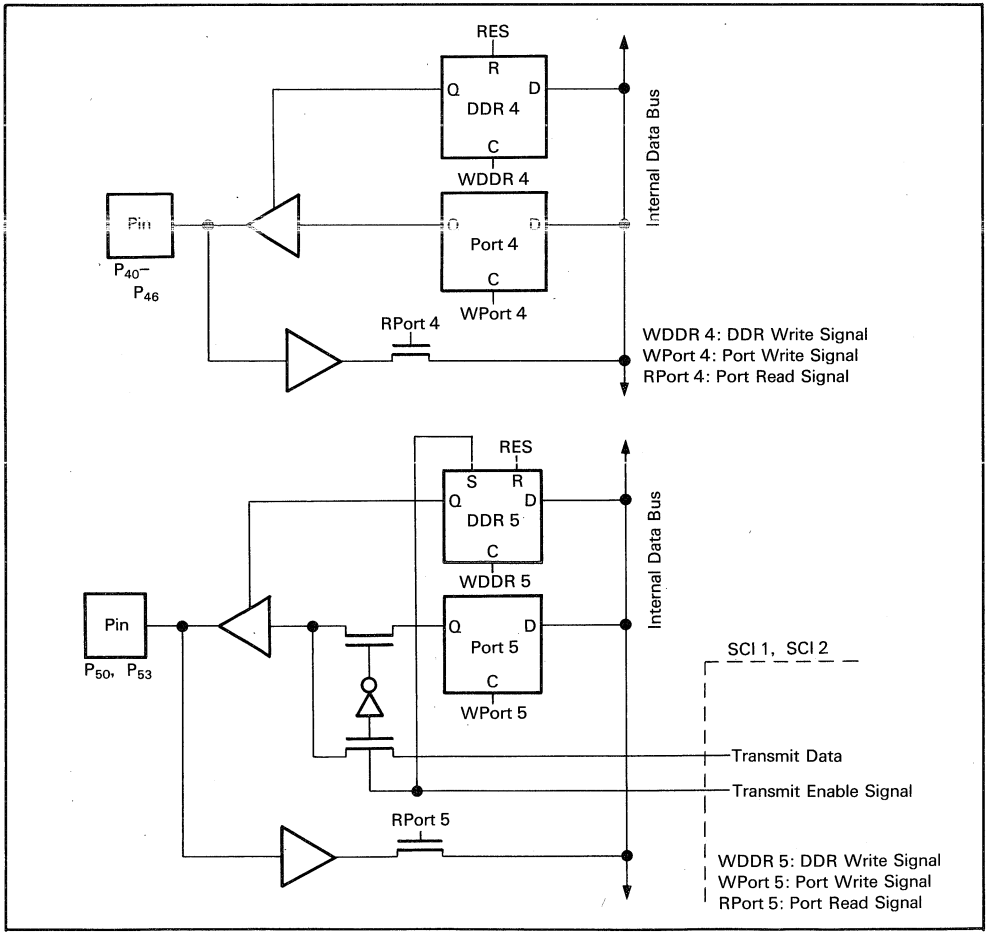


Figure 11. Port 4, Port 5 Block Diagram

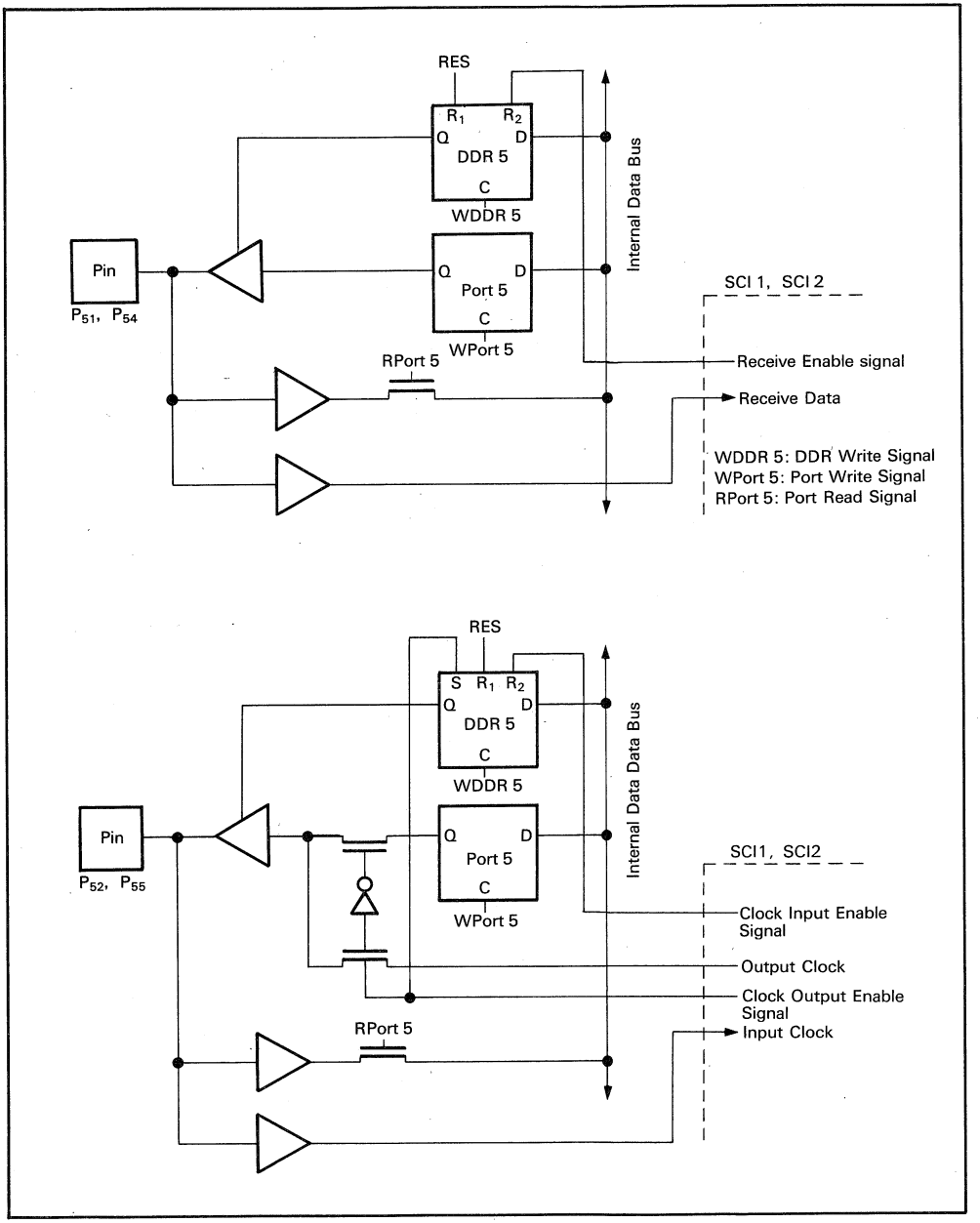


Figure 12. Port 4, Port 5 Block Diagram

Notes

Oscillator

The internal clock signal is obtained from the HD63143A00 oscillator by connecting a crystal to XTAL and EXTAL pins or by inputting an external clock to EXTAL pin. The frequency of the crystal or the external clock should be four times that of the internal clock. The oscillator's divide-by-four circuit outputs a system clock signal whose frequency is twice the operation frequency.

Figure 13 shows a crystal connection. An AT-cut parallel resonant crystal should be used. Required characteristics of the crystal (Co, Rs) and capacitance (CL_1, CL_2) are listed in the table 14.

As shown in figure 13, routing signal lines adjacent to the oscillator may result in faulty oscillation due to induction, and such a board design should be avoided. In addition, the crystal and capacitor should be positioned adjacent to XTAL and EXTAL pins. An example of board design is shown in figure 14.

When applying an external clock, the XTAL pin must be disconnected. External clock duty cycle must be 50±5%, and high level voltage must be more than $V_{CC} \times 0.7$ V.

The frequency of the external clock must be two times that of the internal clock (8 MHz clock for 4 MHz operation) in HD63143B00. With HD63143B00, clock duty cycle must be 50±5%, and high level voltage must be more than 2.0 V.

Table 14. Typical Crystal Characteristics

Item	Oscillation Frequency		
	4 MHz	4 MHz < f ≤ 12.288 MHz	12.288 MHz < f ≤ 16 MHz
Co	< 7 pF	< 7 pF	< 7 pF
Rs	< 60Ω	< 60Ω	< 35Ω
CL_1, CL_2*	10–22 pF±10%	10–22 pF±10%	10 pF±20%

* CL_1, CL_2 Contains stray capacity of wired lines.

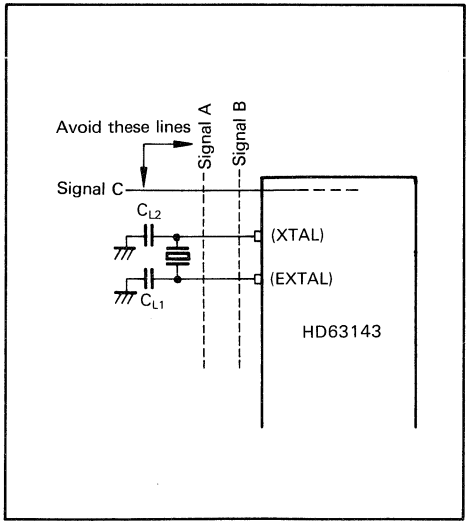


Figure 13. Crystal Connection

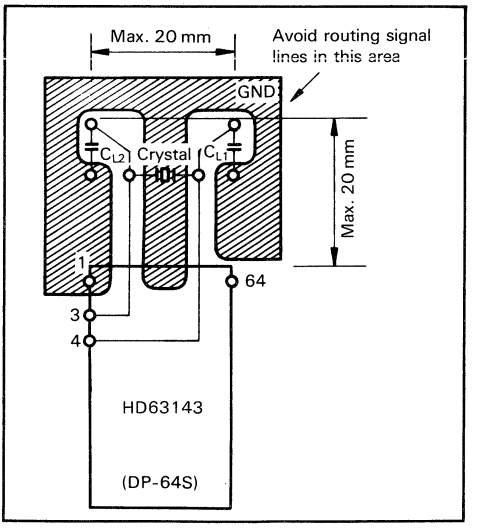


Figure 14. Typical Board Design

Standby Mode

Applying a low level to the $\overline{STBY}$ pin places the HD63143 into standby mode. In standby mode, RAM contents are preserved, all clocks of the HD63143 are inactive, and current dissipation is lowered to 15 μA or less (except for AIcc). All pins except power supply pins (V_{cc}, V_{ss}), $\overline{STBY}$, $\overline{RES}$, and XTAL (outputs low level) are disconnected from internal circuits and the LSI is reset.

HD63143 can return from standby mode by reset start. When entering standby mode with a low level on the $\overline{STBY}$ pin, it does not matter whether the $\overline{RES}$ pin is low or high; however, when returning from standby mode it must be held low until oscillation stabilization. This relationship is shown in figure 15.

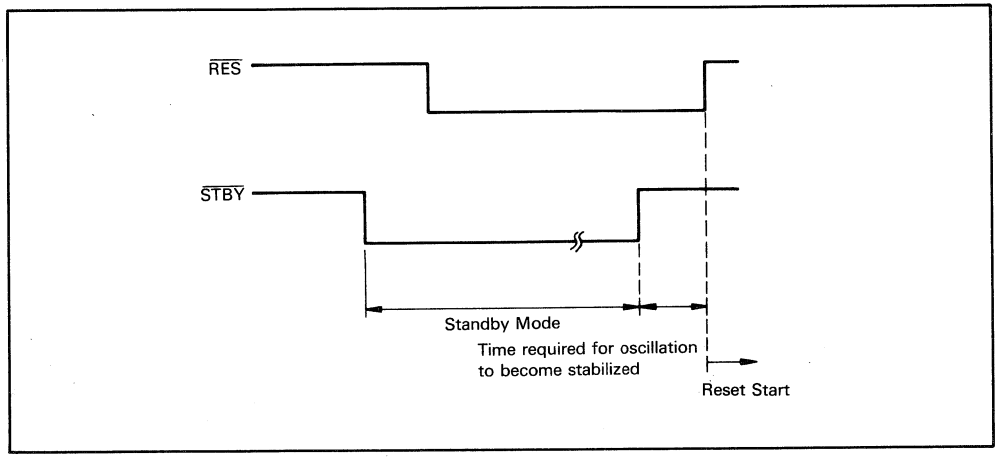


Figure 15. Standby Mode Timing

Notes on UPP Command Setting (1)

The UPP's pulse width resolution depends on the specified value of maximum function number register MFNR: the resolution is inversely proportional to the specified values. Accordingly, to increase resolution, a minimum value should be set in the MFNR according to the number of functions to be executed.

In addition, when a value larger than the necessary minimum value (or 0) is set in MFNR so as to adjust pulse width resolution, set NOP in the command registers (CMR) of unused function numbers in the function table (figure 16). Since the values in the function table after reset are undefined, they may affect the execution of other functions if they are read and executed.

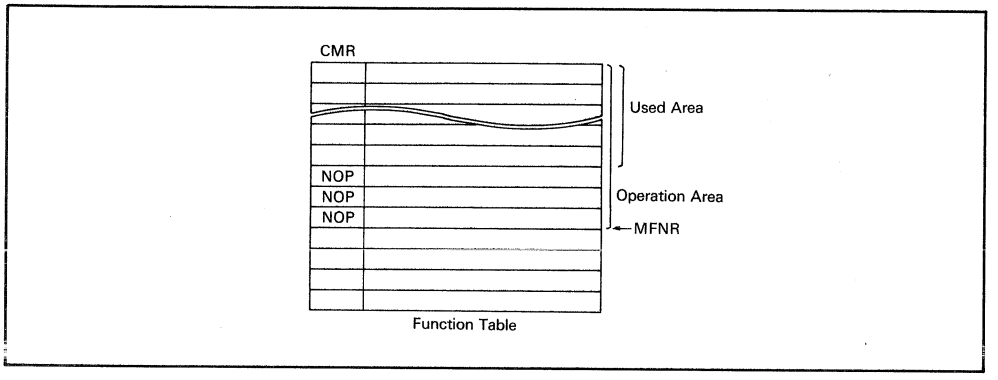


Figure 16. Filling Function Table with NOP

Notes on UPP Command Setting (2)

In the HD63143, an edge detecting cirucit is provided on each pulse input and output of U_0 to U_{23}. Edges are detected by sampling the input and output level and comparing them with the previous sampling value at the timing the function number register (FNR) periodically returns to 0 during UPC operation. Accordingly, while UPC is not in operation, no edges can be detected. In addition, even in operation, narrower pulse edges than the sampling interval cannot be detected (refer to A of figure 17).
Flip-flops for sampling have been cleared by reset. Consequently, as indicated by B of figure 17, if GFE is set while U_0 to U_{23} are 1, rising edges are detected. Accordingly, if edge detection, which is performed at GFE setting, is a problem, avoid such setting combination of the pulse and the edge detecting direction, or set and reset GFE at FNR=1.

At UPC re-start after interruption, flip-flops for sampling store the data just before interruption.

Notes on using capture commands

When the HD63143 generates an interrupt request signal to MPU at a capturing operation at the edge of input signal, a gap will appear between the timing of the interrupt request signal generation and the capturing operation as shown in figure 18. Therefore, extra care should be taken when processing the value in the capture register in the interrupt request routine.

The UPC samples the input signal every time the value of the function number register becomes 0. It detects the edge of the input signal by the change of the sampled value. Interrupt request signal appears immediately after the sampling at which the edge of the input signal has been detected, but the capturing operation is delayed until the capture command is performed after the sampling. Therefore, the value of the capture register is not updated for 5μs (max) at 4 MHz operation. If this dalay time is inconvenient, set the capture command to as small a function number as possible.

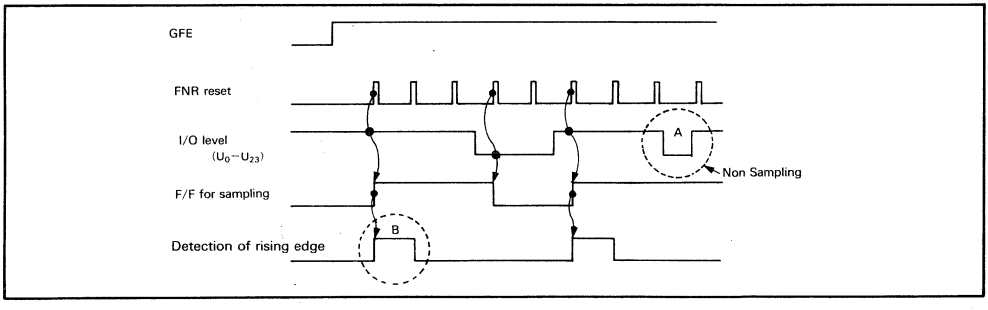


Figure 17. Edge Detection Timing

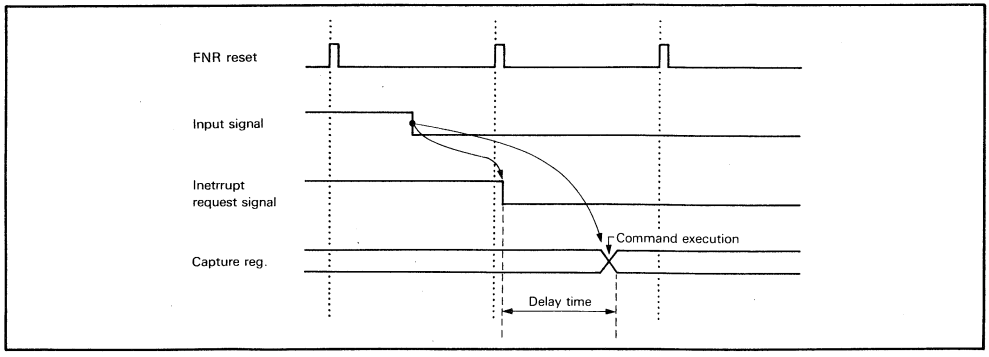


Figure 18. Timing of Interrupt Request and Capture

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	Vcc (Note 2)	−0.3 to + 7.0	V
Input Voltage	Vin (Note 2)	−0.3 to Vcc + 0.3	V
Operating Temperature (Note 1)	Topr	−20 to +75	°C
Storage Temperature	Tstg	−55 to +150	°C
Allowable Output Current	|Io| (Note 3)	10	mA
Total Allowable Output Current	|Σ Io| (Note 4)	100	mA

Notes: 1. Wide temperature range (−40°C to+85°C) version is also available. For details, please contact the sales department.
2. With respect to V_{SS} (system GND)
3. The allowable output current is the maximum current that may be drawn from, or flow out to, one output terminal or one input/output common terminal.
4. The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.
5. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect the reliability of the LSI.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}*	4.5	5.0	5.5	V
Input Low Voltage	V_{IH}*	2.0	–	V_{CC}	V
Input High Voltage	V_{IL}*	0	–	0.8	V
Schmitt-trigger Input Voltage	V_T^-*	1.0	–	2.0	V
Schmitt-trigger Input Voltage	V_T^+*	3.0	–	4.0	V
Operating Temperature	T_{opr}	−20	25	75	°C

Note: * With respect to V_{SS}=0V

Electrical Characteristics

DC Characteristics
(Vcc = 5 V ±10%, Vss = 0 V, Ta = −20°C to+75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Schmitt Trigger Input Voltage	U_8/P_{20}-U_{15}/P_{27}	V_T^-	1.0	–	2.0	V	Figure 19 V_{CC} = 5.0 V
		V_T^+	3.0	–	4.0	V	
		$V_T^+ - V_T^-$	1.0	–	–	V	
Input High Voltage	$\overline{RES}$, $\overline{STBY}$	V_{IH}	Vcc−0.5	–	Vcc+0.3	V	
	EXTAL		Vcc×0.7	–	Vcc+0.3	V	
	Other Inputs		2.0	–	Vcc+0.3	V	
Input Low Voltage	All Inputs	V_{IL}	−0.3	–	0.8	V	
Input Leakage Current	$\overline{RES}$,$\overline{STBY}$, A_0-A_{10},$\overline{CS}$,R/$\overline{W}$, $\overline{DS}$,$\overline{OE}$	$\|I_{IN}\|$	–	–	1.0	μA	V_{in} = 0.5 to V_{CC} − 0.5
Three-State Leakage Current (Off State)	D_0-D_7, READY, U_0/P_{10}-U_7/P_{17}, U_0/P_{20}−U_{15}/P_{27}, P_{40}-P_{46}, P_{50}-P_{55},	$\|I_{TSI}\|$	–	–	1.0	μA	V_{in} = 0.5 to V_{CC} − 0.5
Output High Voltage	All Outputs	V_{OH}	2.4	–	–	V	I_{OH} = −200 μA
			Vcc−0.7	–	–	V	I_{OH} = −10 μA
Output Low Voltage	All Outputs	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output Leakage Current (Off State)	$\overline{INT_0}$,$\overline{INT_1}$	I_{LOH}	–	–	1.0	μA	V_{in}=V_{CC} −0.5V
Input Capacitance	All Inputs	Cin	–	–	15	pF	V_{in} =0 V f =1.0 MHz Ta = 25°C
Current Dissipation (Note 1)		Icc	–	–	30	mA	fopr = 4 MHz
Standby Current		I_{STB}	–	–	15	μA	
RAM Standby Voltage		V_{RAM}	2.0	–	–	V	

Notes: 1. Current dissipation varies in proportion to operating frequency (fopr).
2. fopr=$f_{XTAL}/4$ or $f_{EXT}/4$: HD63143A00
=$f_{EXT}/2$: HD63143B00

AC Characteristics

(Vcc = 5 V ±10%, Vss = 0 V, Ta = −20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Oscillation Stabilization Time	t_{RC}	–	–	20	ms	Figures 20, 31
Operating Frequency	f_{opr}	1.0	–	4.0	MHz	
Output Clock Frequency	f_{CLK}	–	fopr x 2	–	MHz	
Output Clock High Pulse Width	t_{CWH}	55	–	–	ns	
Output Clock Low Pulse Width	t_{CWL}	55	–	–	ns	
Output Clock Rise Time	t_{Cr}	–	–	10	ns	
Output Clock Fall Time	t_{Cf}	–	–	10	ns	
Address Set-up Time	t_{AS}	30	–	–	ns	Figures 21-25, 31
Address Hold Time	t_{AH}	5	–	–	ns	
Delay Time From $\overline{CS}$ low a until READY Low (Other than RAM)	t_{CRD1}	–	–	60	ns	
Delay Time from $\overline{DS}$ Low until READY High — UDR (UPC) (Note)	t_{WAIT}	–	–	3	µs	
Delay Time from $\overline{DS}$ Low until READY High — Others (Note)	t_{WAIT}	–	–	750	ns	
Delay Time from $\overline{DS}$ Higt until READY Low	t_{CRD2}	–	–	80	ns	
$\overline{DS}$ High Pulse Width	t_{DWH}	80	–	–	ns	Figures 21, 23, 24, 31
R/$\overline{W}$ Set-Up Time	t_{RS}	10	–	–	ns	
R/$\overline{W}$ Hold Time	t_{RH}	5	–	–	ns	
Read Data Delay Time (RAM)	t_{RDD}	–	–	140	ns	
Read Data Delay Time from READY High	t_{RRDD}	–	–	60	ns	
Read Data Delay Time from $\overline{OE}$	t_{ORDD}	–	–	80	ns	
Read Data Hold Time	t_{RDH}	10	–	–	ns	
Read Data Hold Time from $\overline{OE}$ High	t_{ORDH}	10	–	–	ns	
Write Data Delay Time (Note)	t_{WDD}	–	–	120	ns	Figures 22, 24, 31
Write Data Set-Up Time	t_{WDS}	100	–	–	ns	
Write Pulse Hold Time from READY High (Note)	t_{WH}	120	–	–	ns	
Write Pulse Low Width	t_{WWL}	100	–	–	ns	
Write Data Hold Time	t_{WDH}	5	–	–	ns	
READY Turn Off Time from $\overline{CS}$ High	t_{RTO}	–	–	50	ns	Figures 23-25

Note: At fopr = 4 MHz. These times are inversely proportional to operating frequency (fopr).

Ports 1, 2, 3, 4, 5
(V_{CC} = 5 V ±10%, V_{SS} = 0 V, Ta = −20°C to +75°C, unless otherwise noted)

Item	Symbol	Min	Max	Unit	Test Condition
Input Data Set-up Time	t_{PDS}	60	–	ns	Figure 26
Input Data Hold Time	t_{PDH}	60	–	ns	
Output Data Delay Time	t_{PDD}	–	170	ns	Figure 27

Serial Comunication Interface (SCI1, SCI2)
(V_{CC} =5 V ±10%, V_{SS} = 0 V, Ta = −20°C to +75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Condition
SCI Input Clock Cycle	Asynchronous	t_{Scyc}	1.0	–	μs	Figure 28
	Synchronous Mode		1.0	–	μs	
SCI Transmit Data Delay Time (Synchronous Mode)		t_{TXD}	–	250	ns	Figure 29
SCI Receive Data Setup Time (Synchronous Mode)		t_{SRX}	250	–	ns	
SCI Receive Data Hold Time (Synchronous Mode)		t_{HRX}	100	–	ns	
SCI Input Clock Pulse Width		t_{PWSCK}	0.4	0.6	t_{Scyc}	Figure 28
Input Clock Rise Time		t_{CKr}	–	100	ns	
Input Clock Fall Time		t_{CKf}	–	100	ns	

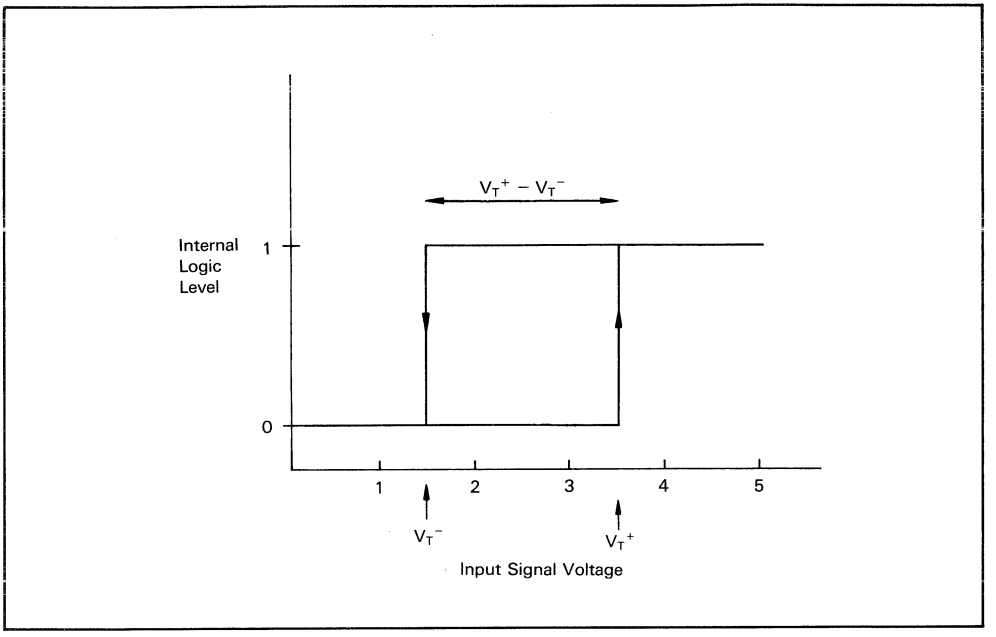


Figure 19. Schmitt Trigger Threshold Level

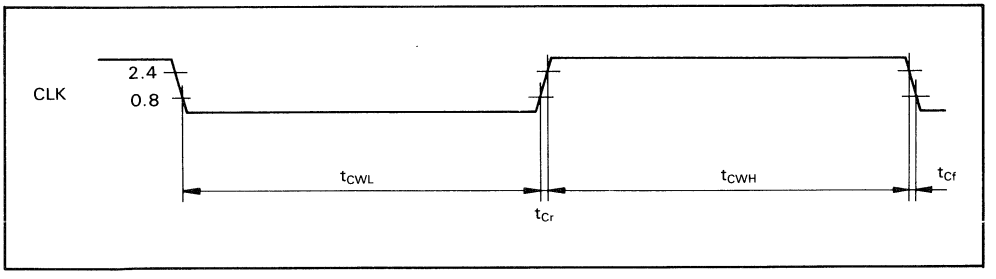
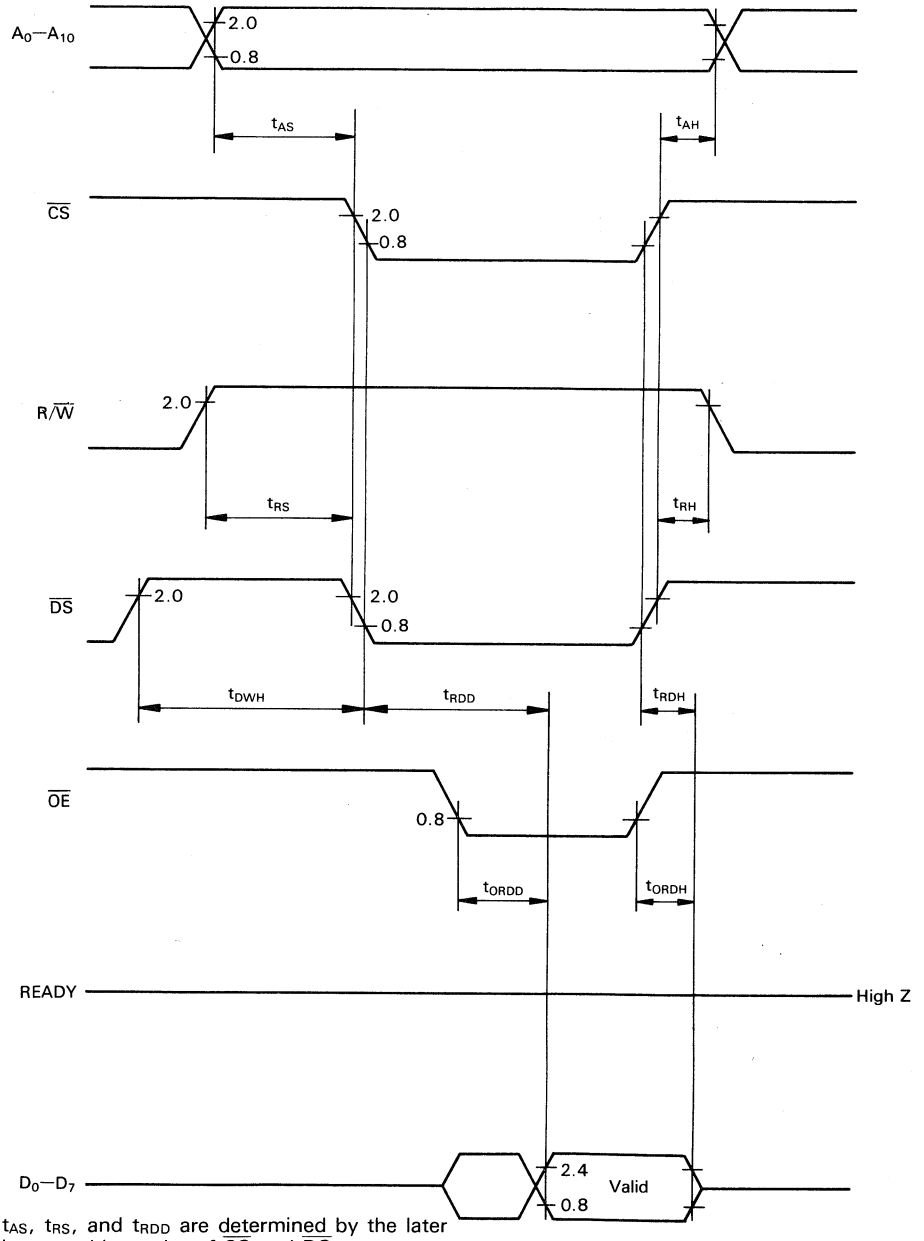
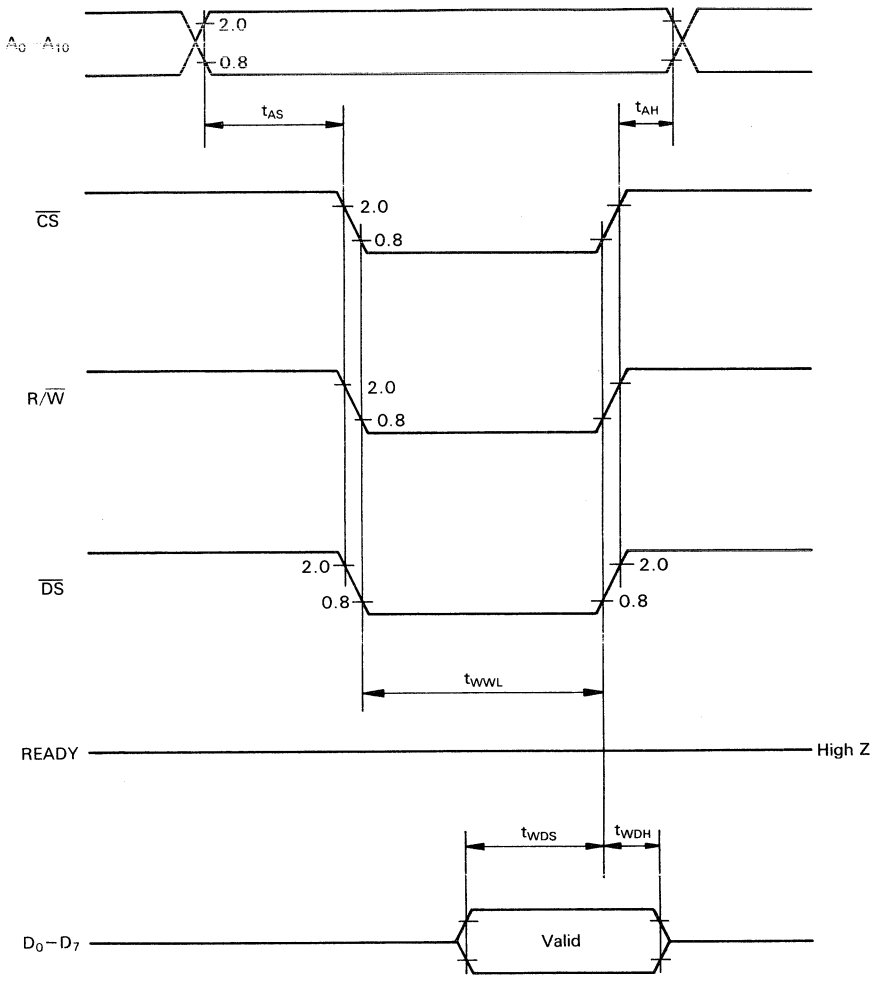


Figure 20. Output Clock Waveform



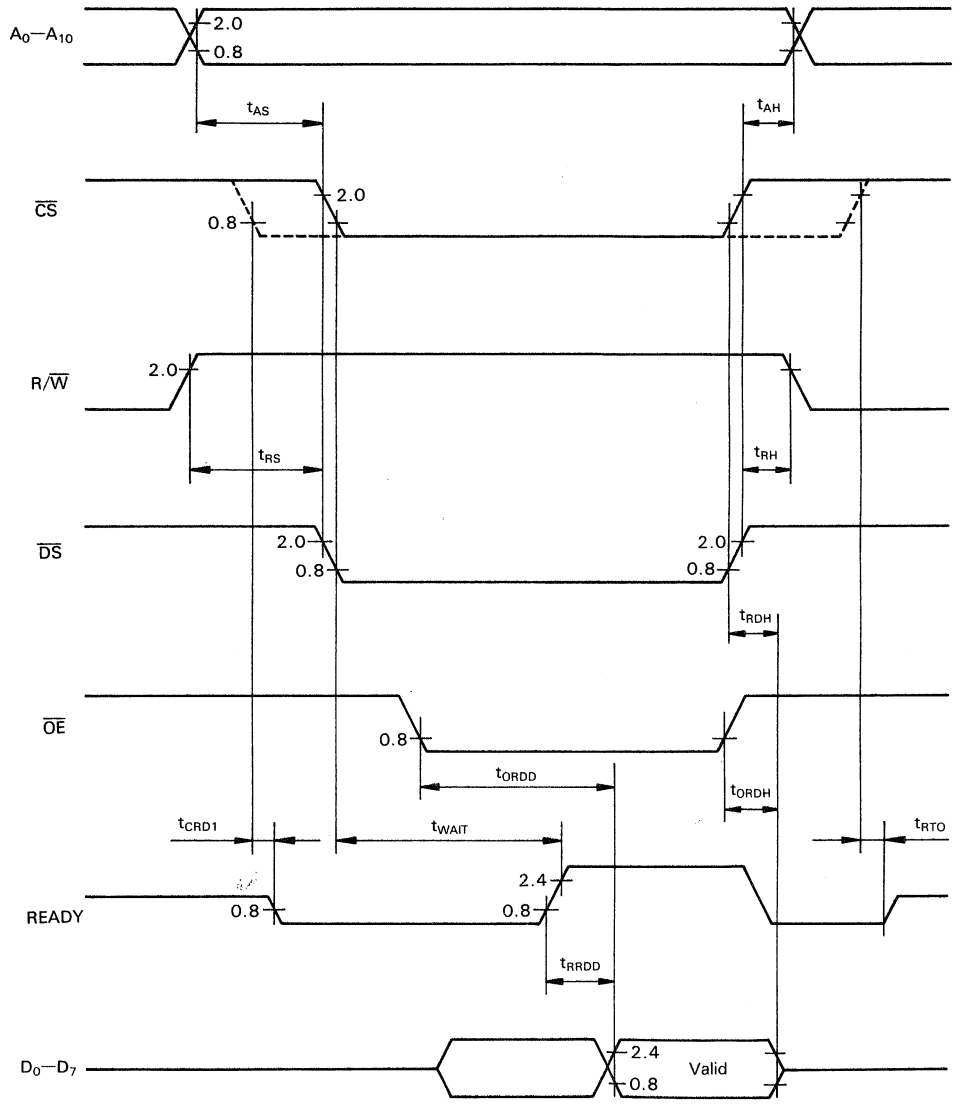
- t_{AS}, t_{RS}, and t_{RDD} are determined by the later low transition point of $\overline{CS}$ and $\overline{DS}$.
- t_{AH}, t_{RH}, and t_{RDH} are determined by the earlier high transition point of $\overline{CS}$ and $\overline{DS}$.

Figure 21. Read Cycle Bus Timing (RAM)



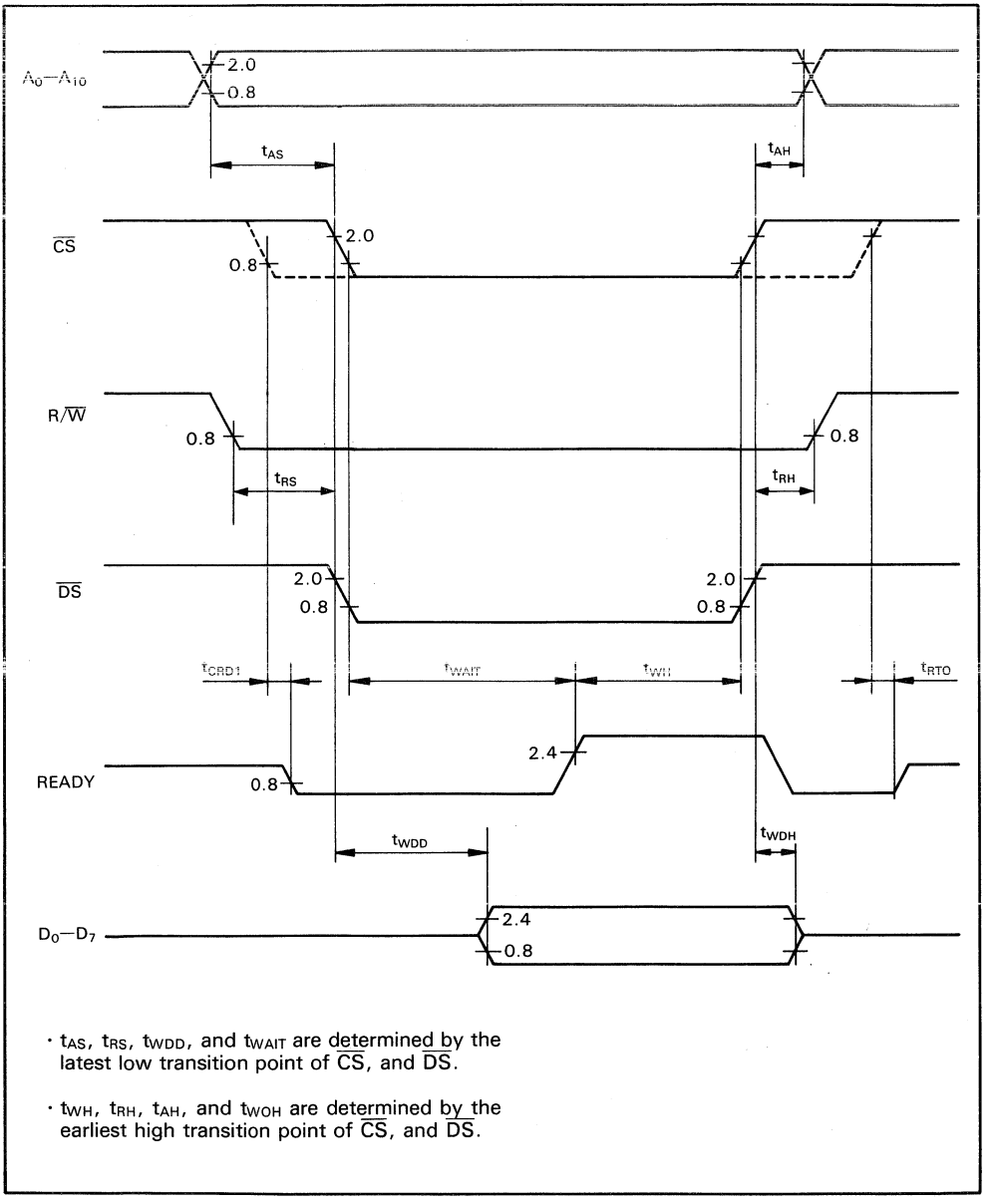
- t_{AS} is determined by the latest low transition point of $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$.
- t_{WWL} is determined by the latest low transition point and the earliest high transition point of $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$.
- t_{AH} is determined by the earliest high transition point of $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$.

Figure 22. Write Cycle Bus Timing (RAM)



- t_{AS}, t_{RS}, and t_{WAIT} are determined by the earlier low transition point of $\overline{CS}$ and $\overline{DS}$.
- t_{AH}, t_{RH}, and t_{RDH} are determined by the earlier high transition point of $\overline{CS}$ and $\overline{DS}$.

Figure 23. Read Cycle Bus Timing (Excluding RAM)



- t_{AS}, t_{RS}, t_{WDD}, and t_{WAIT} are determined by the latest low transition point of $\overline{CS}$, and $\overline{DS}$.
- t_{WH}, t_{RH}, t_{AH}, and t_{WOH} are determined by the earliest high transition point of $\overline{CS}$, and $\overline{DS}$.

Figure 24. Write Cycle Bus Timing (Excluding RAM)

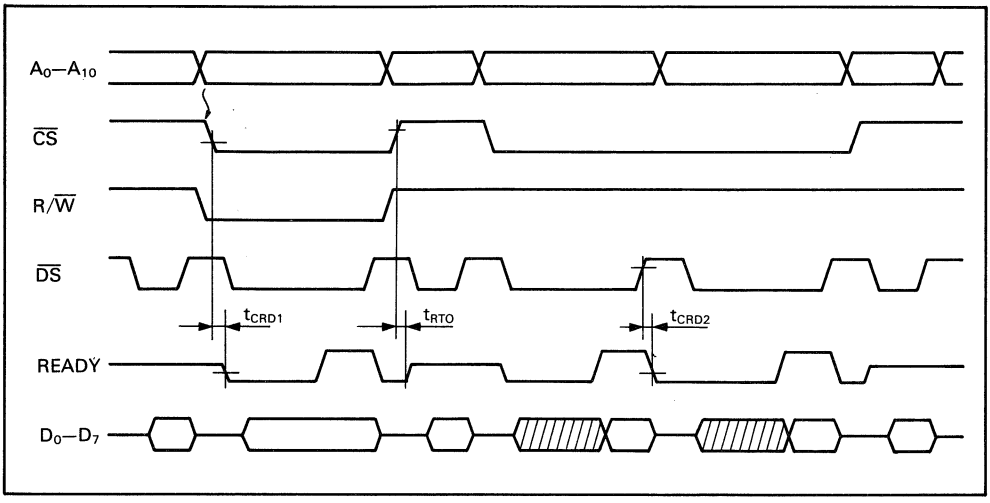


Figure 25. 1-Byte Write and 2-Byte Read Access Ready Timing

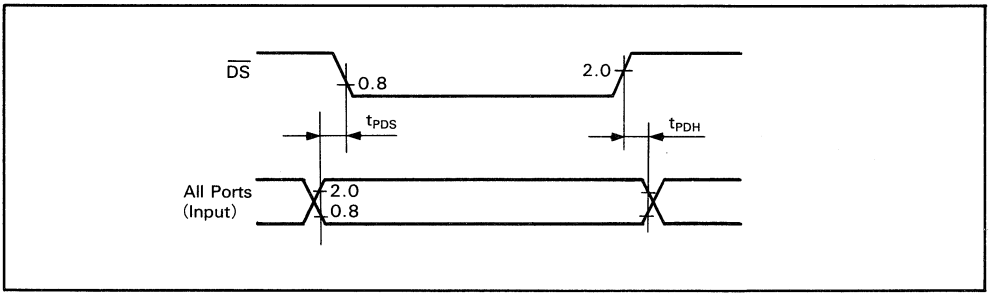


Figure 26. Port Input Timing

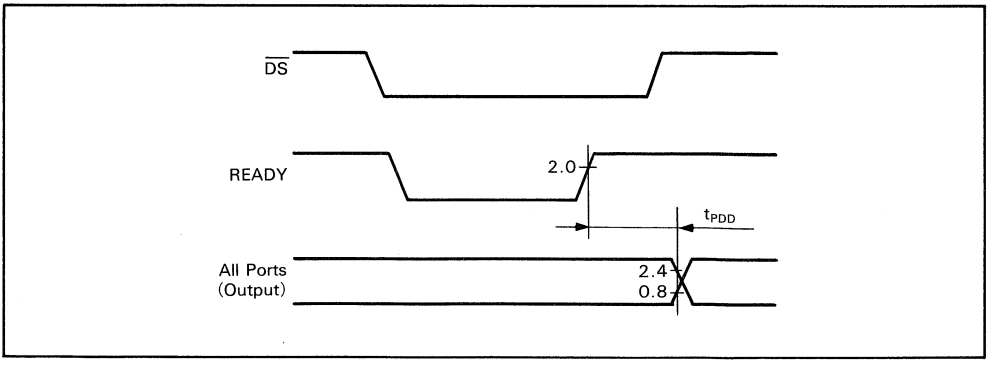


Figure 27. Port Output Timing

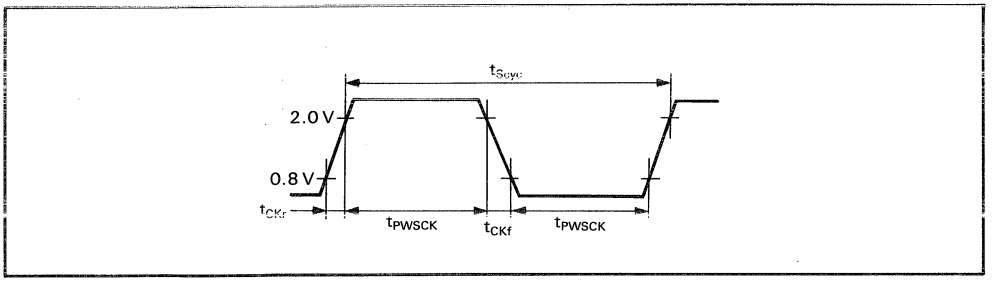


Figure 28. SCI1, SCI2 Input Clock Timing

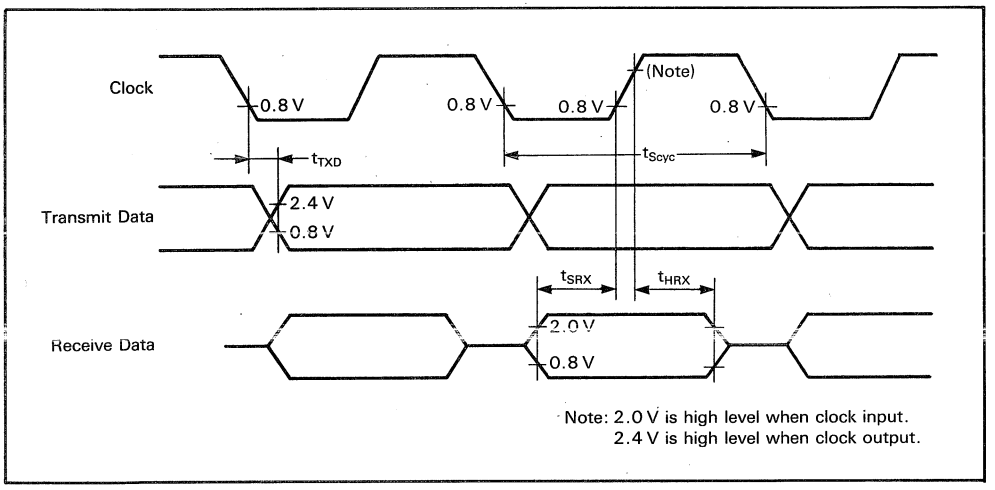


Figure 29. SCI1, SCI2 Synchronous Timing

Output low voltage at measurement is 0.8 V.

Whereas ordinary output low voltage (DC characteristics) is 0.4 V.

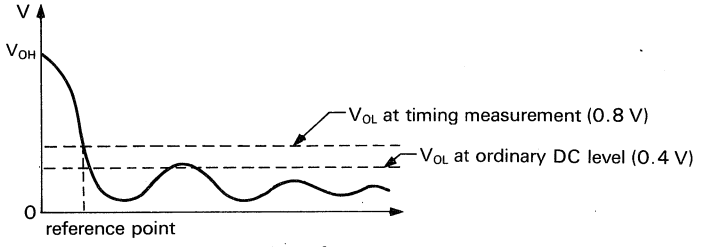


Figure 30. Timing Measurement point of V_{OL}

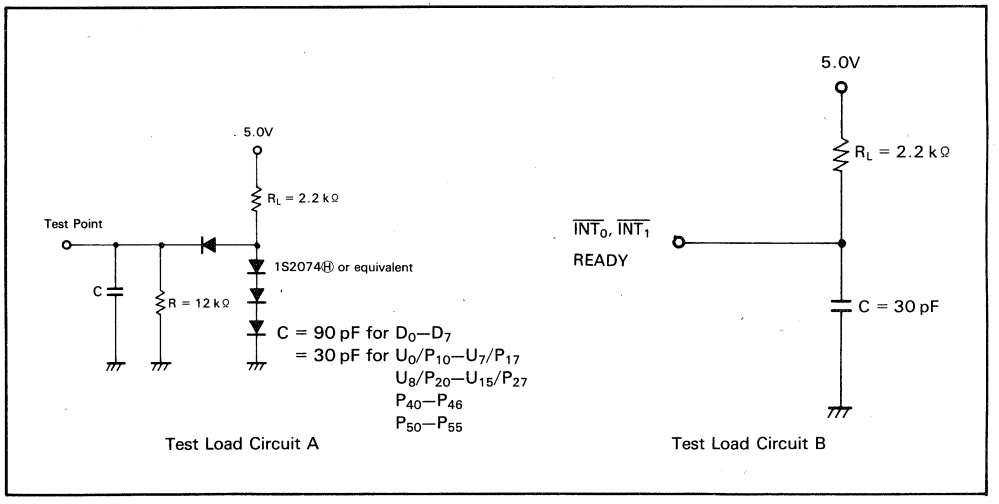


Figure 31. Test Load Circuit

Refer to application note (No. ADE-502-002) for detail of this product.

System Control LSI

HD63310R

Smart Dual Port RAM (S-DPRAM)

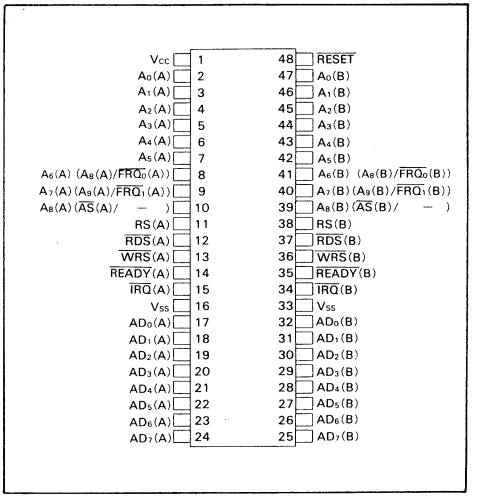
Description

Driven by the declining costs of VLSI CPUs, new multiprocessing and parallel-processing architectures are being explored to break the performance barrier of single CPU designs. A critical factor for multiprocessor performance is the choice of the communication mechanism between CPUs. A poorly designed communication scheme can destroy the potential for a multiprocessor design since message passing overhead can quickly offset the performance advantage of multiple CPUs.

An HD63310R S-DPRAM acts as a communication link between two CPUs. Thus, it replaces older, less flexible communication schemes such as parallel ports and FIFO ICs.

Programmable operating mode and bus interface tailor the S-DPRAM for a wide variety of multiprocessor system designs using industry standard MPUs.

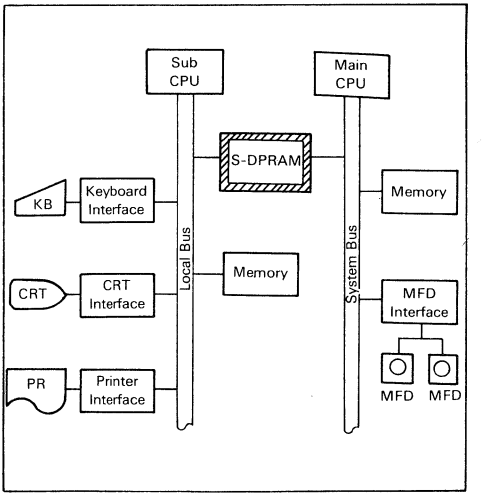
Pin Arrangement



Features

- 1024-byte data buffer with dual ports
  —Configurable as a RAM (DPRAM mode) or two FIFOs (FIFO mode)
- Asynchronous bus operation on each port
- Programmable bus interface
  —Each bus configurable as a multiplexed or non-multiplexed address and data bus.
- Built-in programmable registers
  —8 semaphore registers for multiprocessing applications, 32 user-definable registers
- Programmable outputs
  —Interrupt outputs
  —FIFO status (full/empty, etc) outputs
- High speed operation and low power dissipation 2-μm CMOS circuit
- Single + 5V power supply

System Block Diagram



Pin Description

Symbol	Pin Number	Name	I/O
V_{CC}	1	Power supply	
V_{SS}	16, 33	Ground	
$\overline{RESET}$	48	Reset	I
A_0-A_5(A) A_0-A_5(B)	2-7 47-42	Address bus	I
AD_0-AD_7(A) AD_0-AD_7(B)	17-24 32-25	Address/data bus	I/O
$A_6/A_8/\overline{FRQ_0}$(A) $A_6/A_8/\overline{FRQ_0}$(B)	8 41	Multipurpose line (1): Address bit 6/8, FIFO data request 0	I/O
$A_7/A_9/\overline{FRQ_1}$(A) $A_7/A_9/\overline{FRQ_1}$(B)	9 40	Multipurpose line (2): Address bit 7/9, FIFO data request 1	I/O
$A_8/\overline{AS}$ (A) $A_8/\overline{AS}$ (B)	10 39	Multipurpose line (3): Address bit 8, Address strobe	I
RS (A/B)	11, 38	Register select	I
$\overline{RDS}$ (A/B)	12, 37	Read strobe	I
$\overline{WRS}$ (A/B)	13, 36	Write strobe	I
$\overline{READY}$ (A/B)	14, 35	Ready	O
$\overline{IRQ}$(A/B)	15, 34	Interrupt request	O

Pin Function

This section describes the input and output signals. As shown in "Pin Arrangement", the S-DPRAM has two data ports (designated port A and port B). Identical interface signals are provided for each port except V_{SS}, V_{CC}, and $\overline{RESET}$ which are common to the chip. An "(A)" or a "(B)" after a signal name designates a port A or port B signal.

Power Supply (V_{CC})

V_{CC} is the +5 V ± 5% power supply.

Ground (V_{SS})

V_{SS} is the signal and power ground.

Reset ($\overline{RESET}$)

$\overline{RESET}$ places all the registers of the S-DPRAM in the initial state when asserted (refer to "Register Description" for details). This function is designated a hardware reset, as distinguished from a software reset which can be performed by a program. Active low.

Address Bus (A_0(A)–A_5(A), A_0(B)–A_5(B))

A_0–A_5 are the lower 6-bit address input pins when the I/O bus is configured as non-multiplexed. They should be connected to V_{SS} when the I/O bus is configured as multiplexed. (A CNFG register is selected by the address input 0)

During a RAM access, these lines, together with the A_6, A_7, A_8 address inputs and internal bank select bit, address one of the 1024 RAM bytes (in DPRAM mode).

Table 1. Address and Data Assignment for Each Operating Mode

Signal Name	Register Read/Write DPRAM Mode (Indirect Addressing)		DPRAM Mode (Direct Addressing)		FIFO Mode	
	Non-mult.	Mult.	Non-mult.	Mult.	Non-mult.	Mult.
Address bus A_0-A_5	A_0-A_5	Not used	A_0-A_5	Not used	A_0-A_5	Not used
Address/ data bus AD_0-AD_7	Data D_0-D_7	Address A_0-A_7 Data D_0-D_7	D_0-D_7	A_0-A_7 D_0-D_7	D_0-D_7	A_0-A_5 D_0-D_7
Multi-purpose line (1) $A_6/A_8/\overline{FRQ_0}$	Not used		A_6	A_8	$\overline{FRQ_0}$	
Multi-purpose line (2) $A_7/A_9/\overline{FRQ_1}$	Not used		A_7	A_9	$\overline{FRQ_1}$	
Multi-purpose line (3) $A_8/\overline{AS}$	Not used	$\overline{AS}$	A_8	$\overline{AS}$	Not used	$\overline{AS}$

Notes: 1. Non-mult. I/O bus is configured as non-multiplexed.
Mult. I/O bus is configured as multiplexed address and data bus.

2. A hardware reset places the S-DPRAM in DPRAM mode, and defines the I/O bus as non-multiplexed. The operation mode can be altered by setting the internal CNFG register as required.

During a register access, these lines select one of the 62 internal registers.

Address/Data Bus (AD_0(A)–AD_7(A), AD_0(B)–AD_7(B))

AD_0–AD_7 are the input/output pins for the data bus when the I/O bus is configured as non-multiplexed. They are the input pins for the lower 8-bit address, and input/output pins for data when the I/O bus is configured as multiplexed. Three-state.

Multipurpose Lines (A_6(A)/A_8(A)/$\overline{FRQ_0}$(A), A_6(B)/A_8(B)/$\overline{FRQ_0}$(B), A_7(A)/A_9(A)/$\overline{FRQ_1}$(A), A_7(B)/A_9(B)/$\overline{FRQ_1}$(B), A_8(A)/$\overline{AS}$(A), A_8(B)/$\overline{AS}$(B))

The function of the multipurpose lines varies according to the operation mode of the S-DPRAM (table 1). These functions are as follows.

A_6–A_8 or A_8, A_9 Address Bit (Upper): The A_6–A_8 upper address inputs are used together with A_0–A_5 for RAM addressing (in DPRAM mode), when the I/O bus is configured as non-multiplexed. Since only 512 bytes can be addressed by the address pins, the upper or lower 512 RAM bytes should be selected by the bank select bits (bit 0 or 1) of the CMD register.

When the I/O bus is configured as multiplexed, RAM addressing utilizes A_8 and A_9 as the input pins for the upper address bits, along with lower address bits A_0–A_7.

Address Strobe ($\overline{AS}$): $\overline{AS}$ latches the address A_0–A_7 on the address/data bus AD_0–AD_7 when the I/O bus is configured as a multiplexed bus. The address presented on AD_0–AD_7 pins is latched at the rising edge of $\overline{AS}$. Active low.

FIFO Data Request ($\overline{FRQ_0}$, $\overline{FRQ_1}$): The $\overline{FRQ_0}$/$\overline{FRQ_1}$ active low outputs represent the state of a programmable FIFO threshold: FIFO 0/1 full, empty, not full, or not empty. The operation of these signals are controlled by the internal FRC (FIFO request control) register. Active low.

Register Select (RS(A), RS(B))

RS indicates whether the address specified during the current read/write operation refers to a RAM byte or an internal register. If RS is asserted high, then the address refers to one of the internal registers. If RS is low the address refers to a RAM byte.

Read Strobe ($\overline{RDS}$(A), $\overline{RDS}$(B))

$\overline{RDS}$ selects the S-DPRAM for a read transaction. Whenever $\overline{RDS}$ is asserted low the data from the addressed internal register or RAM location is transferred to the data bus. In case of simultaneous transfer requests from both ports, the internal arbiter determines the order in which the requests are serviced at the falling edge of $\overline{RDS}$. Active low.

Write Strobe ($\overline{WRS}$(A), $\overline{WRS}$(B))

$\overline{WRS}$ selects the S-DPRAM for a write transaction. Whenever $\overline{WRS}$ is asserted low, a write access to an internal register or RAM is initiated. Write transactions are bufferred. The data is temporarily latched into the buffer register upon negation of $\overline{WRS}$. It is subsequently written into the specified internal register or RAM, using the internal clock timing. Active low.

In case of simultaneous transfer requests from both ports, the internal arbiter determines the order in which the requests are serviced. (Detailed explanations are shown in the paragraph "Arbitration (Hardware)".)

Ready ($\overline{READY}$(A), $\overline{READY}$(B))

$\overline{READY}$ reports the successful acceptance of the $\overline{RDS}$ (or $\overline{WRS}$) signal to the MPU. After its assertion, $\overline{RDS}$ (or $\overline{WRS}$) must be kept low for a minimum period specified in the bus timing characteristics in order to assure a proper completion of internal processing. Active low.

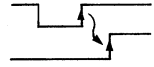
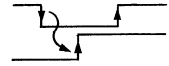
Interrupt Request ($\overline{IRQ}$ (A), $\overline{IRQ}$ (B))

The $\overline{IRQ}$ open-drain output is asserted low when at least one bit of the AND of the corresponding bits of a port's ISRC and IEN register is set to 1. Active low, open drain.

Comparison between HD63310 and HD63310R

The HD63310R is an advanced R version of the HD63310, characterized by the following features: FIFO status operation error has been corrected (already reported by Hitachi Microcomputer Technical Update, TN-PSY-503A), some limitations have been eliminated, and noise resistance has been improved (noise caused by undefined read data has been removed). Table 2 shows a comparison between the HD63310 and HD63310R.

Table 2. HD63310R and HD63310

Item		HD63310RP20	HD63310P20
FCR register	In DPRAM mode	Read/write accessible	Write invalid, read as 0
	In FIFO mode	Read/write accessible	Read/write accessible
$\overline{FRQ}$ output timing characteristics	No. 32; $\overline{FRQ}$ negation delay time (at write access)	t_{FNLW} = 150 ns	t_{FNLW} = 300 ns
$\overline{FRQ}$ output timing specification ($\overline{FRQ}$ timing at write access in level mode) [type 1]		$\overline{FRQ}$ is negated at the rising edge of $\overline{WRS}$ 	$\overline{FRQ}$ is negated at the falling edge of $\overline{WRS}$ 
$\overline{FRQ}$ output timing item	$\overline{FRQ}$ timing at write access in pulse mode [type 1]	No. 35; $\overline{FRQ}$ negation delay time; t_{FNPW} = 250 ns	No. 32; $\overline{FRQ}$ negation delay time; t_{FNLW} = 300 ns
	$\overline{FRQ}$ timing at read access in pulse mode	No. 38; $\overline{FRQ}$ negation delay time; t_{FNPR} = 300 ns	No. 34; $\overline{FRQ}$ negation delay time; t_{FNLR} = 300 ns
Notes	limitations on ISRC register	Removed	Remain

Note: In FIFO operation, the HD63310R is not compatible with the HD63310 in order to improve the FIFO contention error (at enpty condition). Therefore some changes in the circuit are required around the $\overline{FRQ}$ signals.

Block Diagram

The S-DPRAM consists of 1024 bytes of static RAM and 32 bytes of register. See figure 1.

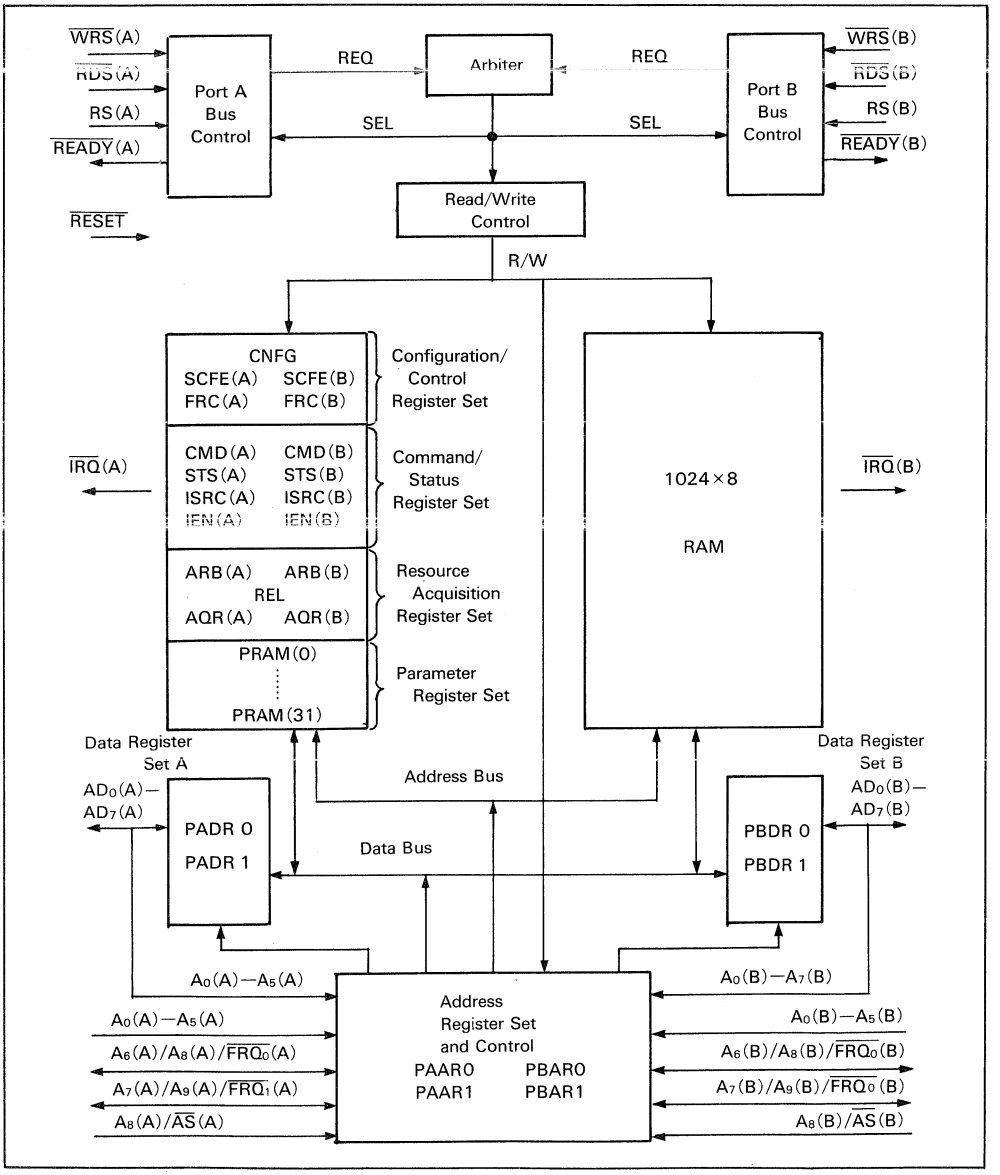


Figure 1. Block Diagram

Register Description

The operation of the S-DPRAM is controlled, as well as monitored, by a number of on-chip user-accessible registers. Some of these registers are shared by both ports, while others are for exclusive use of each port. The CNFG (configuration), REL (release/available), and PRAM (parameter) registers are shared by both ports, while the rest of them are provided for each port. An "(A)" or a "(B)" after a register name indicates a port A or port B register respectively. The internal register configuration is shown in figure 2, and their bit definition is in table 3.

Table 3. Internal Register: Bit Configuration and Operation

Add. #	Reg. Name	Bit Configuration 7	6	5	4	3	2	1	0	Reset	Read/Write Operation 7	6	5	4	3	2	1	0	Remarks
R00	CNFG	ABUS	BBUS	RCFG			0	F1D	F0D	00	R/W					0	R/W		Common SCR
R01	CMD	AP1	AP0	RST	0	0	0	F1FL / B1SL	F0FL / B0SL	00 (Note1)	R/W		RO /W	0	0	0	R/W		SCR
R02	IEN	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	00	R/W								SCR
R03	ISRC	ATT1	ATT0	RELE	FERR	F1F	F1E	F0F	F0E	00 (Note1)	R/W1C								SCR
R04	STS	IRQ	FRQ1	FRQ0	FERR	F1F	F1E	F0F / B1EN	F0E / B0EN	01	R								
R05	ARB	PID								00	R/WID								
R06	AQR	OWN7	OWN6	OWN5	OWN4	OWN3	OWN2	OWN1	OWN0	00	R/W (Note 2)								
R07	REL	AVL7	AVL6	AVL5	AVL4	AVL3	AVL2	AVL1	AVL0	FF	R/W (Note 2)								Common
R08	PA/BDR0	D_7–D_0								un-defined	R/W								
R09	PA/BDR1	D_7–D_0								un-defined	R/W								
R0A	FRC	0	FR1E	FR1T	FR1M	0	FR0E	FR0T	FR0M	00	0	R/W			0	R/W			SCR
R0B	SCFE	CNT1	DEC1	CNT0	DEC0	F1O	F1U	F0O	F0U	00	R/W				R				SCR
P0C	PA/BAR0 (L)	A_7–A_0								00	R/W								
P0D	PA/BAR0 (H)	REG	0	0	0	0	0	A_9	A_8	00	R/W	0	0	0	0	0	R/W		
P0E	PA/BAR1 (L)	A_7–A_0								00	R/W								
P0F	PA/BAR1 (H)	REG	0	0	0	0	0	A_9	A_8	00	R/W	0	0	0	0	0	R/W		
R10 • • • R2F	PRAM	PRAM								un-defined	R/W								

Notes: 1. 00 at a hardware reset state.
At a software reset state, bits 7 and 6 are preserved, while the rest are cleared.
2. Semaphore bits to prevent access contention. OWN0–OWN7 and AVL0–AVL7 are related to each other.
3. R/W ——— Read/write
R ——— Read only
R0 ——— Read as 0 only
SCR ——— Special Control Register
W1C ——— Write 1 to clear
WID ——— Write ID code to set if 0
O ——— Not used; write invalid; read as 0 only
COMMON ——— Shared register

When the S-DPRAM is in DPRAM mode, its indirect addressing capability allows both internal registers and the on-chip RAM to be accessed using address register PA/BAR0 or PA/BAR1 as an address pointer. The value stored in PA/BAR0 will be used as an indirect address whenever a read or write operation is performed through a port's data register PA/BDR0. Similarly, the value contained in PA/BAR1 will be used as an indirect address whenever a read or write operation is performed through a port's data register PA/BDR1.

Using indirect addressing, it is possible to access from port A the registers belonging to port B, and vice versa. The indirect address values 30-3F are reserved for accessing the opposite port's registers. Table 3 summarizes the direct and indirect address allocation for S-DPRAM's internal registers.

In FIFO mode, the indirect addressing is disabled because the address registers are utilized for FIFO control. The opposite port's registers, therefore, are not accessible in this mode.

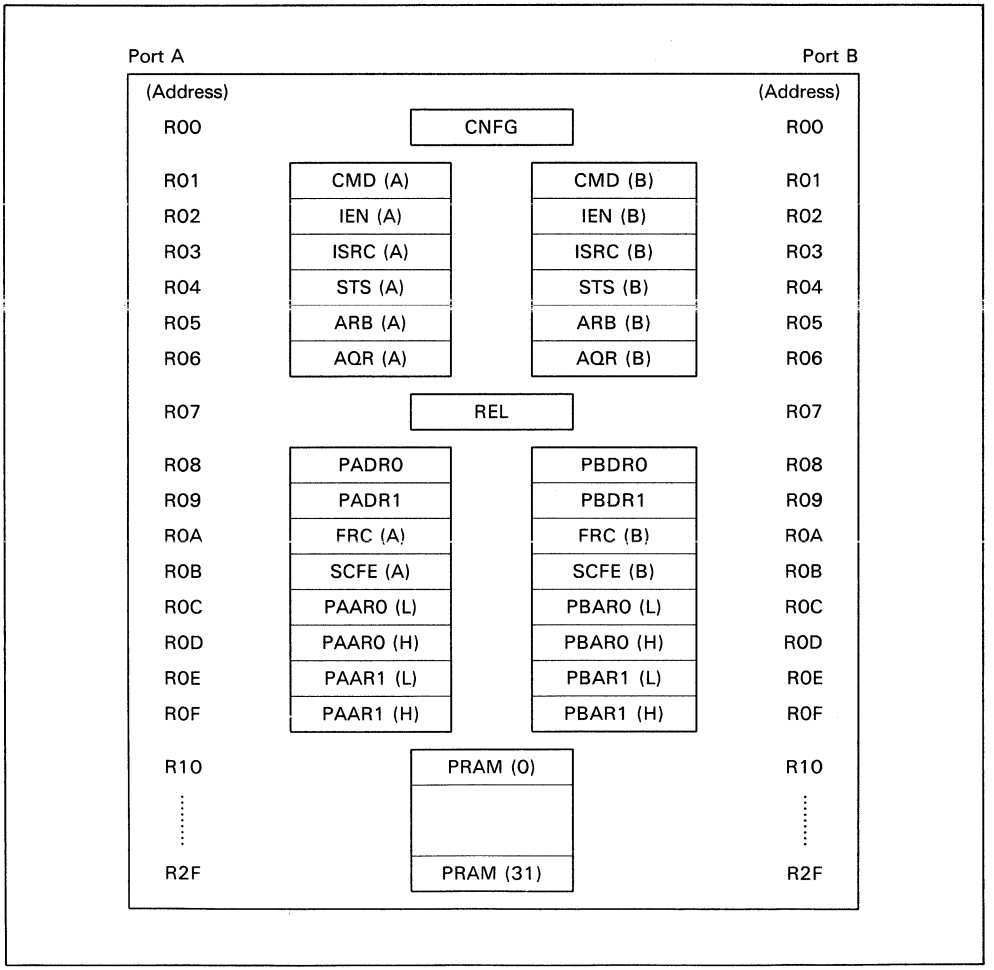


Figure 2. Internal Register Configuration

Table 4. Register Map and Address (In DPRAM mode)

Address	Port A	D	I	Port B	D	I
00 0F	Control Register (A)	○	○	Control Register (B)	○	○
10 2F	Parameter Register	○	○	Parameter Register	○	○
30 3F	Control Register (B)	×	○	Control Register (A)	×	○

Notes: 1. D: Direct addressing mode ○: Accessible
I: Indirect addressing mode ×: Not accessible
2. Address inputs $A_6 - A_9$ are not used for register access. Therefore addresses above 40 are the same as addresses 00–3F.

Configuration Register (CNFG)

The contents of the CNFG register (figure 3) should be defined after a reset, before any other register is accessed.

The ABUS and BBUS respectively define bus A and bus B to be either non-multiplexed or multiplexed address and data buses. The RCFG field defines the on-chip RAM either as DPRAM or as two FIFOs. The F1D/F0D define the data transfer direction between FIFO 1 and FIFO 0 and the data ports. F1D/F0D are not used (ineffective) when the S-DPRAM is set in DPRAM mode by the RCFG.

After a reset, both ports are set in DPRAM mode with the I/O bus configured as non-multiplexed (ABUS=0, BBUS=0, RCFG=000). CNFG is a shared register accessible from both ports.

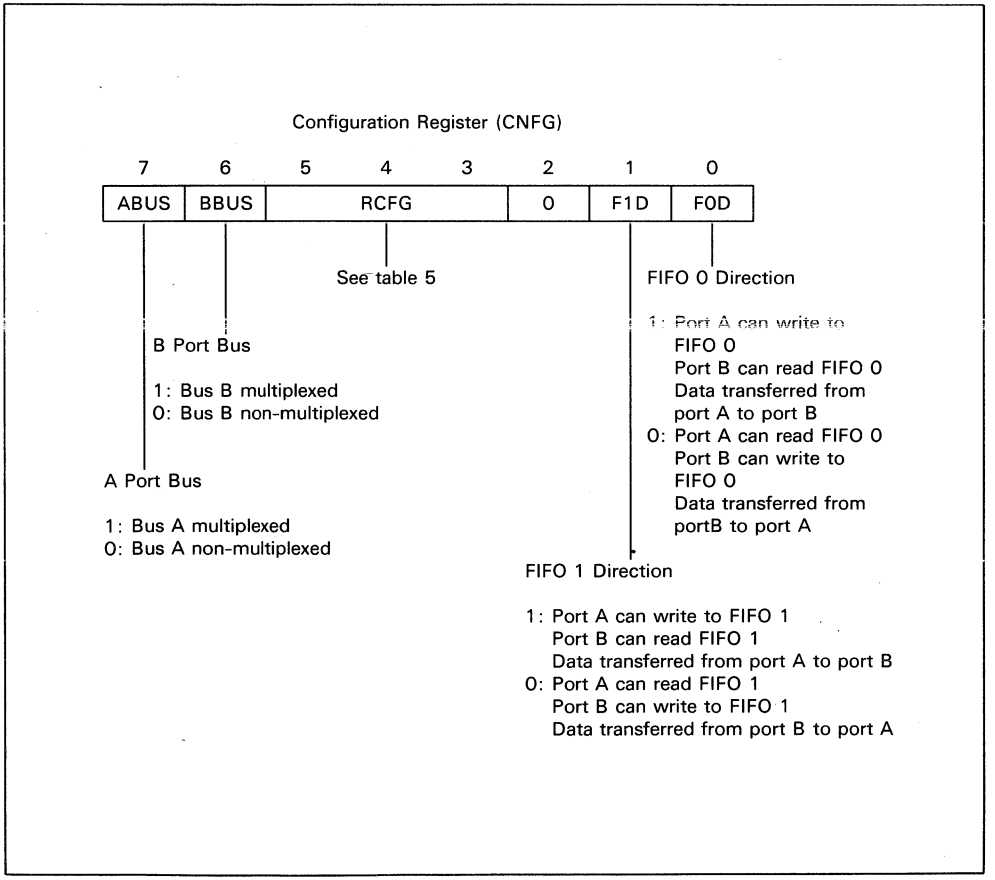


Figure 3. Configuration Register

Command Register (CMD(A), CMD(B))

Writing to a CMD register (figure 4) causes the commands corresponding to the bits set to 1 to be executed. The previous data in the CMD register does not affect the operation. For example, if the data in a bit is 1, writing a 1 to that bit still accesses the corresponding command.

The AP1 and AP0 bits perform interport communication. Writing a 1 to these bits sets bits ATT1 or ATT0 of the ISRC register of the opposite port, reporting a transaction request to that port.

The RST bit places the S-DPRAM in the software reset state. The software reset is slightly different from the hardware reset caused by asserting the RESET pin. Refer to "Reset Operation" for details.

The functions of bits 0 and 1 of the CMD register vary depending on the S-DPRAM operating mode. In FIFO mode, they function as F1FL and F0FL, which initialize the FIFOs. Writing a 1 to F1FL/F0FL causes the following operations:

1. Sets F1E/F0E=1 and F1F/F0F=0 in the STS registers of both ports
2. Sets F1O/F0O=0 and F1U/F0U=0 in the SCFE registers of both ports
3. Sets F1E/F0E=1 in ISRC registers of both ports
4. Flushes FIFO 1/0 (initializes FIFO top and bottom pointers)

In DPRAM mode, they function as B1SL and B0SL, which select the upper or lower 512 bytes of RAM. Setting B1SL to 1 selects the upper 512-byte bank (bank 1). This sets B1EN =1 in the STS register. Setting B0SL to 1 selects the lower 512-byte bank (bank 0). This sets B0EN= 1 in the STS register. If an attempt is made to set both B1SL and B0SL to 1, B1SL will be set to 0 and B0SL will be set to 1, selecting the bank 0. These bits are only used for direct addressing with a non-multiplexed I/O bus. In the multiplexed mode, the A_9 signal selects the bank instead.

Writing a 0 to any bit of the CMD register clears that bit. Reading the CMD register returns the data that was most recently written into the register.

Table 5. 1024-Byte RAM Operation Mode and FIFO Size

RCFG				FIFO Size	
bit5	bit4	bit3	RAM Op Mode	FIFO 1	FIFO 0
0	0	0	DPRAM	—	—
0	0	1	FIFO	0	1024
0	1	0	FIFO	1024	0
0	1	1	FIFO	512	512
1	0	x	FIFO	256	768
1	1	x	FIFO	768	256

Notes: x: Don't care
Unit: bytes

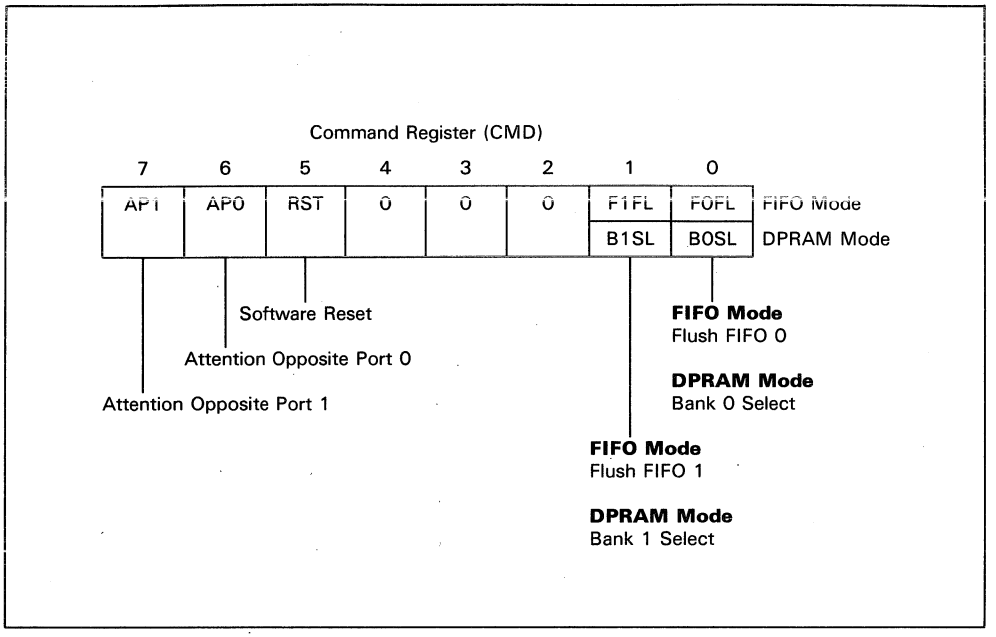


Figure 4. Command Register

Status Register (STS(A), STS(B))

The read-only STS register (figure 5) reports the operational status of the S-DPRAM. The IRQ bit displays the condition of the IRQ output terminal. FRQ1 and FRQ0 display internal signal conditions.

F1E and F0E (FIFO 1/0 empty) are set to 1 at FIFO 1/0 initialization.

FERR (FIFO error) is set when one of F1O, F1U, F0O, or F0U is set in the SCFE register:

FERR = F1O + F1U + F0O + F0U

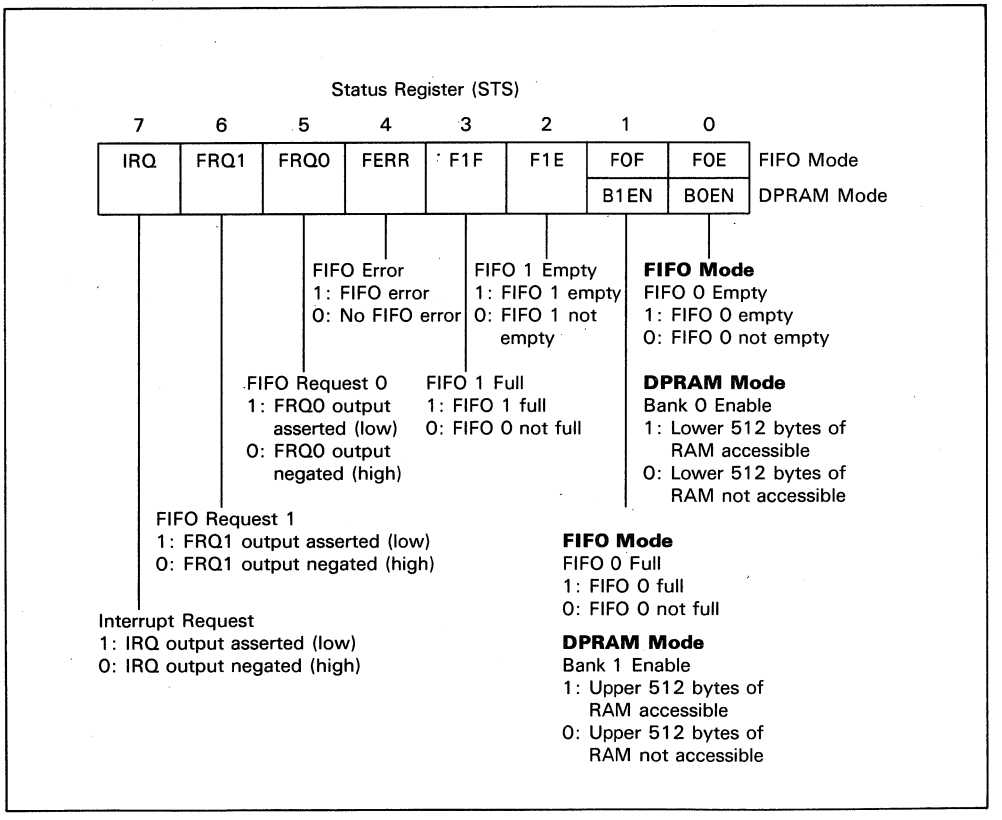


Figure 5. Status Register

Interrupt Source Register (ISRC(A), ISRC (B))

The ISRC register (figure 6) stores interrupt source information. The stored information is preserved regardless of FIFO, ATT, and RELE status change until the ISRC register is cleared. The interrupt request output IRQ is asserted when at least one bit of the AND of corresponding bits of IRSC and IEN registers is set to 1.

The ATT1 and ATT0 bits are set to 1 by a transaction request from the opposite port (AP1/AP0 of opposite port set).

RELE = 1 indicates that the shared resource semaphore of the opposite port has been released. This occurs when a bit of the REL register has changed from 0 to 1 due to the opposite port writing a 1 into the AVL bit of the REL register.

The FERR bit indicates a condition such as FIFO overflow or underflow. the F1F, F1E, F0F, and F0E bits, indicate FIFO full and empty conditions. They are set when the corresponding bit in the STS goes from 0 to 1. These bits in the ISRC register retain their state until the register is cleared. In the STS register, they show the current status when they are read.

Writing a 1 into an ISRC register bit clears that bit. Writing a 0 into a bit has no effect.

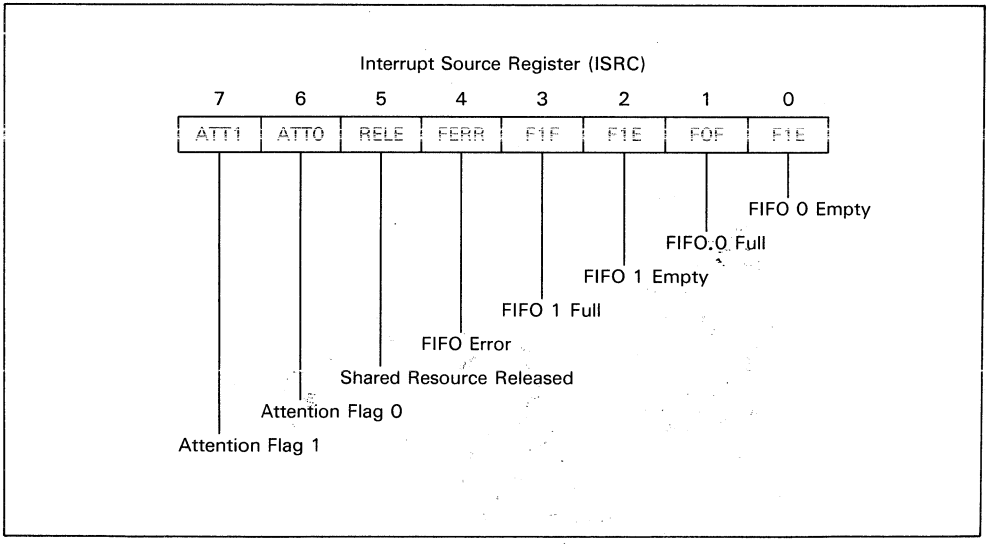


Figure 6. Interrupt Source Register

Interrupt Enable Register

The IEN register (figure 7) masks interrupt conditions in the ISRC register.

The IRQ signal is asserted when the AND of at least one pair of corresponding bits from IEN and ISRC is 1:

$$IRQ = ATT1 \cdot ENA7 + ATT0 \cdot ENA6 + RELE \cdot ENA5 + FERR \cdot ENA4 + F1F \cdot ENA3 + F1E \cdot ENA2 + F0F \cdot ENA1 + F0E \cdot ENA0$$

The IRQ bit of STS is also set when the IRQ signal is asserted.

Arbitration Register (ARB(A), ARB(B))

The ARB register (figure 8) provides a mechanism for multiple CPUs (or multiple processes on a single CPU) sharing a common port to arbitrate among themselves.

This register has a test-and-set hardware logic circuit, and allows system software to manage access to shared resources, including the S-DPRAM itself.

The ARB register access procedure is:

1. The requesting processor writes its ID code into the register.
2. The processor reads back the register. If it reads its own ID, its request has been accepted.
3. The processor makes the data transfer.
4. The processor releases the system resource by writing its ID into the register again.

Write Access: If the PID is 0, then ARB write access is allowed. if the PID is not 0:

1. Writing data equal to the PID clears the PID.
2. Writing data not equal to the PID does not change the PID.

Read Access: If the PID is equal to a processor's ID code, the system resource is owned by that processor. If the PID is not equal to a processor's ID code, the resource is owned by another processor. If the PID equals 0, the resource is free.

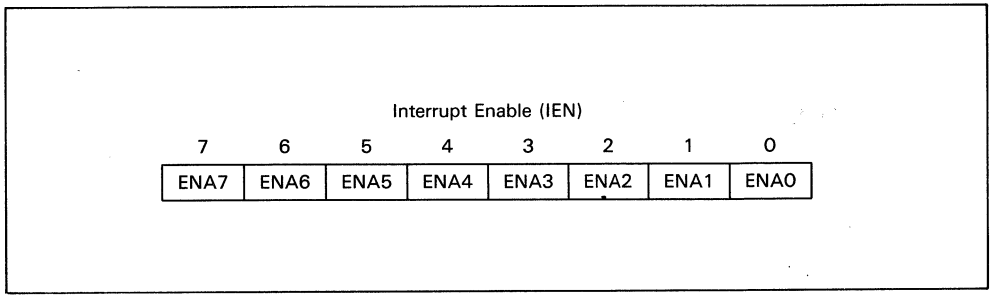


Figure 7. Interrupt Enable Register

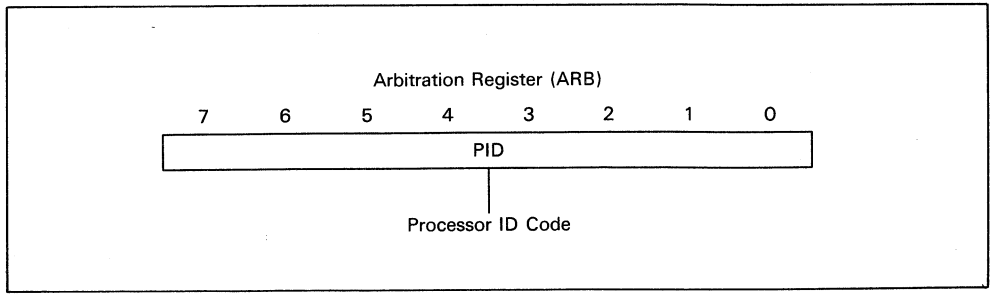


Figure 8. Arbitration Register

Acquire Ownership Register (AQR(A), AQR(B))

The AQR register (figure 9) provides 8 semaphores to arbitrate for exclusive ownership of system resources shared between ports A and B. It is used in conjunction with the REL register. Each of the 8 bits, OWN7-OWN0, can represent ownership of a separate system resource. An AQR register is provided for each port.

A resource is acquired as follows:

1. The requesting processor attempts to write a 1 into the bit corresponding to the desired shared resource.
2. The processor reads the bit back. A 1 indicates that the resource has been successfully acquired. A 0 indicatas that the resource has already been acquired by a device on the opposite port.
   Successfully writing a 1 to an AQR bit simultaneously clears the bit in the same position in the REL register.
3. The processor makes the data transfer.
4. The processor releases the resource by writing a 1 to the corresponding bit of the REL register. The OWN bit in the AQR register will be cleared and the shared resource will be released to the system.

Write Access: An unsuccessful attempt to write a 1 to an OWN bit indicates that the opposite port has acquired ownership of the corresponding shared resource. A successful attempt indicates that the resource has been acquired. On acquisition, a 0 is simultaneously written into the corresponding AVL bit in the REL register.

Read Access: A read access must be performed after an attempt to write a 1 into a bit. Writing a 1 does not guarantee that the bit will be set. When the bit is read as 1, it indicates that the device connected to this port has acquired ownership of the system resource corresponding to the bit.

Once successfully set, the bit remains set until the corresponding bit in the REL register is set or a reset occurs. When the bit is read as 0, it indicates that the request for ownership has failed.

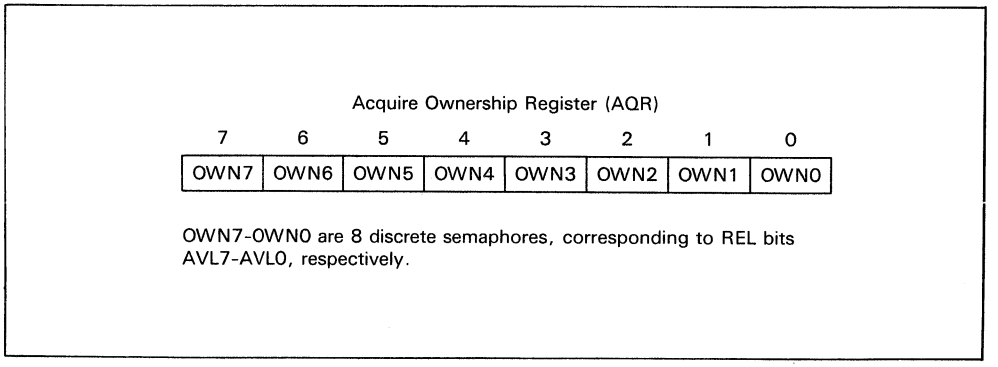


Figure 9. Acquire Ownership Register

Release Available Register (REL)

The REL register (figure 10), in conjunction with a port's AQR register, provides 8 semaphores for interport arbitration of system resources. The register is a bit-mapped summary of available system resources, and a mechanism for either port to release its acquired resources to the system. REL is a shared register accessible from both ports. AVL7-AVL0 correspond to OWN7-OWN0 of the AQR registers of each port.

When a port writes a 1 into a specific bit of the REL register, it releases the corresponding system resource, provided that it is owned by that port. A write access by the opposite port (which doesn't own the resource) causes no action. Successfully writing a 1 into an AVL bit simultaneously writes 0 the OWN bit of the AQR register of the port performing the write.

When the OWN bit is read as 1, it indicates that the corresponding system resource is available. Writing a 1 to an OWN bit of the AQR register simultaneously clears the corresponding AVL bit of the REL register.

The state transition diagram (figure 11) summarizes the relation between the REL register and the AQR registers of ports A and B.

Write Access: Writing a 1 into a bit releases the corresponding shared resource to the system. A port can set an AVL successfully only if the AQR register of that port has a 1 in the same bit position. A port successfully writing a 1 into an AVL bit clears the corresponding OWN bit in that port's AQR register. Writing a 0 has no effect. A transition from 1 to 0 in any bit of the REL register sets the RELE interrupt bit in the ISRC register.

Read Access: When a bit is read as 1, it indicates that the corresponding shared resource is available. The bit remains set until a 1 is written to the corresponding OWN bit of the AQR register. When a bit is read as 0, it indicates that the system resource has been acquired by either port A or port B.

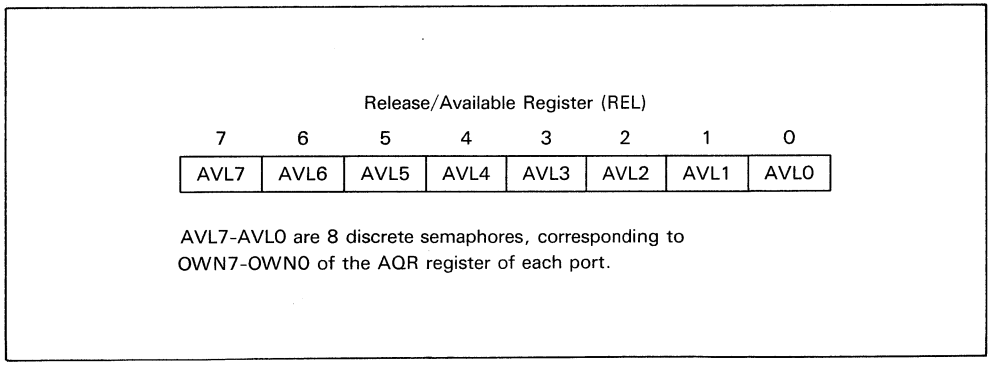
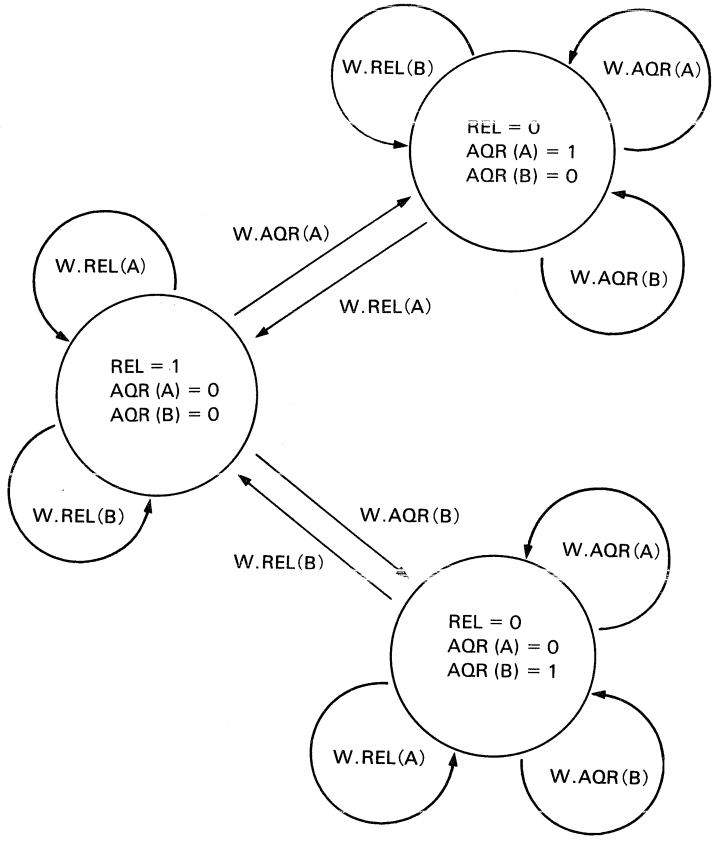


Figure 10. Release/Available Register



Note: W. REL (A): Write 1 to bit of REL (A)
W. REL (B): Write 1 to bit of REL (B)
W. AQR (A): Write 1 to bit of AQR (A)
W. AQR (B): Write 1 to bit of AQR (B)

Figure 11. AQR, REL Register State Transition Diagram

Data Register (PADR0, PBDR0, PADR1, PBDR1)

Each port of the S-DPRAM has two data registers (figure 12). The data transferred through these registers depends on the S-DPRAM operating mode.

DPRAM Mode, Indirect Addressing Operation: An access to a port's data register in DPRAM mode results in an indirect access to the target register or RAM. If PADR0 or PBDR0 is accessed, the address will be supplied by PAAR0 or PBAR0. If PADR1 or PBDR1 is accessed, the address will be supplied by PAAR1 or PBAR1 (table 6).

The opposite port's registers are also accessible in indirect addressing mode. This facilitates system status checking and more efficient data transfer. Also, in this mode the SCFE register can be defined to allow the address register to increment by 1, decrement by 1, or remain unchanged after each indirect access.

FIFO Mode: During FIFO mode, accessing these registers transfers data to and from the two FIFOs. The data transfer direction is defined by bits F1D and F0D in the CNFG register.

PADR0 or PBDR0 transfer data between FIFO 0 and the corresponding port. Similarly PADR1 or PBDR1 transfer data between FIFO 1 and the corresponding port (table 7).

The RAM address for FIFO accesses is internally supplied from the port address registers PAAR0, PBAR0, PAAR1, and PBAR1 (table 8). The registers are automatically incremented after each transfer. These registers should not be accessed in FIFO mode.

Table 6. Address Register Used as Pointer

Port	Accessed Data Register	Pointer Address Register
Port A	PADR 0	PAAR 0
	PADR 1	PAAR 1
Port B	PBDR 0	PBAR 0
	PBDR 1	PBAR 1

Table 7. FIFO 0/1 and Data Registers

Port	FIFO	Accessed Data Register
Port A	FIFO 0	PADR 0
	FIFO 1	PADR 1
Port B	FIFO 0	PBDR 0
	FIFO 1	PBDR 1

Table 8. Address Control in FIFO Mode

FIFO	Pointer	Address Register
FIFO 0	Bottom (read)	PAAR 0
	Top (write)	PBAR 0
FIFO 1	Bottom (read)	PAAR 1
	Top (write)	PBAR 1

Note: Top = Top of FIFO, address for write transaction
Bottom = Bottom of FIFO, address for read transaction

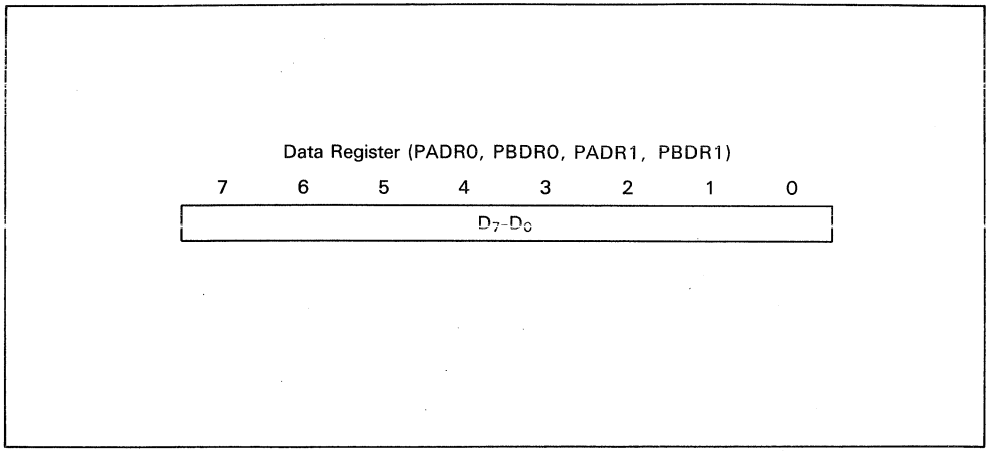


Figure 12. Data Register

FIFO Request Control Register (FRC(A), FRC(B))

The FRC registers (figure 13) control the FIFO request output signals $\overline{FRQ_1}$ and $\overline{FRQ_0}$ in FIFO mode.

The FR1E and FR0E bits enable $\overline{FRQ_1}$ and $\overline{FRQ_0}$ outputs, respectively. The FR1T and FR0T bits define the assertion conditions of these signals (tables 9, 10).

The FR1M and FR0M bits specify whether $\overline{FRQ_1}$ and $\overline{FRQ_0}$ are asserted as pulse or level outputs. As a pulse output, a $\overline{FRQ_1}$ or $\overline{FRQ_0}$ pulse is asserted each time a FIFO bus transaction occurs in the specified direction, and is held for as long as the asserting condition remains true. As a level output, $\overline{FRQ_1}$ or $\overline{FRQ_0}$ level is held asserted as long as the asserting condition remains true. (See timing chart for details.)

Table 9. $\overline{FRQ_1}$ Assertion Condition

F1D (CNFG Reg)	Data Access Direction	FR1T	Assertion Condition Port A	Port B
0	A: Read	1	FIFO 1 full	FIFO 1 empty
	B: Write	0	FIFO 1 not empty	FIFO 1 not full
1	A: Write	1	FIFO 1 empty	FIFO 1 full
	B: Read	0	FIFO 1 not full	FIFO 1 not empty

Table 10. $\overline{FRQ_0}$ Assertion Condition

F0D (CNFG Reg)	Data Access Direction	FR0T	Assertion Condition Port A	Port B
0	A: Read	1	FIFO 0 full	FIFO 0 empty
	B: Write	0	FIFO 0 not empty	FIFO 0 not full
1	A: Write	1	FIFO 0 empty	FIFO 0 full
	B: Read	0	FIFO 0 not full	FIFO 0 not empty

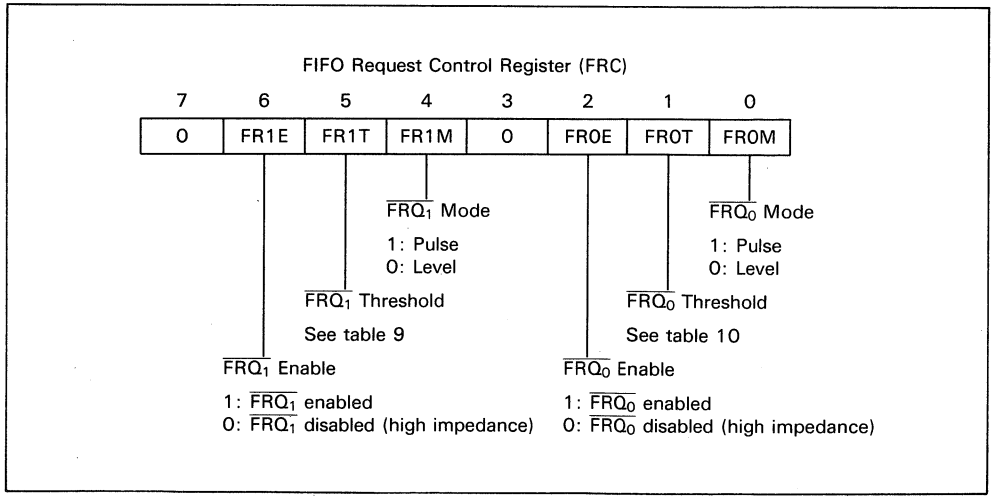


Figure 13. FIFO Request Control Register

Sequence Control and FIFO Error Register (SCFE(A), SCFE(B))

The SCFE register (figure 14) has 4 bits for address register control, and 4 bits for FIFO error indication.

The upper 4 bits (CNT1, DEC1, CNT0, DEC0) control the corresponding address register count. If CNT1/CNT0 = 0, the address register will not change after access to the corresponding data register. If CNT1/CNT0 = 1, the address register will decrement by when DEC1/DEC0 = 1 or increment by 1 when DEC1/DEC0 = 0 (table 11).

Table 11. Address Register Count Control (DPRAM-Indirect Addressing Mode)

Accessed Data Register	CNT0	Address Register DEC0 Counting			CNT1	DEC1
PADR1/PBDR1	PAAR1/PBAR1	0	x	x	x	+ 0
		1	0	x	x	+ 1
		1	1	x	x	− 1
PADR0/PBDR0	PAAR0/PBAR0	x	x	0	x	+ 0
		x	x	1	0	+ 1
		x	x	1	1	− 1

Note: x = Don't care

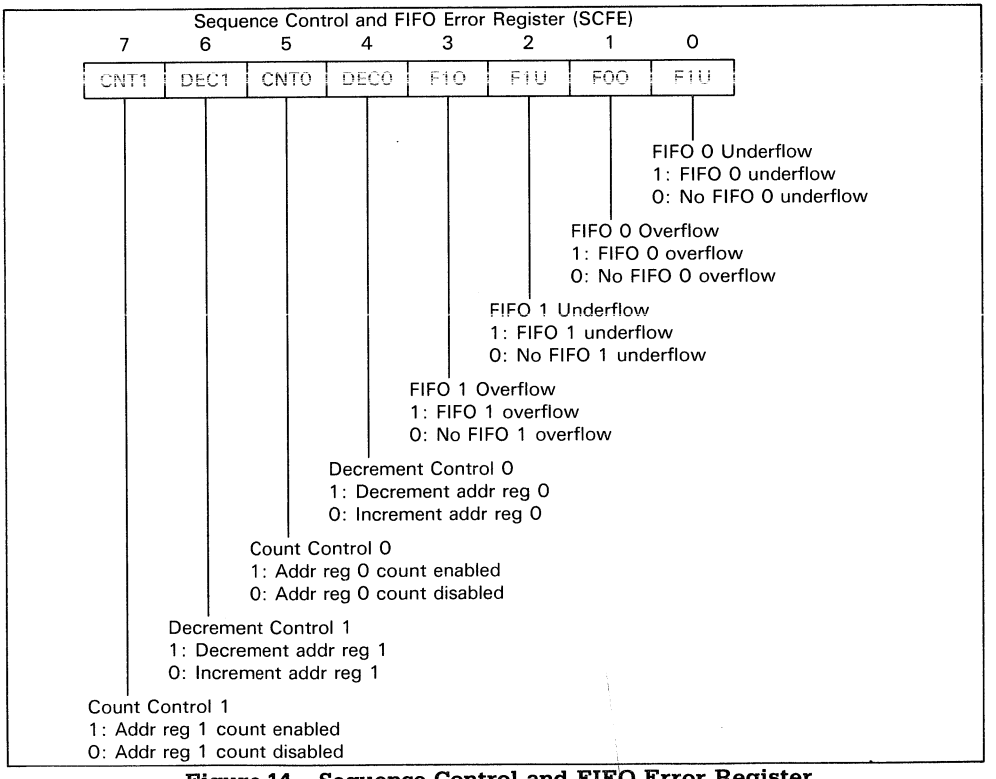


Figure 14. Sequence Control and FIFO Error Register

The lower 4 bits (F1O, F1U, F0O, F0U) indicate FIFO 1/0 overflow and underflow errors. After these errors are detected, the FIFO must be initialized using the F0FL and F1FL bits of the CMD register. These bits remain set until the FIFO is initialized until a reset occurs.

Address Register (PAAR0, PBAR0, PAAR1, PBAR1)

The S-PDRAM has two address registers (figure 15) for each port. These registers specify the RAM or register address during indirect addressing in DPRAM mode. The automatic address count is controlled by the CNT1, DEC1, CNT0, and DEC0 bits of the SCFE registers. In FIFO mode, these registers are used as the read/write pointers, and cannot be accessed externally.

Parameter Registers (PRAM31-PRAM0)

The 32-byte PRAM registers PRAM31-PRAM0 (figure 16) are user definable registers. They can be used for passing parameters between ports, or for extra storage space. These registers are shared by both ports.

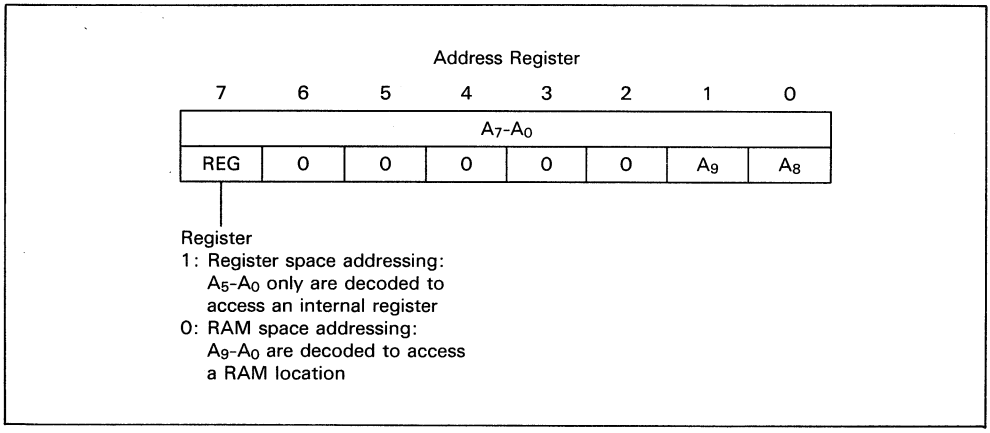


Figure 15. Address Register

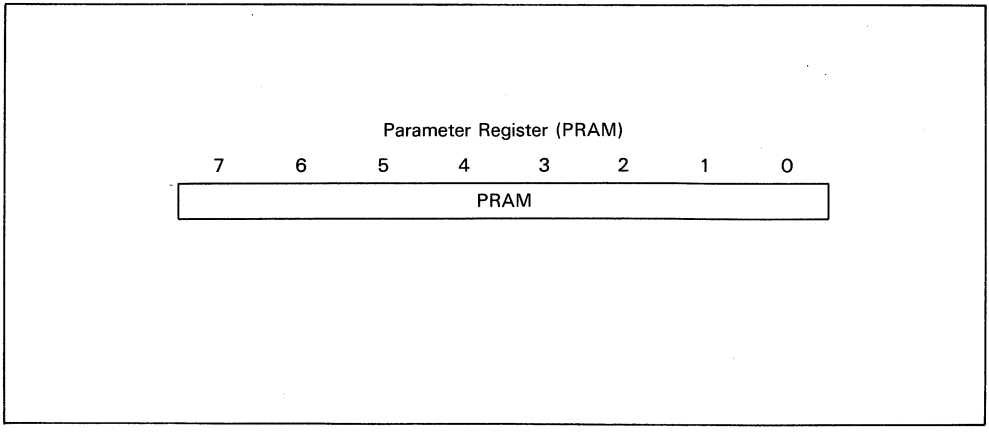


Figure 16. Parameter Register

Reset

Figures 17 and 18 show the procedure for driving the S-DPRAM after reset.

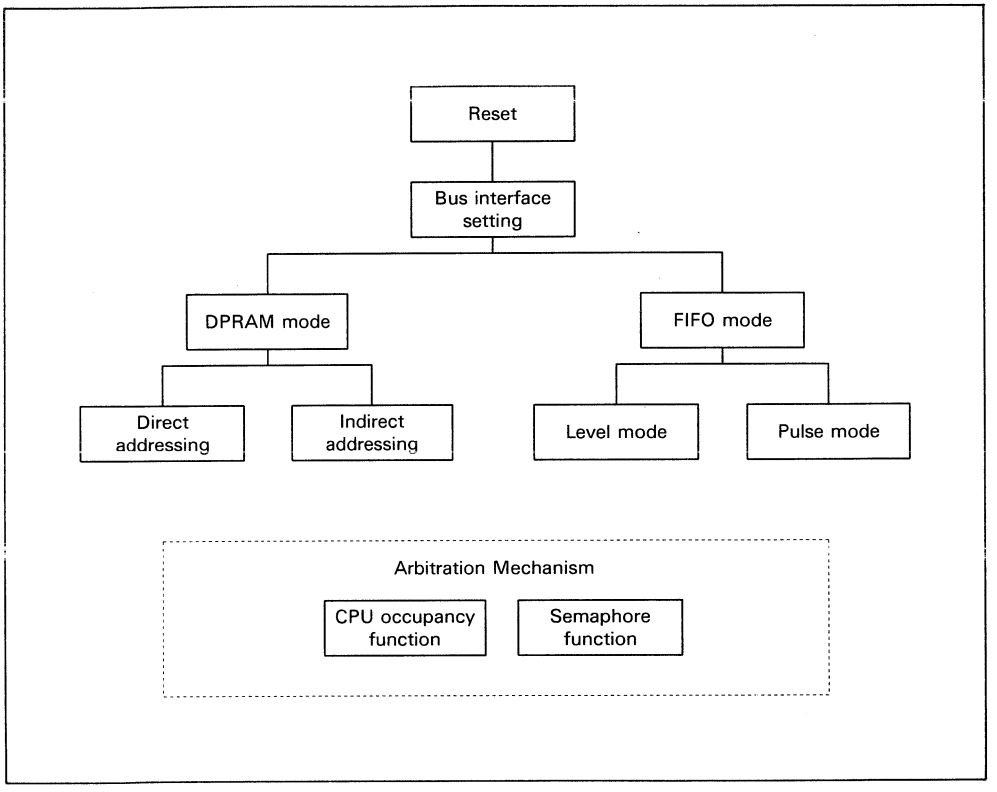


Figure 17. S-DPRAM Setup

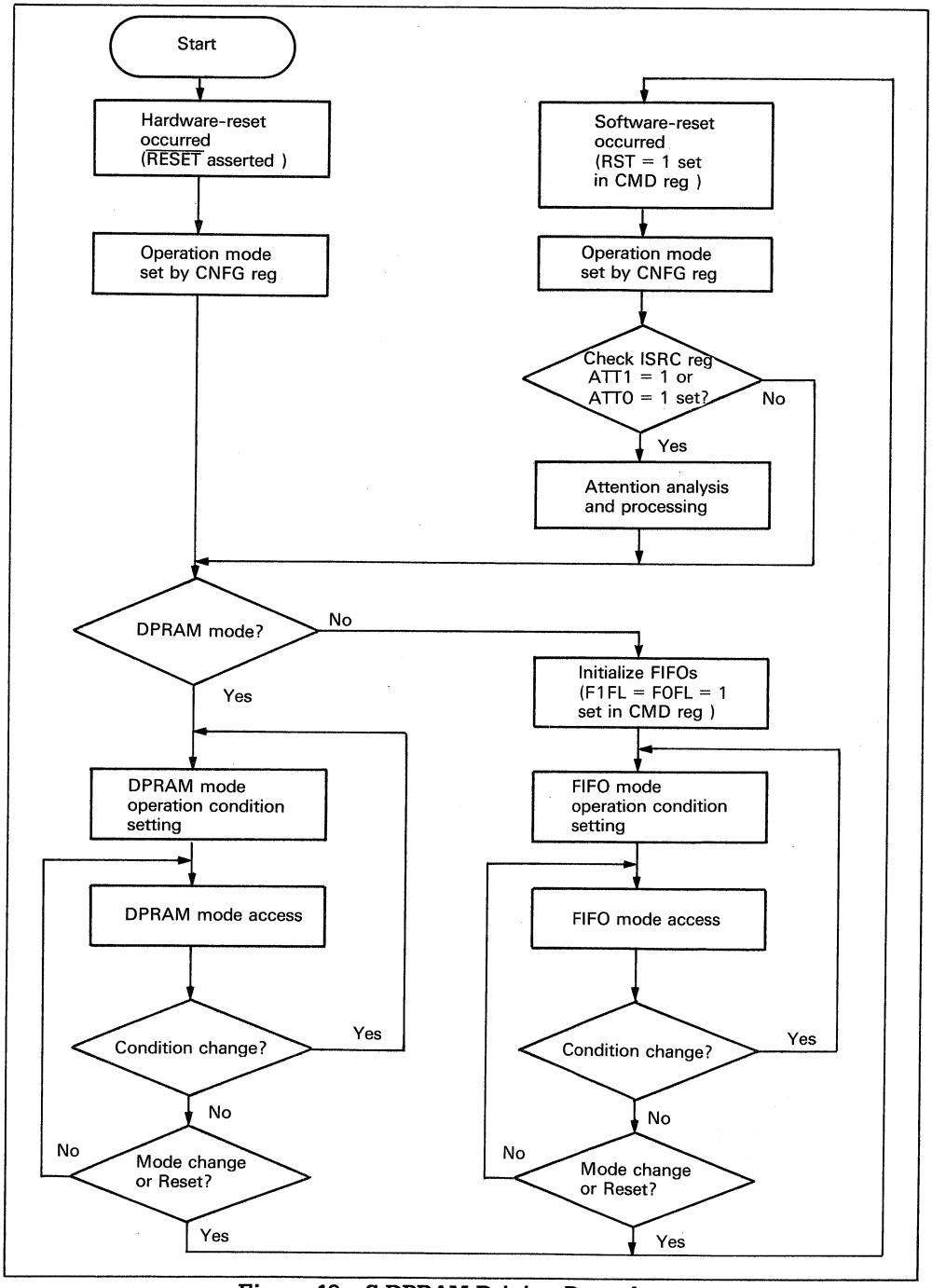


Figure 18. S-DPRAM Driving Procedure

The S-DPRAM performs two types of reset operations: hardware reset due to an external signal assertion and software reset due to a command setting (table 12).

- Hardware reset: Asserting the $\overline{\text{RESET}}$ input places the S-DPRAM into the initial state. Hardware reset is used for system initialization such as power-on reset, and must be performed after applying power.
- Software reset: Writing a 1 into the RST bit of the CMD register of either port initializes the device. Software reset does not affect the interrupt flags (AP1 and AP0 of CMD register or ATT1 and ATT0 of ISRC register).

  Owing to this architecture, the S-DPRAM can recognize an interrupt request from the opposite port even after reset.

The S-DPRAM is set to the status shown in table 12 after initialization, and is therefore operable immediately after reset in a normal interface system.

Bus Interface

Each port's I/O bus can be configured as a non-multiplexed or multiplexed address and data bus. Non-multiplexed mode is selected when ABUS/BBUS bit of the CNFG register is set to 0, and multiplexed mode when it is 1. In the bus connection example of figure 19, port A is configured as a non-multiplexed bus and port B as a multiplexed bus.

In multiplexed mode, the lower address is input via address data pins AD_0-AD_7. Therefore, address pins A_0-A_5 of A_0-A_7 are left unused. A_6 and A_7, which are multipurpose lines, are switched to A_8 and A_9 and used as input pins for the upper address. It should be noted that the unused A_0-A_5 must be connected to GND. Since the S-DPRAM is set to non-multiplexed mode after initialization, the CNFG register must be accessed first to have the I/O bus multiplexed. If A_0-A_5 are set to 0 by connecting them to GND, the CNFG register at register address 00 is automatically selected by asserting $\overline{\text{WRS}}$ or $\overline{\text{RDS}}$. Therefore, RS must be set high.

Table 12. S-DPRAM Status After Reset

Item	Status					
Internal register	Refer to table 3 "Internal Register: Bit Configuration and Operation"					
RAM	Not affected					
FIFO status flags		Empty	Full	Underflow	Overflow	
	FIF01	0	0	0	0	Not Empty and
	FIF00	0	0	0	0	Not Full
Terminal (both ports)	Multipurpose line (1): A_6, Multipurpose line (2): A_7, Multipurpose line (3): A_8, Data bus AD_0-AD_7: high impedance $\overline{\text{IRQ}}$: high impedance $\overline{\text{READY}}$: high level					
Operation mode	Mode: DPRAM mode Bus interface: non-multiplexed bus Access method: direct addressing method (bank = 0)					

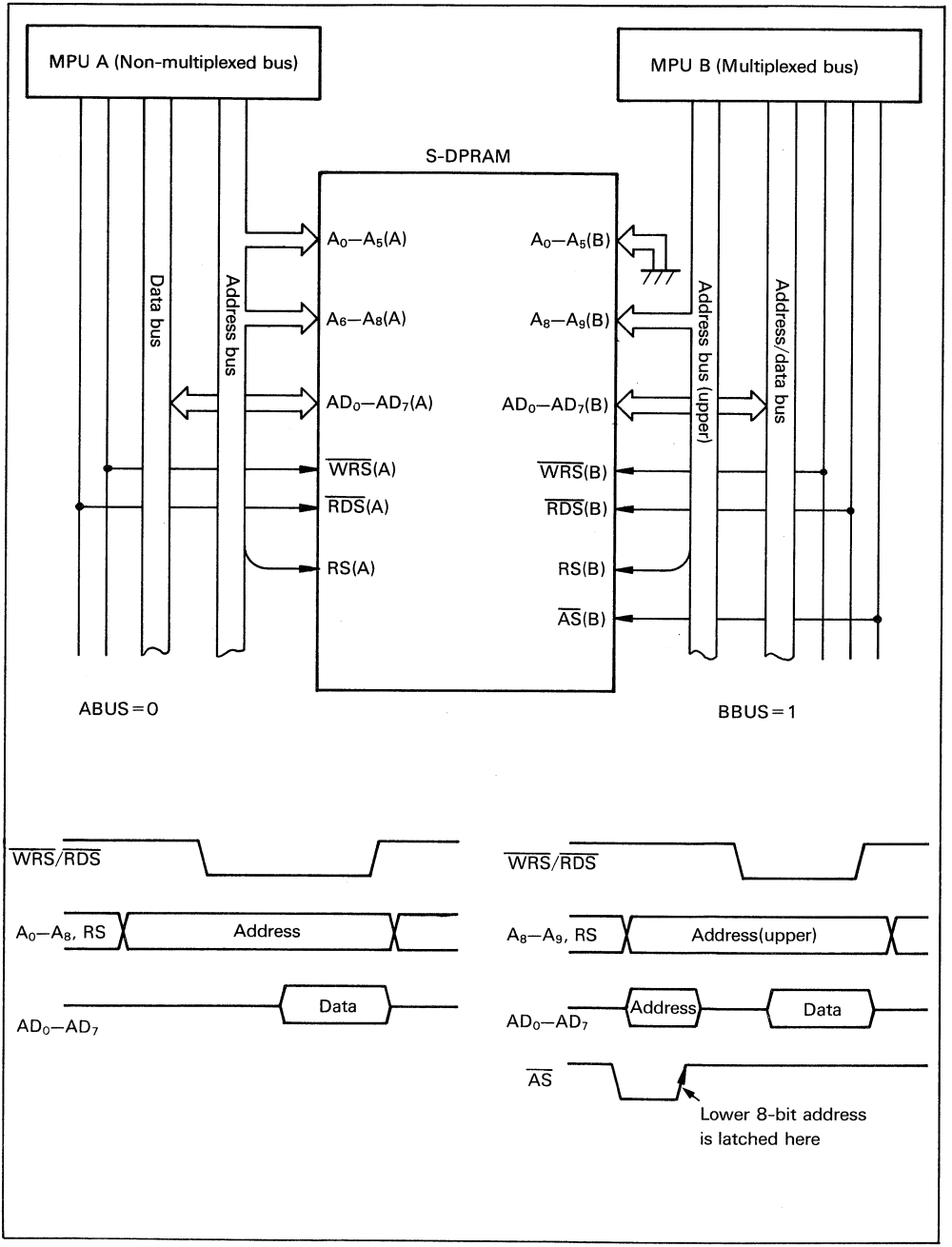


Figure 19. Bus Connection Example

Operation Mode

Two types of operation modes can be programmed in the S-DPRAM: DPRAM mode and FIFO mode. DPRAM mode is selected when the RCFG field of the CNFG register is 000, and FIFO mode when it is other than 000. (See table 5 "1024-Byte RAM Operation Mode and FIFO Size".) Please note that the registers may have various functions depending on the operation mode. Table 13 shows the bit configuration of registers in each mode.

Table 13. Bit Configuration of Internal Registers

DPRAM mode (RCFG = 000)

Address	Register name	Bit configuration 7	6	5	4	3	2	1	0
R00	CNFG	ABUS	BBUS	RCFG			0	—	—
R01	CMD	AP1	AP0	RST	0	0	0	—	—
								B1SL	B0SL
R02	IEN	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0
R03	ISRC	ATT1	ATT0	RELE	—	—	—	—	—
R04	STS	IRQ	0	0	0	0	0	—	—
								B1EN	B0EN
R05	ARB	PID							
R06	AQR	OWN7	OWN6	OWN5	OWN4	OWN3	OWN2	OWN1	OWN0
R07	REL	AVL7	AVL6	AVL5	AVL4	AVL3	AVL2	AVL1	AVL0
R08	PA/B DR0	D_7-D_0 (Indirect addressing)							
R09	PA/B DR1	D_7-D_0 (Indirect addressing)							
R0A	FRC	0	—	—	—	0	—	—	—
R0B	SCFE	CNT1	DEC1	CNT0	DEC0	0	0	0	0
R0C	PA/B AR0(L)	A_7-A_0							
R0D	PA/B AR0(H)	REG	0	0	0	0	0	A_9	A_8
R0E	PA/B AR1(L)	A_7-A_0							
R0F	PA/B AR1(H)	REG	0	0	0	0	0	A_9	A_8
R10 : R2F	PRAM	PRAM							

FIFO mode (RCFG ≠ 000)

Address	Register name	Bit configuration 7	6	5	4	3	2	1	0
R00	CNFG	ABUS	BBUS	RCFG			0	F1D	F0D
R01	CMD	AP1	AP0	RST	0	0	0	F1FL	F0FL
								—	—
R02	IEN	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0
R03	ISRC	ATT1	ATT0	—	FERR	F1F	F1E	F0F	F0E
R04	STS	IRQ	FRQ1	FRQ0	FERR	F1F	F1E	F0F	F0E
								—	—
R05	ARB	PID							
R06	AQR	OWN7	OWN6	OWN5	OWN4	OWN3	OWN2	OWN1	OWN0
R07	REL	AVL7	AVL6	AVL5	AVL4	AVL3	AVL2	AVL1	AVL0
R08	PA/B DR0	D_7-D_0							
R09	PA/B DR1	D_7-D_0							
R0A	FRC	0	FR1E	FR1T	FR1M	0	FR0E	FR0T	FR0M
R0B	SCFE	—	—	—	—	F1O	F1U	F0O	F0U
R0C	PA/B AR0(L)	FIFO 0: A=Read pointer (L), B=Write pointer (L)							
R0D	PA/B AR0(H)	FIFO 0: A=Read pointer (H), B=Write pointer (H)							
R0E	PA/B AR1(L)	FIFO 1: A=Read pointer (L), B=Write pointer (L)							
R0F	PA/B AR1(H)	FIFO 1: A=Read pointer (H), B=Write pointer (H)							
R10 : R2F	PRAM	PRAM							

Note: 0: Write causes no action, and read as 0 only.
—: Invalid in the specified operation mode.

DPRAM Mode

In DPRAM mode, 1024-byte RAM can be used as shared memory accessible from either port A or B. The address space accessible at a time differs depending on the bus interface configuration: non-multiplexed or multiplexed (table 15).

- Non-multiplexed mode: Up to 512 bytes can be addressed via A_0-A_8. All addresses are accessible due to bank switching by B1SL (upper) and B0SL (lower) bits of the CMD register.
- Multiplexed mode: Up to 1024 bytes can be addressed via AD_0-AD_7, A_8, and A_9. All addresses are accessible.

To increase efficiency in software development, two types of addressing methods are implemented: direct addressing and indirect addressing.

Direct Addressing Mode: In direct addressing mode, the target address is specified by externally supplied address signals and internal bank select bits B1SL and B0SL. When the I/O bus is non-multiplexed, bank select bit information is reflected on A_9. Table 14 shows how the address space is specified by B1SL and B0SL and how its status is reflected on the B1EN and B0EN bits of the STS register.

Indirect Addressing Mode: In indirect addressing mode, the target address is obtained by accessing the data register. When the data register is accessed, the corresponding address register is referenced, and memory is accessed according to this information. Therefore, the target address must be written into the address register before accessing the data register.

Table 14. Direct Addressing Mode Address Space

CMD Register Write			STS Register Read	
B1SL	**B0SL**	**Address space**	**B1EN**	**B0EN**
0	0	Not affected	Not affected	
0	1	000–1FF (lower)	0	1
1	0	200–3FF (upper)	1	0
1	1	000–1FF (lower)	0	1

Table 15. DPRAM Mode Table (RCFG=000)

		Address to be Accessed			
Addressing	**Bus interface**	**RS**	**Address inputs**	**Register**	**Associated Register**
Direct Addressing	Non-multiplexed	0	A_0-A_5 A_6-A_8	STS reg: B1EN, B0EN (A9)	CMD reg: B1SL, B0SL (for bank selection)
	Multiplexed	0	AD_0-AD_7 A_8, A_9	—	—
Indirect Addressing	Non-multiplexed	1	A_0-A_5 P(A/B) DR0 P(A/B) DR1	—	SCFE reg: CNT1, DEC1, SCFE reg: CNT0, DEC0 (for address counting)
	Multiplexed	1	AD_0-AD_5 P(A/B) DR0 P(A/B) DR1	—	PA/BAR0, PA/BAR1 register (for address reference)

Note: Refer to table 6 in the data register section for the relation between data register and address register in indirect addressing mode.

In indirect addressing mode, the address can be automatically incremented or decremented after each read/write access of the data register. Either increment, decrement, or no count can be selected by setting the SCFE register. This automatic address count function facilitates sequential memory access. In addition, two memory groups can be separately accessed because there are two channels of address registers for each port.

FIFO Mode

In FIFO mode, memory is configured as a buffer with first-in/first-out facilities. This mode is effective for sequential data communications between transmitter and receiver having different data transfer speeds. FIFO mode is selected when the RCFG field of the CNFG register equals any bit pattern from 001 to 111. In this mode, RAM is configured as two FIFOs. The size of each FIFO is determined by the RCFG field code (See table 5).

The FIFO-associated registers are listed in table 16. They are implemented for both ports independently. FIFOs 0 and 1 are separately controlled by these registers. The RCFG field and FERR bit are shared by FIFO 0 and 1, while the others are respectively provided for each FIFO.

Indirect addressing mode is disabled in FIFO mode, since the address registers are used for FIFO read/write pointers. Therefore, the opposite port's registers are not accessible in this mode. Refer to the subsection "Special FIFO Mode Application" for access to the opposite port's registers.

The S-DPRAM $\overline{FRQ}$ output signal represents FIFO status. The multipurpose line functions as $\overline{FRQ}$ in FIFO mode. The FRC register controls the following with respect to $\overline{FRQ}$: output enabled or disabled, assertion condition, and output waveform mode. In particular, for output waveform mode, either level mode or pulse mode can be selected depending on the system used.

Table 16. FIFO-Associated Registers

	Associated Bit		
Register Name	**FIFO 0**	**FIFO 1**	**Function**
CNFG	RCFG		FIFO configuration (001 – 111)
	F0D	F1D	FIFO data transfer direction
CMD	F0FL	F1FL	FIFO initialization
STS	FRQ0	FRQ1	$\overline{FRQ_0}$ & $\overline{FRQ_1}$ outputs status
	FERR		FIFO error status
	F0F, F0E	F1F, F1E	FIFO full or empty
ISRC	FERR		FIFO error status
	F0F, F0E	F1F, F1E	FIFO full or empty
FRC	FR0E, FR0T, FR0M	FR1E, FR1T, FR1M	$\overline{FRQ_0}$, $\overline{FRQ_1}$ mode setting
SCFE	F0O, F0U	F1O, F1U	FIFO overflow or underflow
Read/write register	PADR0 (Note) PBDR0 (Note)	PADR1 (Note) PBDR1 (Note)	Data register to be accessed
Read pointer write pointer	PAAR0 (Note) PBAR0 (Note)	PAAR1 (Note) PBAR1 (Note)	Address reg to be referenced

Note: Register name

Level Mode: Level mode is selected when the FR1M or FR0M bit of the FRC register is set to 0. In this mode, $\overline{FRQ}$ is asserted continuously as long as the assertion condition defined by FR1T or FR0T remains true. In level mode, data transfer is allowed if only the detected $\overline{FRQ}$ level is low. Example 1 shows a handshaking protocol realized using this mode.

Example 1:
FIFO partition: FIFO 1 (1024 bytes)
·····RCFG = 010
Data transfer direction: Port A to B
·····F1D = 1
Output enable: $\overline{FRQ1}$ output enabled
·····FR1E = 1
Waveform mode: Level mode·····FR1M = 0
Threshold: A = Empty, B = Full·····FR1T = 1

Port A
(1) $\overline{FRQ}$ is asserted and FIFO is judged to be empty.
(2) CPU writes up to 1024 bytes of data into FIFO
(3) Wait until the next assertion.

Port B
(1) $\overline{FRQ}$ is asserted and FIFO is judged to be full.
(2) CPU reads up to 1024 bytes of data from FIFO
(3) Wait until the next assertion.

Data transfer is carried out by repeating procedures (1) to (3). A different handshaking protocol uses different threshold conditions.

Example 2:
Threshold: A = Not full, B = Not empty
·····FR1T = 0
(Other conditions are the same as those in example 1)

Port A
(1) $\overline{FRQ}$ is asserted and FIFO is judged to be not full.
(2) Write access continues until $\overline{FRQ}$ is negated (until FIFO becomes full)

Port B
(1) $\overline{FRQ}$ is asserted and FIFO is judged to be not empty.
(2) Read access continues until $\overline{FRQ}$ is negated (until FIFO becomes empty)

Data transfer is carried out by repeating procedures (1) to (2).

Notes for HD63310R interface: The $\overline{FRQ}$ signal of the HD63310R is negated after it completes the $\overline{WRS}$ cycle. and therefore $\overline{FRQ}$ acknowledge timing must be specified after $\overline{WRS}$ cycle completion. In general, t_{FNLW}, the $\overline{FRQ}$ negation delay time at write access, is 150 ns. Taking the delay due to access contention into account, at least 400 ns of delay is required after $\overline{WRS}$ negation.

Pulse Mode: Pulse mode is selected when the FR1M or FR0M bit of the FRC register is set to 1. In this mode, $\overline{FRQ}$ is asserted and negated repeatedly each time a data transfer occurs as long as the assertion condition defined by FR1T or FR0T remains true. In pulse mode, handshaking takes place by detecting the falling edge of $\overline{FRQ}$ (figure 20).

Example:
FIFO partition: FIFO 0 (1024 bytes)
····· RCFG = 001
Data transfer direction: Port B to A
····· F0D = 0
Output enable: $\overline{FRQ0}$ output enabled
····· FR0E = 1

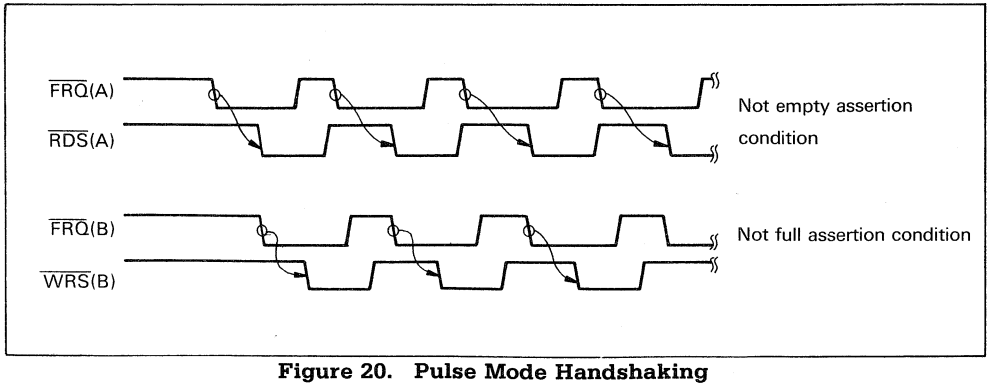


Figure 20. Pulse Mode Handshaking

Waveform mode: Pulse mode
..... FR0M = 1
Threshold: A = Not empty, B = Not full
..... FR0T = 0

Port A— Reads 1-byte of data from FIFO upon each assertion of $\overline{FRQ}$

Port B— Writes 1-byte of data into FIFO upon each assertion of $\overline{FRQ}$

In pulse mode, handshaking is performed by detecting the falling edge of $\overline{FRQ}$, and therefore special timing is not required. In addition, overrun (excessive write/read access) due to $\overline{FRQ}$ delay as in level mode cannot occur, since the falling pulse count agrees with the transfer byte count in this mode.

FIFO Operation: Figure 21 illustrates an example of FIFO operation. In FIFO mode, RAM is configure as two ring-shaped memories. Each memory has read/write pointers and thus can be accessed independently. The PBAR (0/1) and PAAR (0/1) registers, used in indirect addressing DPRAM mode, are assigned here as write pointer and a read pointer, respectively. These pointers are automatically incremented upon each access. During write access, a write pointer is incremented after writing data into the address indicated by the write pointer. In the same way, a read pointer is incremented after reading data from the address indicated by the read pointer. When a write pointer value equals a read pointer value, FIFO memory is considered to be empty. When a write pointer value exceeds a read pointer value by one, FIFO memory is considered to be full. These FIFO statuses are represented by the status bits of internal registers or are output via the $\overline{FRQ}$ line.

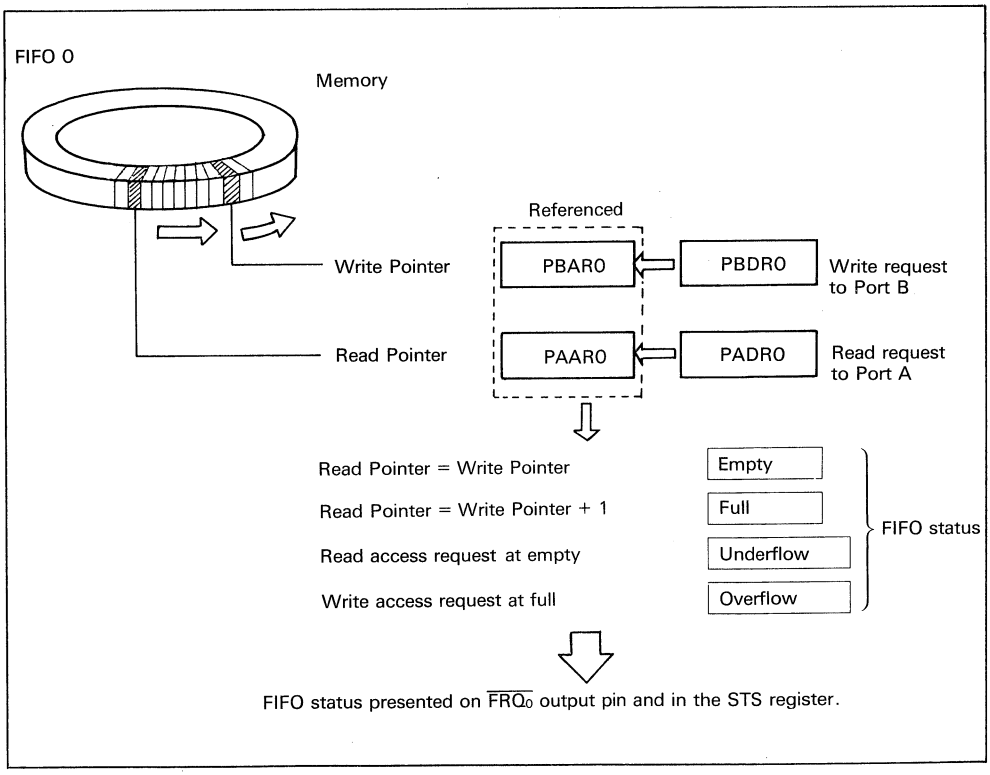


Figure 21. FIFO 0 Control Example (Transfer Direction: Port B to Port A)

Special FIFO Mode Application: The S-DPRAM has been basically designed as an interface between CPUs. Therefore, there are some limitations when it is used with non-intelligent devices. In particular, when the S-DPRAM is used in FIFO mode, some registers must be set and therefore the S-DPRAM cannot support an interface between non-intelligent devices.

Figure 22 shows an example of an interface between a CPU and non-intelligent device. In this example, the CPU reads sequential digital data that is converted from analog data through synchronous sampling with a clock; the digital data is then stored into FIFO. Moreover, the FIFO status is returned to the A/D converter via the FRQ line. The S-DPRAM performs handshaking by referring to this signal's status.

- Non-intelligent device setting: The address bus must be fixed to the address of the data register of the FIFO being used. $\overline{RS}$ and $\overline{RDS}$ must be set to high, and the sampling clock for A/D conversion must be input to $\overline{WRS}$. This clock circuit must be controlled using $\overline{FRQ}$.

- Register setting: Through the non-intelligent device's port, only the data register is accessible, and therefore each register must be set through the CPU's port. The opposite port's registers can be accessed using the indirect addressing method, but in FIFO mode this method cannot be used. Accordingly, the S-DPRAM must be placed in FIFO mode after the FIFO-associated registers of the opposite port are set using the indirect addressing method in DPRAM mode.

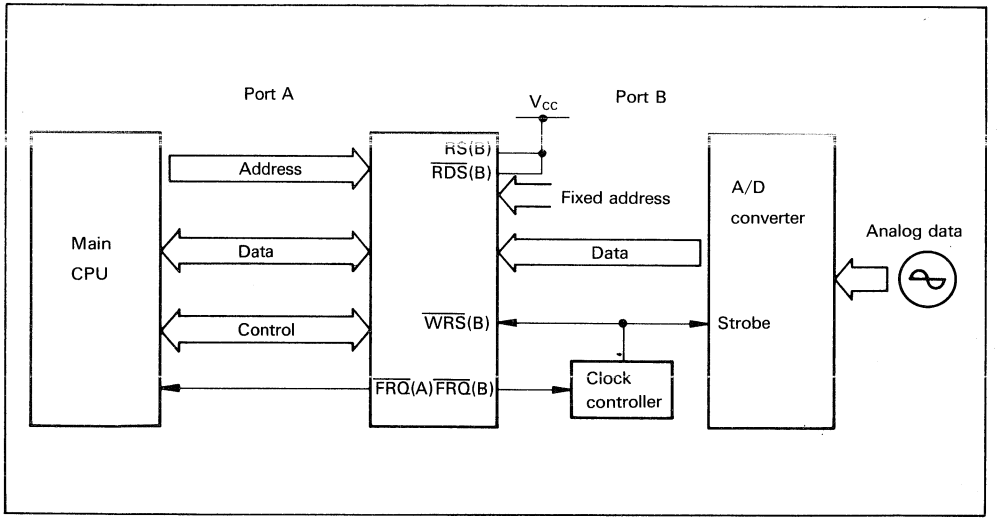


Figure 22. FIFO Application Example (CPU-A/D Converter Interface)

General Notes for FIFO Mode: Keep the following in mind when operating in FIFO mode.

1. Mode Transition: Switching from DPRAM or FIFO operation mode does not affect the contents of registers or RAM. The FIFO status flag is reset upon transition from FIFO mode to DPRAM mode. However, when the address that will result in empty or full status is stored in DPRAM mode, the FIFO status flag is not set even if the S-DPRAM is switched to FIFO mode.

2. Underflow and overflow: Attempting a read access after empty status causes an underflow and invalid data is read out. The read pointer is incremented and the empty flag is reset. In the same way, a write access after full status causes an overflow and data at the bottom of the stack is destroyed. The write pointer is incremented and the full flag is reset.

3. Data transfer direction: When data access against the transfer direction specified by CNFG is requested, flags and FIFO operation are not affected except that input and output are replaced by each other. That is, when A to B direction is specified, a write access to port B results in a successful data write to B, and a read access from port A results in a successful data read from A; internal operation is not affected. However, it should be noted that the $\overline{FRQ}$ output condition is reversed.

4. FIFO partitioning and addresses: Table 17 shows how memory addresses are allocated corresponding to FIFO partitions.

Arbitration

The S-DPRAM arbitration function supports multiprocessor systems. It facilitates effective data communications between multiple CPUs on one system bus or between two system buses. There are two arbitration methods:
1. Software arbitration by register flag control
2. Hardware arbitration by an internal arbiter

This section describes the software arbitration control method. Hardware arbitration will be described later in the section about internal operation.

The S-DPRAM incorporates the following registers for interprocessor arbitration: arbitration register (ARB), acquire ownership register (AQR), and release/available register (REL). These registers only act as flags to control interprocessor arbitration, and are not directly related to S-DPRAM operations. Accordingly, they are designated as a flag register group and clearly distinguished from the special control register (SCR) group and address/data register group.

These registers are used for two types of arbitration: CPU occupancy or semaphore function, depending on the architecture of the multiprocessor system (table 18).

Table 17. FIFO Memory Addresses

RCFG			Memory address	
b5	b4	b3	FIFO 1	FIFO 0
0	0	1	—	000–3FF
0	1	0	000–3FF	—
0	1	1	200–3FF	000–1FF
1	0	x	300–3FF	000–2FF
1	1	x	100–3FF	000–0FF

CPU Occupancy Function

In a system having several processors on one system bus (multimaster bus system), each processor can acquire ownership of the system bus, and thus there may be contention for control of a shared resource (I/O, memory, etc). To avoid this contention, the S-DPRAM uses the ARB register to indicate which processor currently controls the shared resource . Figure 23 shows an example of a multiprocessor system configuration. In this system, processor A, B, and C, on one system bus, are connected with processor D via the S-DPRAM, sharing the I/O devices. For one of processors A, B, and C to drive the I/O controller normally, one processor must occupy the I/O device for a specific period. The following procedure gives processor A control of the printer (figure 24).

1. Processor A writes its ID code into the ARB register to acquire bus ownership of port A. After acquiring the bus ownership, processor A starts to transfer data to processor D dia the S-DPRAM, and then processor D drives the printer.
2. Since processor A performs data output on a page basis, there is an interval between one page and another when no data transfer is executed. The system bus is released to the other processors so as not to decrease system throughput.
3. However, during this interval, if processor B attempts to write its ID code into ARB, it is rejected because ARB already has the ID code of processor A (figure 25). Thus, this effective arbitration mechanism prevents processor B from using the S-DPRAM.
4. Thereafter, the bus ownership is returned to processor A and data transfer is resumed. After finishing a series of processes, processor A clears ARB by writing its ID code into ARB again, and bus ownership is then released.

Table 18. Arbitration Function

	Related Register	Mode	Function	Application
CPU occupancy function	ARB (Arbitration ownership register)	DPRAM FIFO	Requesting processor writes its ID code into ARB. The processor can acquire the S-DPRAM if the request is accepted. If ARB contains another ID code, the request is rejected.	Determines which CPU among multiple CPUs on one system bus can acquire the shared resource S-DPRAM
Semaphore function	AQR, REL (Acquire/ ownership, release/ available registers)	DPRAM	Setting AQR register bit indicates that the S-DPRAM is currently acquired by the CPU of the requesting port, and that the opposite port request is to be rejected. Ownership is released by setting the corresponding bit of REL.	Determines which CPU on which system bus can acquire the shared resource S-DPRAM

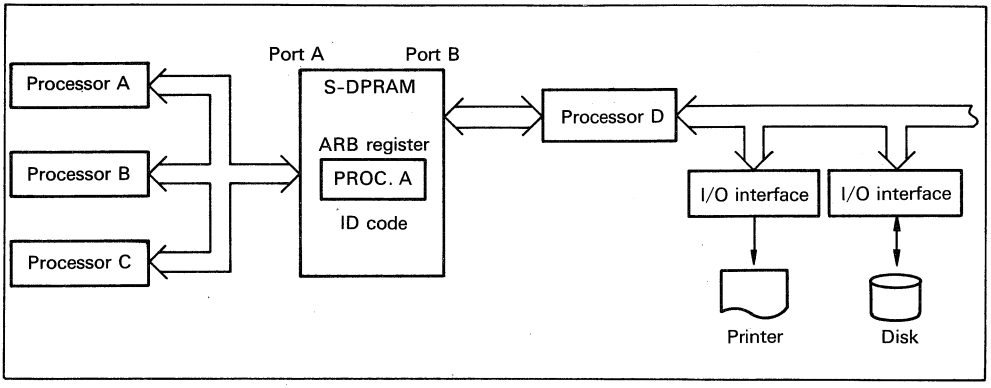


Figure 23. Multiprocessor System Configuration Example (CPU Occupancy Function)

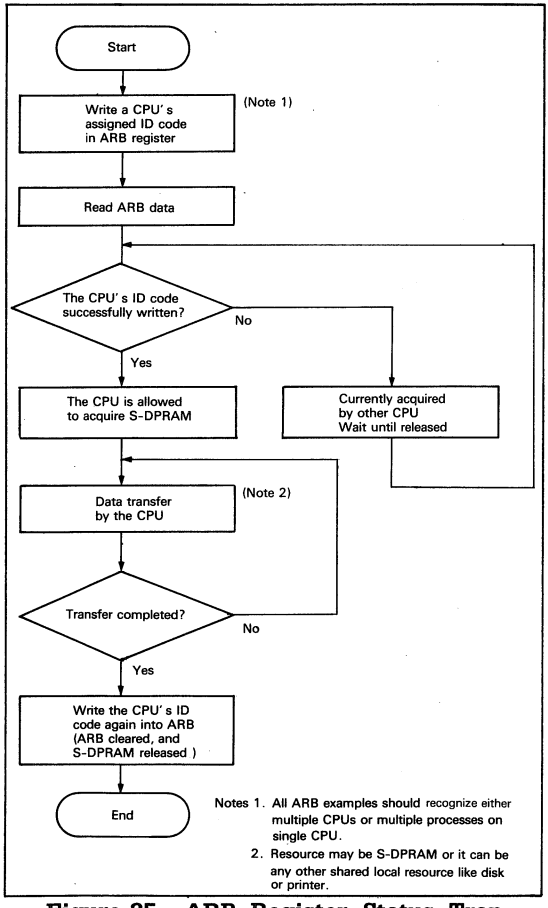


Figure 25. ARB Register Status Transition

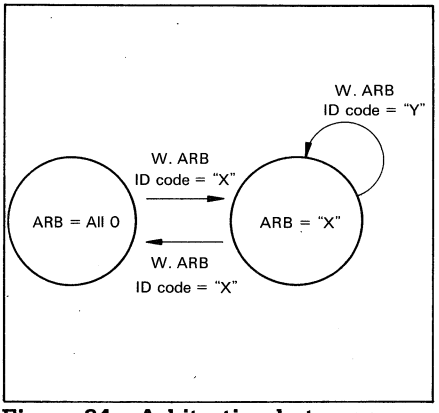


Figure 24. Arbitration between CPUs on One System Bus

Semaphore Function

For a system sharing a resource between two system buses, the S-DPRAM AQR (acquire ownership) and REL (release/available) registers arbitrate access contention in the case of simultaneous requests from both ports. These registers have the following functions and are used as a pair.

- AQR register: Represents ownership of one port against the opposite port
- REL register: Relinquishes the acquired ownership

The AQR register implements "test and set" logic circuit in hardware. "Test" logic checks the current ownership status of a resource, and "set" logic establishes the ownership of a resource before it can be acquired by another requestor.

Each register provides eight semaphores, which can discrete control eight shared resources. For instance, if 1024-byte memory is divided into eight areas, each area can be represented by a corresponding semaphore bit.

This mechanism can be applied not only to the memory of the S-DPRAM itself but also other I/O devices.

Figure 26 shows an example of a multiprocessor system configuration. In this system, processors A and B, which are respectively allocated to ports A and B, share two I/O devices and two blocks of memory in the S-DPRAM. These four resources are controlled by referring to the four corresponding semaphore bits (figure 27).

1. Processor A attempts to write a 1 into the corresponding semaphore bit AA3 to read out data from a disk. If it is successful, gate GA3 is opened and connected to the system bus of processor A. Data transfer can then be initiated between processor A and the disk.
2. At this time, if processor B attempts to write a 1 into AA3 in order to access the same disk, it is not allowed and processor B must wait until the disk is released from processor A (figure 28).
3. However, since shared resources other than this disk are free, processor B can acquire them by writing a 1 into AB0-AB2.
4. In the same way, processor A cannot access the shared resources currently acquired by processor B.
5. After each processor has completed its desired processing, the AQR register bit can be cleared by writing a 1 into the same bit position of the REL register; the corresponding shared resource is then released.

In this way, resources shared between two system buses can be effectively controlled via the semaphore registers. Note that this arbitration mechanism can also be applied to a single processor executing multiple tasks by means of time sharing.

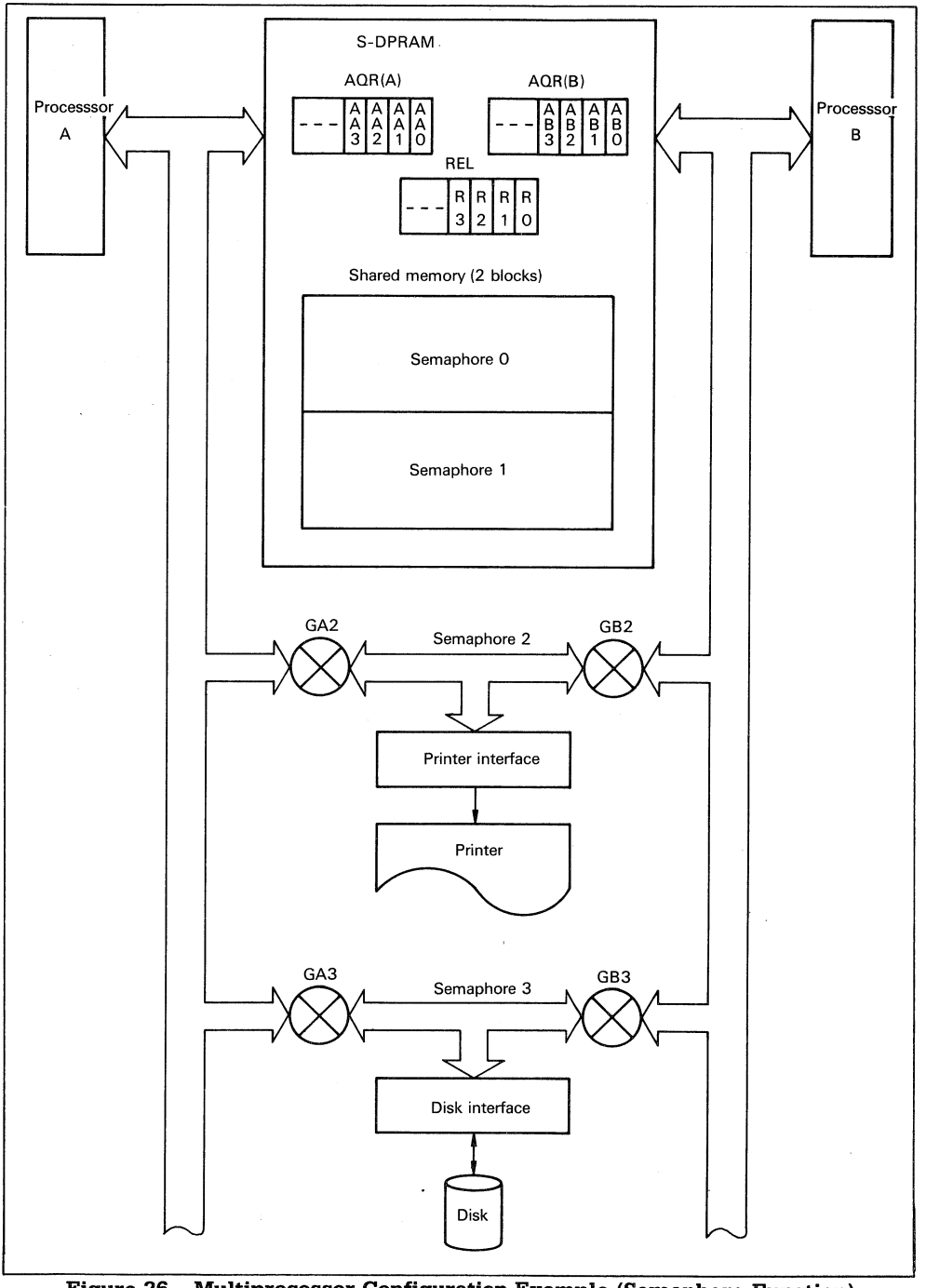


Figure 26. Multiprocessor Configuration Example (Semaphore Function)

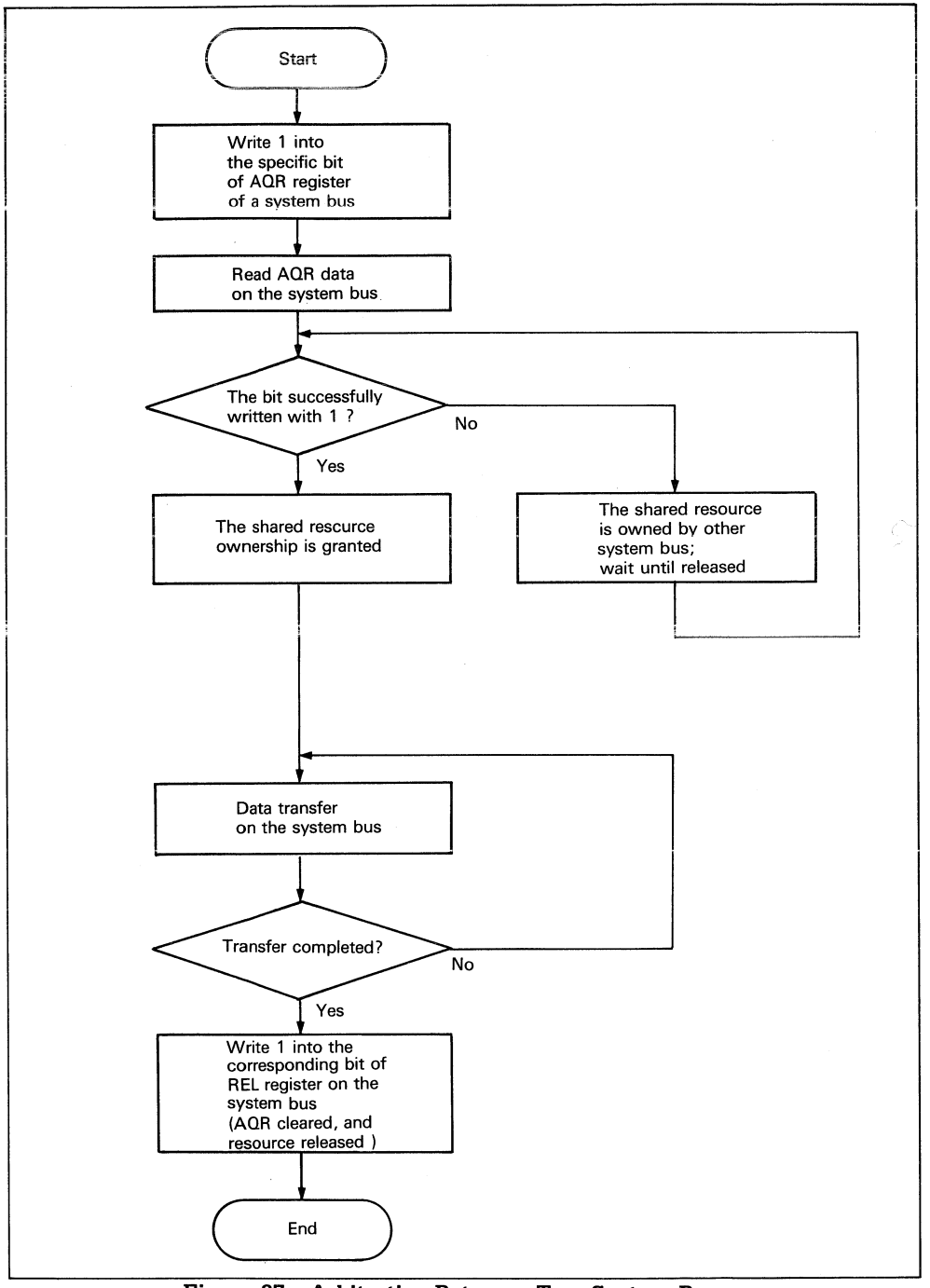
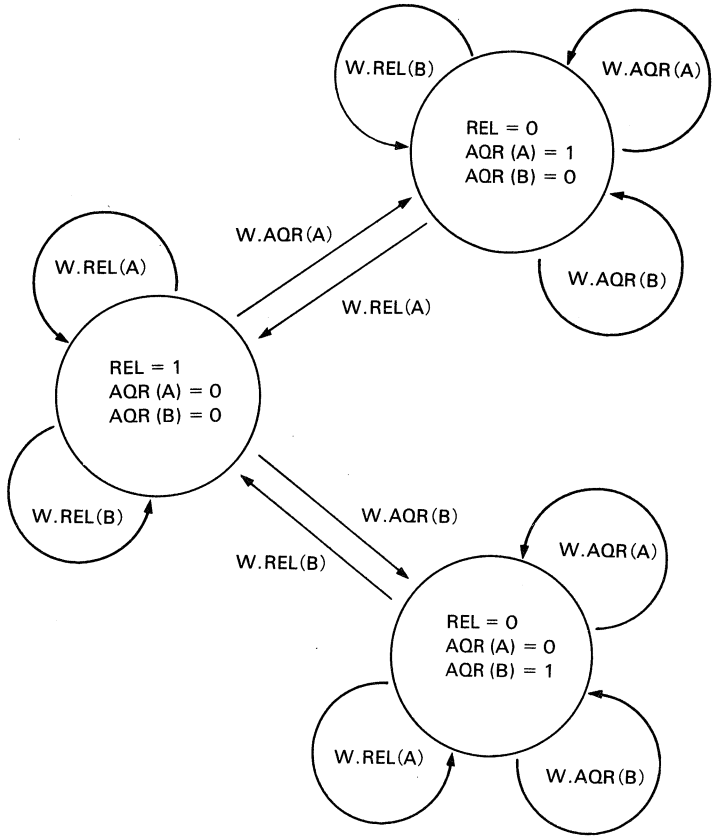


Figure 27. Arbitration Between Two System Buses



Note: W. REL (A): Write 1 to bit of REL (A)
W. REL (B): Write 1 to bit of REL (B)
W. AQR (A): Write 1 to bit of AQR (A)
W. AQR (B): Write 1 to bit of AQR (B)

Figure 28. Semaphore Register Status Transition

Internal Operation Description

Port A and port B can independently read and write internal registers and the 1024-byte RAM array of the S-DPRAM. Access requests from both ports are entirely asynchronous, and therefore access contention may occur. To avoid this contention, the internal arbiter determines the order in which the requests are serviced.

It should be noted that processing start timing may be somewhat delayed in the following cases:

1. Handling access contention between both ports
2. Waiting until busy state, which is caused by a buffered write operation

To handle this problem, the S-DPRAM $\overline{\text{READY}}$ signal indicates whether a posted request can be accepted or not. Using $\overline{\text{READY}}$, an effective interface circuit can be organized to properly control timing.

Write Operation

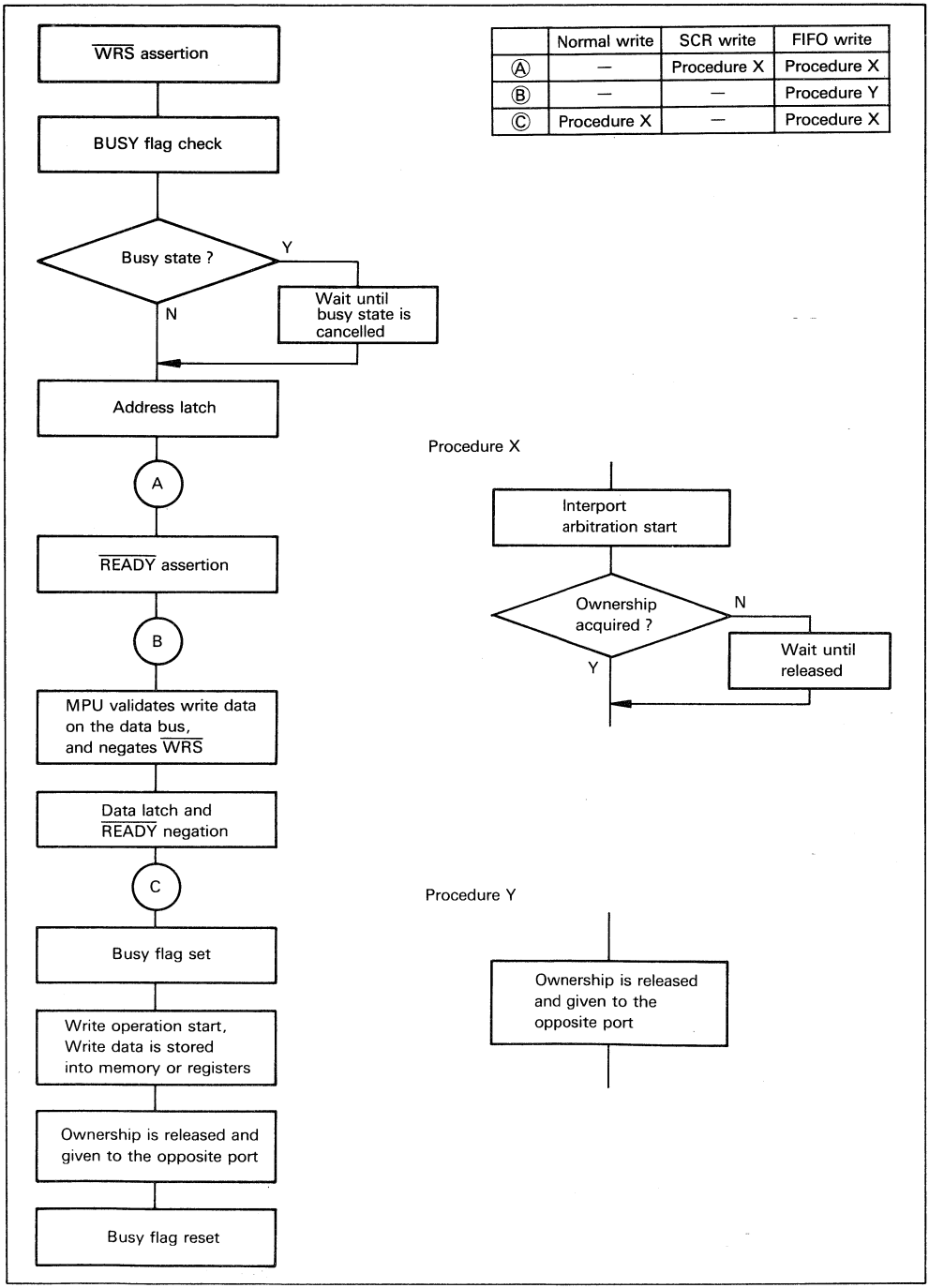
The S-DPRAM implements a buffered write operation. It is initiated by $\overline{\text{WRS}}$ assertion. When $\overline{\text{WRS}}$ is negated, write data is temporarily latched in a buffer register. Thereafter, the write operation can proceed according to the internal sequence. (SCR write and FIFO write are excluded.) Buffered write is characterized as follows:

1. Actual processing is executed during $\overline{\text{WRS}}$ high, and therefore $\overline{\text{READY}}$ is not delayed even when access contention occurs. In general, the negation period is longer than the assertion period in MPU access. Consequently, cycle times can be used effectively and system throughput can be improved.
2. For an interface between systems having different cycle times, one cycle of one port may last as long as several cycles of the other port. While $\overline{\text{WRS}}$ is asserted, an access contention cannot occur, and therefore system throughput is not reduced.

In the buffered write operation, actual processing starts while $\overline{\text{WRS}}$ is negated. Consequently, the next request cannot be serviced until the previous is finished. This state is called a busy state, and the busy flag is set accordingly. Figure 29 shows the S-DPRAM write operation sequence.

Read Operation

$\overline{\text{RDS}}$ assertion initiates read operations. In comparison with the write operation, read operation is entirely completed during $\overline{\text{RDS}}$ low. Consequently, busy states cannot occur. Figure 30 shows the S-DPRAM read operation sequence.



	Normal write	SCR write	FIFO write
Ⓐ	—	Procedure X	Procedure X
Ⓑ	—	—	Procedure Y
Ⓒ	Procedure X	—	Procedure X

Figure 29. Write Transaction

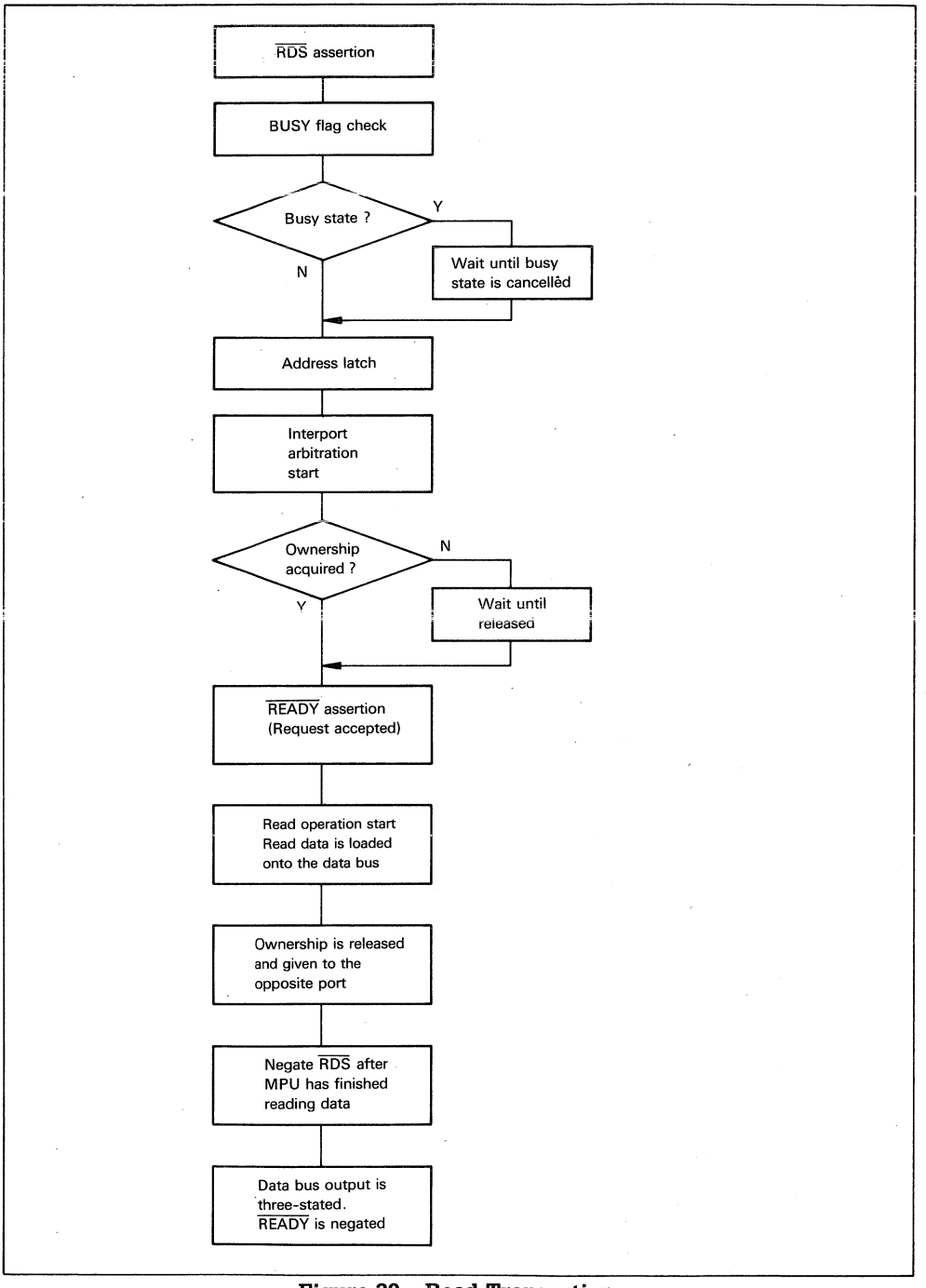


Figure 30. Read Transaction

Processing Mode

The S-DPRAM implements four types of processing modes: SCR white, FIFO write, normal write, and normal read. One of these modes is selected corresponding to memory or registers to be accessed. Figure 31 shows the timing chart for each mode.

SCR Write (Special Control Register Write)

Registers which directly control the S-DPRAM itself or are closely related to its operation are called special control registers (SCR). In SCR write mode, arbitration is performed at the falling edge of $\overline{WRS}$, and thereafter ownership is retained even during $\overline{WRS}$ or low. Consequetly, access requests from the opposite port cannot be accepted during $\overline{WRS}$ low. In other words, $\overline{READY}$ of the opposite port cannot be asserted until $\overline{WRS}$ is negated.

This mode is selected by directly accessing the registers in table 19. However, it should be noted that normal write mode is selected if they are indirectly accessed.

FIFO Write

The S-DPRAM is set to FIFO mode by setting a bit field from 001-111 into RCFG of the CNFG register. In FIFO mode, FIFOs can be read written to accessing data registers (table 20). In FIFO write mode, arbitration is performed at the falling edge of $\overline{WRS}$; ownership is then released after checking FIFO status during $\overline{WRS}$ low. Thereafter, arbitration starts again at the rising edge of $\overline{WRS}$, and data write is executed during $\overline{WRS}$ high.

Table 19. Special Control Registers

	R0	R1	R2	R3	RA	RB
Direct addressing (DPRAM mode, FIFO mode)	CNFG (COM)	CMD (A/B)	IEN (A/B)	ISRC (A/B)	FRC (A/B)	SCFE (A/B)

Table 20. FIFO Write Data Registers

	R8	R9
Indirect addressing (FIFO mode)	P(A/B)DR0	P(A/B)DR1

Normal Write

Write accesses other than SCR write and FIFO write are all designated as normal writes. That is, write accesses to registers other than SCR (by direct access) or to RAM, and all write accesses executed by indirect addressing belong to this mode (table 21). In this mode, arbitration is performed at the rising edge of $\overline{WRS}$ and data write is executed during $\overline{WRS}$ high (buffered write). Therefore, $\overline{READY}$ is not delayed even in the case of simultaneous access requests, except that processing from the previous cycle is continued.

Normal Read

All read accesses are made in normal read mode (table 22). Data read is completed during $\overline{RDS}$ low, and $\overline{READY}$ cannot be delayed due to busy states in the next cycle. In this mode, arbitration is performed at the falling edge of $\overline{RDS}$, and data read is executed in the order determined through arbitration. When the read data becomes valid, ownership is given to the opposite port after the data is latched into the output registers, and $\overline{READY}$ is then asserted. Therefore, the opposite port is not kept waiting by strobe conditions as for SCR.

Table 21. Normal Write Registers and RAM

	Register						RAM
Direct addressing (DPRAM mode, FIFO mode)	R4 STS (A/B)	R5 ARB (A/B)	R6 AQR (A/B)	R7 REL (COM)	RC-RF Address register (A/B)	R10-R2F Parameter register (COM)	M000
Indirect addressing (DPRAM mode)	R0-RF: Requesting port's control register R10-R2F: Shared parameter register R30-R3F: Opposite port's control register						M3FF

Table 22. Normal Read Register and RAM

	Register	RAM
Direct addressing (DPRAM mode, FIFO mode)	R0-RF: Requesting port's control register R10-R2F: Shared parameter register R30-R3F: Opposite port's control register	M000
Indirect addressing (DPRAM mode, FIFO mode)		M3FF

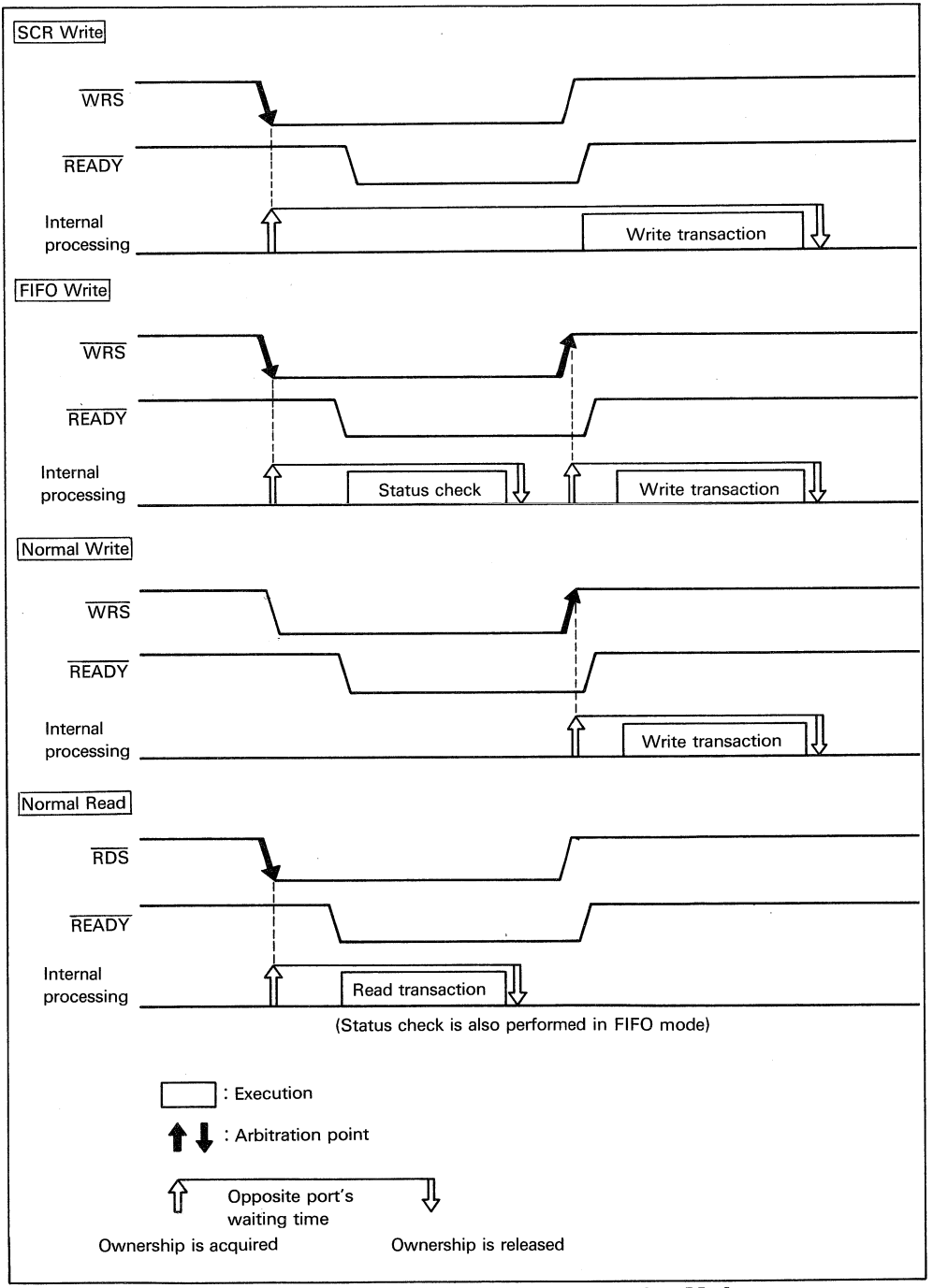


Figure 31. Timing Chart for Each Processing Mode

S-DPRAM Expansion

S-DPRAM Capacity Expansion

The S-DPRAM incorporates a 1024-byte RAM, but its capacity can be expanded if necessary. Figure 32 shows an example of a system with a 2-kbyte RAM.

S-DPRAM capacity can be expanded in the same way as other standard memories without any restrictions. In a RAM-expanded system, there must be a mechanism to control which S-DPRAM is accessed. This is done by combining CS (chip select), obtained by decoding the upper address, and $\overline{RDS}/\overline{WRS}$.

$\overline{IRQ}$ of each S-DPRAM can be processed independently, or processed jointly by connecting all $\overline{IRQ}$ lines together. $\overline{IRQ}$ is an open-drain output, and can easily be wired-ORed with a pull-up resistor.

Each S-DPRAM is assigned to a different address, and thus can be exclusively accessed. Therefore, negative logic OR is applied to all S-DPRAM $\overline{READY}$s to return $\overline{READY}$ to the MPU when at least one $\overline{READY}$ is asserted. That is, $\overline{READY}$ lines are connected by an AND gate.

S-DPRAM capacity can be expanded in DPRAM mode only. For the S-DPRAM in FIFO mode, its capacity cannot be expanded since the functions related to expansion of the $\overline{FRQ}$ signal, etc, are not supported.

S-DPRAM Bit Width Expansion

The S-DPRAM basically supports an 8-bit data bus, but its bit width can be expanded to 16 bits or 32 bits. Figure 32 shows an example of a system with a 16-bit data bus.

The bit width can also be expanded in the same way as with other standard memories. $\overline{RDS}$ and $\overline{WRS}$, generated by address control and other input signals, must be connected to each S-DPRAM in parallel.

In this system, data read/write must be executed after both upper byte and lower byte S-DPRAMs are ready for data transfer. Therefore, $\overline{READY}$s must be connected by an OR gate to return $\overline{READY}$ to the MPU when both $\overline{READY}$s are asserted.

Please note that each S-DPRAM can arbitrate independently using its own arbiter. Accordingly, port ownership may be confused between the upper and lower byte S-DPRAMs. For example, when the MPU accesses two S-DPRAM simultaneously, port A is selected for upper bytes and port B for lower bytes, or vice versa. In this way, two S-DPRAMs may respectively acquire different MPUs (figure 34).

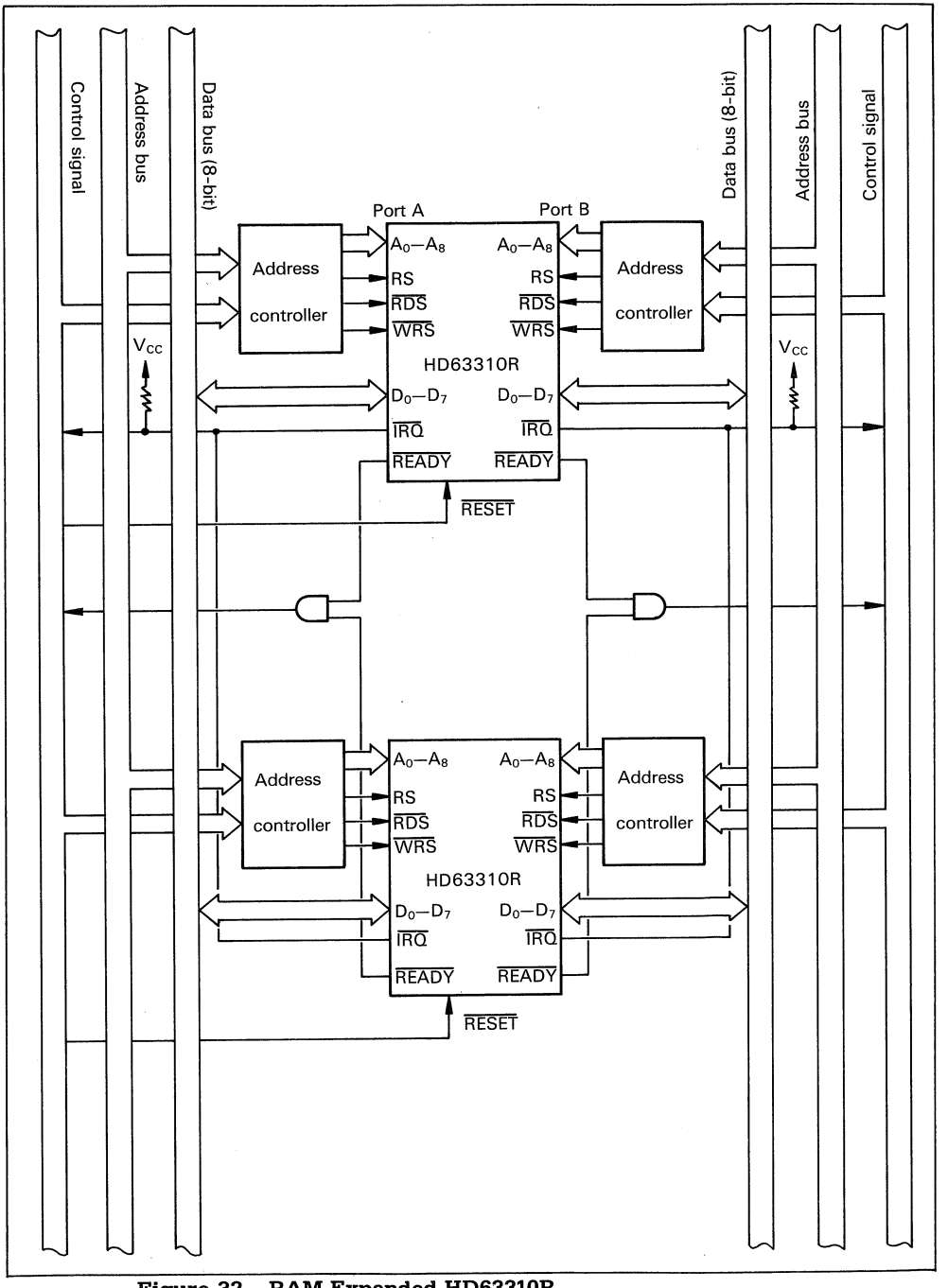


Figure 32. RAM-Expanded HD63310R (DPRAM Mode, 8-Bit Width, Address Expansion)

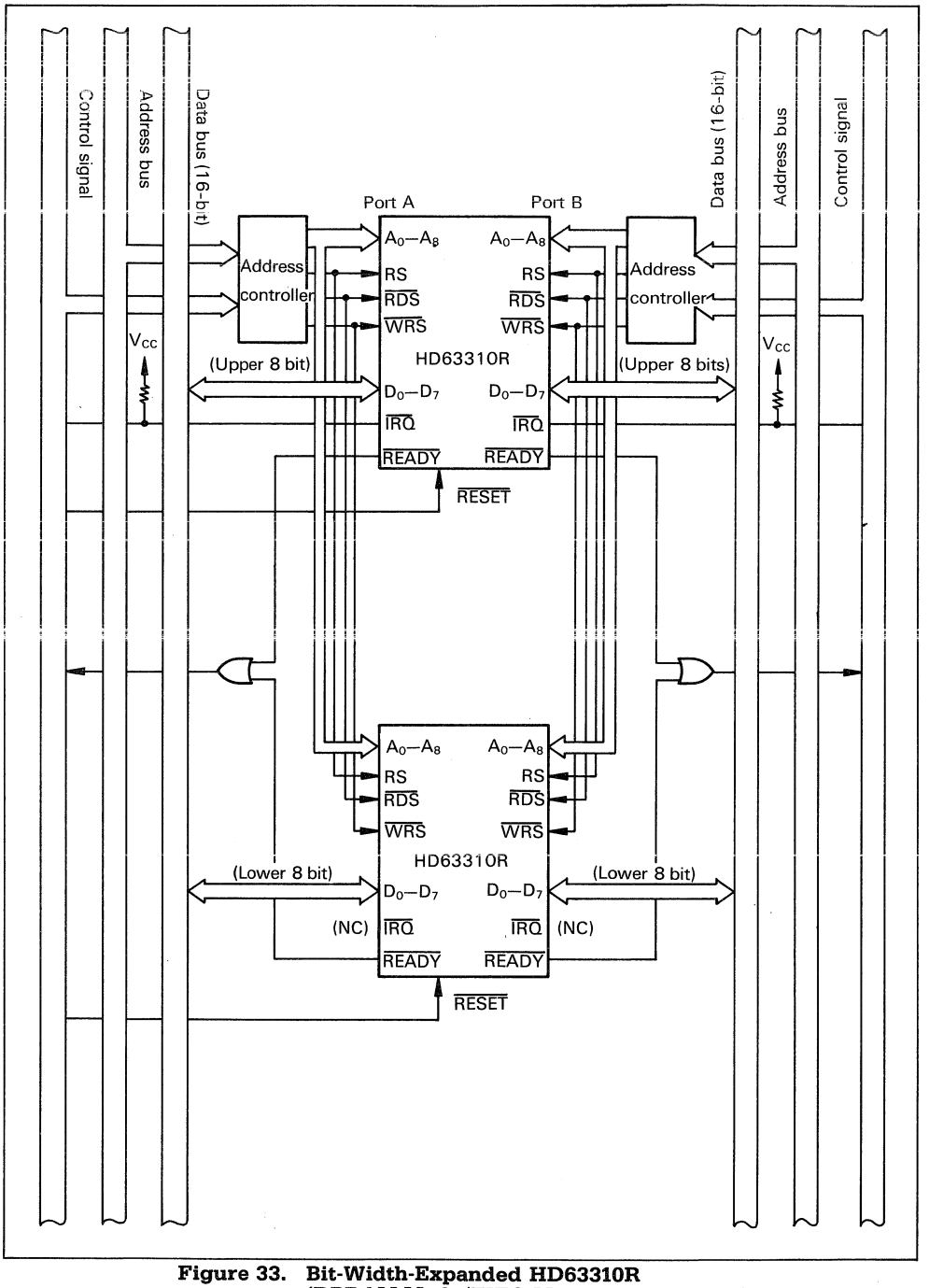


Figure 33. Bit-Width-Expanded HD63310R (DPRAM Mode/FIFO Mode, 16-Bit Width)

$\overline{\text{READY}}$ is asserted by the S-DPRAM which has acquired ownership, but it cannot be returned to the MPU until the other $\overline{\text{READY}}$ is asserted. In this case, if one of the S-DPRAMs is writing to an SCR (special control register) by direct addressing, the system may be deadlocked. As described before, if an access contention has occurred in an SCR write, $\overline{\text{READY}}$ of the opposite port is not asserted until SCR write is negated. Therefore, the MPU cannot accept $\overline{\text{READY}}$ and thus cannot negate $\overline{\text{WRS}}$. As a result, the system may be deadlocked.

Special attention must therefore be paid when designing a system performing word access involved in SCR write, as follows:

1. SCR write should be executed by indirect access to that normal write mode is selected.
2. The opposite port should not be accessed during SCR write.
3. SCR write should be executed on a byte basis.

One $\overline{\text{IRQ}}$ is enough to control the system; $\overline{\text{IRQ}}$ of the lower byte S-DPRAM can be disconnected.

Bit width expansion can be applied to the S-DPRAM in FIFO mode. In this case, $\overline{\text{FRQ}}$ signals must be connected by an OR gete, as for $\overline{\text{READY}}$.

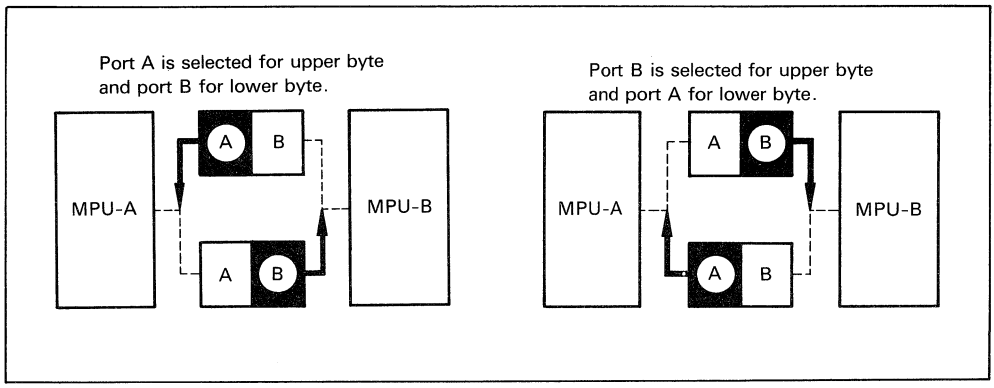


Figure 34. Port Ownership Confusion in Bit-Width-Expanded System

Notes for Use

Upgrading Power Supply Lines

Since the HD63310 is a high-speed CMOS LSI, a large peak current may flow at signal transitions. If the peak current is not adequately handled, a power supply drop or ground electric potential rise may occur. In general, to handle this peak current, a bypass capacitor should be connected to the device. The following lists some recommendations for this bypass capacitor.

1. A bypass capacitor which can handle high frequencies should be used, such as a titanium ceramic tantalum condenser.
2. The bypass capacitor must be located as near as possible to the power supply pins to ensure the smallest bus inductance.
3. Thick gauge wiring should be used to connect the power supply to the circuit board.

$\overline{\text{FRQ}}$ Signal Interface

The HD63310R negates the $\overline{\text{FRQ}}$ signal after completing the $\overline{\text{WRS}}$ cycle, and therefore $\overline{\text{FRQ}}$ acknowledge timing must be specified as after the point of $\overline{\text{WRS}}$ cycle completion.
In general, t_{FNLW} (the $\overline{\text{FRQ}}$ negation delay time at write access) is 150 ns. Taking the delay due to access contention into account, at least 400 ns of delay is required after $\overline{\text{WRS}}$ negation.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} (Note 2)	−0.3 to +7.0	V
Input Voltage	Vin (Note 2)	−0.3 to V_{CC} +0.3	V
Allowable Output Current	|Io| (Note 3)	5	mA
Total Allowable Output Current	|Σ Io| (Note 4)	60	mA
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +150	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect the reliability of the LSI.
2. With respect to V_{SS} (system GND)
3. The allowable output current is the maximum current that may be drawn from, or flow out to, one output terminal or one input/output common terminal.
4. The total allowable output current is the total sum of currents that may be drawn from, or flow out to, output terminals or input/output common terminals.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} (Note)	4.75	5.0	5.25	V
Input Voltage	V_{IH} (Note)	2.2	–	V_{CC}	V
	V_{IL} (Note)	0	–	0.8	V
Operating Temperature	Topr	0	25	70	°C

Note: With respect to V_{SS} (system GND)

Electrical Charcteristics

DC Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0°C to +70°C, unless otherwise noted)

Item		Sym.	Min	Max	Unit	Test Condition
Input High Voltage		V_{IH}	2.2	V_{CC}	V	
Input Low Voltage		V_{IL}	V_{SS} −0.3	0.8	V	
Input Leakage Current	$A_0(A)-A_5(A)$, $A_0(B)-A_5(B)$, RS(A), RS(B), $\overline{RDS}$(A), $\overline{RDS}$(B), $A_8(A)/\overline{AS}(A)$, $A_8(B)/\overline{AS}(B)$, $\overline{WRS}$(A), $\overline{WRS}$(B), $\overline{RESET}$	Iin	−2.5	2.5	μA	Vin = 0 to V_{CC}
Three-State (Off State) Leakage Current	$AD_0(A)-AD_7(A)$, $AD_0(B)-AD_7(B)$, $A_6(A)/A_8(A)\overline{FRQ_0}(A)$, $A_6(B)/A_8(B)/\overline{FRQ_0}(B)$, $A_7(A)/A_9(A)/\overline{FRQ_1}(A)$, $A_7(B)/A_9(B)/\overline{FRQ_1}(B)$	I_{TSI}	−10	10	μA	Vin = 0 to V_{CC}
Output Leakage Current	$\overline{IRQ}$(A), $\overline{IRQ}$(B)	I_{LOH}	−10	10	μA	V_{OH} = V_{CC}
Output High Voltage		V_{OH}	V_{CC} − 1.0	−	V	I_{OH} = −400 μA
			V_{CC} − 0.1	−	V	I_{OH} ≦ −10 μA
Output Low Voltage	$AD_0(A)-AD_7(A)$, $AD_0(B)-AD_7(B)$, $A_6(A)/A_8(A)/\overline{FRQ_0}(A)$, $A_6(B)/A_8(B)/\overline{FRQ_0}(B)$, $A_7(A)/A_9(A)/\overline{FRQ_1}(A)$, $A_7(B)/A_9(B)/\overline{FRQ_1}(B)$, $\overline{READY}$(A), $\overline{READY}$(B)	V_{OL}	−	0.5	V	I_{OL} = 2 mA
	$\overline{IRQ}$(A), $\overline{IRQ}$(B)		−	0.5	V	I_{OL} = 3.2 mA
Input Capacitance		Cin	−	20	pF	Vin = 0 V, Ta = 25°C, f = 1.0 MHz
Output Capacitance		Cout	−	20		
Current Dissipation	Operating Mode	I_{CC}	−	30	mA	V_{CC} = 5.25 V, V_{IH} = 2.2 V, V_{IL} = 0.8 V
	Standby Mode ($\overline{RDS}$, $\overline{WRS}$ = High)		−	1	mA	V_{CC} = 5.25 V, V_{IH} = V_{CC} − 0.2 V, V_{IL} = 0.2 V

Timing Measurement

The timing measurement point for the output level is defined at the following point throughout this specification:

V_{OL} = 0.8 V, V_{OH} = 2.0 V

The output level at stable condition (DC characteristics) is defined at following point:

V_{OL} (DC) = 0.5 V, V_{OH} (DC) = V_{CC} − 1.0 V

See figure 35.

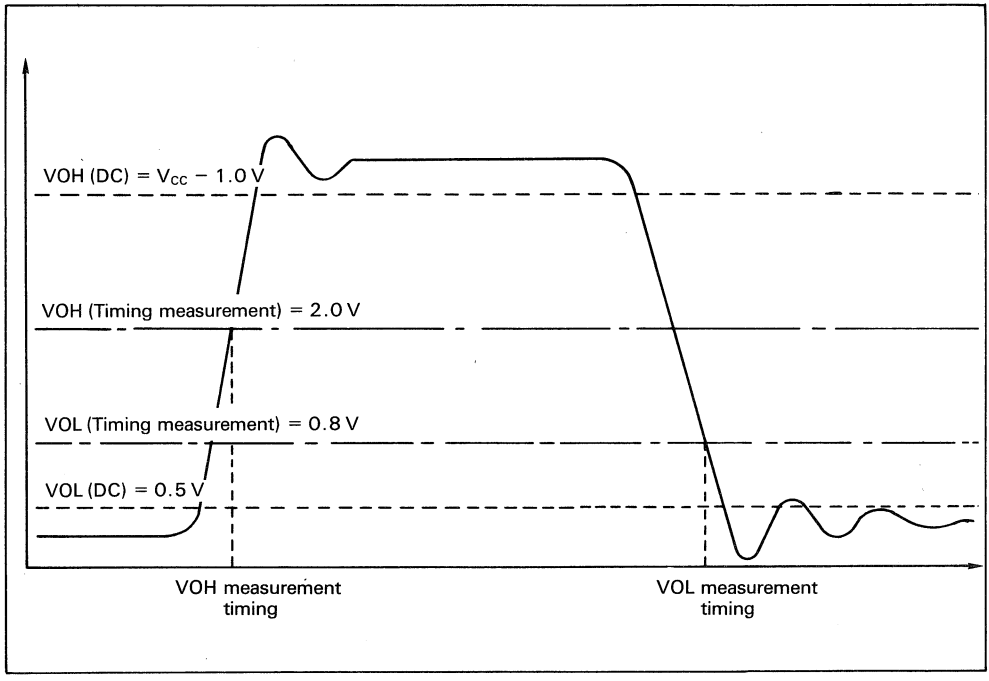


Figure 35. Test Measurement Points

AC Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0 °C to +70 °C, unless otherwise noted)

Bus Timing

No.	Item		Symbol	HD63310RP20 Min	HD63310RP20 Max	Unit	Figures
1	Address Setup Time (A_0–A_9)		t_{AS}	0		ns	Fig 36-39
2	Address Hold Time (A_0–A_9)		t_{AH}	0		ns	
3	Address Setup Time (RS)		t_{ASRS}	0		ns	
4	Address Hold Time (RS)		t_{AHRS}	15		ns	
5	Address Setup Time ($\overline{AS}$)		t_{ASAS}	40		ns	Fig 37,39
6	Address Hold Time ($\overline{AS}$)		t_{AHAS}	0		ns	
7	$\overline{AS}$ Low Level Width		t_{ASLW}	40		ns	
8	$\overline{AS}$ Setup time		t_{ASS}	0		ns	
9	$\overline{READY}$ Delay Time (Read)		t_{RYRD}		(note 1)	ns	Fig 36,37
10	$\overline{READY}$ Release Time (Read)		t_{RYRH}	0	60	ns	
11	Read Data Delay Time	Direct Addressing Access	t_{DDR}		120	ns	
		Indirect Addressing/ FIFO Access			170	ns	
11A	Read Data Access Time (Note 2)	Direct Addressing Access	t_{ACC}		200	ns	
		Indirect Addressing/ FIFO Access			250	ns	
12	Read Data Hold Time		t_{DHR}	10		ns	
13	Data Bus 3-State Off Time		t_{DTOF}		60	ns	
14	Data Bus 3-State On Time		t_{DTON}		60	ns	
15	$\overline{READY}$ Delay Time (Write)		t_{RYWD}		(note 1)	ns	Fig 38,39
16	$\overline{READY}$ Release Time (Write)		t_{RYWH}	0	60	ns	
17	Write Data Setup Time		t_{DSW}	60		ns	
18	Write Data Hold Time		t_{DHW}	0		ns	
19	$\overline{RDS}$ Hold Time	Direct Addressing Access	t_{RDSH}	120		ns	Fig 36,37
		Indirect Addressing/ FIFO Access		170		ns	
20	$\overline{WRS}$ Hold Time	Except FIFO Access	t_{WRSH}	120		ns	Fig 38,39
		FIFO Access		170		ns	
21	$\overline{RDS}$ Recovery Time		t_{RRC}	70		ns	Fig 36,37
22	$\overline{WRS}$ Recovery Time		t_{WRC}	70		ns	Fig 38,39
23	Recovery Time ($\overline{RDS}$ to $\overline{WRS}$)		t_{RWRC}	70		ns	Fig 44
24	Recovery Time ($\overline{WRS}$ to $\overline{RDS}$)		t_{WRRC}	70		ns	

$\overline{FRQ}$ Output Timing

No.		Item	Symbol	HD63310RP20 Min	HD63310RP20 Max	Unit	Figures
31	Level Mode	$\overline{FRQ}$ Assert Delay Time (Read)	t_{FALR}		300	ns	Fig 40
32		$\overline{FRQ}$ Negate Delay Time (Write)	t_{FNLW}		150	ns	
33		$\overline{FRQ}$ Assert Delay Time (Write)	t_{FALW}		150	ns	
34		$\overline{FRQ}$ Negate Delay Time (Read)	t_{FNLR}		300	ns	
35	Pulse Mode	$\overline{FRQ}$ Negate Delay Time (Write)	t_{FNPW}		250	ns	Fig 41
36		$\overline{FRQ}$ Assert Delay Time (Write)	t_{FAPW}		300	ns	
37		$\overline{FRQ}$ Pulse Width (Write) (Note 4)	t_{FPPW}	100		ns	
38		$\overline{FRQ}$ Negate Delay Time (Read)	t_{FNPR}		300	ns	
39		$\overline{FRQ}$ Assert Delay Time (Read)	t_{FAPR}		80	ns	
40		$\overline{FRQ}$ Pulse Width (Read) (Note 4)	t_{FPPR}	30		ns	
41	Register Write	$\overline{FRQ}$ assert Delay Time	t_{FARW}		150	ns	Fig 43
42		$\overline{FRQ}$ Negate Delay Time	t_{FNRW}		150	ns	

$\overline{IRQ}$, $\overline{RESET}$ Timing

No.	Item	Symbol	HD63310RP20 Min	HD63310RP20 Max	Unit	Figures
51	$\overline{IRQ}$ Response Time (Register Write)	t_{RS1}		300	ns	
52	$\overline{IRQ}$ Release Time	t_{IR}		600	ns	Fig. 47
53	$\overline{IRQ}$ Response Time (FIFO Access)	t_{RS2}		300	ns	
54	$\overline{RESET}$ Low Level Width	t_{RL}	200		ns	Fig. 48
55	$\overline{RDS}$ Wait Time from $\overline{RESET}$ Negate	t_{RESR}	70		ns	Fig. 45
56	$\overline{WRS}$ Wait Time from $\overline{RESET}$ Negate	t_{RESW}	70		ns	

$\overline{RDS}$, $\overline{WRS}$ Timing

No.	Item	Symbol	HD63310RP20 Min	HD63310RP20 Max	Unit	Figures
61	$\overline{RDS}$ Fall Time	t_{RF}		25	ns	Fig 46
62	$\overline{RDS}$ Rise Time	t_{RR}		25	ns	
63	$\overline{WRS}$ Fall Time	t_{WF}		25	ns	
64	$\overline{WRS}$ Rise Time	t_{WR}		25	ns	

Notes: 1. The $\overline{READY}$ signal is used to synchronize, and the delay time depends on the access condition of both ports. For example, when both ports request the data read simultaneously, one port goes to wait state and the $\overline{READY}$ signal delays. A detailed explanation is shown in "READY Timing".
2. Two port access with no contention timing.
3. No. 31-42 include no wait state.
4. No. 37 $\overline{FRQ}$ pulse width depends on No. 20 $\overline{WRS}$ hold time.
   No. 40 $\overline{FRQ}$ pulse width depends on No. 19 $\overline{RDS}$ hold time.
5. No. 51-No. 54 include no wait state.

$\overline{\text{READY}}$ Delay Timing, No Access Contention (DPRAM/FIFO Mode)

No.	Item		Min	Max	Unit	Figure
R1	Read		—	110	ns	Fig 47-50
R2	Write	Normal	—	110	ns	Fig 47-54
		SCR	—	125	ns	
		FIFO	—	125	ns	

$\overline{\text{READY}}$ Delay Timing, Access Contention (DPRAM Mode)

No.	Item	Contention	Preceding Access	Subsequent Access	Min	Max	Unit	Figure
R3	Read	Read-read	Normal read (Indirect)	Normal read (Dir/Ind)	—	355	ns	Fig 47
R4		Write-read	Normal write (Indirect)	Normal read (Dir/Ind)	—	355	ns	
R5		Write (SCR)-read	SCR write	Normal read (Dir/Ind)	—	250	ns	
R6	Write	Read-write (SCR)	Normal read (Indirect)	SCR write	—	370	ns	Fig 48
R7		Write-write (SCR)	Normal write (Indirect)	SCR write	—	370	ns	
R8		Write (SCR)-write (SCR)	SCR write	SCR write	—	250	ns	

$\overline{\text{READY}}$ Delay Time, Port Busy (DPRAM Mode)

No.	Item	Contention	Preceding Access	Subsequent Access	Min	Max	Unit	Figure
R9	Read	Write-read Port busy	Normal write (Indirect)	Normal read (Dir/Ind)	—	285	ns	Fig 51
R10	Write	Write-write Port busy	Normal write (Indirect)	SCR write	—	285	ns	Fig 52

Notes: 1. $\overline{\text{READY}}$ delay time does not depend on whether the access mode is direct or indirect at nonaccess contention.
2. The $\overline{\text{WRS}}$ arbitration point does not affect the $\overline{\text{READY}}$ delay time in normal mode since it appears at the negative edge, which is at the end of the cycle. Therefore, the $\overline{\text{READY}}$ delay time for normal write contention is the same as for no access contention.
3. For access invlolving SCR write, $\overline{\text{READY}}$ delay time depends on the negative edge of $\overline{\text{RDS}}$ or $\overline{\text{WRS}}$ of the connected port. Please keep this in mind when designing a system. For details, see "S-DPRAM Bit width Expansion" and "Processing Mode".

$\overline{\text{READY}}$ Delay Time, Access Contention (FIFO Mode)

No.	Item	Contention	Preceding Access	Subsequent Access	Min	Max	Unit	Figure
R11	Read	Read-read	FIFO read Normal read FIFO read	FIFO read FIFO read Normal read	—	355	ns	Fig 49
R12		Write-read	FIFO write Normal write FIFO write	FIFO read FIFO read Normal read	—	355	ns	
R13		Write (SCR)-read	SCR write	FIFO read	—	250	ns	
R14	Write	Read-write	FIFO read Normal read FIFO read FIFO read	FIFO write FIFO write Normal write SCR write	—	370	ns	Fig 50
R15		Write-write	FIFO write Normal write FIFO write FIFO write	FIFO write FIFO write Normal write SCR write	—	370	ns	
R16		Write (SCR)-write	SCR write	FIFO write	—	250	ns	

$\overline{\text{READY}}$ Delay Time, Port Busy (FIFO Mode)

No.	Item	Contention	Preceding Access	Subsequent Access	Min	Max	Unit	Figure
R17	Read	Write-read	FIFO write Normal write FIFO write	FIFO read FIFO read Normal read	—	285	ns	Fig 53
R19	Write	Write-write	FIFO write Normal write FIFO write FIFO write	FIFO write FIFO write Normal write SCR write	—	285	ns	Fig 54

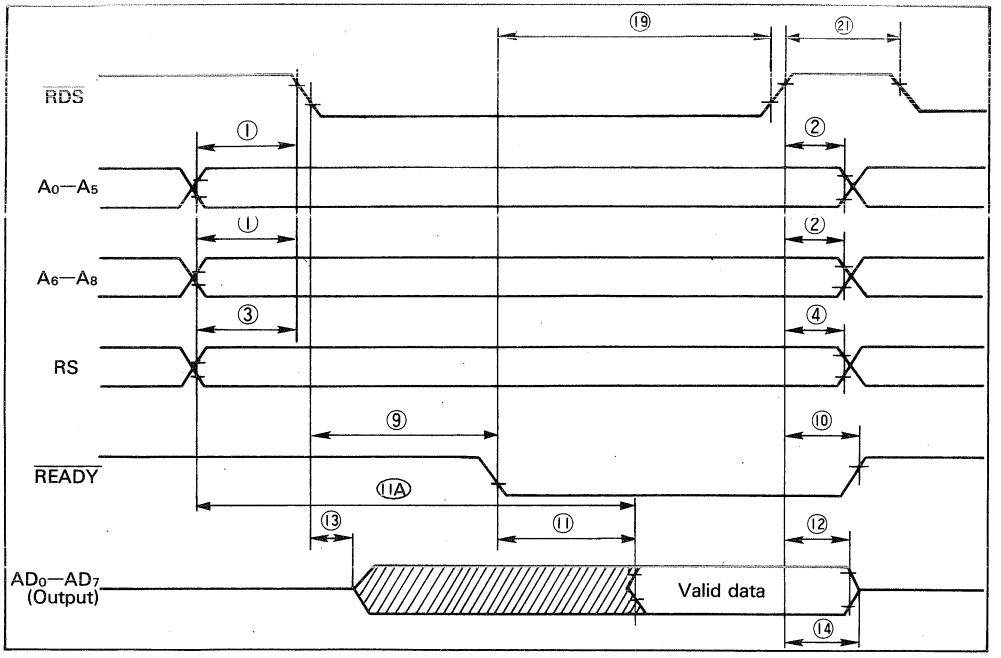


Figure 36. Non-Multiplexed Bus Read Timing

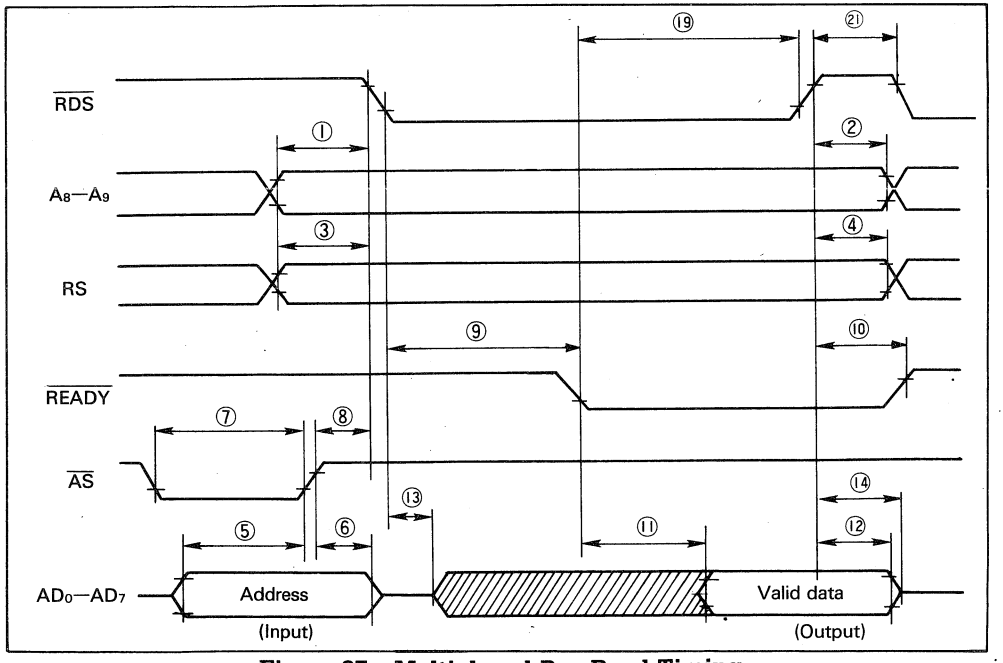


Figure 37. Multiplexed Bus Read Timing

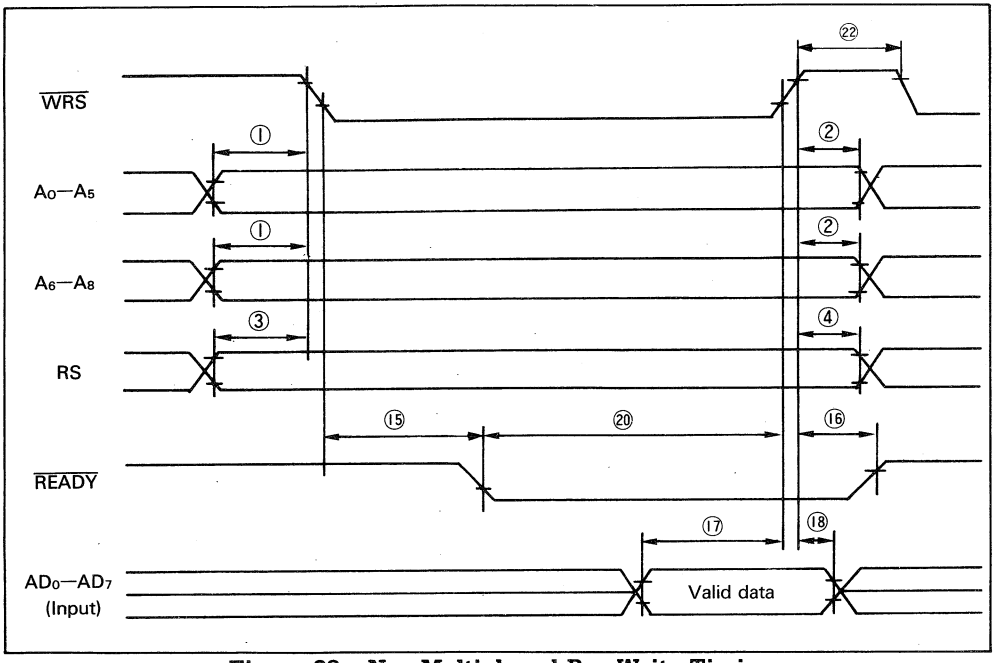


Figure 38. Non-Multiplexed Bus Write Timing

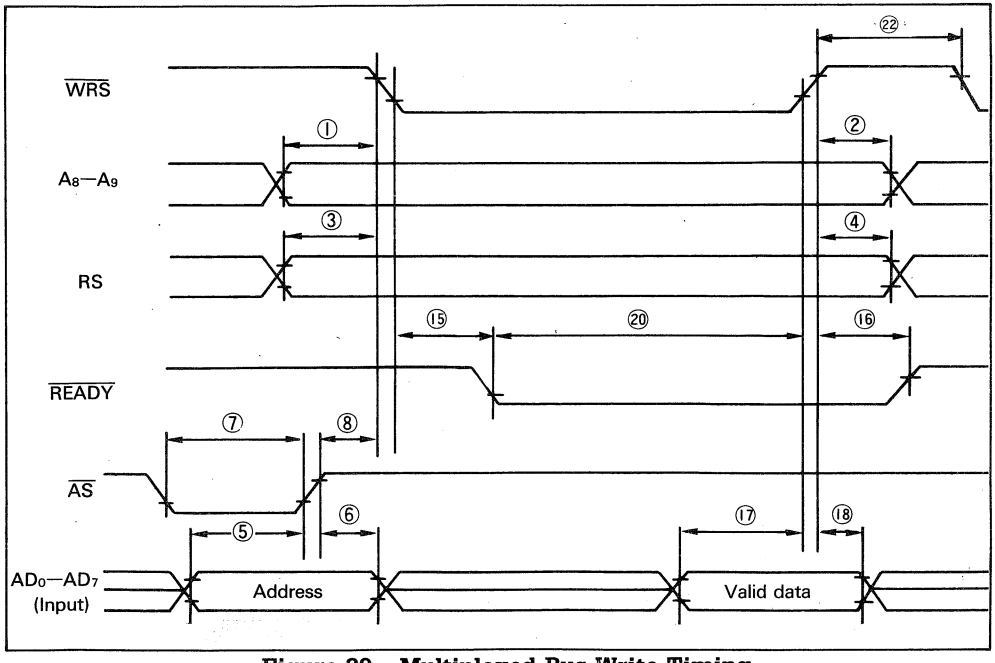


Figure 39. Multiplexed Bus Write Timing

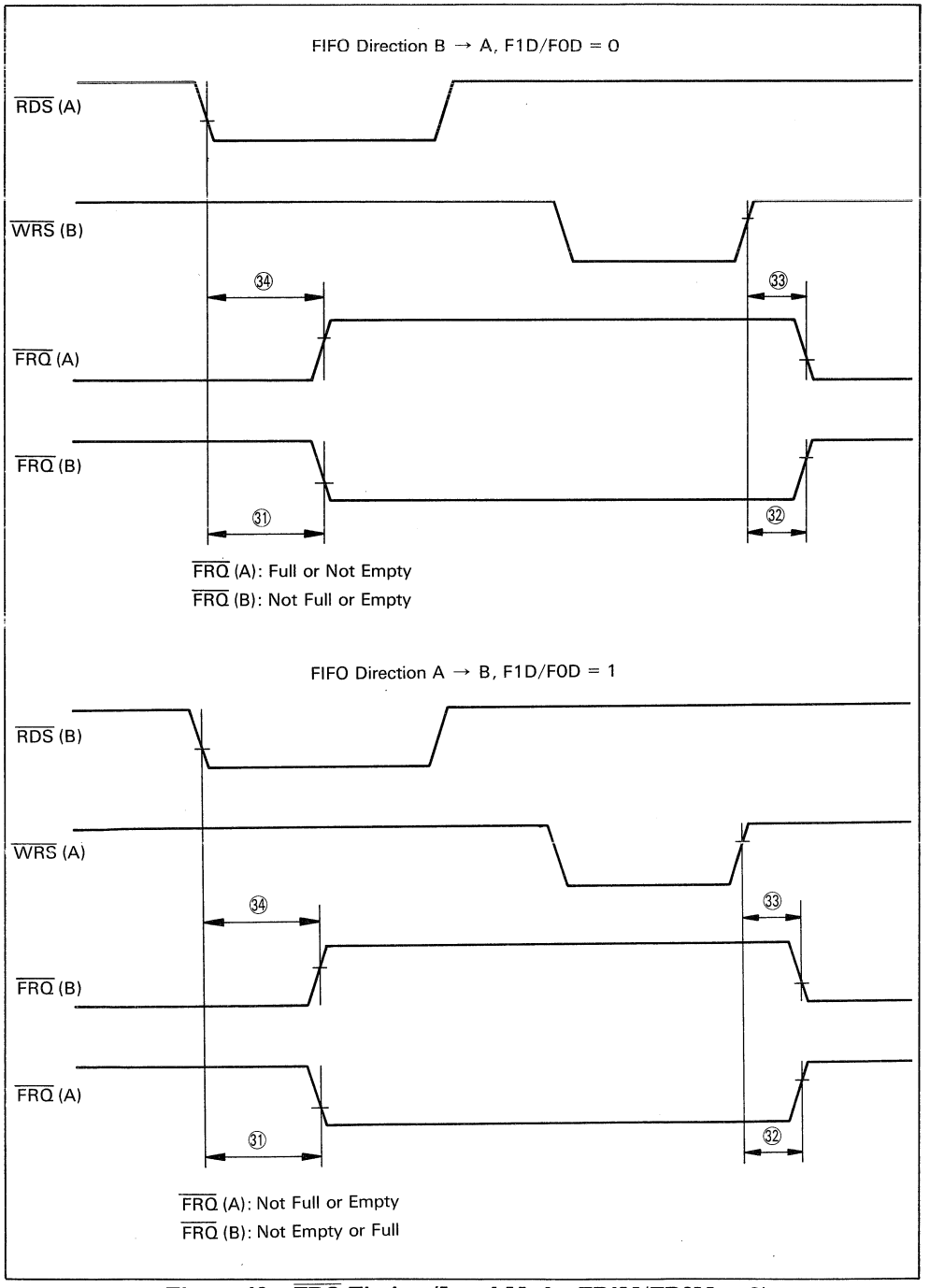


Figure 40. $\overline{FRQ}$ Timing (Level Mode, FR1M/FR0M = 0)

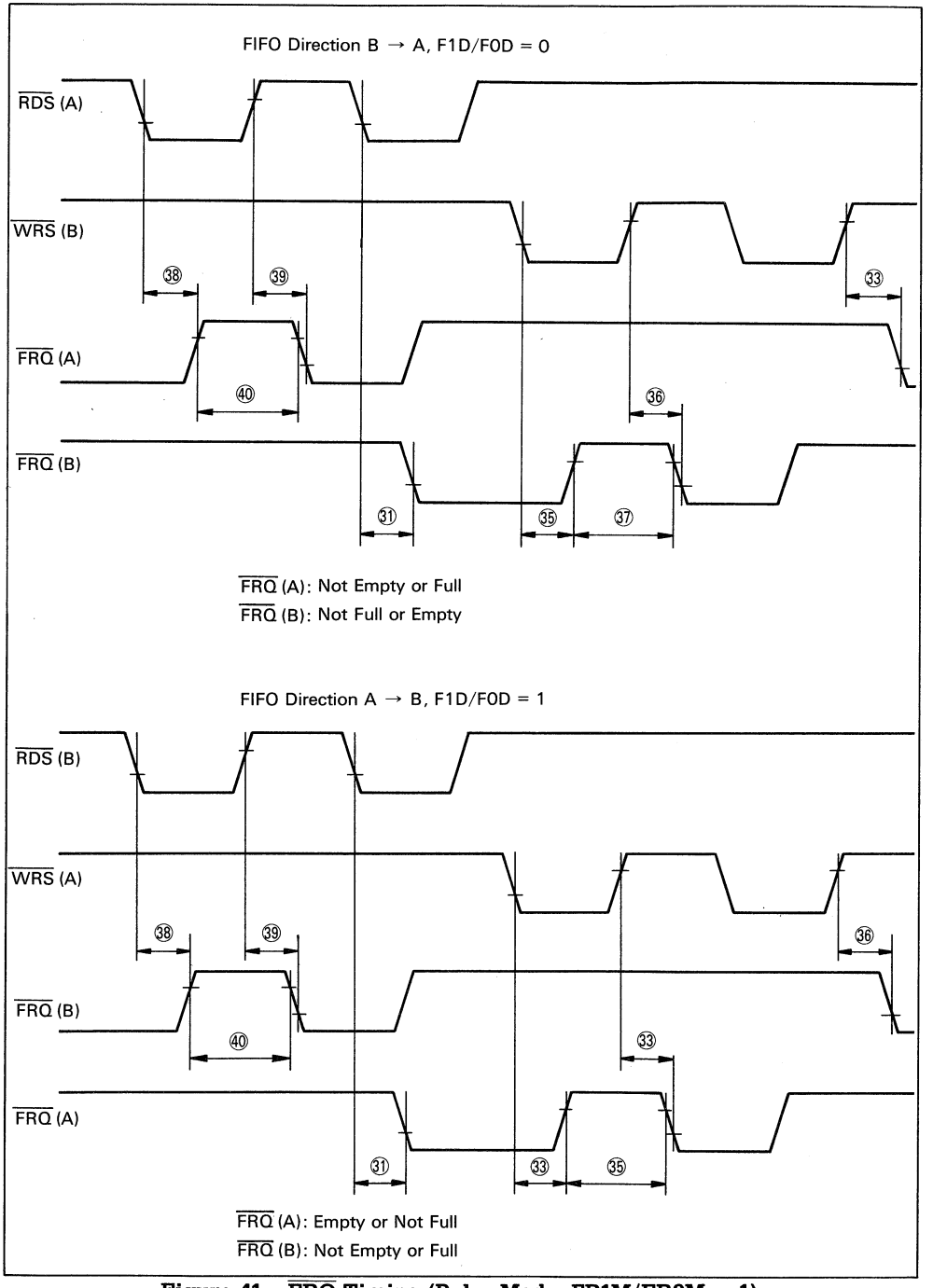


Figure 41. $\overline{\text{FRQ}}$ Timing (Pulse Mode, FR1M/FR0M = 1)

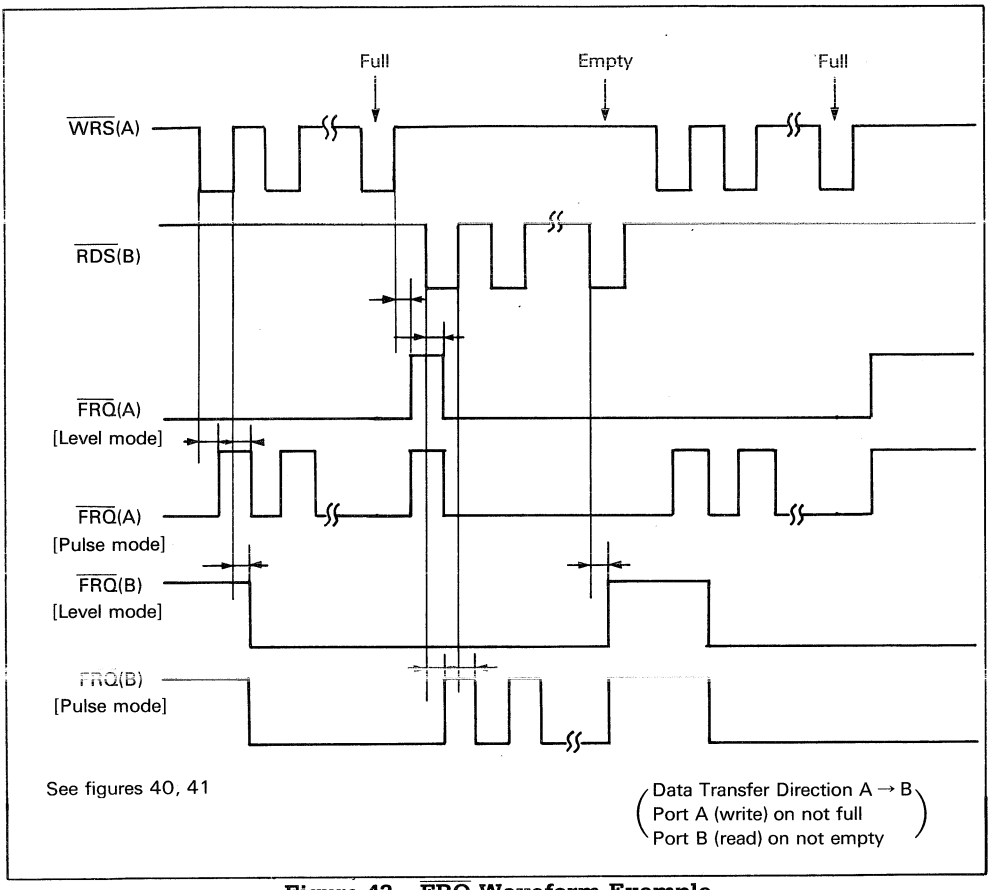


Figure 42. $\overline{\text{FRQ}}$ Waveform Example

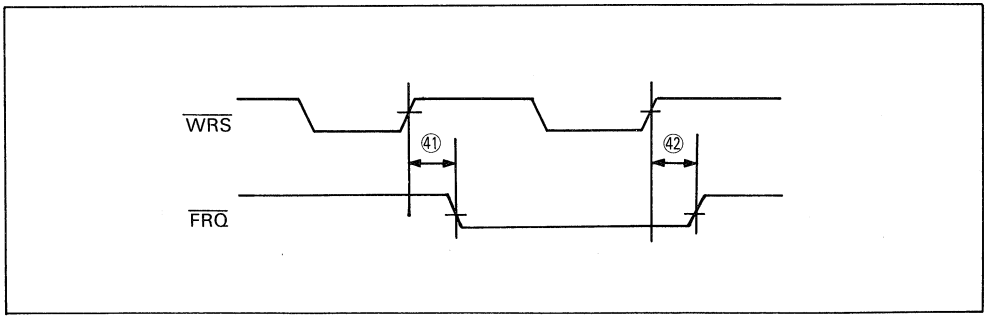


Figure 43. $\overline{\text{FRQ}}$ Timing (FRC Register Write)

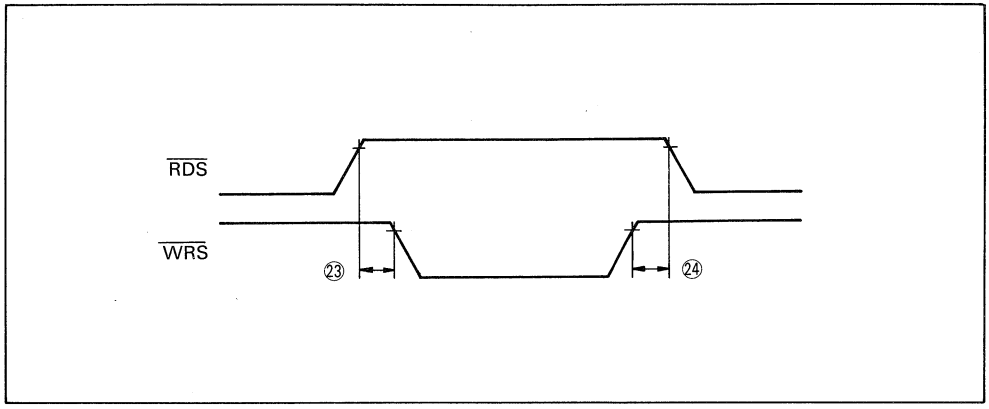


Figure 44. Recovery Time between $\overline{RDS}$ and $\overline{WRS}$ (Same Port)

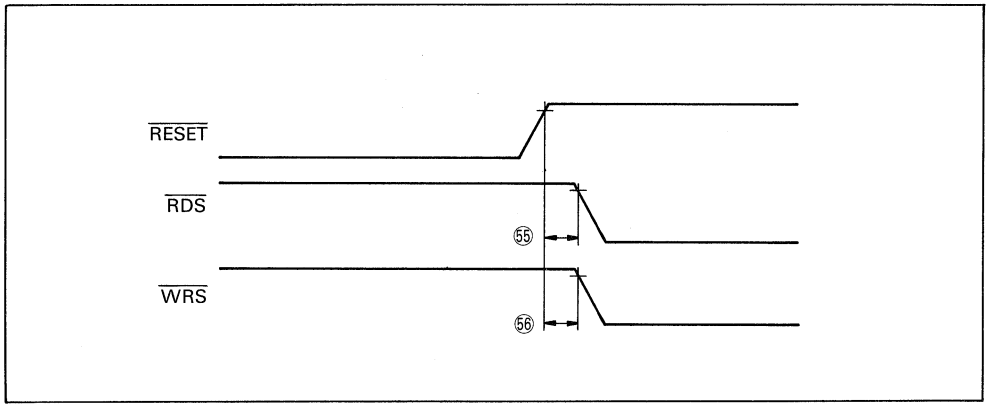


Figure 45. $\overline{RDS}$, $\overline{WRS}$ Wait Time from $\overline{RESET}$ Negate

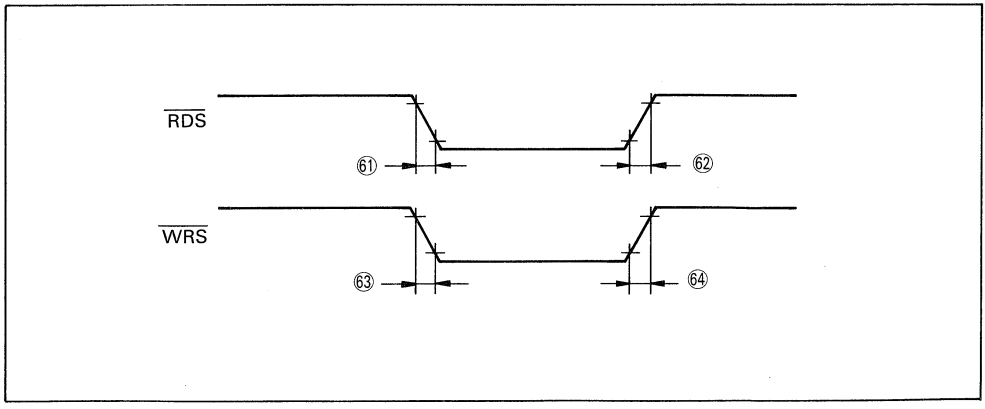
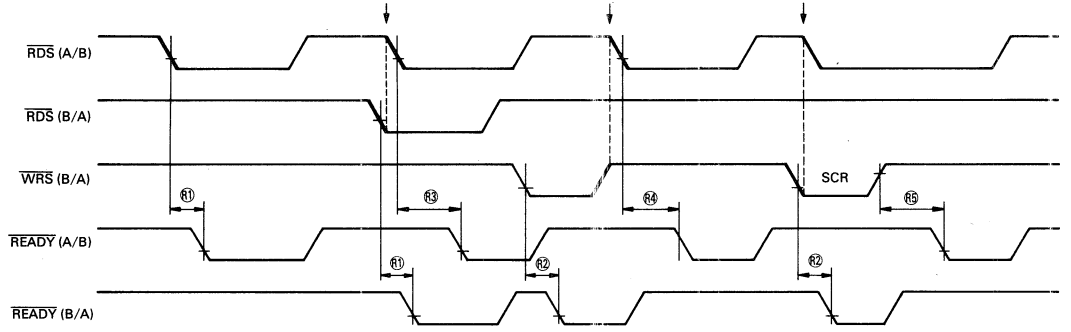
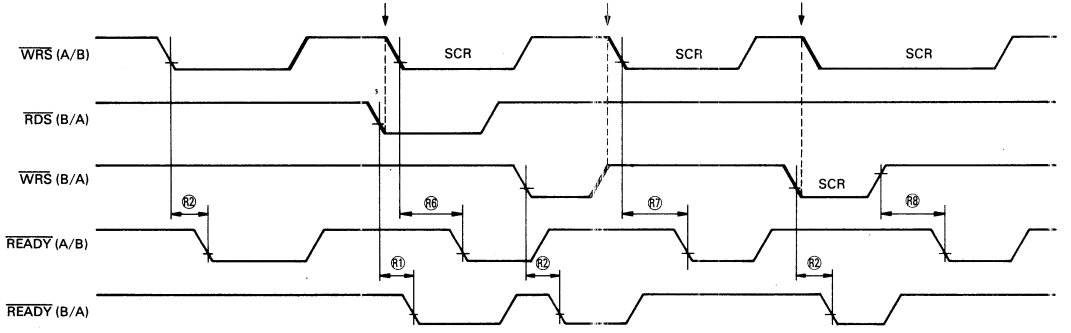


Figure 46. $\overline{RDS}$, $\overline{WRS}$ Timing



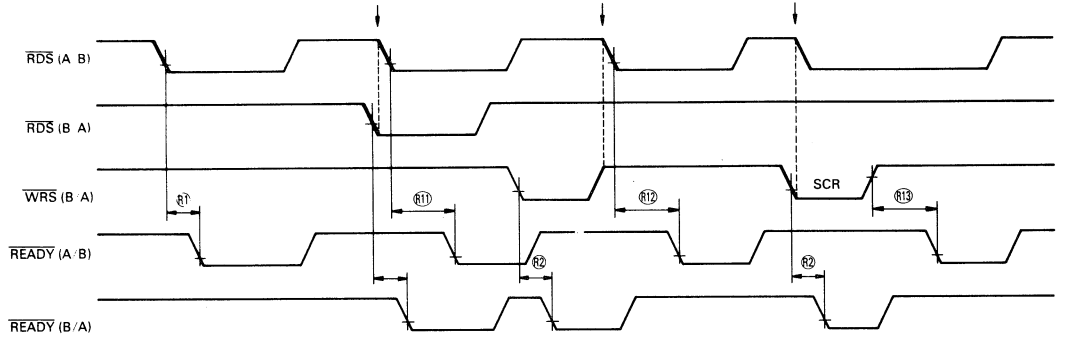
Note: Bold lines indicate arbitration. When a signal's arbitration point is before the broken line, the operation indicated by the signal precedes the operation indicated by the broken line.

Figure 47. $\overline{\text{READY}}$ Delay Timing, Read Contention (DPRAM Mode)



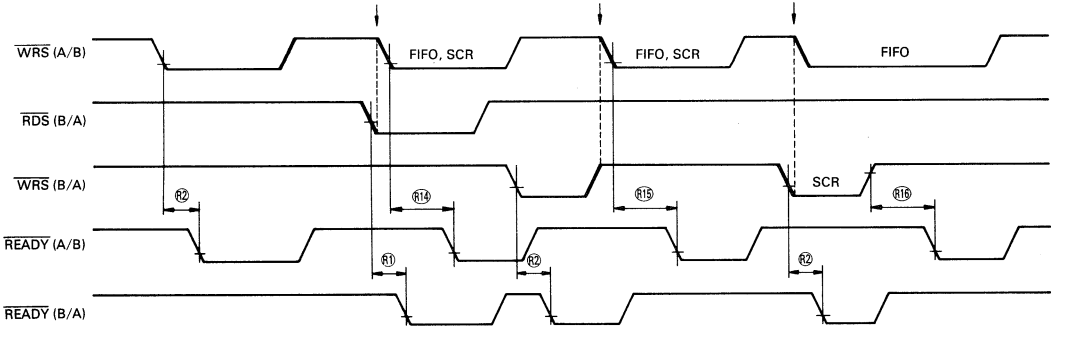
Note: Bold lines indicate arbitration. When a signal's arbitration point is before the broken line, the operation indicated by the signal precedes the operation indicated by the broken line.

Figure 48. $\overline{\text{READY}}$ Delay Timing, Write Contention (DPRAM Mode)



Note: Bold lines indicate arbitration. When a signal's arbitration point is before the broken line, the operation indicated by the signal precedes the operation indicated by the broken line.

Figure 49. $\overline{\text{READY}}$ Delay Timing, Read Contention (FIFO Mode)



Note: Bold lines indicate arbitration. When a signal's arbitration point is before the broken line, the operation indicated by the signal precedes the operation indicated by the broken line.

Figure 50. $\overline{\text{READY}}$ Delay Timing, Write Contention (FIFO Mode)

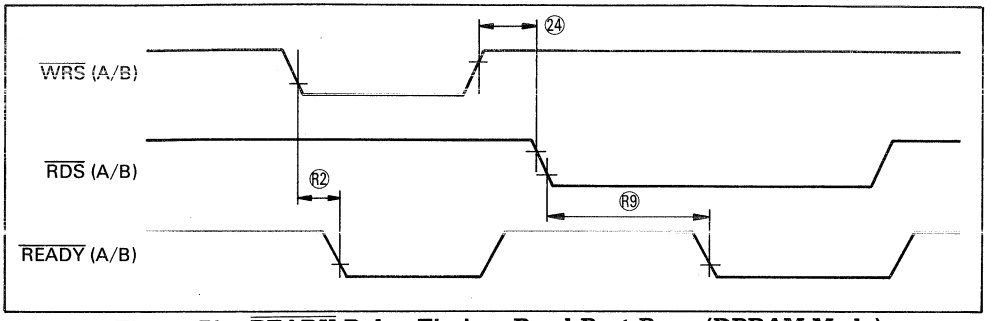


Figure 51. $\overline{\text{READY}}$ Delay Timing, Read Port Busy (DPRAM Mode)

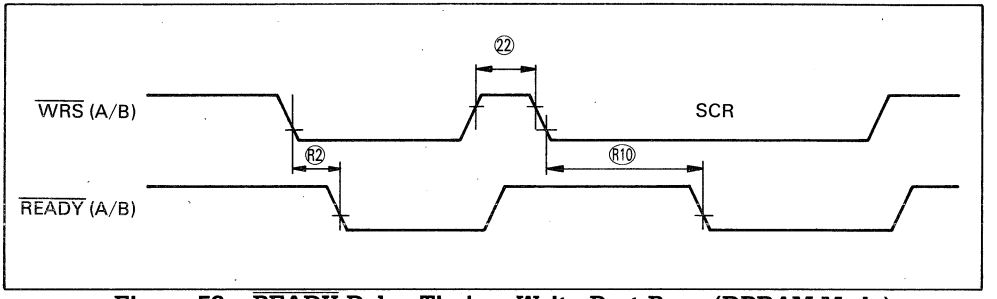


Figure 52. $\overline{\text{READY}}$ Delay Timing, Write Port Busy (DPRAM Mode)

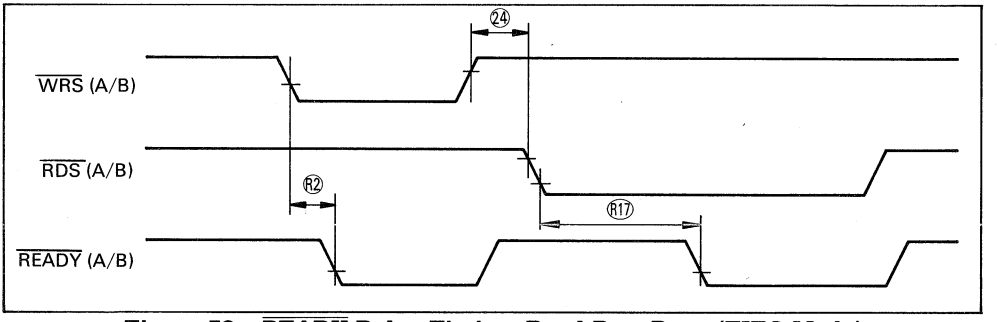


Figure 53. $\overline{\text{READY}}$ Delay Timing, Read Port Busy (FIFO Mode)

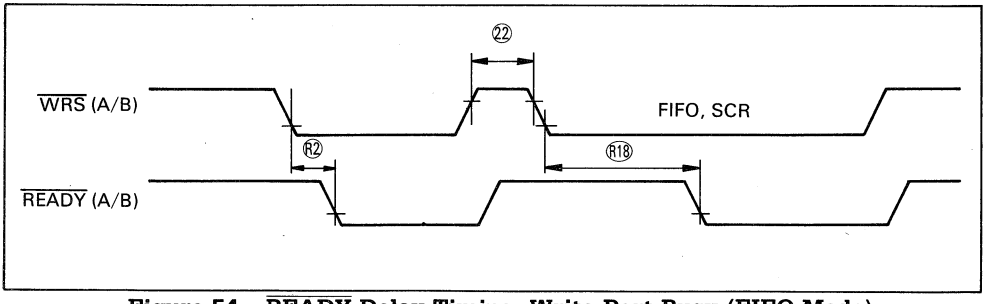


Figure 54. $\overline{\text{READY}}$ Delay Timing, Write Port Busy (FIFO Mode)

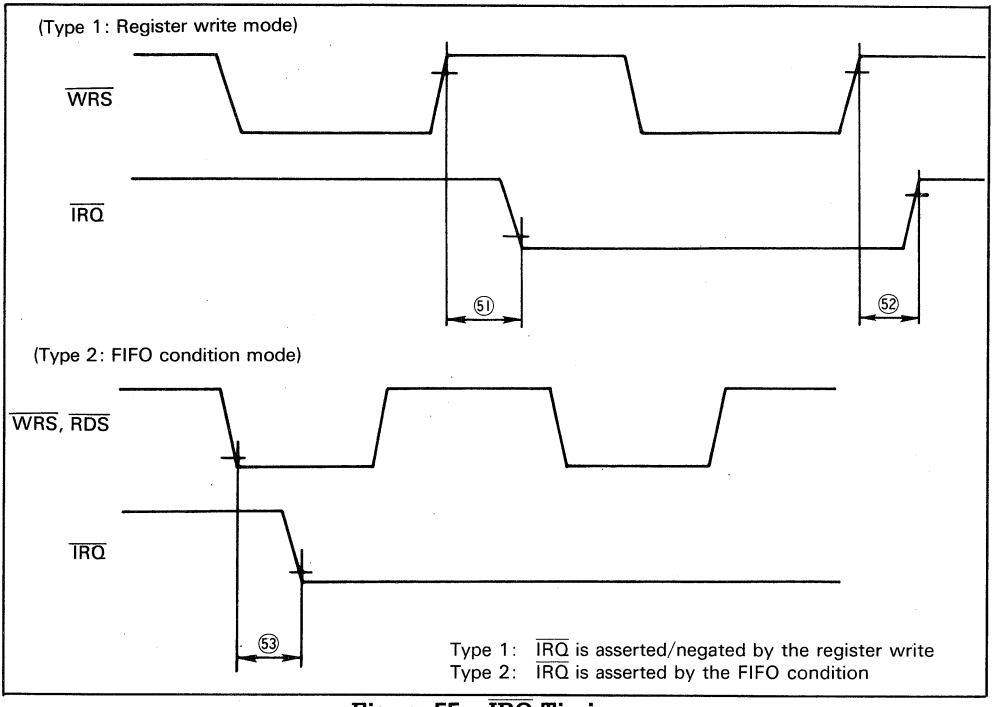


Figure 55. IRQ Timing

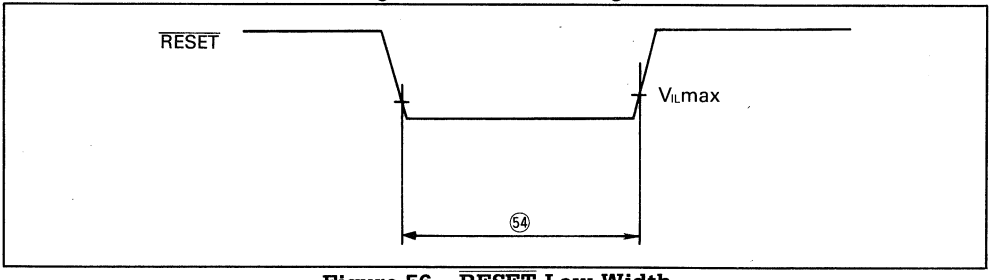


Figure 56. RESET Low Width

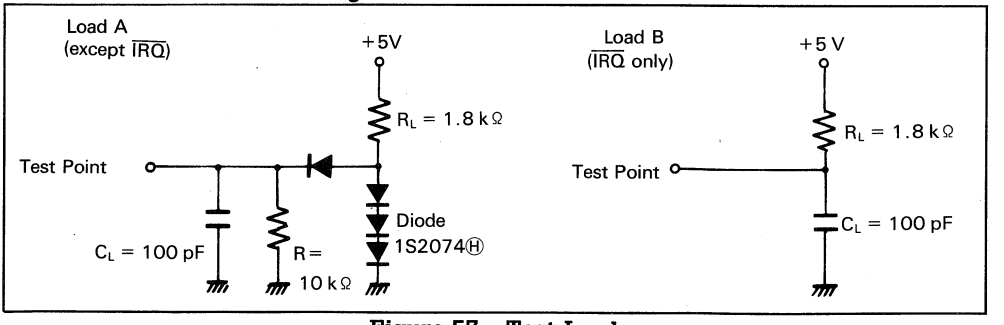


Figure 57. Test Load

Refer to application note (No. 68−3−18) for detail of this product.

Digital Signal Processor

HD61810 (DSP)

The HD61810 is a single-chip general-purpose digital signal processors. High-speed floating-point ALU and MULT are provided internally to perform addition/subtraction and multiplication simultaneously in only one cycle, 250 ns (4 MFLOPS).
Moreover, the lower power consumption is realized by employing a high-density CMOS process. It can support a wide range of applications; telecommunication, speech processing, image processing and control which need a high-speed product-sum operation.

Key Features

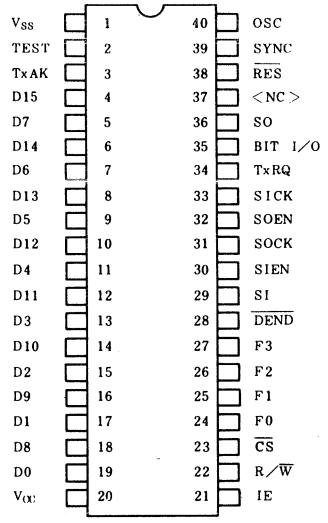
Hardware

- Fixed-point arithmetic (16 bits)
- Floating-point arithmetic (mantissa: 16 bits, exponent: 4 bits)
- Includes high-speed floating-point ALU (250 ns) and multiplier (250 ns)
- High throughput by pipeline control and horizontal microinstructions
- 32-bit dynamic range of floating-point arithmetic
- Internal large capacity memories
  Instruction ROM : 512 x 22 bits
  Data RAM : 200 x 16 bits
  (2-port accessible)
  Data ROM : 128 x 16 bits
- Parallel I/O compatible with 8/16 bit microcomputer interface
- 16-bit serial input/output
- Parallel I/O allows the forcible change of contents of the internal registers (program counter and control register).
- DMA operation between the HD61810 and the external memory
- Interrupt by parallel I/O, serial input and serial output
- Up to 2 levels of nesting of subroutine and interrupt
- A single power supply of +5V
- Low power disippation 250 mW typ

Software

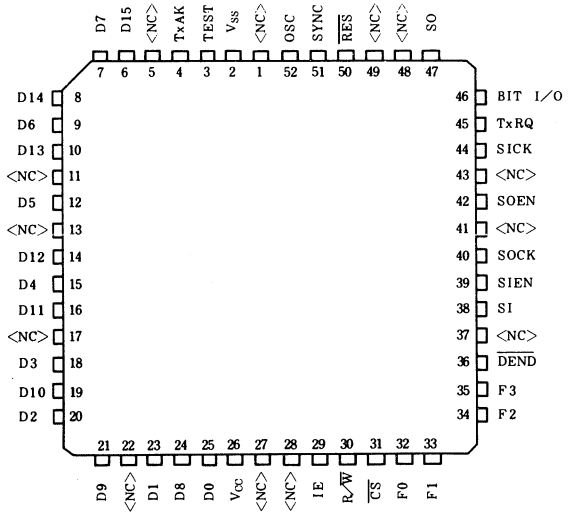
- Fixed-point/floating-point arithmetic instruction set
- All instructions are executed in only one cycle.
- Floating-point arithmetic needs no scaling function during the operation and realizes a high-precision arithmetic.
  (Representable value of ACC: 0, $\pm 2^{-23}$ to $\pm 2^{7}$)
- One instruction executes addition/subtraction, multiplication, memory read (2-port), memory write, RAM/ROM pointer increment and repeat counter decrement in parallel.
- Two kinds of addressing mode (direct-and-pointer-addressing mode)
- Repeat instruction allows an efficient programming of repetitive product-sum operation.

■ Pin Arrangement



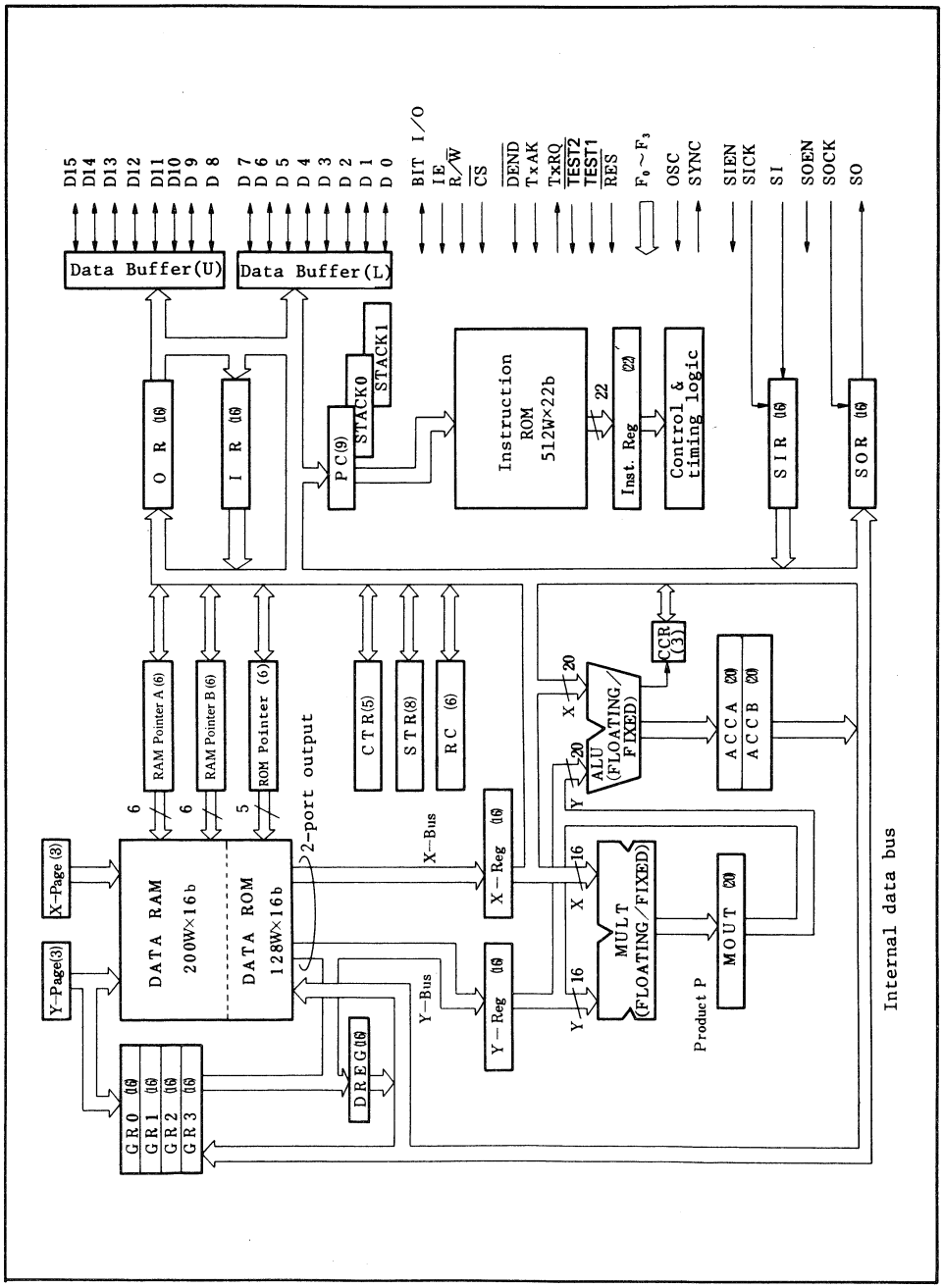
(Top View)

(NOTE) Any line should not be connected to <NC> pins.
DIC/DIP PACKAGE PIN ASSIGNMENT



(Top View)

(NOTE) Any line should not be connected to <NC> pins.
PLCC PACKAGE PIN ASSIGNMENT



HD61810 Block Diagram

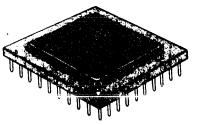
Refer to user's manual (No. AD-E0091) for detail of this product.

HD61811 (DSP-RAM)

The DSP RAM (HD61811) is a high performance digital signal processor using RAM in place of ROM in the DSP (HD61810), which permits desired programs to be load by external control. In addition, as the DSP-RAM provides the same instruction set and functions as the DSP, it can be used for the DSP evaluation and low volume production.

For detail of the basic operation of the DSP-RAM, see the DSP user's manual. This data sheet concentrates on the differences from the DSP.

HD61811Y



(PC-68)

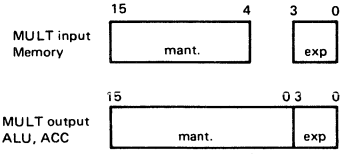
■ KEY FEATURES

- High-speed arithmetic operations (instruction cycle: 250 ns)
  Floating point arithmetic (realizes 32-bit dynamic range)
  Pipeline control
  Horizontal micro instructions Same instruction set as DSP (HD61810)
- Large capacity memories
  512 x 22-bit instruction RAM
  200 x 16-bit data RAM [1] (2-port accessible)
  128 x 16-bit data RAM [2]
- System bus compatible with 6800 family microcomputer through 8/16-bit parallel I/O ports
- Serial I/O interface for up to 16 bits
- Interrupt by three factors (end of three kinds of data I/O transfer: papallel I/O, serial input and serial output)
- Two nesting levels of subroutine and interrupt
- The store program is alterable.

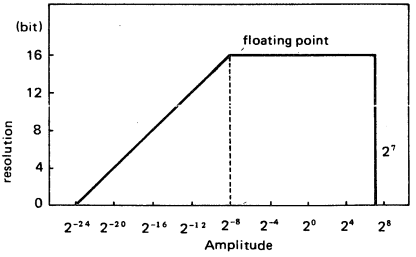
■ ARCHITECTURE

● Floating Point Arithmetic

The HD61811 can perform some kinds of floating point arithmetics (multiplication, addition and subtraction) in parallel in single instruction cycle (250 ns). Floating point arithmetic allows 32-bit dynamic range in spite of the 16-bit resolution.



Data format (floating point)



■ DIFFERENCES BETWEEN THE DSP AND THE DSP-RAM

In the DSP-RAM (HD61811), RAM is used in place of ROM in the DSP (HD61810). The following table describes differences between the DSP and the DSP-RAM.

Table 1 The DSP and the DSP-RAM

	HSP (HD61810)	DSP-RAM (HD61811)
Instruction memory	Instruction ROM (512W x 22b)	Instruction RAM (512W x 22b)
Data memories	Data RAM (200W x 16b)	Data RAM [1] (200W x 16b)
	Data ROM (128W x 16b)	Data RAM [2] (128W x 16b)
Parallel I/O functions	Provides one mode only. (Normal mode)	Provides two modes. (Normal mode and test mode)
Control register	Consists of five bits. (W/B, BIT I/O, TxRQ, OVFP, DMA)	Adds AT bit (bit 6) to conventional bits.

■ INSTRUCTION RAM

The instruction RAM is organized as 512 words by 22-bit, which is the same capacity as the instruction ROM of the DSP. Locations $1E7 through S1FE can be used for user's program, though unusable in the DSP. Location $1FE (the last address) is a vector address for interrupt, so the user must store the jump instruction here for a jump to an interrupt service routine.

The contents of the instruction RAM are undefined at power-on. First of all, an auxiliary program must be written to the instruction RAM through external data bus ($D_0 \sim D_{15}$). This program execution permits working the DSP-RAM. For details, see 'HD61811 APPLICATION CIRCUIT'.

A 22-bit word data in this RAM is divided into two for transfer; the upper bits (U, 11 bits) and the lower bits (L, 11 bits).

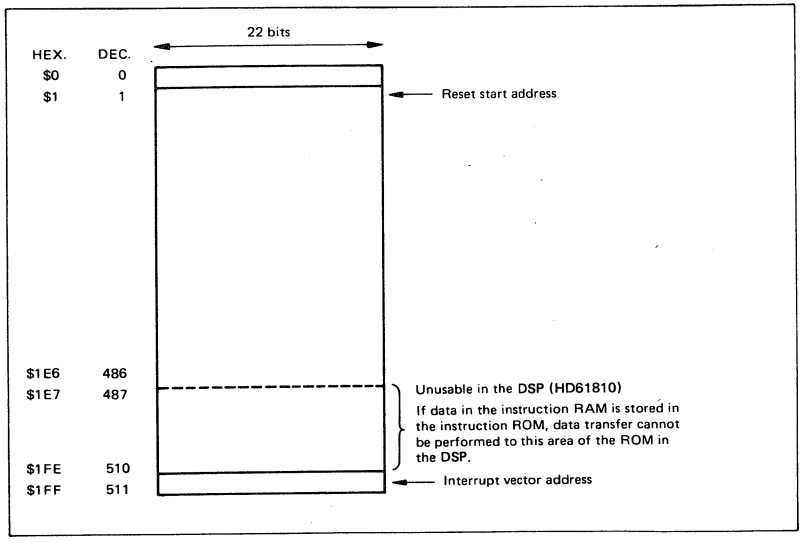


Fig. 1 Instruction RAM

■ DATA RAM

The DSP-RAM (HD61811) provides two data RAMs.

• Data RAM [1]

Data RAM [1] is organized as 200 words by 16 bits, corresponding to the data RAM in the DSP (HD61810).

• Data RAM [2]

Data RAM [2] is organized as 128 words by 16 bits, corresponding to the data ROM in the DSP.

A write to data RAM must be performed by software.

There are two modes of data memory addressing: pointer addressing and direct addressing. In pointer addressing mode, the RAM pointer A/B are used for the addressing of the data RAM [1] and the ROM pointer for the data RAM [2]. The address pointer for generating data 'RAM' [2] address is called the 'ROM' pointer in order to standardize the technical term between the HD61810 and the HD61811.

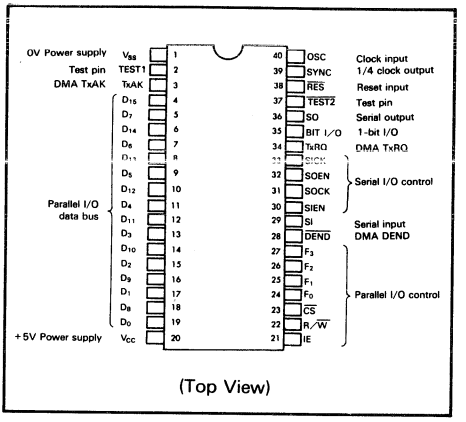
Refer to user's manual (No. AD-E0091) for detail of this product.

HD81810(DSP-W)

The HD81810, HD81A810 is member of the DSP family of single-chip general-purpose digital signal processors which can be used in the wide-range ambient temperature. High-speed floating-point ALU and MULT are provided internally to perform addition/subtraction and multiplication simultaneously in only one cycle,

HD81810 : 250 ns / instruction
HD81A810 : 200 ns / instruction

Its instruction set and the hardware are completely compatible with the HD61810 (DSP). Moreover, the lower power consumption is realized by employing a high-density CMOS process. It can support a wide range of applications; telecommunication, speech processing, image processing and control which need a high-speed product-sum operation.



Key Features

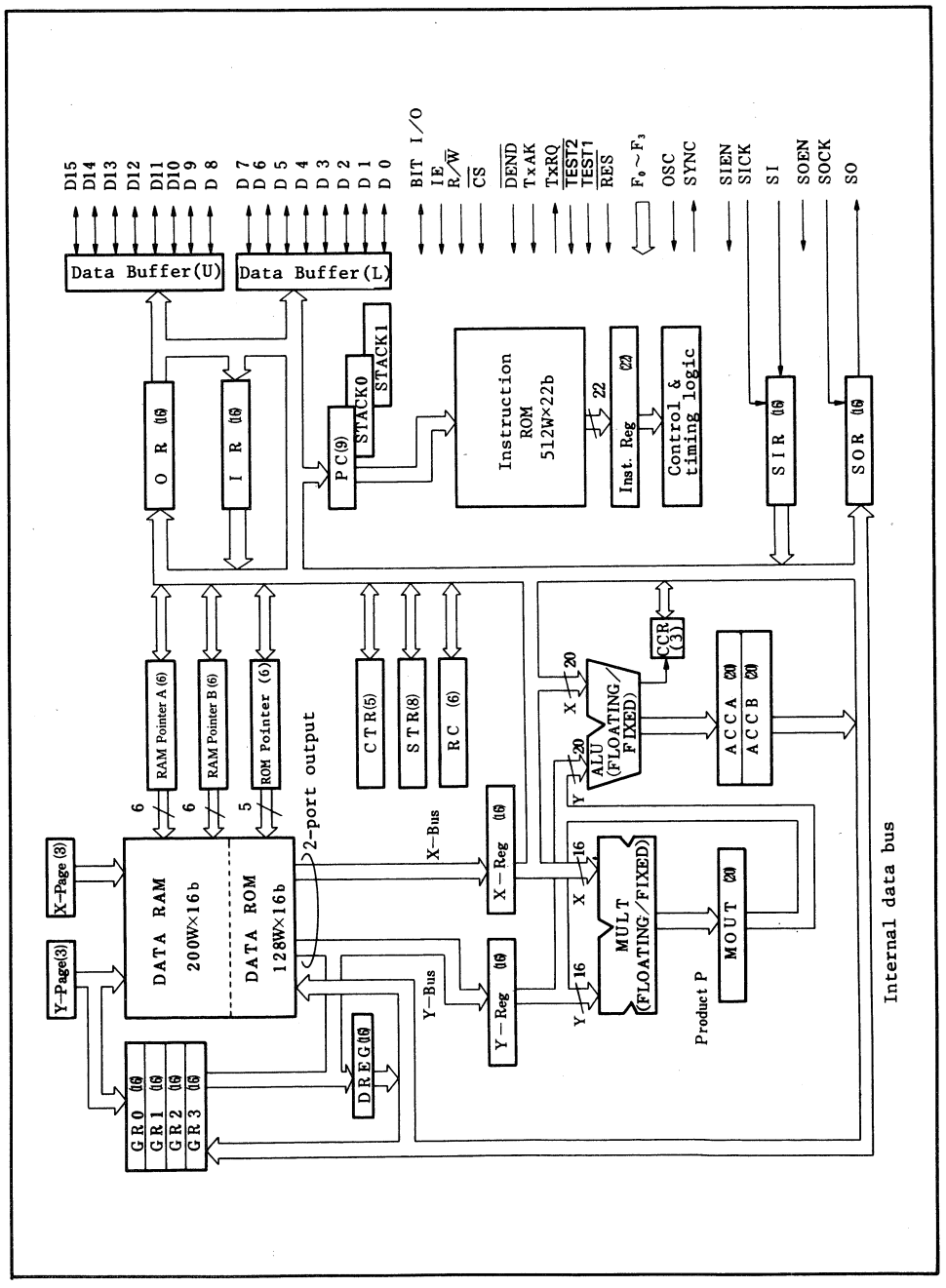
Hardware

- Fixed-point arithmetic (16 bits)
- Floating-point arithmetic (mantissa: 16 bits, exponent: 4 bits)
- Includes high-speed floating-point ALU and multiplier
- High throughput by pipeline control and horizontal microinstructions
- 32-bit dynamic range of floating-point arithmetic
- Internal large capacity memories
  - Instruction ROM : 512 x 22 bits
  - Data RAM : 200 x 16 bits (2-port accessible)
  - Data ROM : 128 x 16 bits
- Parallel I/O compatible with 8/16 bit microcomputer interface
- 16-bit serial input/output
- Parallel I/O allows the forcible change of contents of the internal registers (program counter and control register).
- DMA operation between the HD81810, HD81A810 and the external memory
- Interrupt by parallel I/O, serial input and serial output
- Up to 2 levels of nesting of subroutine and interrupt
- A single power supply of +5V
- Low power dissipation 150 mW typ
- Operating temperature –40 – +85°C

Software

- Fixed-point/floating-point arithmetic instruction set
- All instructions are executed in only one cycle.
- Floating-point arithmetic needs no scaling function during the operation and realizes a high-precision arithmetic.
  (Representable value of ACC: 0, $\pm 2^{-23}$ to $\pm 2^{7}$)
- One instruction executes addition/subtraction, multiplication, memory read (2-port), memory write, RAM/ROM pointer increment and repeat counter decrement in parallel.
- Two kinds of addressing mode (direct-and-pointer-addressing mode)
- Repeat instruction allows an efficient programming of repetitive product-sum operation.

* For the processor of higher speed (20 ns), refer to the HITACHI sales office.



HD81810, HD81A810 Block Diagram

Preliminary

HD81820 (DSP-E)
HD817820 (DSP-E ZTAT)

Floating-Point Digital Signal Processor

The HD81820/HD817820 is a high-speed digital signal processor which can perform addition/subtraction and multiplication simultaneously in only one cycle of 100 ns (10 MFLOPS), using a built-in floating-point ALU and floating-point multiplier. In addition, this processor enables a high degree of parallel processing, facilitating the preparation of highly-efficient programs.

The HD817820 provides instruction object codes compatible with the HD81820 Hitachi floating-point digital signal processor.

The instruction ROM and data ROM of the HD81820 are MASK ROMs.

The instruction ROM and data ROM of the HD817820 are PROMs, which can be written/verified by the same specifications as the HM27256 using a PROM writer.

Moreover, since the new CMOS process adopted by the HD81820/HD817820 enables high-speed operation and low-power dissipation, this processor can support a wide range of applications such as telecommunications, speech processing, image processing and control functions, i.e., applications which require high-speed product summation and filter processing.

Key Features

Hardware

- Fixed-point arithmetic operation (16 bits) and floating-point arithmetic operations (mantissa: 16 bits, exponent: 4 bits)
- Internal high-speed floating-point ALU (100 ns) and multiplier (100 ns) (16-bit + 4-bit)
- High throughput enabled by pipeline control and horizontal microinstructions
- 32-bit dynamic range for floating-point arithmetic operation
- Internal large-capacity memories:
  Instruction ROM: 2 kwords (2024) x 22 bits
  Data RAM: 512 words x 20 bits
  Data ROM: 512 words x 20 bits
- Parallel I/O compatible with 8/16-bit microcomputer interface
- 16-bit serial input/output
- Forcible change of internal register contents (PC, CTR) by parallel I/O
- Interrupt by parallel I/O, serial input and serial output
- Up to 4 levels of nesting for subroutines and interrupts
- A single power supply of +5 V
- Low-power dissipation of 150 mW typ.

Software

- Fixed-point/Floating-point instruction set
- Instructions executed in only one cycle
- High-precision floating-point arithmetic operations requiring no scaling function
- Addition/subtraction, multiplication, memory read (2-port), memory write, pointer increment, repeat counter decrement, each by one instruction
- Three kinds of addressing modes
- Repeat instruction which enables efficient programming of repetitive product summation operations.

Benchmark Values (Floating-Point Operations)

Arithmetic operations

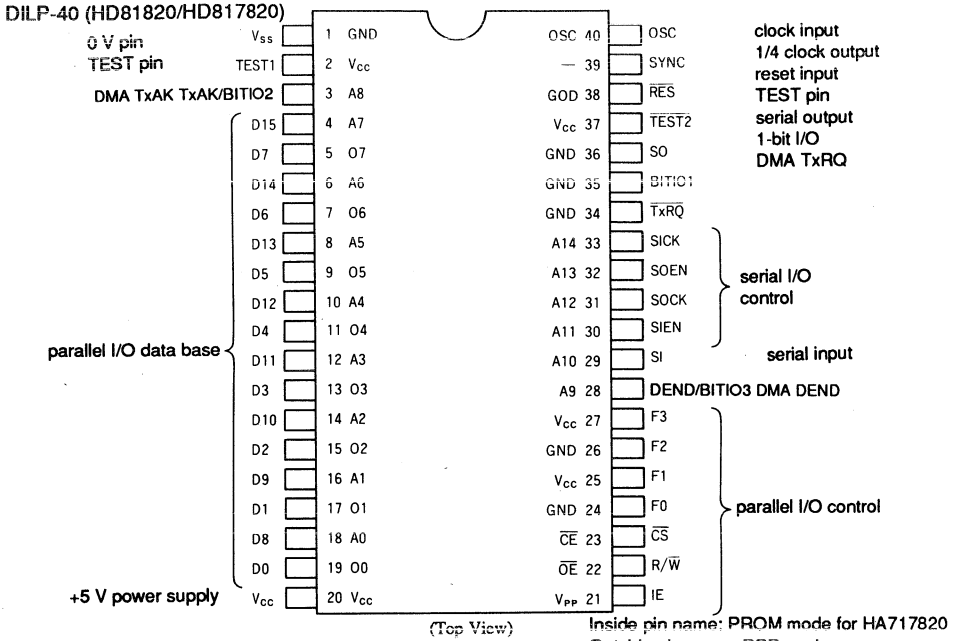
Operation	Execution time	Notes
Addition/Subtraction	100 ns	Addition/Subtraction can be performed in parallel with multiplication.
Multiplication	100 ns	
Inverse	2.3 µs	
Division	3.5 µs	Division can be performed in 2.5 µs if an inverse number is used.
Square root	5.9 µs	
SIN(X), COS(X)	2.6 µs	Both SIN(X) and COS(X) can be obtained simultaneously
ATAN(X)	9.4 µs	

Signal processing

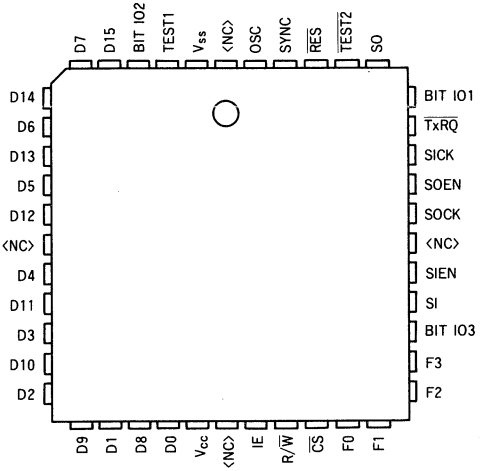
Operation	Execution time	Notes
Transversal filter	0.1 µs/TAP	
Biquad filter	0.6 µs/element	
64-point conplex FFT	0.36 ms	Loop processing

Pin Arrangement

DILP-40 (HD81820/HD817820)



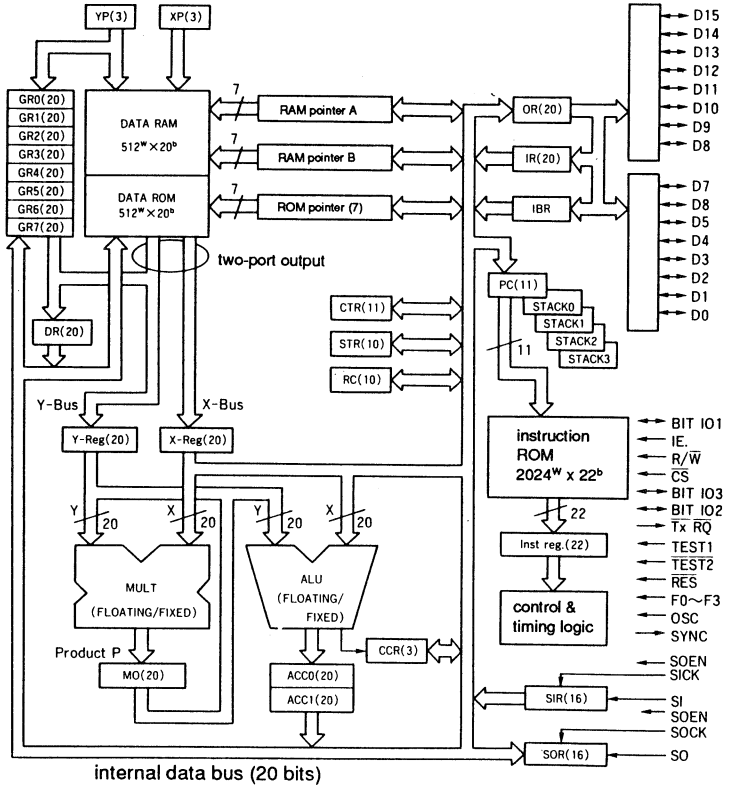
PLCC-44 (HD817820)



(Top View)

*This pin arrangement is used for DSP mode. For PROM mode, see DILP-40 pin arrangement.

Block Diagram



Parallel Processing In ALU Operation

The DSP-E provides an efficient ALU operation instruction set, which allows some operations to be performed in parallel. The ALU operation in each addressing mode is described below.

ALU operation in page indirect/page direct addressing mode

The following five operations are performed in parallel.

Example: ADDF (YP, XP), ACC0 [ALU] MULTF (YP, XP), MO [MULT] ST ACC0, (YP) [ST] INCRA [RAMP] NOPRO; [ROMP]

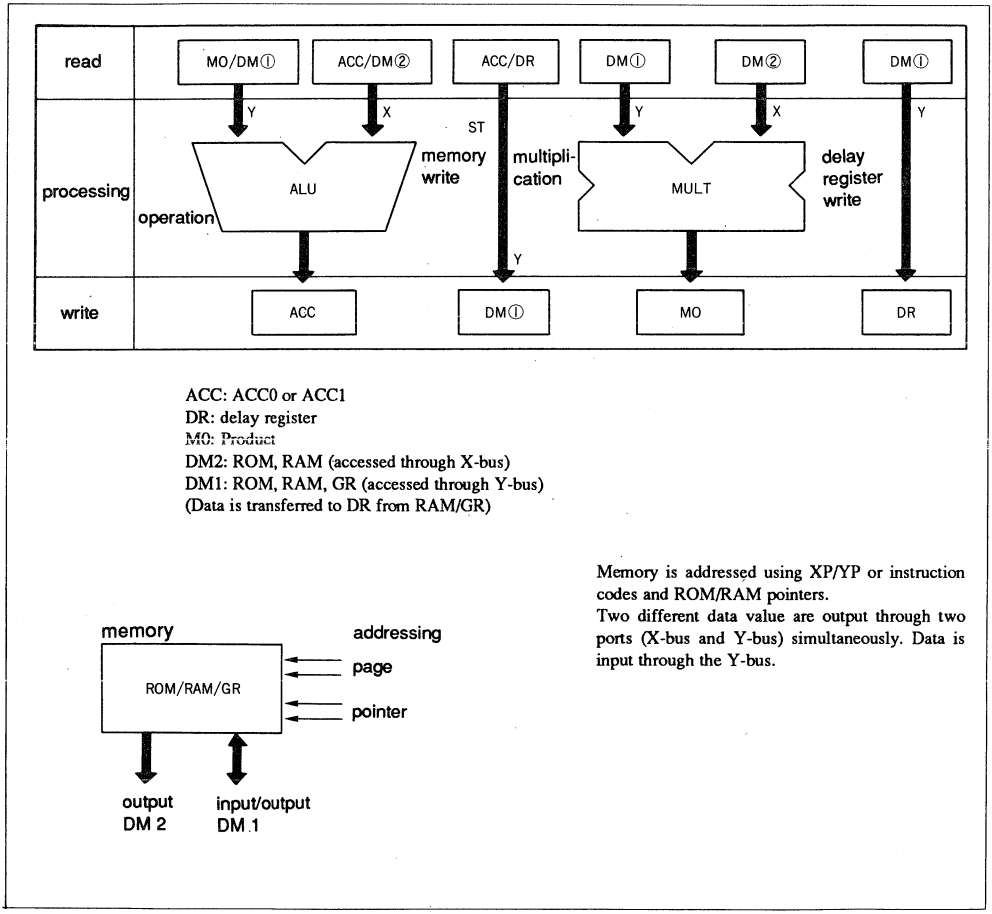


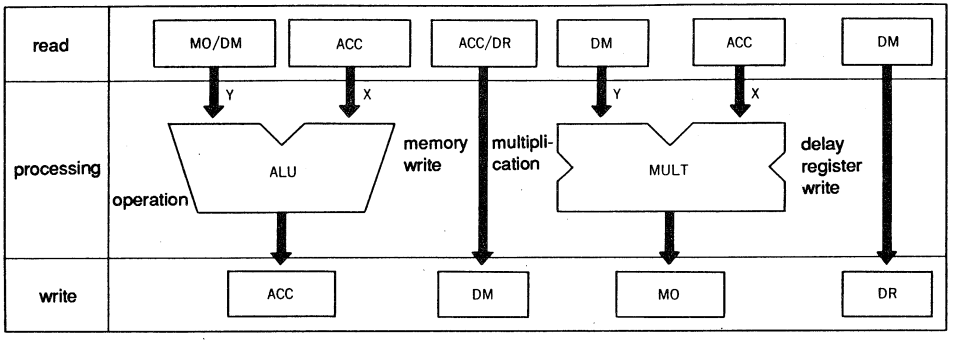
Figure 1. Parallel Operation of DSP-E

Data in ACC, P, DR and MO are used in the next instruction cycle. Of all registers, MO and DR are free-running registers and their contents change every instruction cycle. Moreover, they cannot be restored from RAM.

Therefore, special attention is needed when an interrupt is enabled, because data in MO and DR before an interrupt cannot be preserved.

ALU operation in direct addressing mode

Example: ADDF (DM0, 10, ACC0), ACC0 [ALU] MULTF (DM0, 10, ACC0), MO [MULT] ST ACC0, DM0, 10; [ST]



ACC: ACC0 or ACC1
DR: delay register
MO: product
DM: ROM, RAM (accessed by specifying addresses directly)
(Only RAM data is written to DR)
'DM0, 10' indicates memory address location H'10 in page 0.

Figure 2. Parallel Operation of DSP-E

Programmable ROM Operation (HD817820 Only)

The DSP-E on-chip PROM is programmed in PROM mode. In this mode the DSP-E does not operate.

PROM can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 40-to-28 pin socket adapter. Note that addresses H'0000 through H'4FFF are assigned to PROM.

An 4-MHz clock must be input through the OSC pin, and in addition, Vcc power can also be used as the power source of the external clock circuit. It is recommended to use a ceramic oscillator whose oscillation setup time is short. An oscillator is included in the socket adapter which assigns 28 pins of the DSP-E pins to PROM programming in the same way as a standard EPROM.

Notes

1. Be careful that the PROM programmer, socket adapter and LSI match. Using the wrong programmer or socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.

2. PROM must be programmed with V_{PP} = 12.5 V (other PROMs use 21 V). If 21 V is applied to the DSP-E, the LSI may be permanently damaged. 12.5 V is Intellec 27256 V_{PP}.

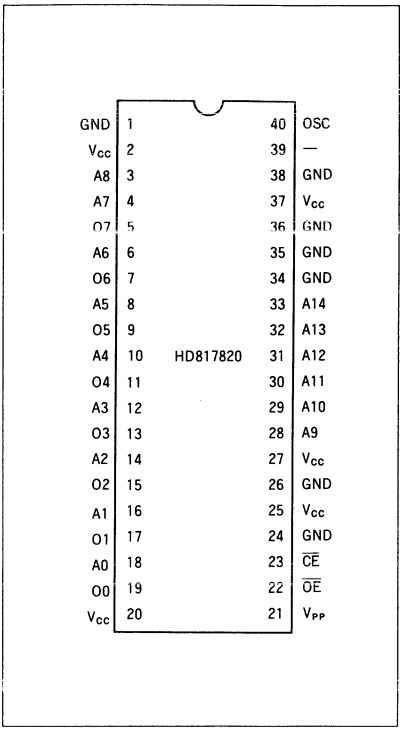


Figure 3. Pin Assignment in PROM mode

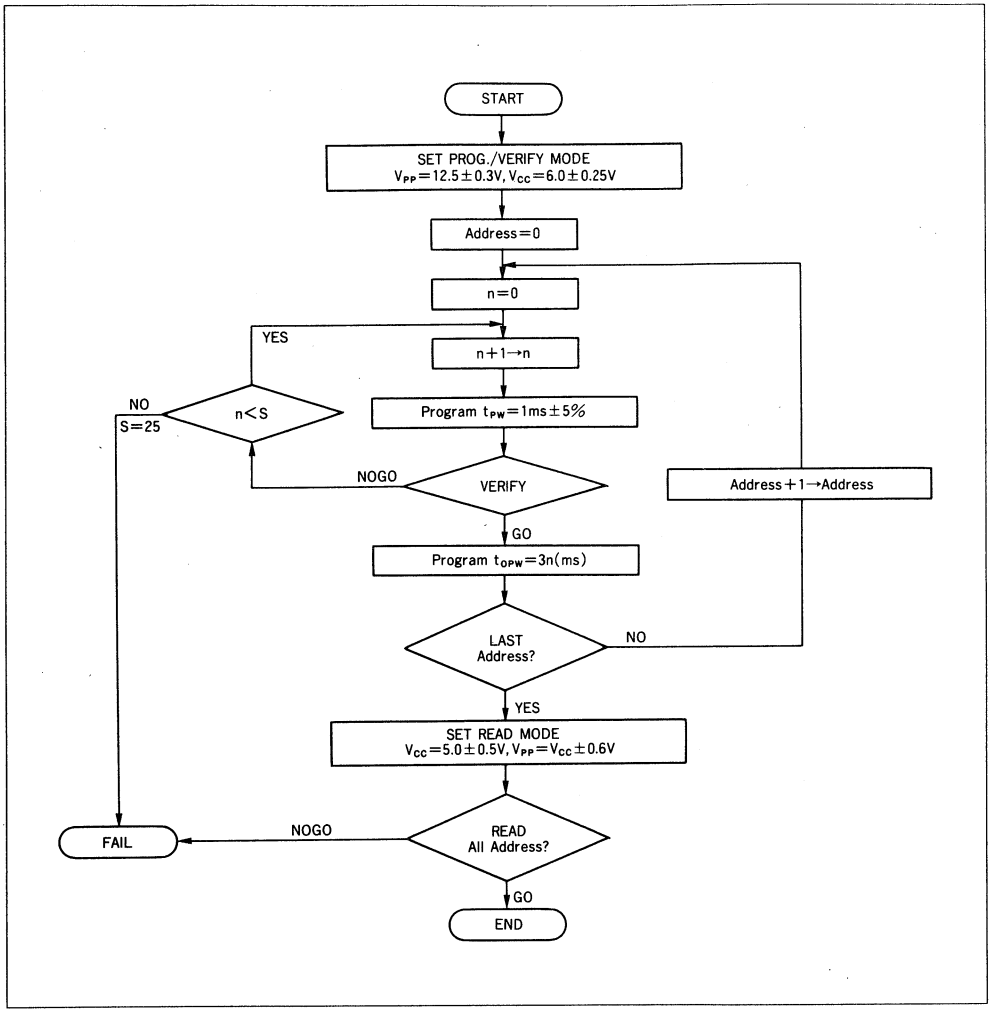


Figure 4. Procedure for High-Speed Programming

Programming Electrical Characteristics

DC characteristics (V_{CC} = 6 V ± 0.25 V_{PP} = 12.5 V + 0.3 V, V_{SS} = 0 V, Ta = 25°C ± 5°C, unless otherwise specified)

Items		Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	O0–O7, A0–A14, $\overline{OE}$, $\overline{CE}$	V_{IH}		2.2	—	V_{CC} + 0.3	V
Input low voltage	O0–O7, A0–A14, $\overline{OE}$, $\overline{CE}$	V_{IL}		–0.3	—	0.8	V
Output high voltage	O0–O7	V_{OH}	I_{OH} = 200 µA	2.4	—	—	V
Output low voltage	O0–O7	V_{OL}	I_{OL} = 1.6 mA	—	—	0.45	V
Input leakage current	O0–O7, A0–A14, $\overline{OE}$, $\overline{CE}$	$\|I_{LI}\|$	Vin = 5.25/0.5 V	—	—	2	µA
V_{CC} current		I_{CC}	fosc = 4 MHz	—	—	100	mA
V_{PP} current		I_{PP}		—	—	50	mA

HD81831Y10 (DSP-I)

Preliminary

Digital Signal Processor (100 ns version)

The HD81831Y10(DSP-I) is a single chip processor with storedprogram capability designed for digital signal processing including image processing.

The DSP-I can perform multiply and accumulate at a ultra-high speed of 100 ns(10MIPS).Moreover,it achieves high throughput by performing data operation and data transfer simultaneously.

The DSP-I incorporates two-dimensional addressing operation functions and powerful bit processing functions for image processing, realizing high speed repetitive operations and division. Since its internal memory space consists only of RAM, programs can be changed depending on the application,thus enabling the DSP-I to perform various types of signal processing. Moreover, the DSP-I has a large external data memory space of 16M words, and a host MPU can be interfaced to multiple DSP-Is in a multiprocessor system to enhance throughput.

The DSP-I can be widely used for various application requiring high speed and high accuracy operations such as image processing, communications and control systems.

Hardware Features

- 32-bit high speed fixed point ALU and 16-bit high speed fixed point multiplier incorporated
- Built–in high speed bit processing unit (BPU)
- High speed data processing of 10 MIPS (100 ns)
- High throughput owing to pipeline operations and horizontal microinstructions
- Two-hierarchical instruction structure allowing data operations and data transfer to occur simultaneously
- High speed data transfer achieved with double buffer method using multi-bank large capacity internal data RAM
- Three types of addressing operation units incorporated
- N-bit barrel rotator incorporated
- Wait function for low speed external data memory
- Built-in large capacity memory
  instruction RAM:
  microinstruction: 1024 words × 48 bits
  picoinstruction: 64 words × 16 bits
  data RAM: 512 words × 4 pages × 16 bits
- Large external data memory space of 16M words × 16 bits
- External instruction memory expandable up to 15 k words × 48 bits
- 8/16-bit microcomputer interface
- Multiprocessor function
  Control command communication between the host MPU and multiple DSP-Is using processor numbers
  Task communication for cascade connection
- Internal register contents which can be changed forcibly by commands from the host MPU
- DMA operation with the host MPU or other external devices
- High speed transfer of a large amount of data or program (PIO transfer)
- 4 level subroutine nesting
- +5 V single power supply
- Package : 135-pin PGA

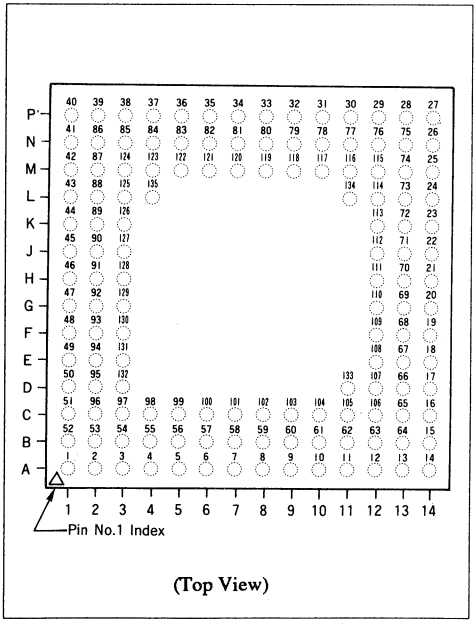
Software Features

- Each operation instruction executed in a single machine cycle.
- Tow-hierarchical instruction format: microinstructions and picoinstructions
- Data read, addition/subtraction, multiplication, data write, internal data RAM addressing operations, data transfer to external data memory, external data memory addressing oprations and repeat counter decrementation, all executed by a single instruction
- Two-dimensional addressing operation executed by a single instruction
- Continuous access operation over a large external data memory space of 16M words
- Division executed in 20 program steps using a division instruction.
- Three types of repeat functions
  n-step high speed repeat instruction
  loop instruction
  loop due to program jump
- Program transfer mode (PIO mode) allowing high speed teansfer between a host MPU and internal data RAM and instruction RAM
- Various types of high speed bit processing performed in word units (such as word synthesizing, word matching, run-length measurement)

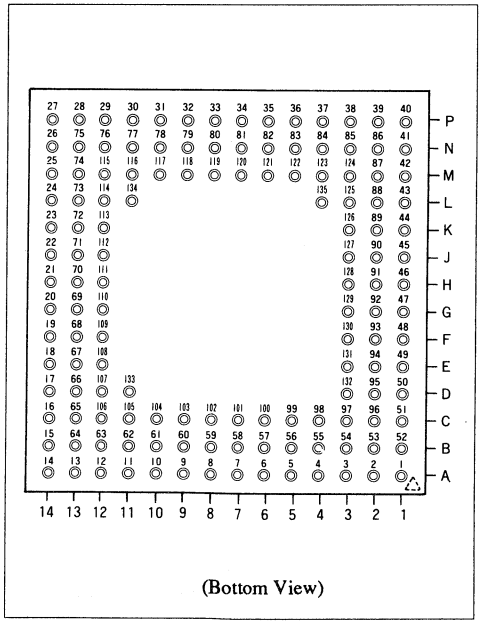
Bench Marks

Operation	Execution time
32-bit ALU Opeation (ADD/SUB/SHIFT etc.)	100 ns
16 × 16 → 32-bit multiplication	100 ns
32 × 32 → 64-bit multiplication	4 µs
Multiply and accumulate operation	100 ns
Division	2 µs
Complex FFT 256 points	1.30 ms
Complex FFT 512 points	2.90 ms
Complex FFT 1024 points	7.66 ms
Affine transformation (binary data of white and black pixels, when using external instruction memory)	1 µs/pixel
Space filter (3 × 3 pixel filter) (when using internal instruction RAM)	1.2 µs/pixel
Space filter (3 × 3 pixel filter) (when using external instruction memory)	2 µs/pixel
Variable-density histogram	0.6 ns/pixel
Transversal filter	100 ns/TAP

Pin Arrangement

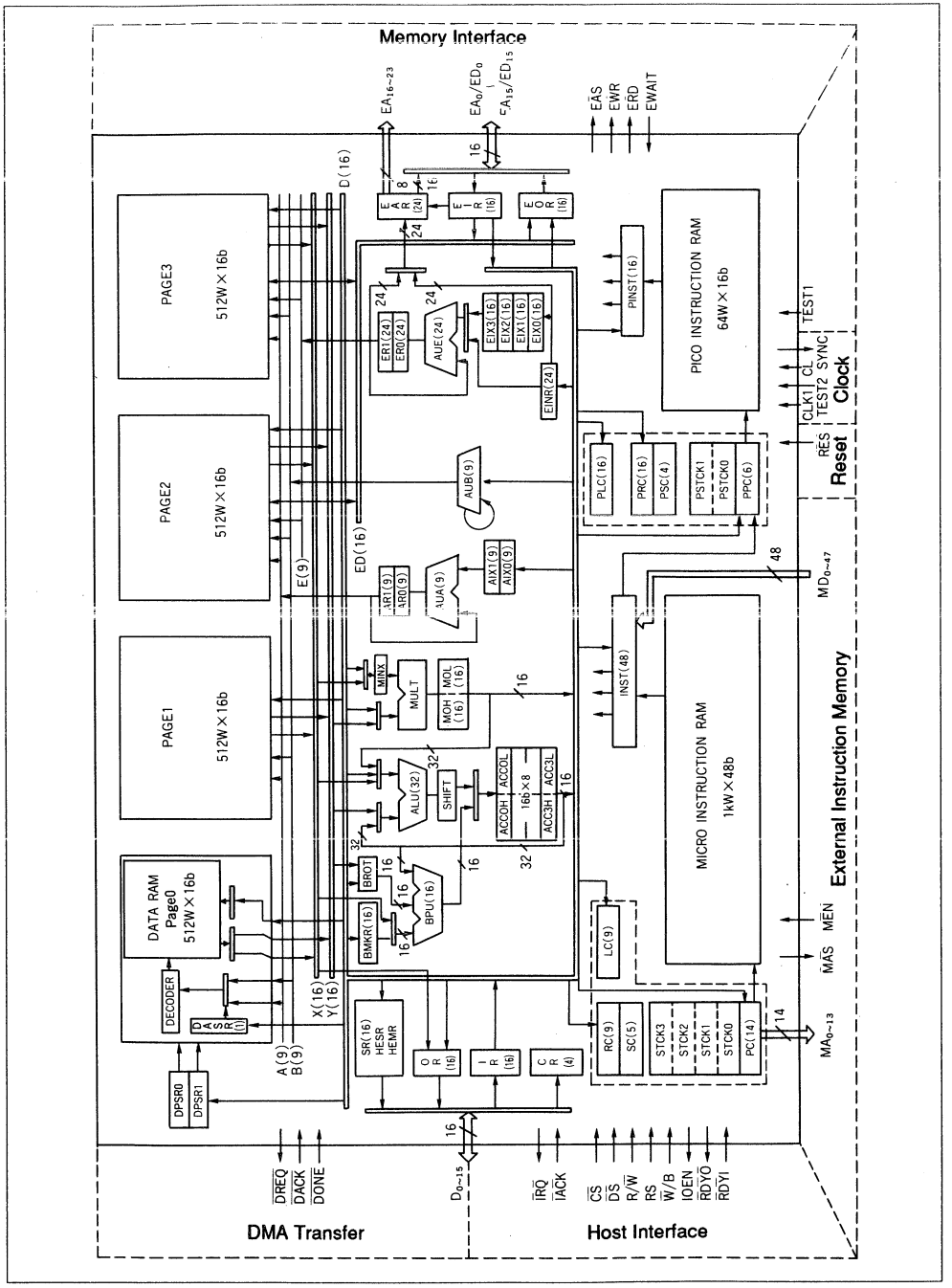


(Top View)



(Bottom View)

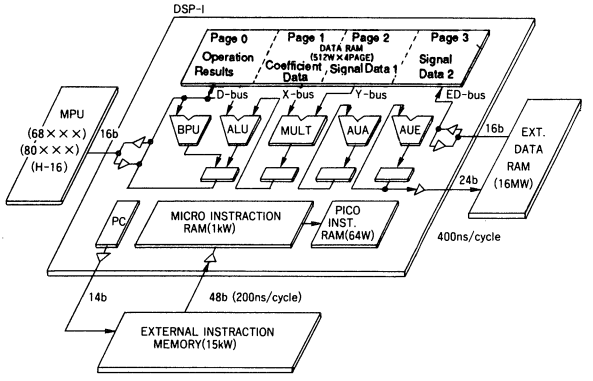
Block Diagram



Architecture

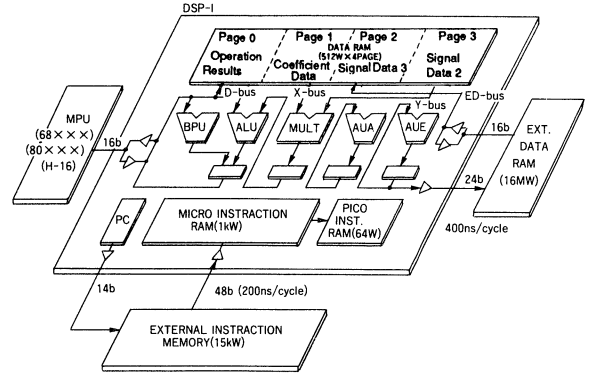
Data Operation and Data Transfer (Executed in Parallel)

The DSP-I provides microinstructions controlling data operations and picoinstructions controlling data transfer between internal data RAM and external data memory. These two instruction sets can operate independent of each other. In addition, the DSP-I includes 4 pages of internal data RAM, which can be used as a data cache by assigning each page to be controlled by microinstruction or picoinstruction. Therefore, using these functions, the DSP-I can perform data operations in parallel with data transfer between internal data RAM and external data memory. This enables high data throughput.



(a) The DSP-I performs data operations using signal data 1.

Simultaneously, it transfers signal data 2 required for the next data operation from external data memory into page 3.



(b) After completing data operations (a), the DSP-I interchanges page 2 and page 3. It then executes data operations using signal data 2 of page 3. Simultaneously, it transfers signal data 3 from external data memory to page 2 preparatory to the next data operation.

Figure 1. Example of Double Buffer Operation

Double-Hierarchical Format Instructions

Operations of microinstructions and picoinstructions are shown in figure 2. A picoprogram is activated by a microinstruction, after which it operates independent of microprograms. A picoprogram is activated by describing the address of the picoprogram to be activated in the microinstruction. To synchronize the operations of microinstructions and picoinstructions, microprogram execution must be halted by the WAIT instruction to wait for the picoprogram to stop.

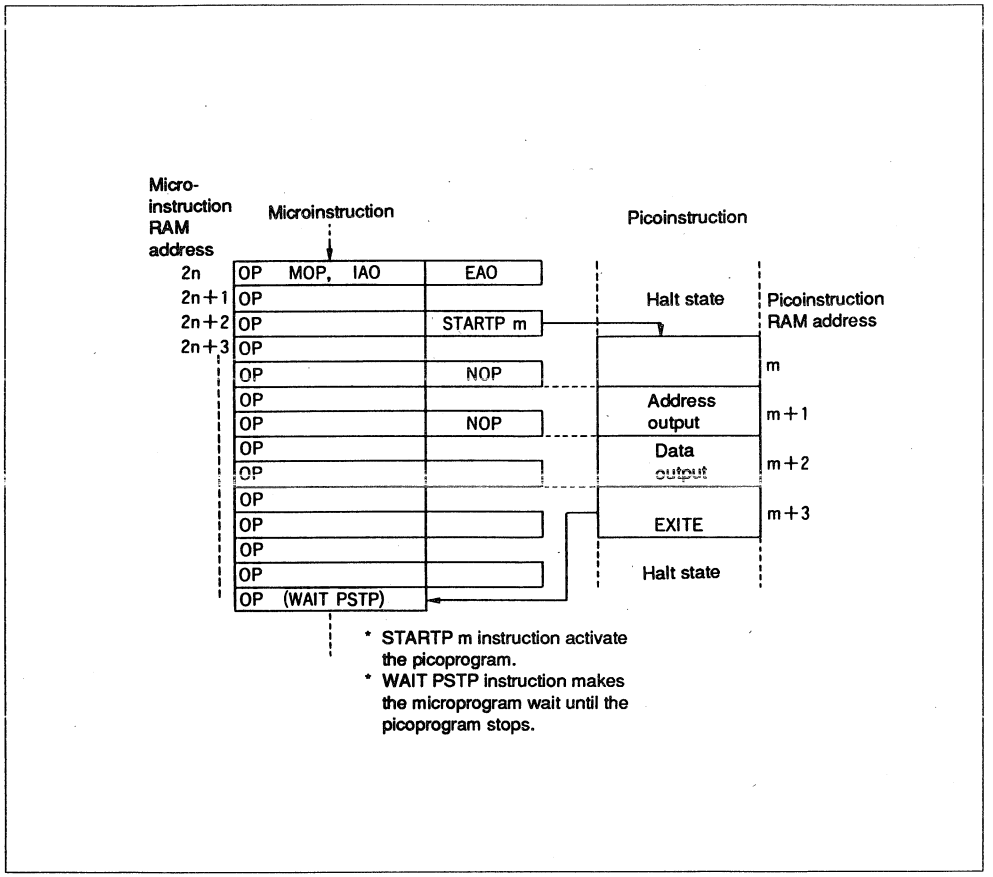


Figure 2. Microinstructions and Picoinstructions Operation

Multiprocessor System

The host MPU communicates with the DSP-I using control commands.

The DSP-I has a 12-bit processor number expressed two-dimensionally (DSP-I identification number).Thus it can be used in a multiprocessor system consisting of up to 64 x 64 DSP-Is (See figure 3). In a multiprocessor system, all DSP-Is are connected to the same system bus. Each DSP-I uses its processor number to determine whether or not the host MPU control commands are given to itself.

Processor number of zero is used for global communication. As figure 3 shows, both X number and Y number are specified when a single DSP-I communicates with the host MPU, but either X number or Y number is zero when the host MPU communicates with all DSP-Is along a row (X direction) or column (Y direction). In addition, when both X and Y numbers are zero, all DSP-Is communicate with the host MPU.

Processor number
(12 bits)

Configuration of processor number and command

indicates the DSP-I which communicates with the host MPU.

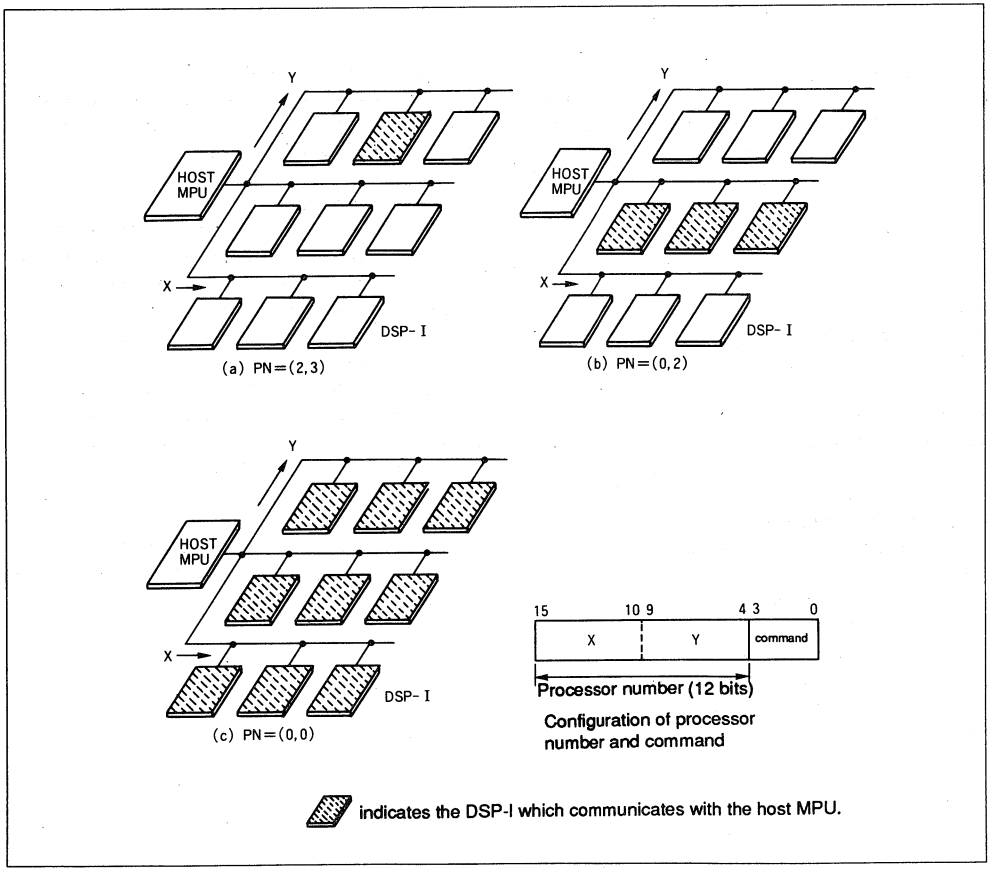


Figure 3. Example of Multiprocessor System

Instruction Execution Cycle Time and Memory Access Time

The DSP-I provides two types of instruction sets: microinstructions and picoinstructions, and incorporates instruction memory for each instruction set. The DSP-I is characterized by ultra-high speed operations, but it can use low-speed external memory. Table 1 summarizes instruction execution cycle times.

Table 1 Instruction Execution Cycle Time (when basic clock cycle time is 100 ns)

Instruction memory	Microinstruction execution time	Data operation and internal data RAM addressing execution time	External data memory access time	
			Microinstruction (EAO field)	Picoinstruction
Internal	100 ns	100 ns	400 ns	400 ns
External	200 ns	200 ns	800 ns	

Bit processing unit (BPU)

The DSP-I has a high-performance bit processing unit (BPU) which realizes a high-speed image processing. Figure 4 shows block diagram of the bit processing unit. Table 2 lists examples of bit processing.

This bit processing unit consists of the following:

Bit rotator (BROT)

The bit rotator (BROT) rotates left 16-bit data (bits 0-15) from Y bus or D bus. It also provides bit reverse function for 16-bit data. The BROT performs bit rotation and bit reverse in one instruction cycle. The BROT instruction or the rotate register (BRTC, 4 bits) specifies the rotate value as an immediate value. The BRTC is a counter register which is incremented while shifting data. The rotated data is stored in the accumulator or used in an operation with the other operand.

Mask data generator (MSKG)

The mask data generator is used to generate mask data depending on rotate value N.

These mask data realizes high-speed performance: synthesis of two word data and bit data substitution.

Mask data register (BMKR)

This register stores an optional mask data in addition to the mask data generated by the MSKG. The BMKR is set by the MOV instruction.

Logic operation block

This block performs a logic operation (AND, OR,XOR) between BROT data and accumulator data (or the result of AND of mask data and ACC), which realizes data synthesis.

Priority Encoder (PE)

This block performs priority encoding data via BROT, priority encoding selects the first bit location to be set to 1 from the MSB side. The PE realizes data normalization and run length measurement.

Bit counter

This block is used to count the number of bits set to 1 in word data via BROT, which realizes pattern matching between two word data.

Table 2. Examples of Bit Processings

Processing	Number of Steps DSP-I	Number of Steps HD61810	Description
Bit substitution	1	3	Word 1, Word 2, Synthesized word
Two-word synthesis	2	17	Word 1, Word 2, Synthesized word
Pattern matching with masking	2	51	Data, Dictionary, Mask, Number of matched bits
Run length measurement	7	64	One-word data, COUNT n_K

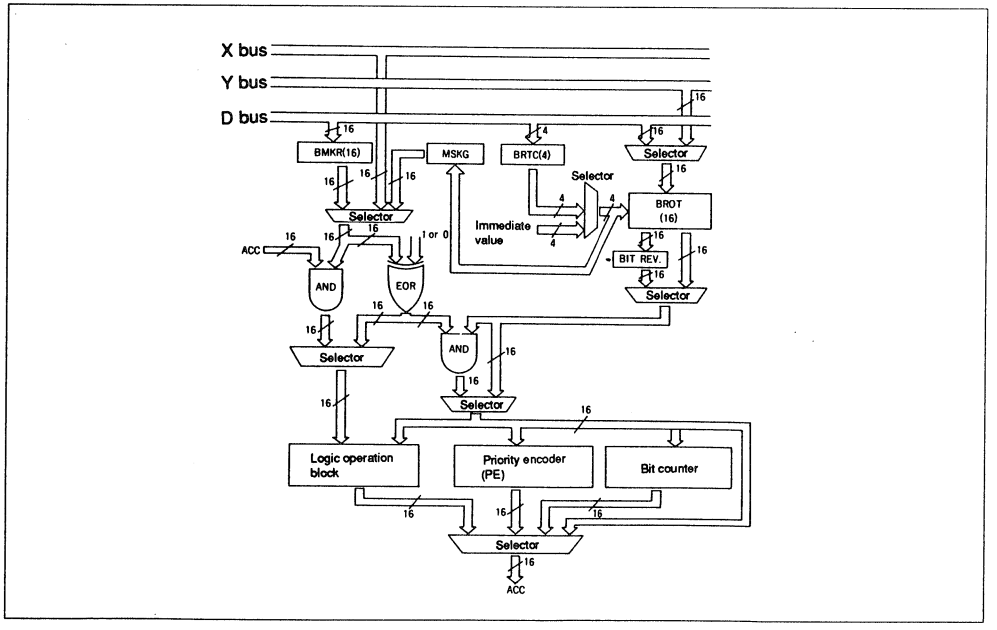


Figure 4. BPU (Bit Processing Unit) Configuration

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